OPAx170 36V、单电源、SOT553 封装、低功耗运算放大器超值系列

1 特性

- 电源电压范围：2.7V 至 36V，±1.35V 至 ±18V
- 低噪声：19 nV/√Hz
- 已过滤的射频干扰 (RFI) 输入
- 输入范围包括负电源
- 输入范围运行至正电源
- 轨至轨输出
- 增益带宽：1.2MHz
- 低静态电流：每个放大器 110μA
- 高共模抑制：120dB
- 低偏置电流：15pA（最大值）
- 采用行业标准封装和微型封装

2 应用范围

- 电源模块内的跟踪放大器
- 商用电源
- 变频器放大器
- 桥式放大器
- 温度测量
- 应力计放大器
- 精密积分器
- 电池供电仪器
- 测试设备

3 说明

OPA170、OPA2170 和 OPA4170 器件 (OPAx170) 属于 36V、单电源、低噪声运算放大器系列。该系列放大器采用微型封装，能够在 2.7V (±1.35V) 至 36V (±18V) 的电源电压范围内运行。它们在保证低静态电流的情况下提供令人满意的偏移、漂移和带宽。单通道、双通道和四通道版本均具有相同的技术规格，可最大程度地提高设计灵活性。

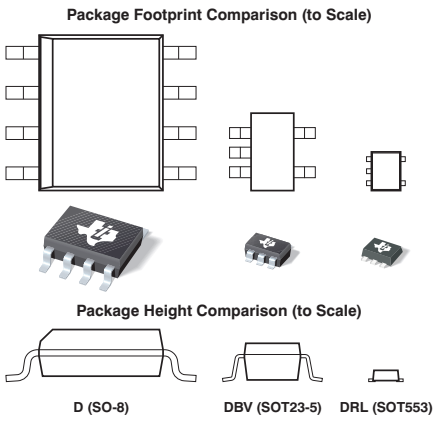
多数运算放大器仅有一个指定的电源电压，OPAx170 系列运算放大器则有所不同，其可在 2.7V 至 36V 的电压范围内额定运行。超出电源轨的输入信号不会导致相位反转。OPAx170 系列在电容负载高达 300pF 时保持稳定。输入信号可在负电源轨以下 100mV 到正电源轨以上 2V 范围内保持正常运行。请注意，这些器件可在正电源轨之上 100mV 的满轨到轨输入上运行，但是在正电源轨 2V 内运行时，性能会受到影响。OPAx170 运算放大器的额定工作温度范围为 -40°C 至 125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA170	SOIC (8)	4.90mm x 3.91mm
	SOT (5)	1.60mm x 1.20mm
	SOT-23 (5)	2.90mm x 1.60mm
OPA2170	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
	VSSOP (8)，微型封装	2.30mm x 2.00mm
OPA4170	SOIC (14)	8.65mm x 3.91mm
	薄型小外形尺寸封装 (TSSOP) (14)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

36V 运算放大器的最小封装



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (September 2012) to Revision C **Page**

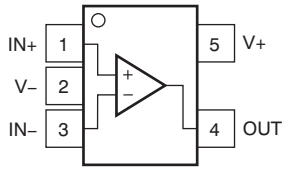
- 已添加 当前的封装标识符至 *特性*列表和*说明*部分 ... 1
- 已添加 *引脚功能表*，*ESD 额定值表*，*建议运行条件表*，*详细 说明*部分，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision A (September 2011) to Revision B **Page**

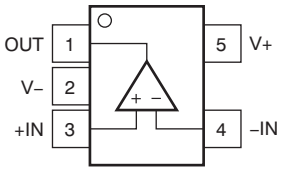
- 已添加 “*超值系列*”至文档标题 ... 1

5 Pin Configuration and Functions

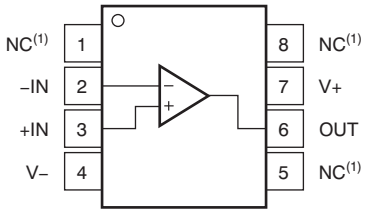
OPA170: DRL Package
5-Pin SOT
Top View



OPA170: DBV Package
5-Pin SOT-23
Top View



OPA170: D Package
8-Pin SOIC
Top View

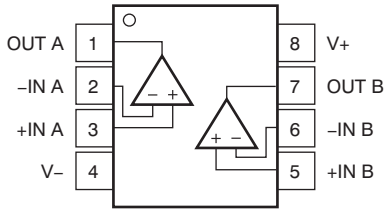


Pin Functions: OPA170

PIN				I/O	DESCRIPTION
NAME	SOT	SOT-23	D		
IN– (–IN)	3	4	2	I	Negative (inverting) input
IN+ (+IN)	1	3	3	I	Positive (noninverting) input
NC(1)	—	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	4	1	6	O	Output
V+	5	5	7	—	Positive (highest) power supply
V–	2	2	4	—	Negative (lowest) power supply

(1) NC indicates no internal connection.

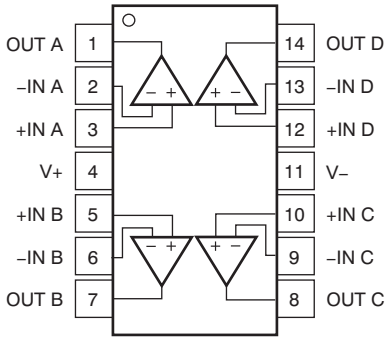
OPA2170: D, DGK, and DCU Packages
8-Pin VSSOP, SOIC, and VSSOP (*micro* size)
Top View



Pin Functions: OPA2170

PIN				I/O	DESCRIPTION
NAME	SOIC	VSSOP	VSSOP (*micro* size)		
–IN A	2	2	2	I	Inverting input, channel A
–IN B	6	6	6	I	Inverting input, channel B
+IN A	3	3	3	I	Noninverting input, channel A
+IN B	5	5	5	I	Noninverting input, channel B
OUT A	1	1	1	O	Output, channel A
OUT B	7	7	7	O	Output, channel B
V–	4	4	4	—	Negative (lowest) power supply
V+	8	8	8	—	Positive (highest) power supply

OPA4170: D and PW Packages
14-Pin SOIC and TSSOP
Top View



Pin Functions: OPA4170

PIN			I/O	DESCRIPTION
NAME	SOIC	TSSOP		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	9	9	I	Inverting input, channel C
–IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V–	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

	MIN	MAX	UNIT
Supply voltage	–20	20	V
Single supply voltage		40	V
Signal input pin voltage	(V–) – 0.5	(V+) + 0.5	V
Signal input pin current	–10	10	mA
Output short-circuit current(2)	Continuous		
Operating ambient temperature, T_A	–55	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V+ – V–)	2.7	36	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information: OPA170

THERMAL METRIC(1)		OPA170			UNIT
		D (SOIC)	DBV (SOT-23)	DRL (SOT)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	245.8	208.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.9	133.9	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	83.6	42.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.5	18.2	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89.5	83.1	42.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Thermal Information: OPA2170

THERMAL METRIC(1)		OPA2170			UNIT
		D (SOIC)	DCU (VSSOP, *micro* size)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	175.2	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.1	74.9	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	22.2	130	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	1.6	5.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	22.8	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.6 Thermal Information: OPA4170

THERMAL METRIC(1)		OPA4170		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.7 Electrical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C		0.25	±1.8	mV
		T_A = –40°C to 125°C			±2	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		±0.3	±2	µV/°C
PSRR	Input offset voltage vs power supply	V_S = 4 V to 36 V, T_A = –40°C to 125°C		1	±5	µV/V
	Channel separation, dc			5		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		±8	±15	pA
		T_A = –40°C to 125°C			±3.5	nA
I_{OS}	Input offset current	T_A = 25°C		±4	±15	pA
		T_A = –40°C to 125°C			±3.5	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz		22		nV/√Hz
		f = 1 kHz		19		nV/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range[1]		(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = ±2 V, (V–) - 0.1 V < V_{CM} < (V+) - 2 V, T_A = –40°C to 125°C	90	104		dB
		V_S = ±18 V, (V–) - 0.1 V < V_{CM} < (V+) - 2 V, T_A = –40°C to 125°C	104	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 4 V to 36 V, (V–) + 0.35 V < V_O < (V+) - 0.35 V, T_A = –40°C to 125°C	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			1.2		MHz
SR	Slew rate	G = +1		0.4		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = +1, 10-V step		20		µs
		To 0.01% (12-bit), V_S = ±18 V, G = +1, 10-V step		28		µs
	Overload recovery time	V_{IN} × Gain > V_S		2		µs
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 3 V_{RMS}		0.0002%		

(1) The input range can be extended beyond (V+) – 2 V up to V+. See the *Typical Characteristics* and *Application and Implementation* sections for additional information.

Electrical Characteristics (接下页)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from positive rail	I_L = 0 mA, V_S = 4 V to 36 V	10			mV
		I_L sourcing 1 mA, V_S = 4 V to 36 V	115			mV
V_O	Voltage output swing from negative rail	I_L = 0 mA, V_S = 4 V to 36 V			8	mV
		I_L sinking 1 mA, V_S = 4 V to 36 V			70	mV
V_O	Voltage output swing from rail	V_S = 5 V, R_L = 10 kΩ; T_A = –40°C to 125°C	(V–) + 0.03		(V+) – 0.05	V
		R_L = 10 kΩ, A_{OL} ≥ 110 dB, T_A = –40°C to 125°C	(V–) + 0.35		(V+) – 0.35	V
I_{SC}	Short-circuit current		–20		17	mA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			pF
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0 A		900		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A; T_A = 25°C		110	145	µA
		I_O = 0 A; T_A = –40°C to 125°C			155	µA
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–55		150	°C

6.8 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

表 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1
Offset Voltage Drift Distribution	图 2
Offset Voltage vs Temperature	图 3
Offset Voltage vs Common-Mode Voltage	图 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	图 5
Offset Voltage vs Power Supply	图 6
I_B and I_{OS} vs Common-Mode Voltage	图 7
Input Bias Current vs Temperature	图 8
Output Voltage Swing vs Output Current (Maximum Supply)	图 9
CMRR and PSRR vs Frequency (Referred-to-Input)	图 10
CMRR vs Temperature	图 11
PSRR vs Temperature	图 12
0.1-Hz to 10-Hz Noise	图 13
Input Voltage Noise Spectral Density vs Frequency	图 14
THD+N Ratio vs Frequency	图 15
THD+N vs Output Amplitude	图 16
Quiescent Current vs Temperature	图 17
Quiescent Current vs Supply Voltage	图 18
Open-Loop Gain and Phase vs Frequency	图 19
Closed-Loop Gain vs Frequency	图 20
Open-Loop Gain vs Temperature	图 21
Open-Loop Output Impedance vs Frequency	图 22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	图 23, 图 24
No Phase Reversal	图 25
Positive Overload Recovery	图 26
Negative Overload Recovery	图 27
Small-Signal Step Response (100 mV)	图 28, 图 29
Large-Signal Step Response	图 30, 图 31
Large-Signal Settling Time (10-V Positive Step)	图 32
Large-Signal Settling Time (10-V Negative Step)	图 33
Short-Circuit Current vs Temperature	图 34
Maximum Output Voltage vs Frequency	图 35
EMIRR IN+ vs Frequency	图 36

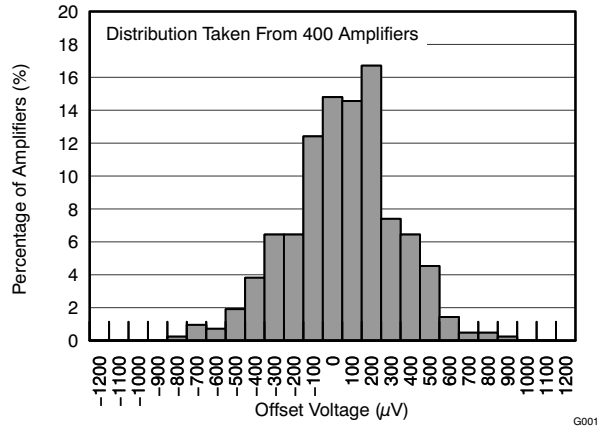


图 1. Offset Voltage Production Distribution

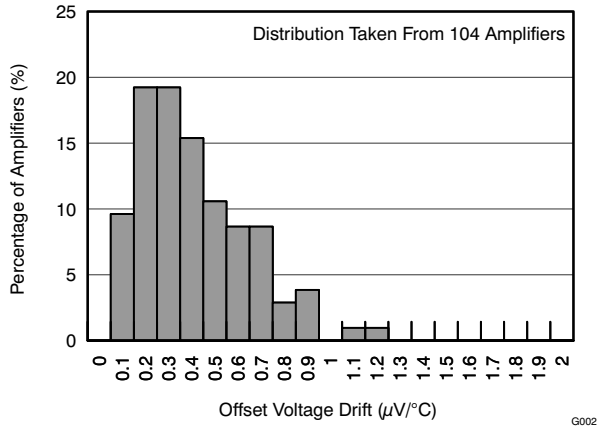


图 2. Offset Voltage Drift Distribution

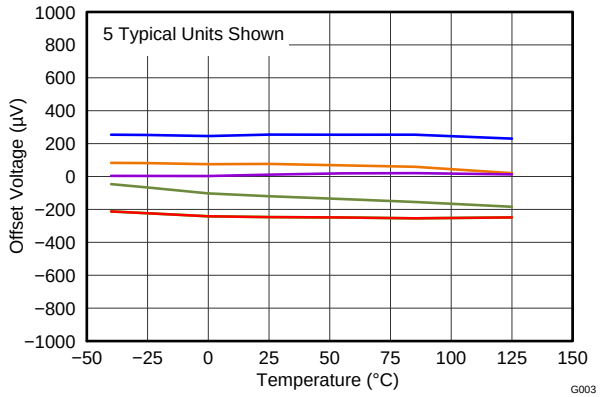


图 3. Offset Voltage vs Temperature

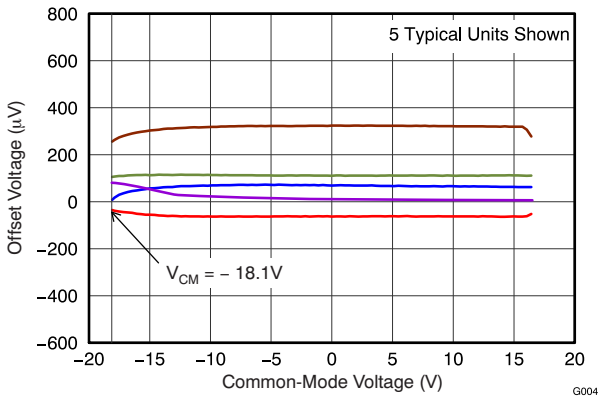


图 4. Offset Voltage vs Common-Mode Voltage

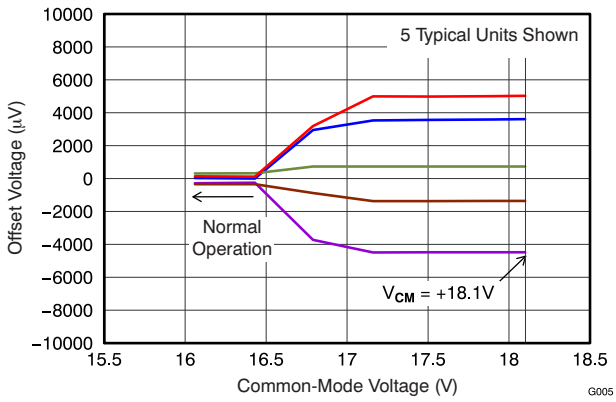


图 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

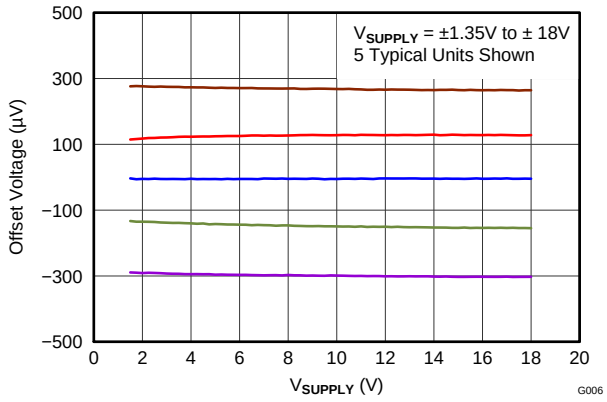


图 6. Offset Voltage vs Power Supply

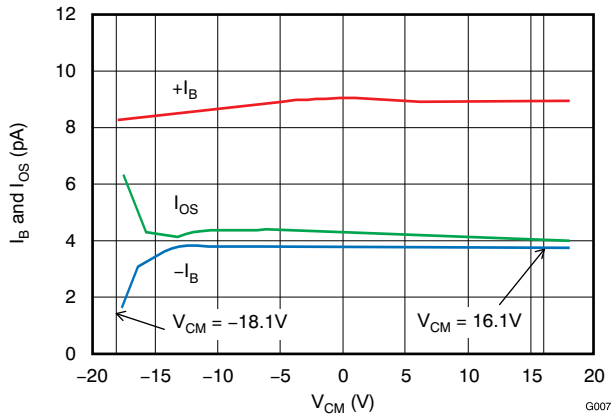


图 7. I_B and I_{OS} vs Common-Mode Voltage

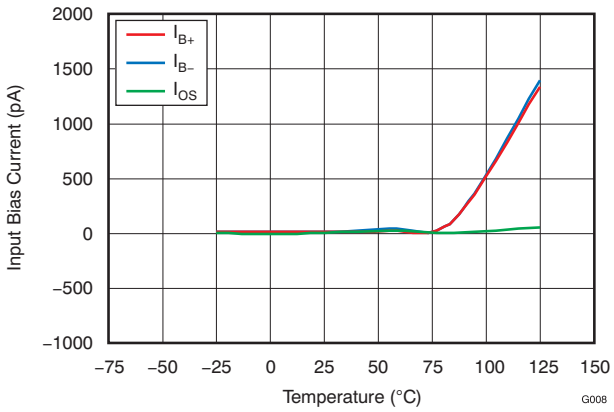


图 8. Input Bias Current vs Temperature

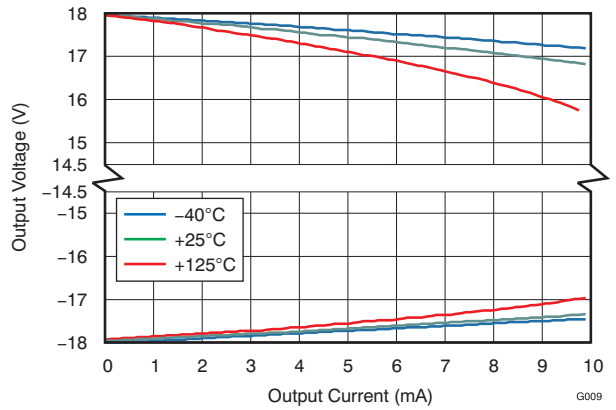


图 9. Output Voltage Swing vs Output Current (Maximum Supply)

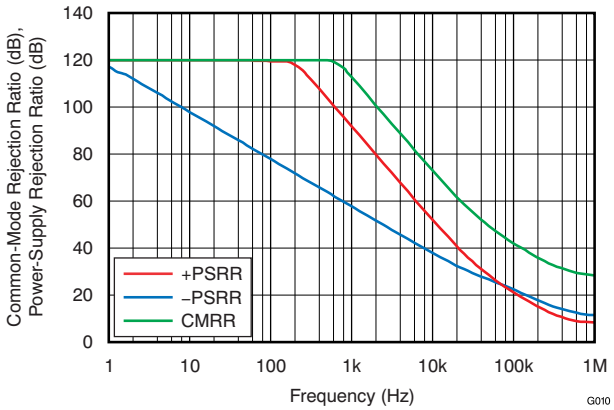


图 10. CMRR and PSRR vs Frequency (Referred-to Input)

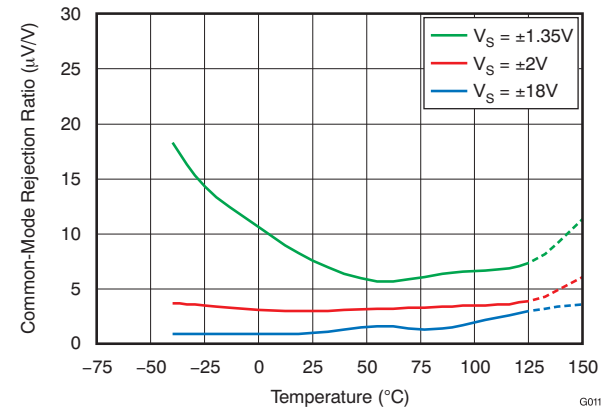


图 11. CMRR vs Temperature

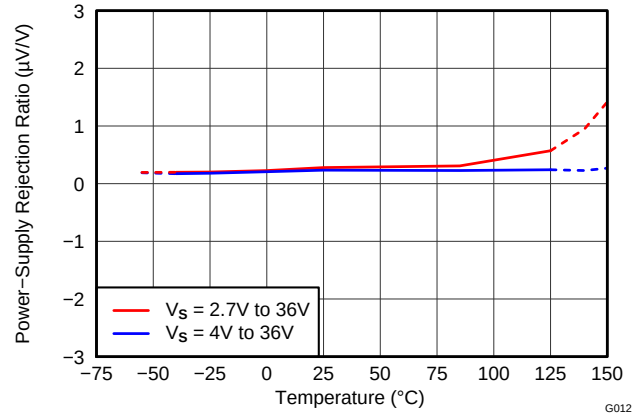


图 12. PSRR vs Temperature

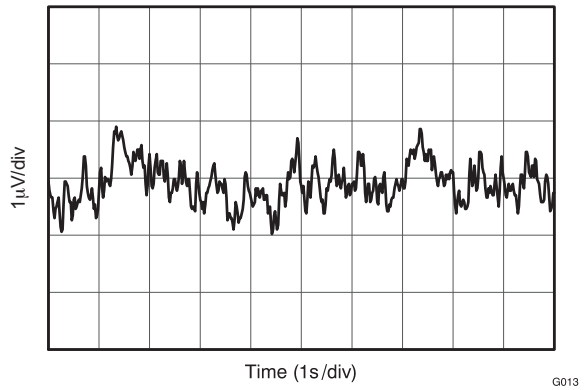


图 13. 0.1-Hz to 10-Hz Noise

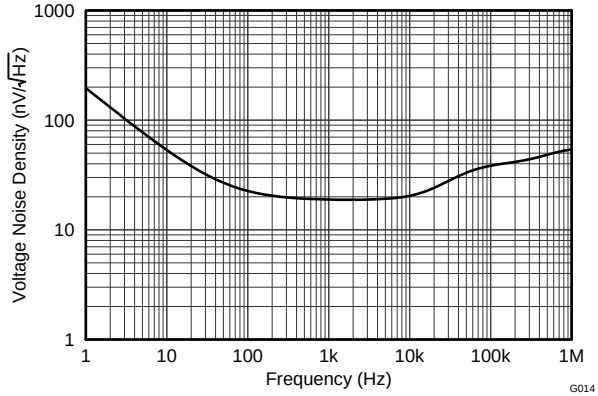


图 14. Input Voltage Noise Spectral Density vs Frequency

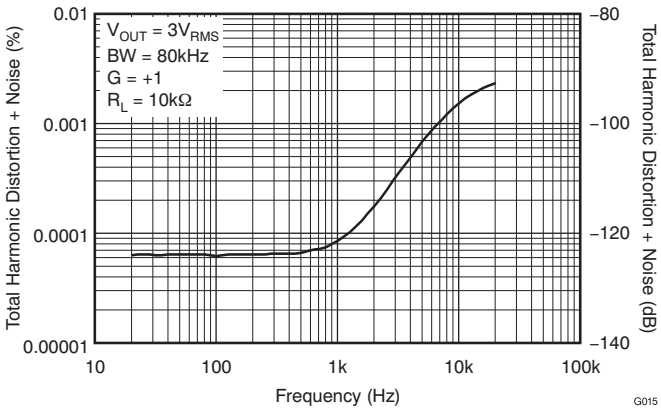


图 15. THD+N Ratio vs Frequency

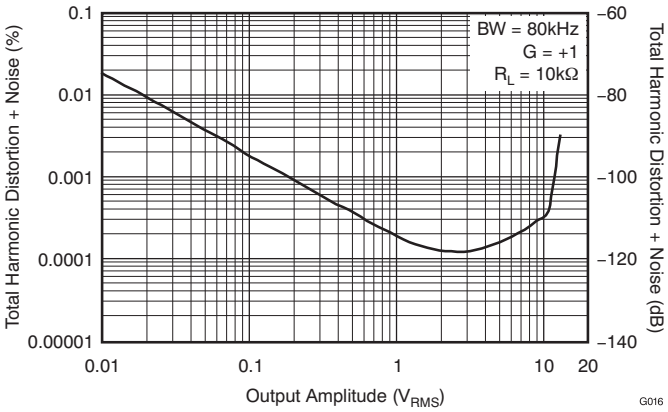


图 16. THD+N vs Output Amplitude

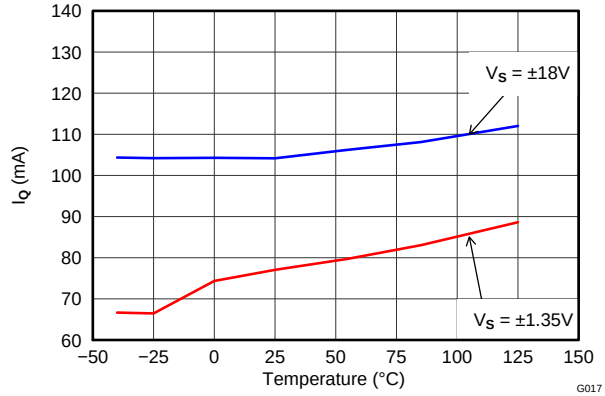


图 17. Quiescent Current vs Temperature

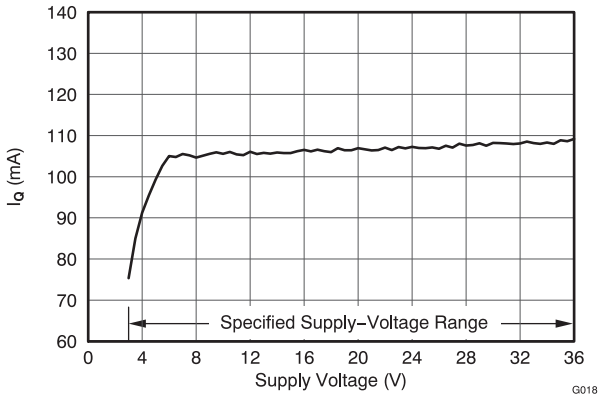


图 18. Quiescent Current vs Supply Voltage

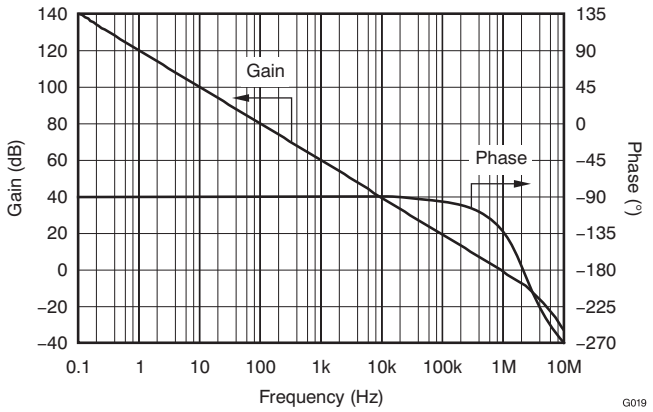


图 19. Open-Loop Gain and Phase vs Frequency

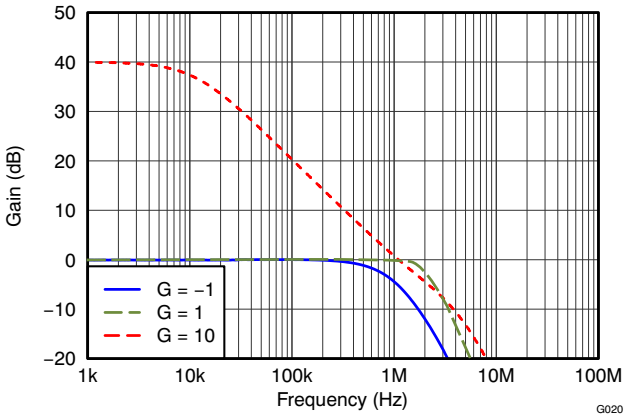


图 20. Closed-Loop Gain vs Frequency

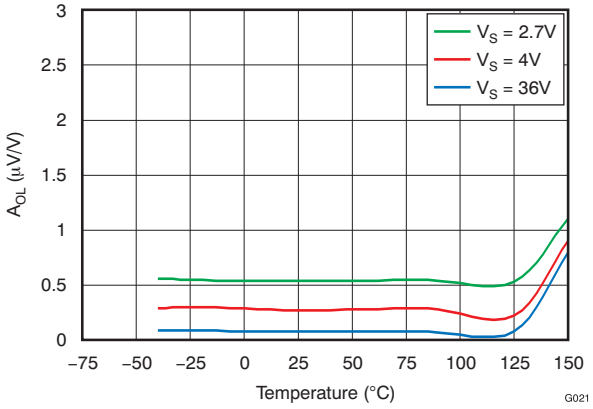


图 21. Open-Loop Gain vs Temperature

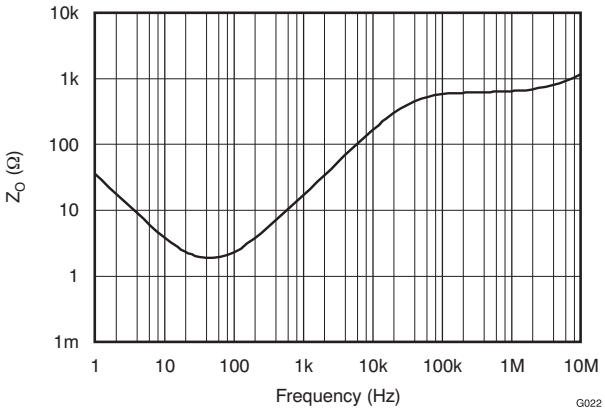
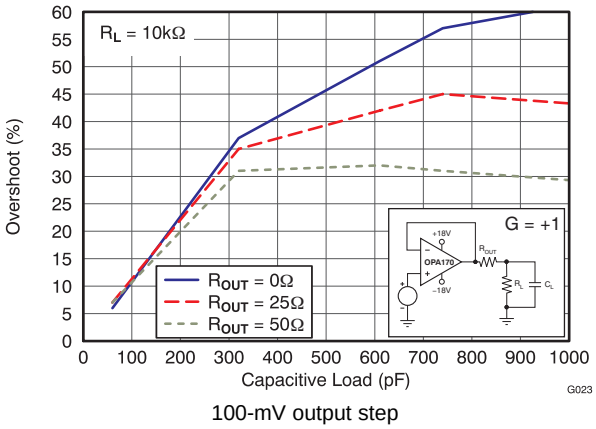
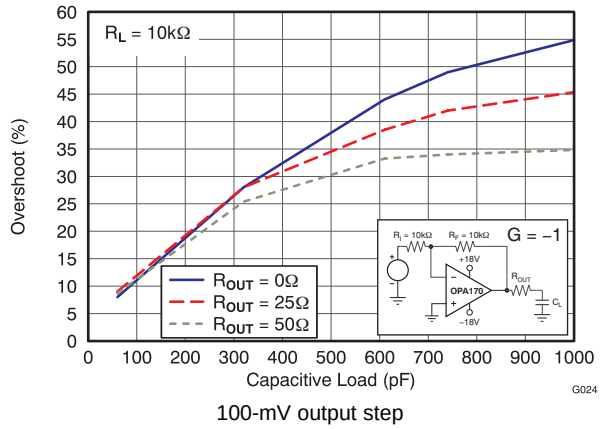


图 22. Open-Loop Output Impedance vs Frequency



100-mV output step

图 23. Small-Signal Overshoot vs Capacitive Load



100-mV output step

图 24. Small-Signal Overshoot vs Capacitive Load

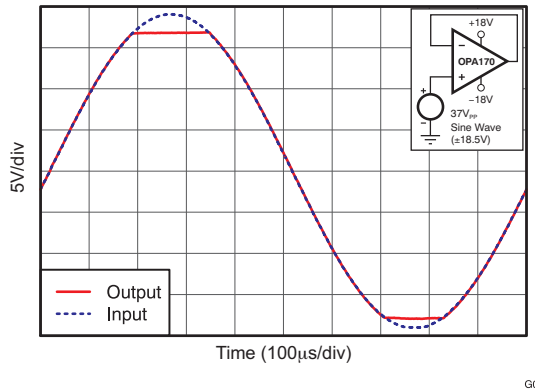


图 25. No Phase Reversal

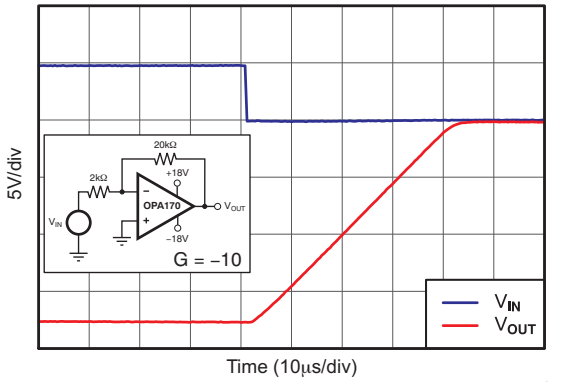


图 26. Positive Overload Recovery

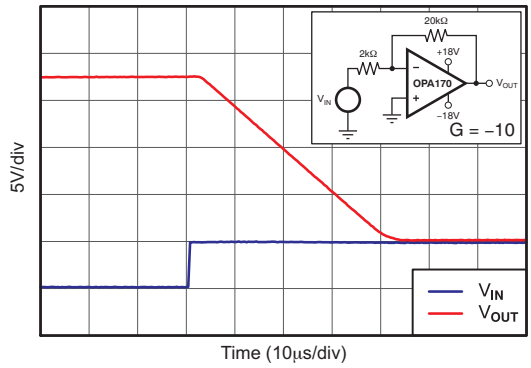


图 27. Negative Overload Recovery

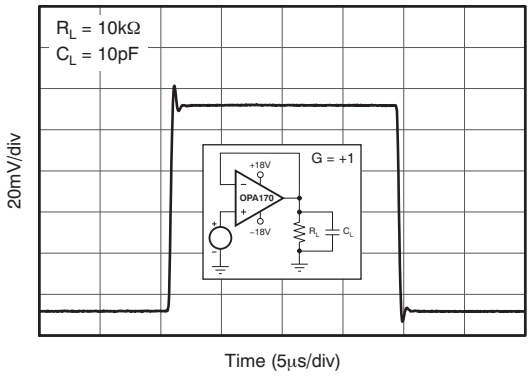


图 28. Small-Signal Step Response (100 mV)

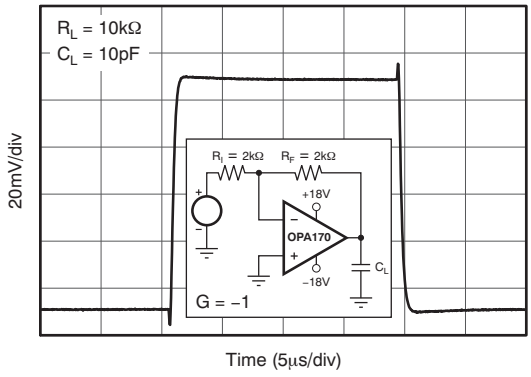


图 29. Small-Signal Step Response (100 mV)

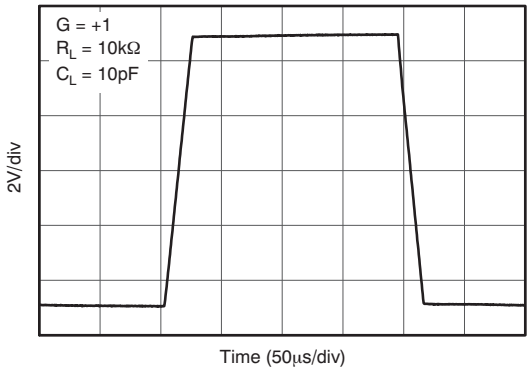


图 30. Large-Signal Step Response

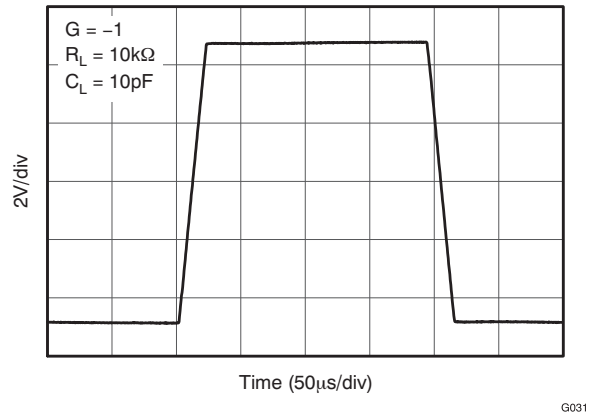
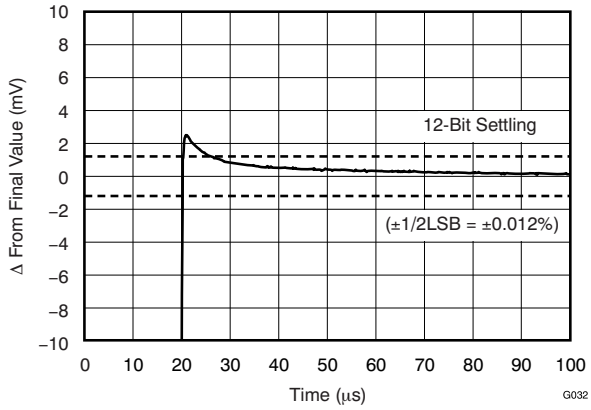
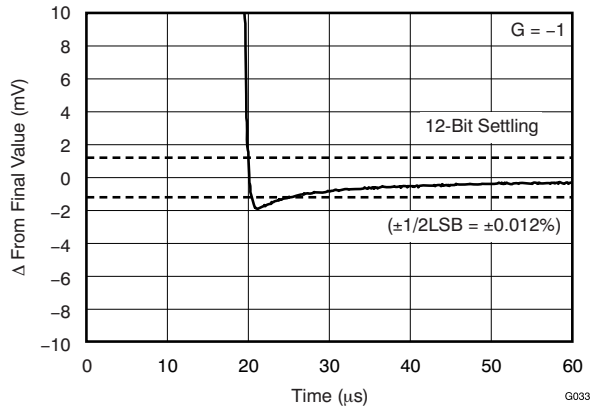


图 31. Large-Signal Step Response



10-V positive step

图 32. Large-Signal Settling Time



10-V negative step

图 33. Large-Signal Settling Time

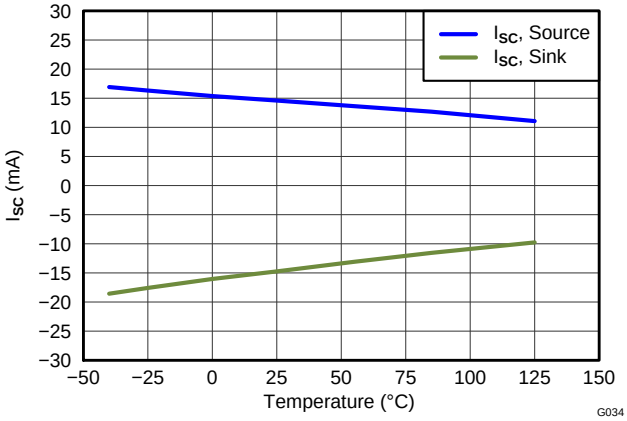


图 34. Short-Circuit Current vs Temperature

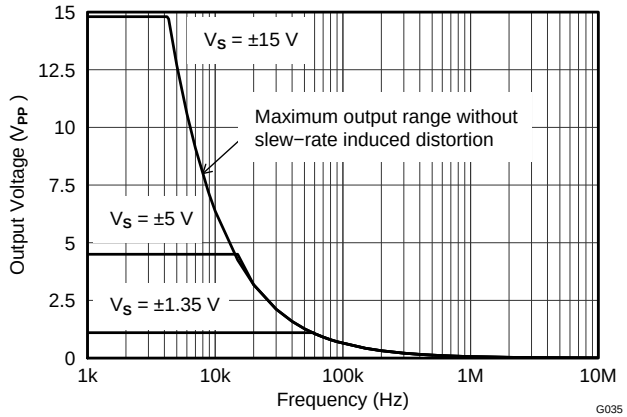


图 35. Maximum Output Voltage vs Frequency

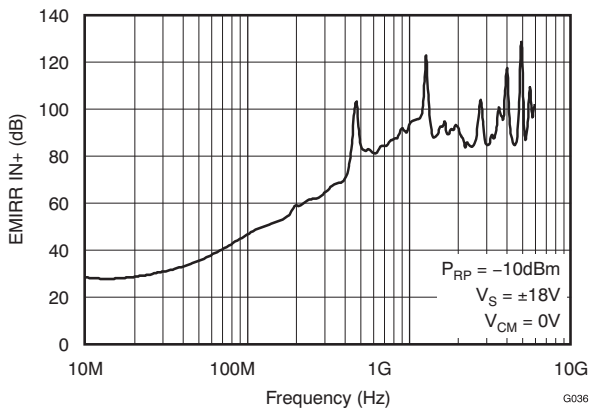


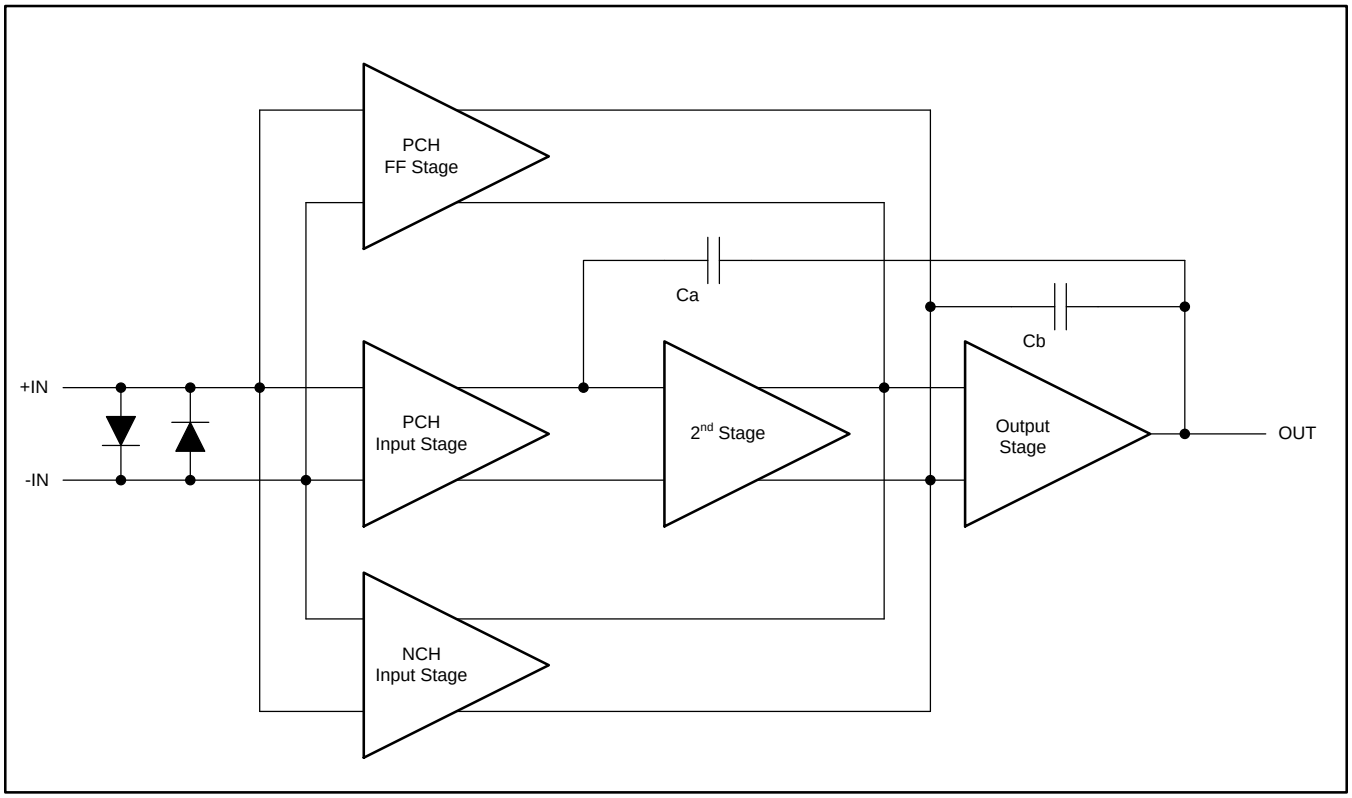
图 36. EMIRR IN+ vs Frequency

7 Detailed Description

7.1 Overview

The OPAx170 family of operational amplifiers provides high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 2 μV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPAx170 family of amplifiers is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V). Many of the specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

Feature Description (接下页)

7.3.2 Phase-Reversal Protection

The OPAx170 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx170 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in 图 37.

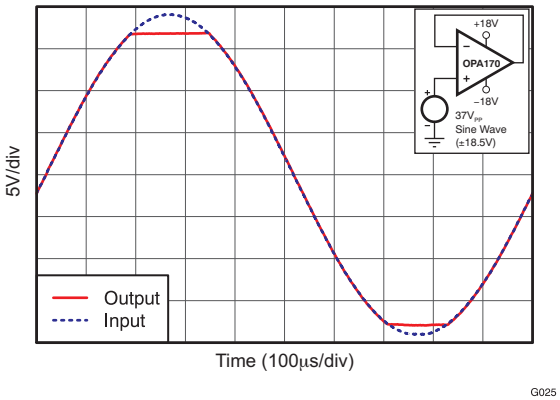


图 37. No Phase Reversal

7.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 38 illustrates the ESD circuits contained in the OPAx170 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (接下页)

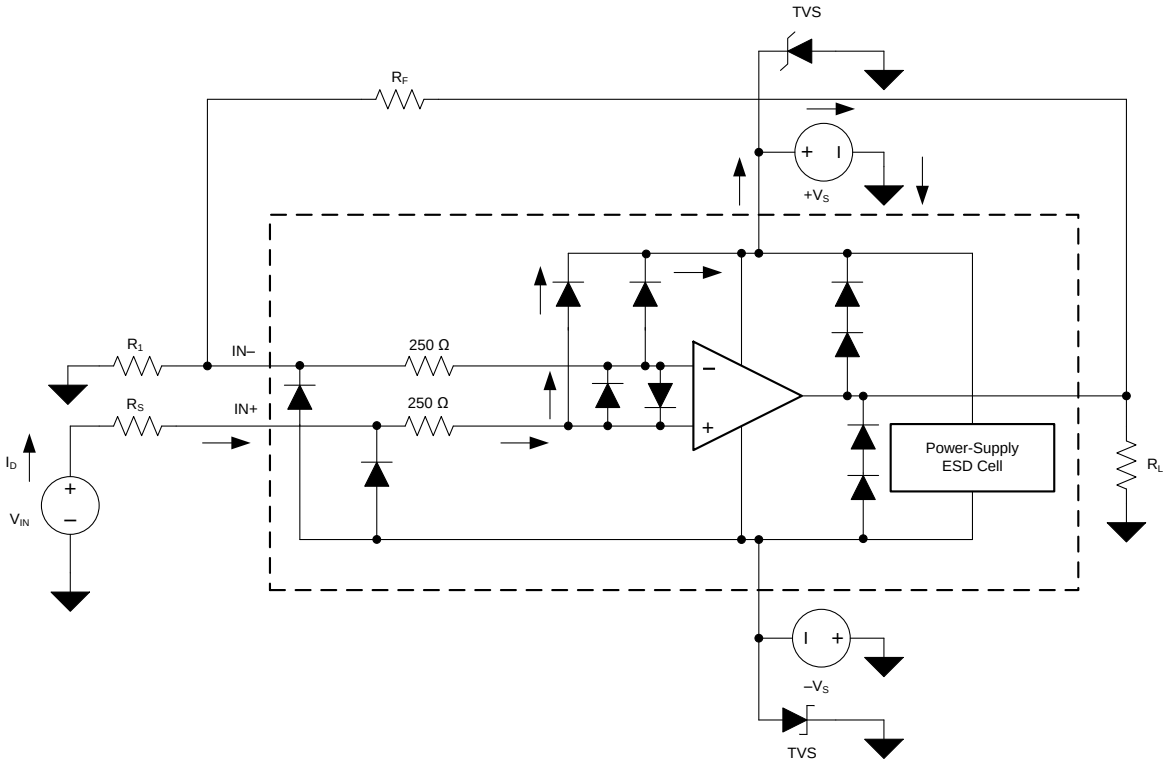


图 38. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx170 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (refer to 图 38), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 38 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Feature Description (接下页)

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 图 38. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPAx170 input pins are protected from excessive differential voltage with back-to-back diodes; see 图 38. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx170. 图 38 illustrates an example configuration that implements a current-limiting feedback resistor.

7.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx170 have been optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Refer to 图 39 and 图 40 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to applications bulletin AB-028, *Feedback Plots Define Op Amp AC Performance* (SBOA015), for details of analysis techniques and application circuits.

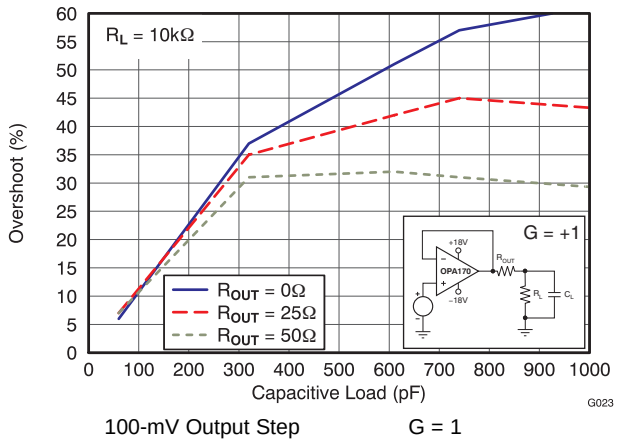


图 39. Small-Signal Overshoot vs Capacitive Load

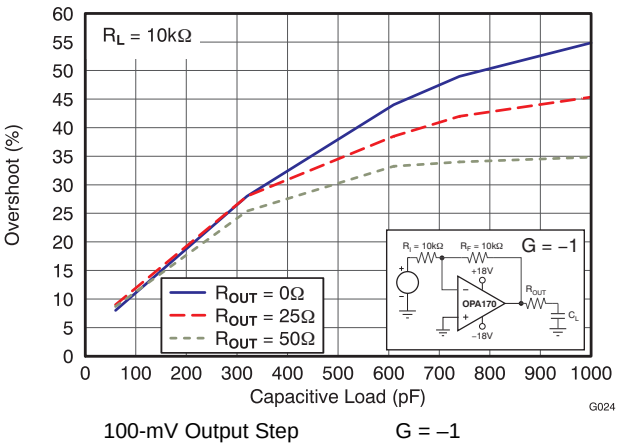


图 40. Small-Signal Overshoot vs Capacitive Load

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx170 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in 表 2.

表 2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER		MIN	TYP	MAX	UNIT
Input common-mode voltage		(V+) – 2		(V+) + 0.1	V
Offset voltage			7		mV
	vs temperature		12		µV/°C
Common-mode rejection			65		dB
Open-loop gain			60		dB
Gain-bandwidth product			0.3		MHz
Slew rate			0.3		V/µs

7.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx170 is approximately 2 µs.

8 Application and Implementation

> **注**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx170 family of operational amplifiers provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Follow the additional recommendations in *Layout Guidelines* in order to achieve the maximum performance from this device. Many applications may introduce capacitive loading to the output of the amplifier (potentially causing instability). One method of stabilizing the amplifier in such applications is to add an isolation resistor between the amplifier output and the capacitive load. The design process for selecting this resistor is given in *Typical Application*.

8.2 Typical Application

This circuit can be used to drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (Riso) to stabilize the output of an operational amplifier. Riso modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.

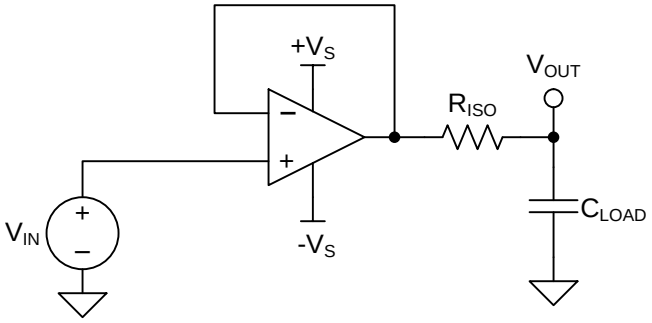


图 41. Unity-Gain Buffer With R_{ISO} Stability Compensation

8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

8.2.2 Detailed Design Procedure

图 41 shows a unity-gain buffer driving a capacitive load. 公式 1 shows the transfer function for the circuit in 图 41. Not shown in 图 41 is the open-loop output resistance of the operational amplifier, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in 公式 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB/decade. 图 42 depicts the concept. The 1/β curve for a unity-gain buffer is 0 dB.

Typical Application (接下页)

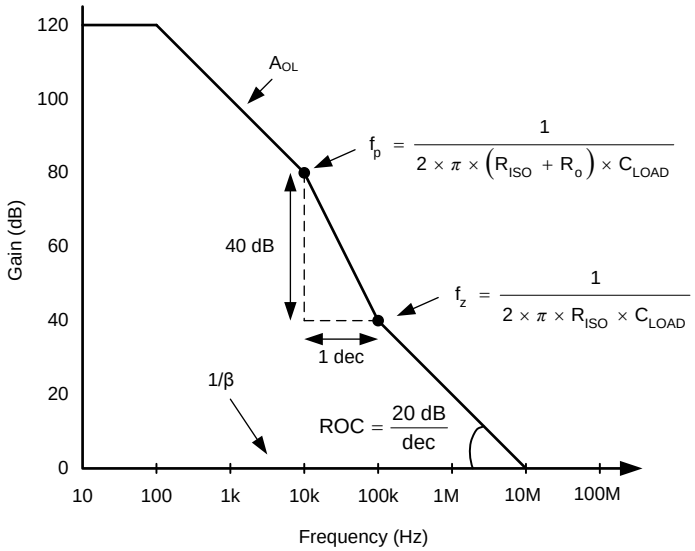


图 42. Unity-Gain Amplifier With R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. 表 3 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA170, refer to the Precision Design, *Capacitive Load Drive Solution Using an Isolation Resistor* (TIPD128).

表 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.3 Application Curve

Using the described methodology, the values of R_{ISO} that yield phase margins of 45º and 60º for various capacitive loads were determined. The results are shown in 图 43.

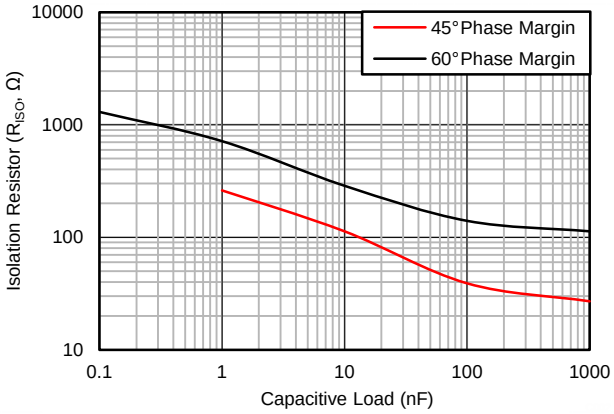


图 43. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

9 Power Supply Recommendations

The OPAx170 is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V); many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see application report SLOA089, *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 图 45, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

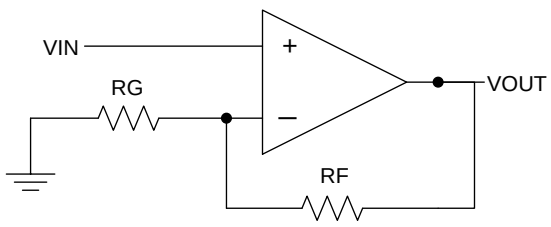


图 44. Schematic Representation

Layout Example (接下页)

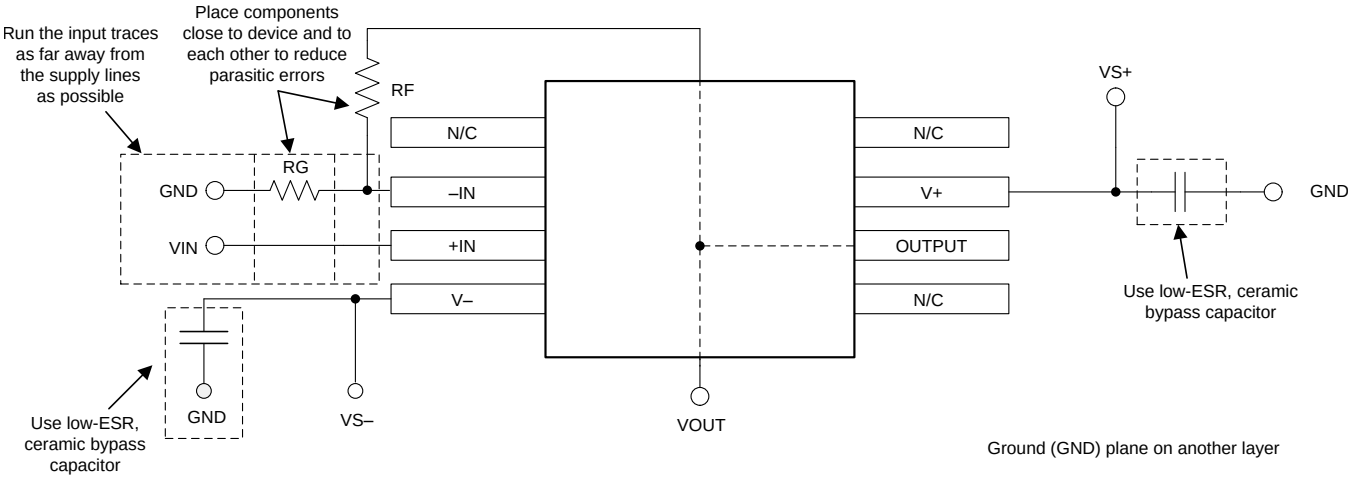


图 45. Operational Amplifier Board Layout for a Noninverting Configuration

11 器件和文档支持

11.1 器件支持

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 开发支持

11.1.2.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。 TINA-TI™ 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.2.2 DIP 适配器 EVM

DIP 适配器 EVM 工具提供了一种简单而低成本的方式来针对小型表面贴装 IC 进行原型设计。评估工具适用于以下 TI 封装：D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (MSOP-8)、DBV（SOT23-6、SOT23-5 和 SOT23-3）、DCK（SC70-6 和 SC70-5）和 DRL (SOT563-6)。DIP 适配器 EVM 也可搭配引脚排使用或直接与现有电路相连。

11.1.2.3 通用运算放大器评估模块 (EVM)

通用运放 EVM 是一系列通用空白电路板，可简化采用各种 IC 封装类型的电路板原型设计。借助评估模块电路板设计，可以轻松快速地构造多种不同电路。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、MSOP、TSSOP 和 SOT23 封装。

注

这些电路板均为空白电路板，用户必须自行提供 IC。TI 建议您在订购通用运放 EVM 时申请几个运放器件样品。

11.1.2.4 TI 高精度设计

TI 高精度设计是由 TI 公司的高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整 PCB 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

器件支持 (接下页)

11.1.2.5 WEBENCH®滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。WEBENCH Filter Designer 通过选择 TI 运算放大器以及 TI 供应商合作伙伴的无源组件来构建优化滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® Filter Designer。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

11.2 文档支持

11.2.1 相关文档

相关文档如下（下载网站 www.ti.com.cn）：

- *《反馈曲线图定义运算放大器交流性能》*（文献编号：SBOA015）
- *《采用隔离电阻的电容式负载驱动器解决方案》*（文献编号：TIPD128）
- *《电路板布局布线技巧》*（文献编号：SLOA089）

11.3 相关链接

表 4 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 4. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
OPA170	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2170	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA4170	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

TINA-TI, E2E are trademarks of Texas Instruments.
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All other trademarks are the property of their respective owners.

11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA170AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O170A	Samples
OPA170AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI	Samples
OPA170AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSVI	Samples
OPA170AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O170A	Samples
OPA170AIDRLR	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAQ	Samples
OPA170AIDRLT	ACTIVE	SOT-5X3	DRL	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DAQ	Samples
OPA2170AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A	Samples
OPA2170AIDCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC	Samples
OPA2170AIDCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPQC	Samples
OPA2170AIDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPNI	Samples
OPA2170AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPNI	Samples
OPA2170AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2170A	Samples
OPA4170AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170	Samples
OPA4170AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4170	Samples
OPA4170AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170	Samples
OPA4170AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4170	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA170 :

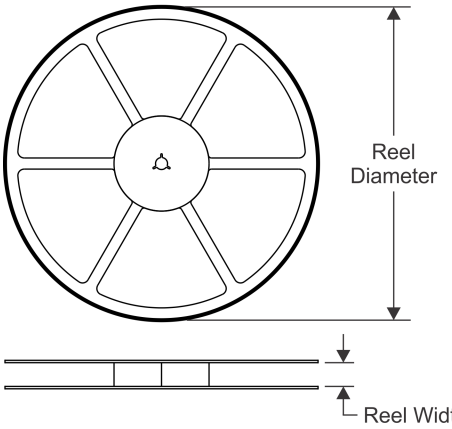
- Enhanced Product: OPA170-EP

NOTE: Qualified Version Definitions:

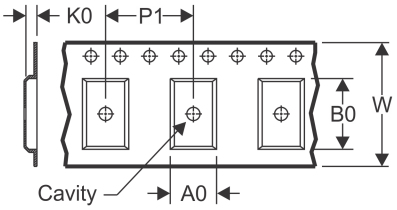
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

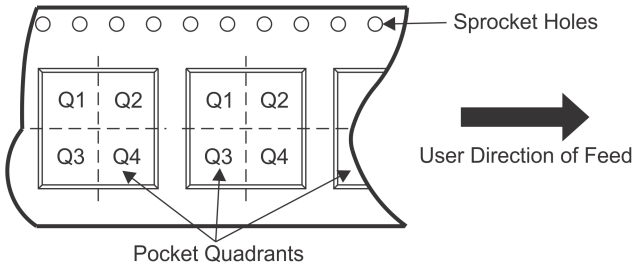


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

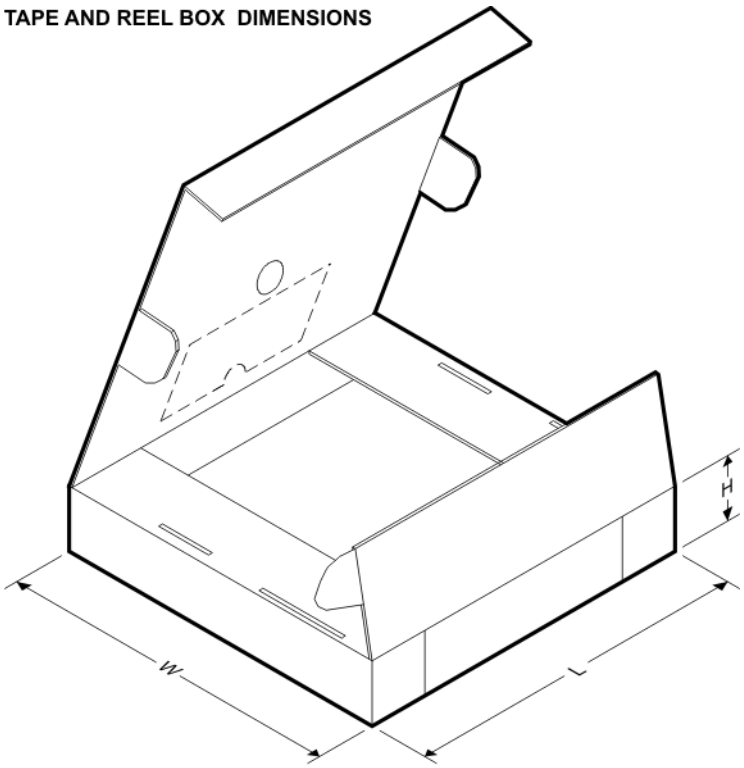
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA170AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA170AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA170AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA170AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA170AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA170AIDRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA170AIDRLT	SOT-5X3	DRL	5	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA2170AIDCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2170AIDCUT	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2170AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2170AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4170AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4170AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

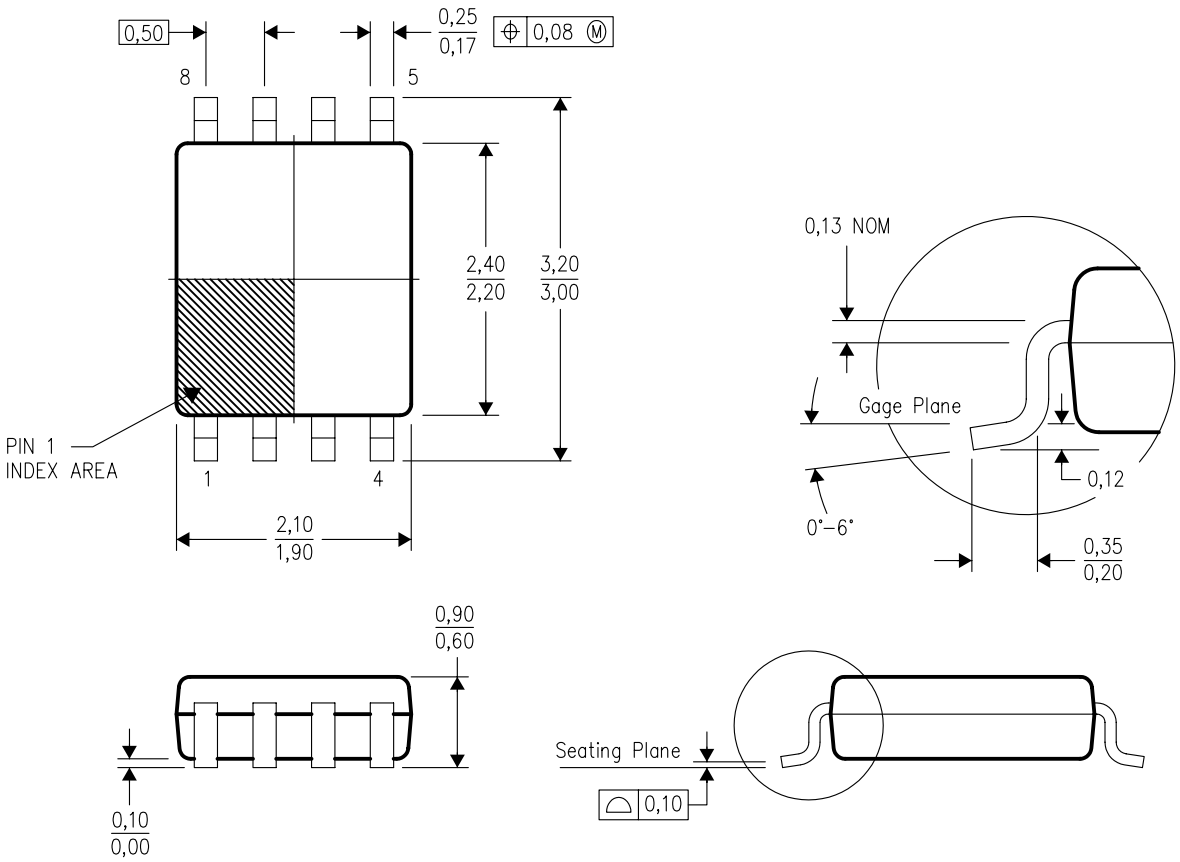
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA170AIDBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
OPA170AIDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA170AIDBVT	SOT-23	DBV	5	250	195.0	200.0	45.0
OPA170AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA170AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA170AIDRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
OPA170AIDRLT	SOT-5X3	DRL	5	250	202.0	201.0	28.0
OPA2170AIDCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
OPA2170AIDCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
OPA2170AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2170AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA4170AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4170AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

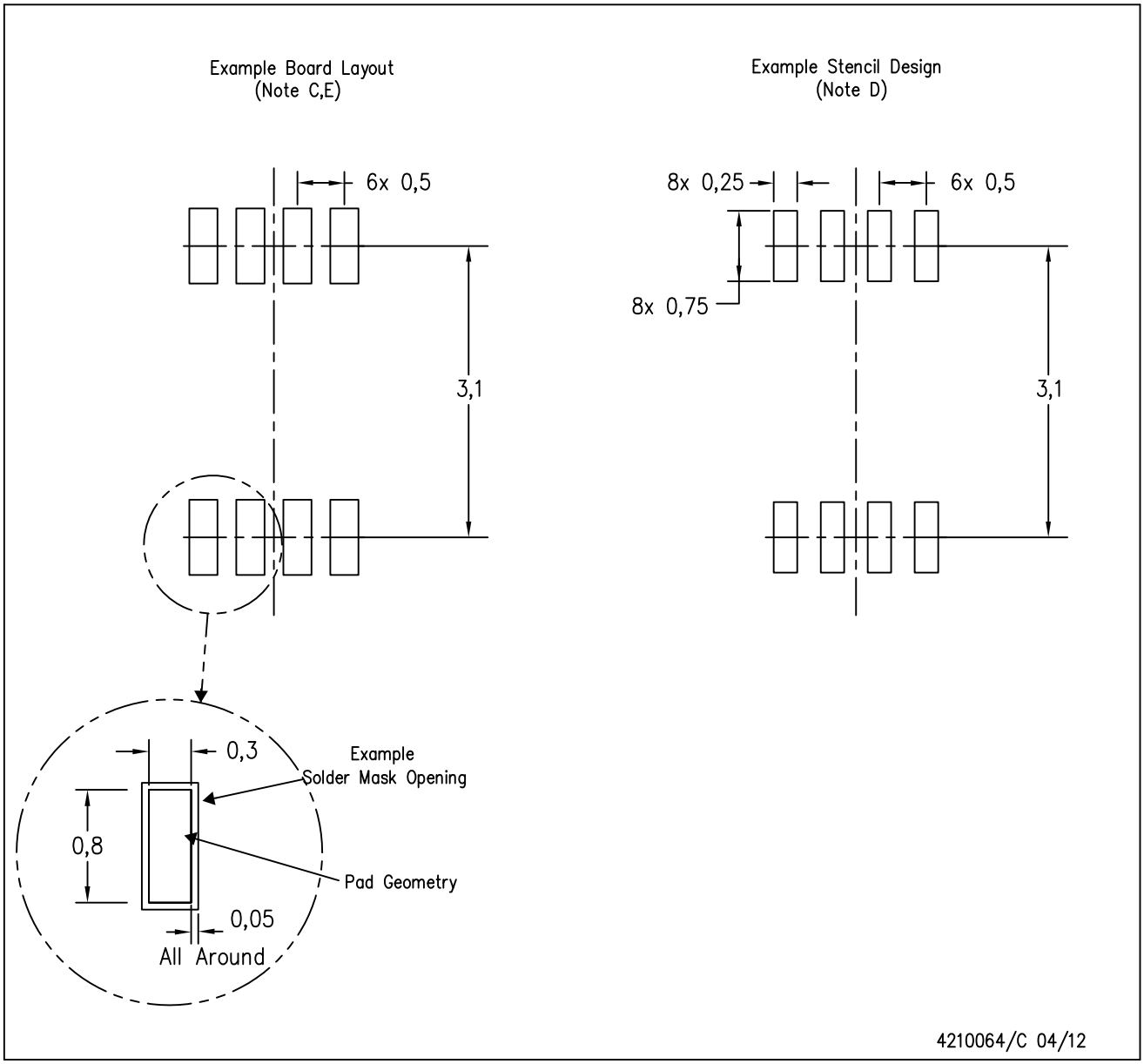
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



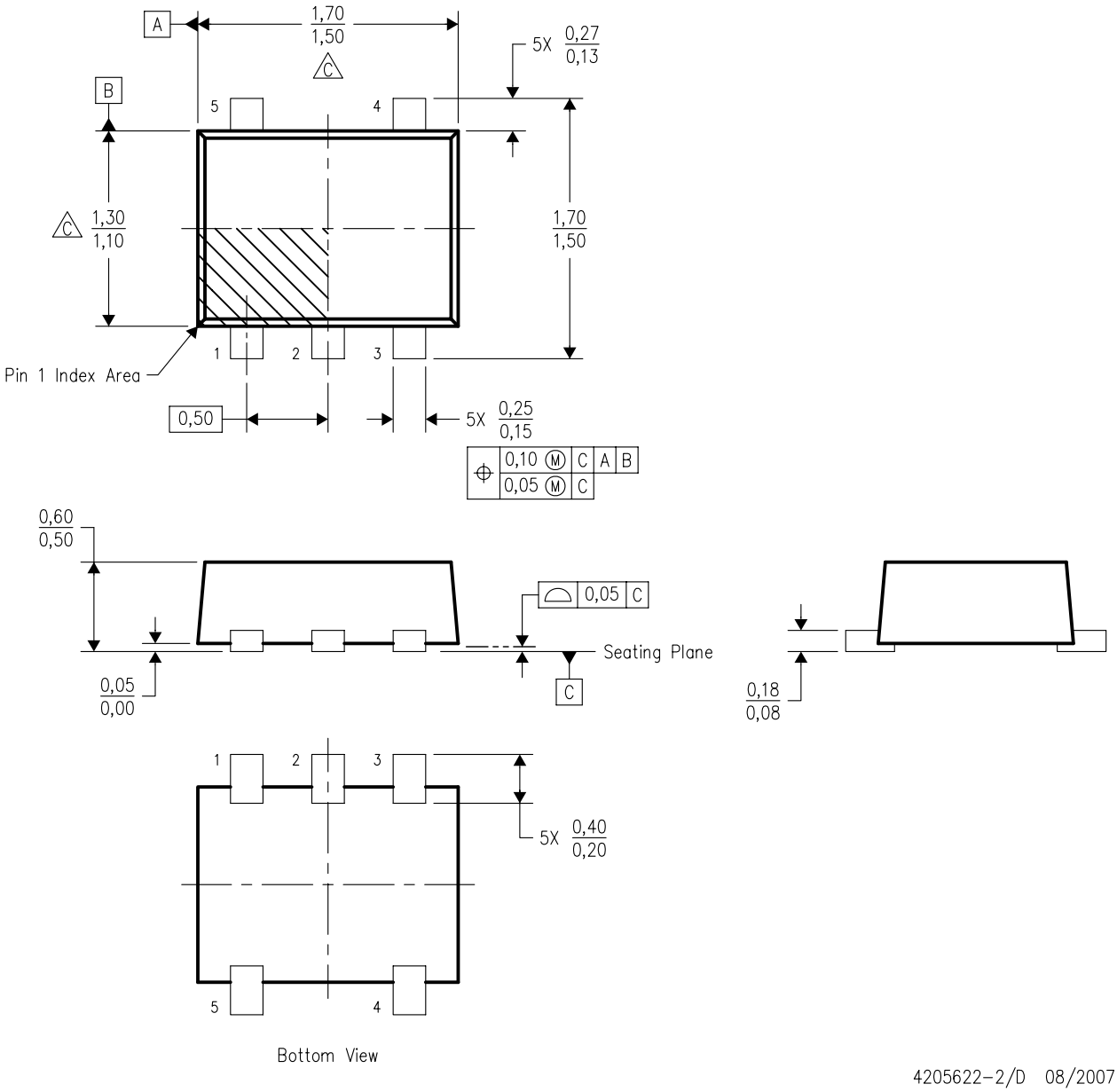
4200503/F 07/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



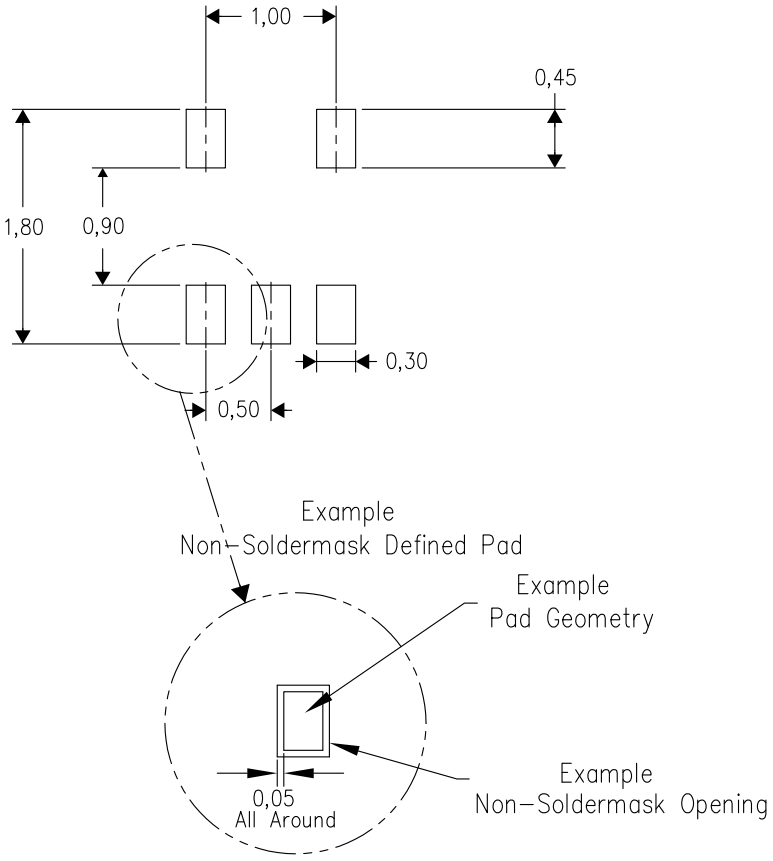
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



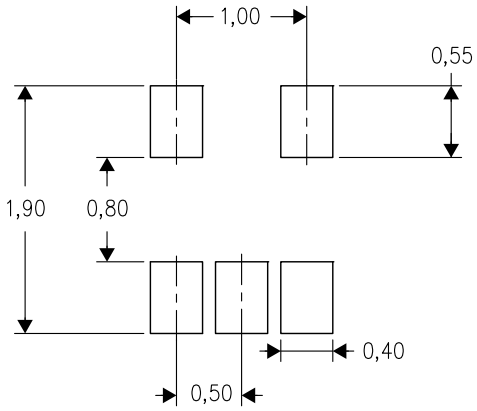
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



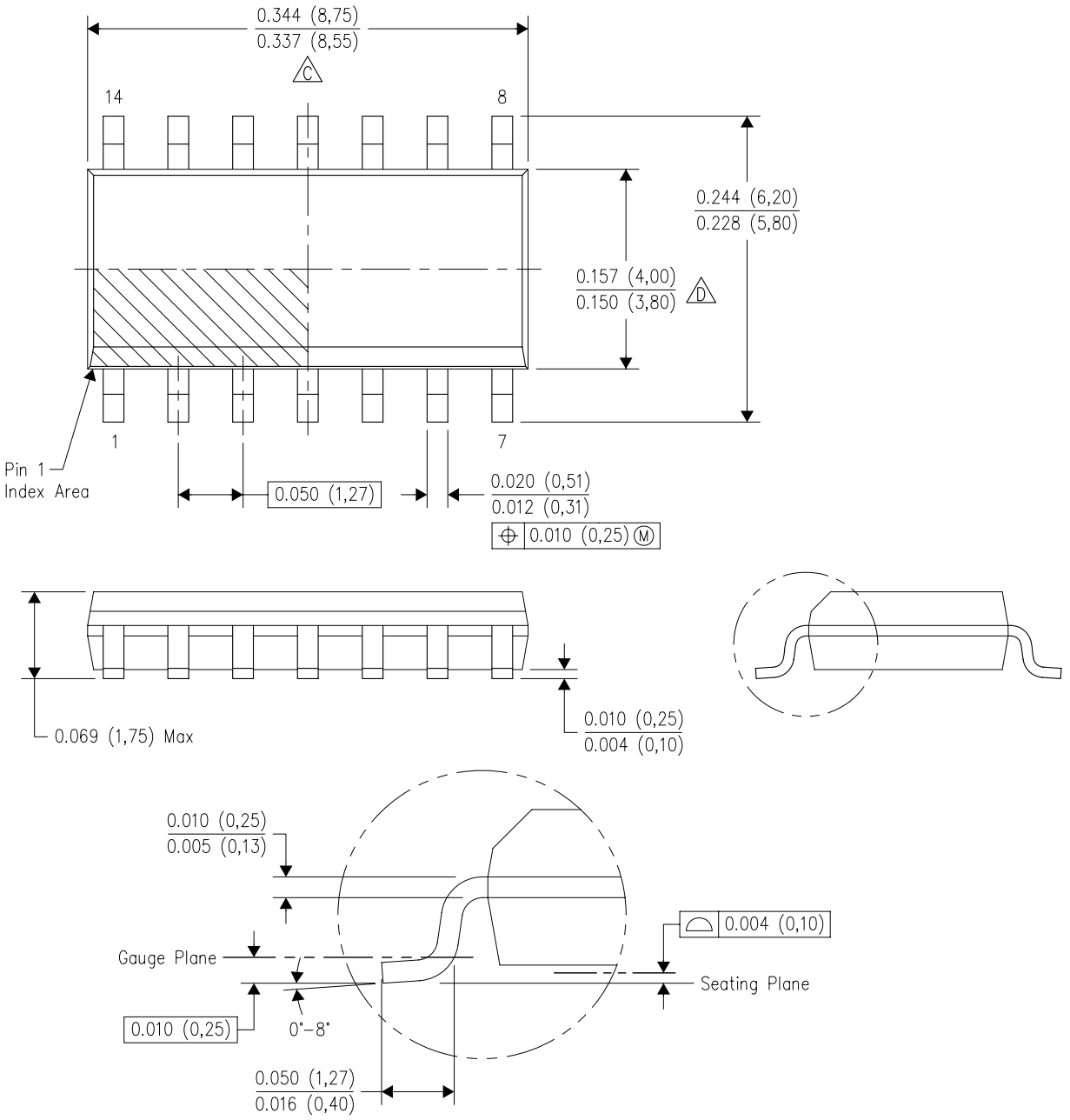
Example Stencil Design
(Note E)



4208207–2/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

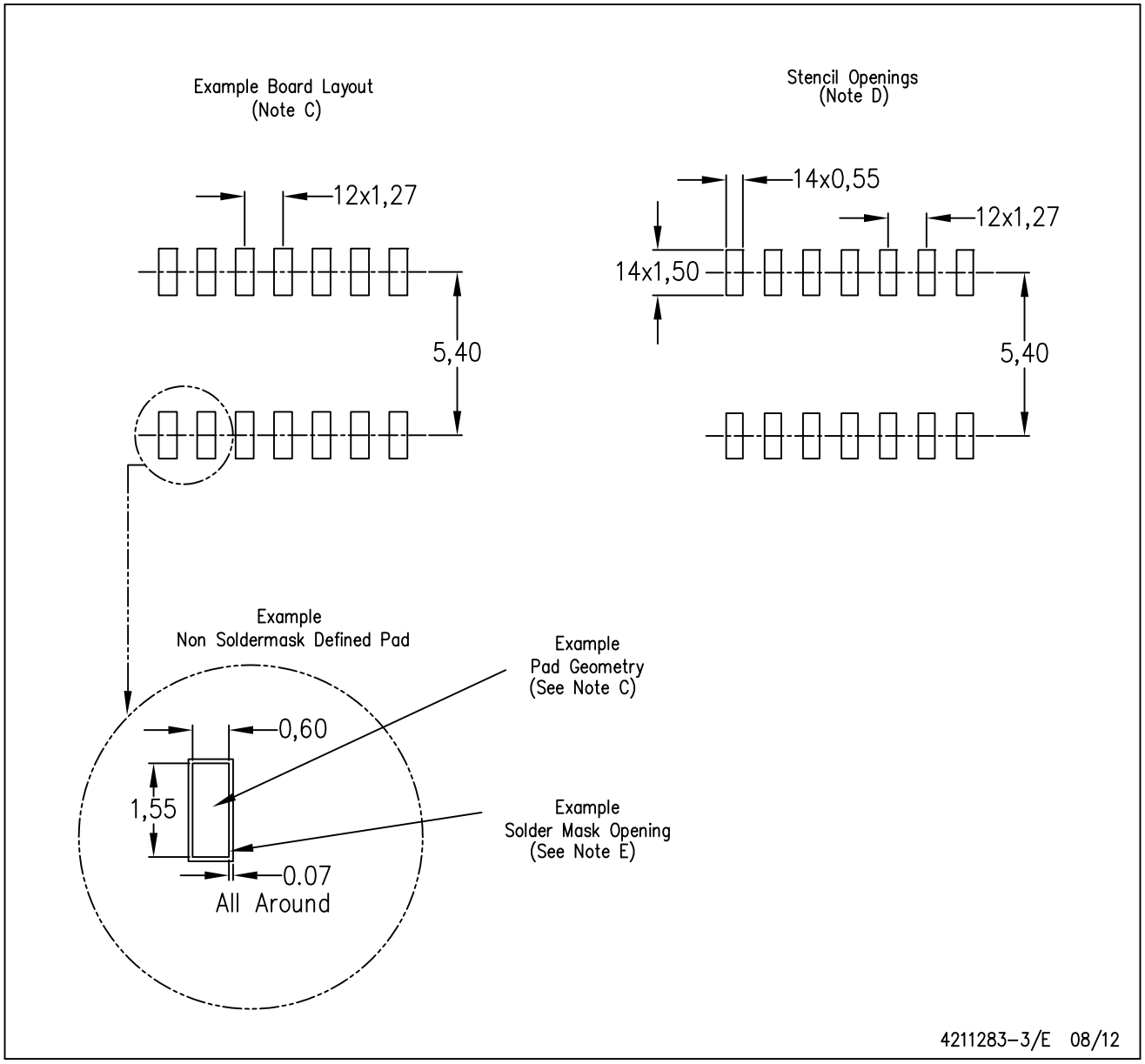
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

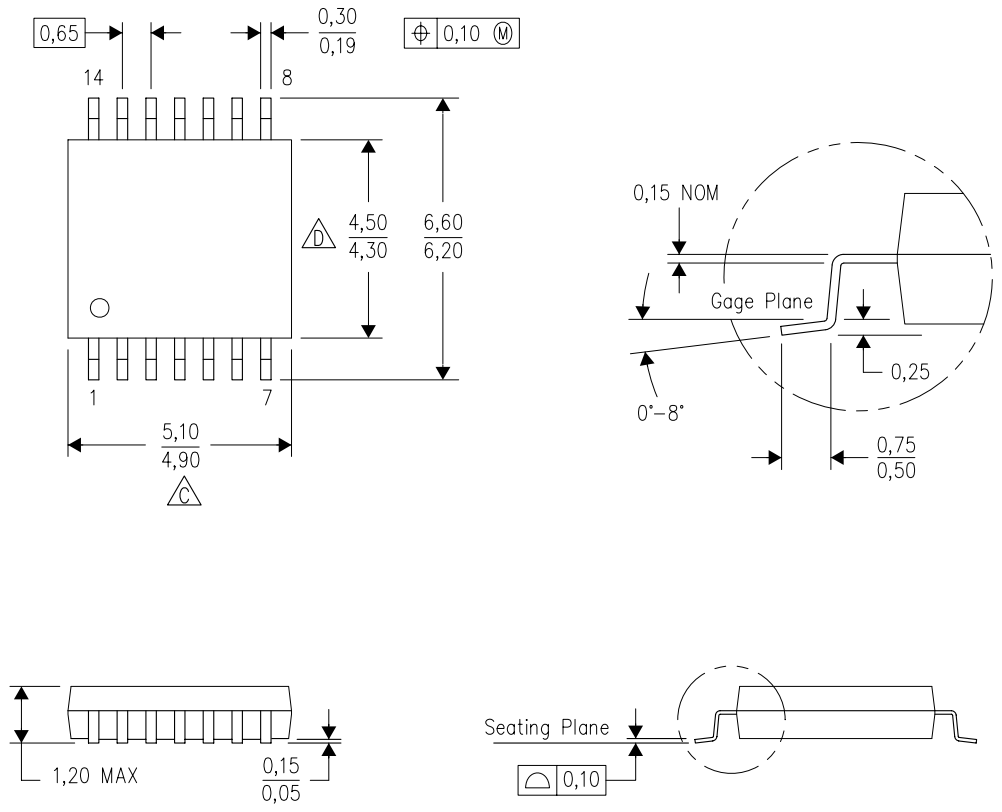
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

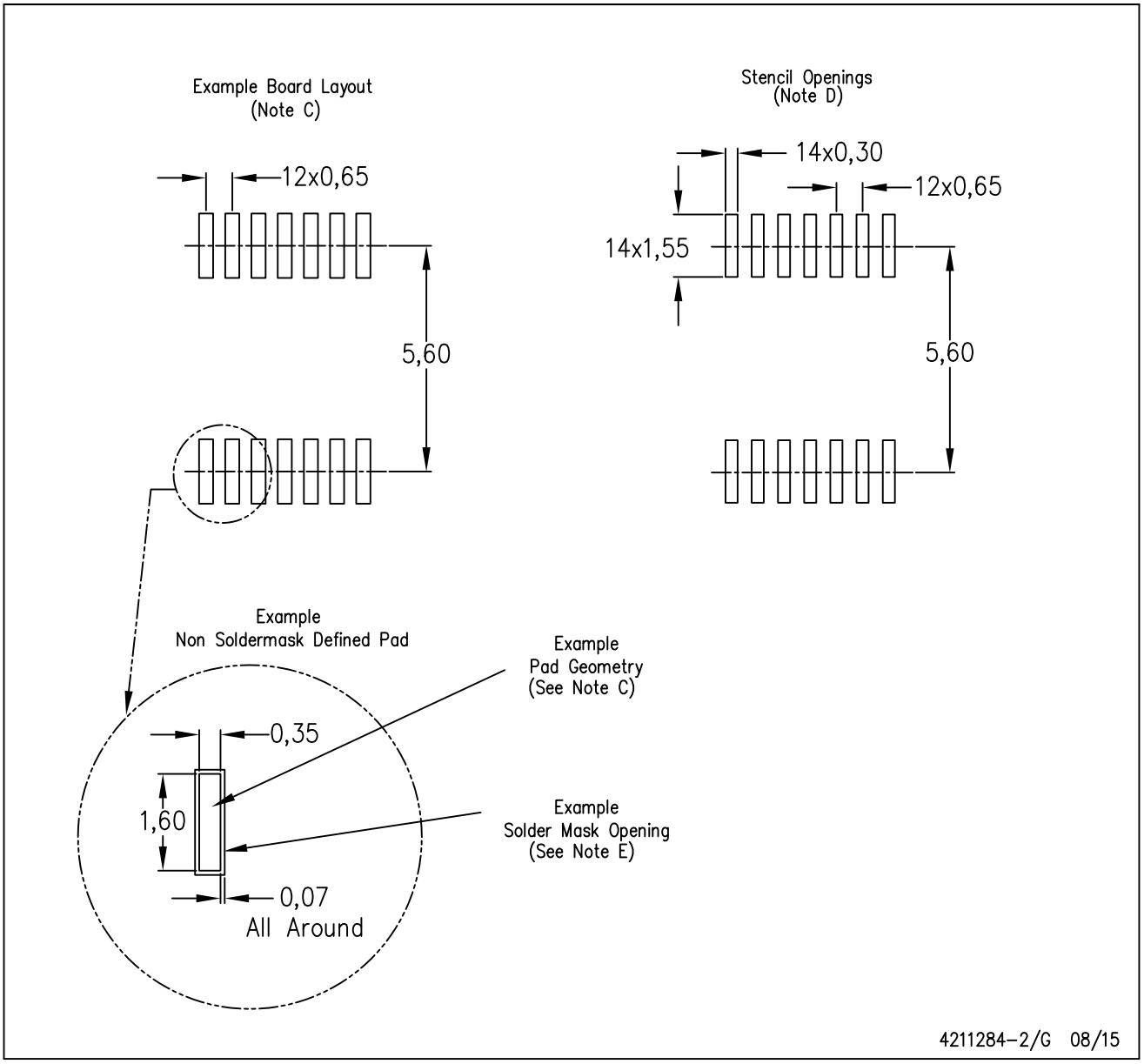
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

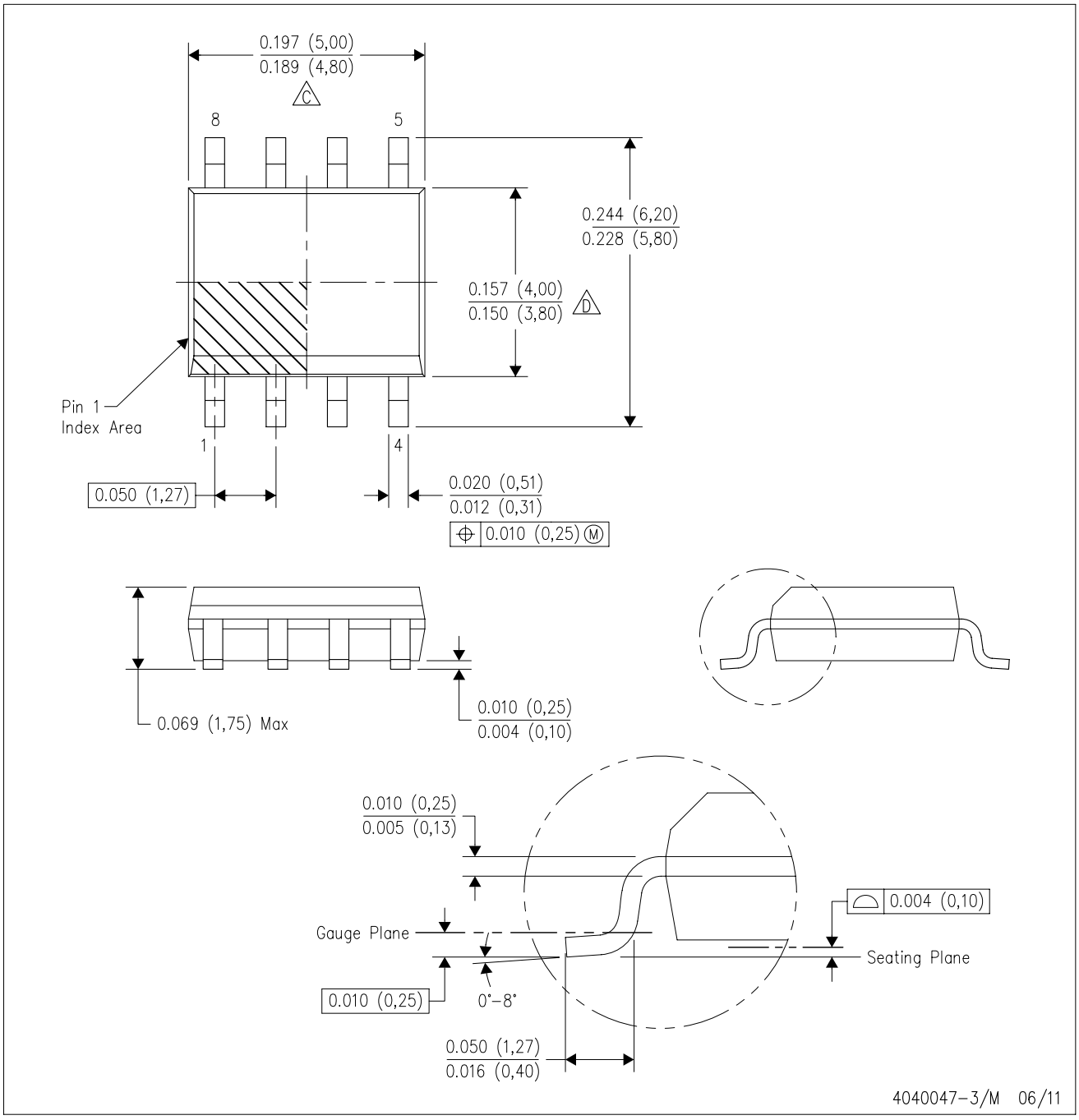
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



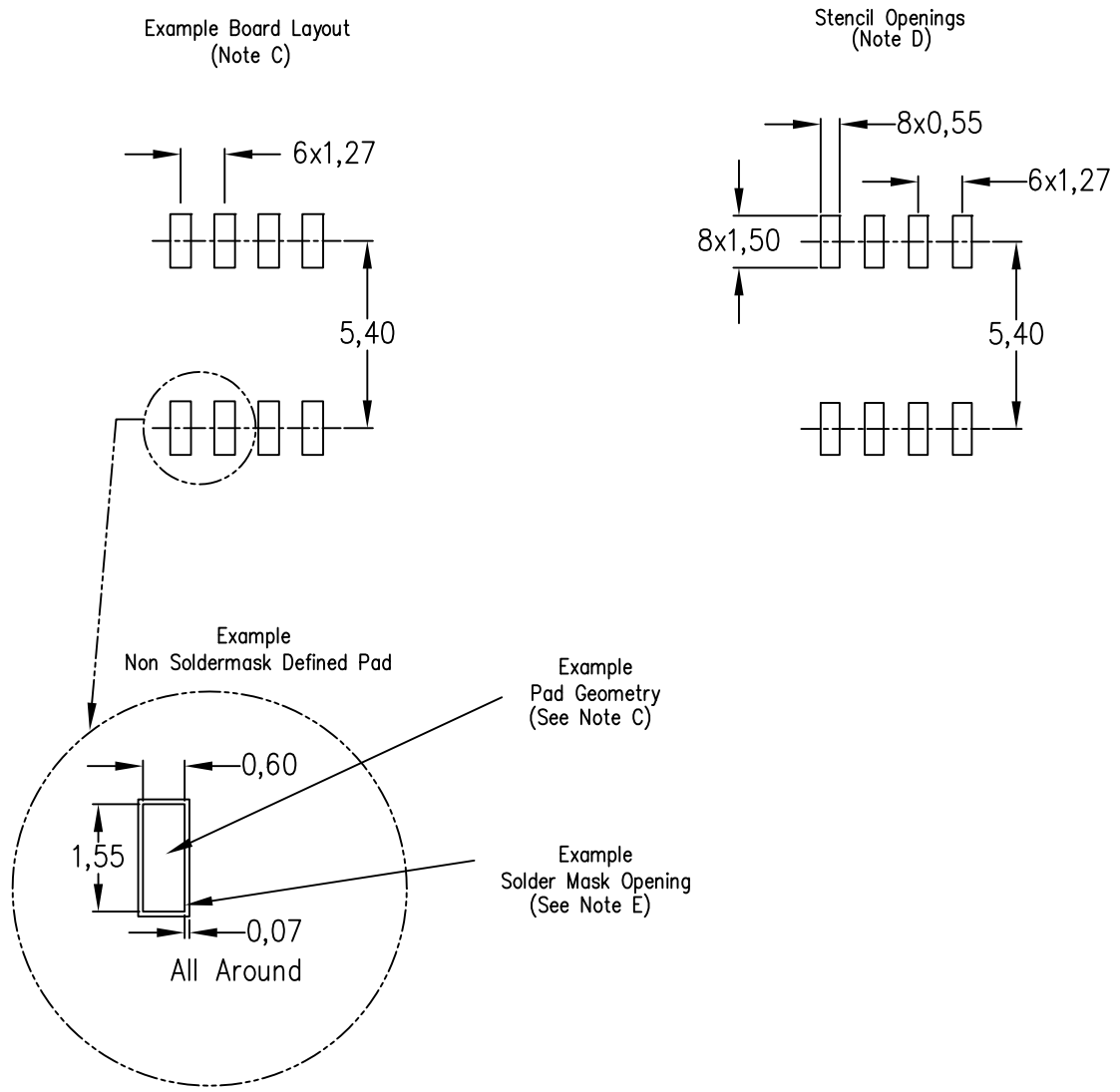
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



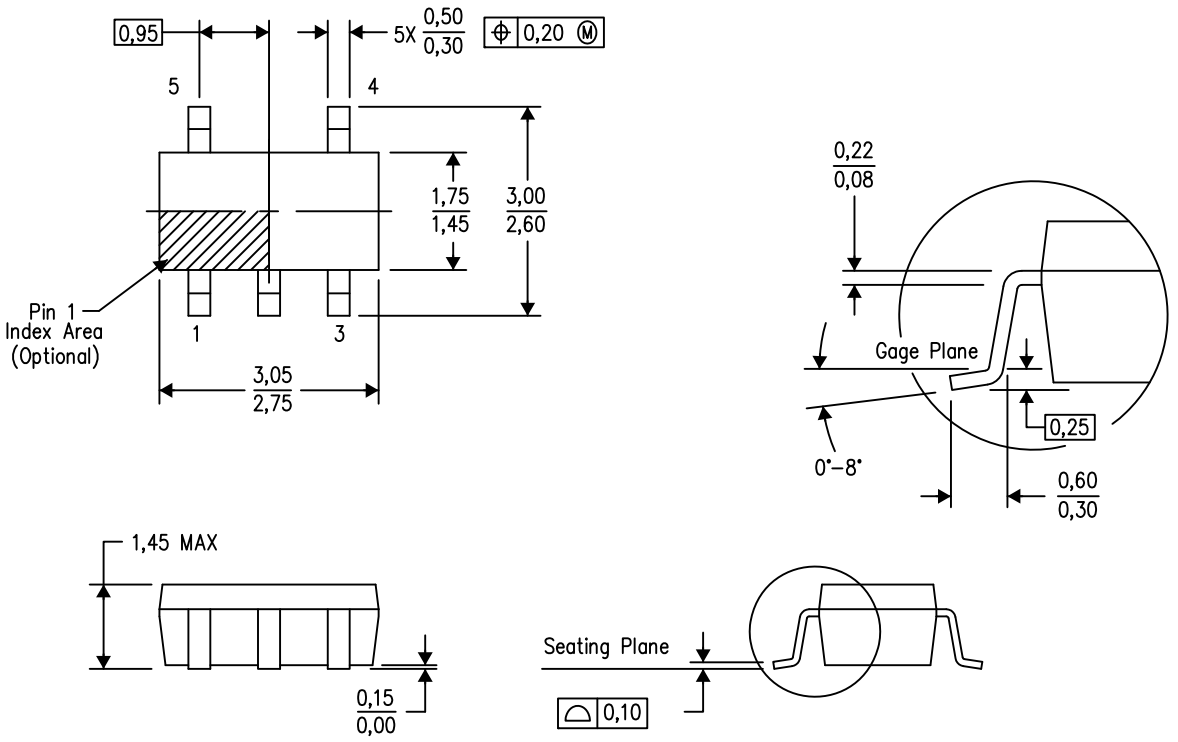
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

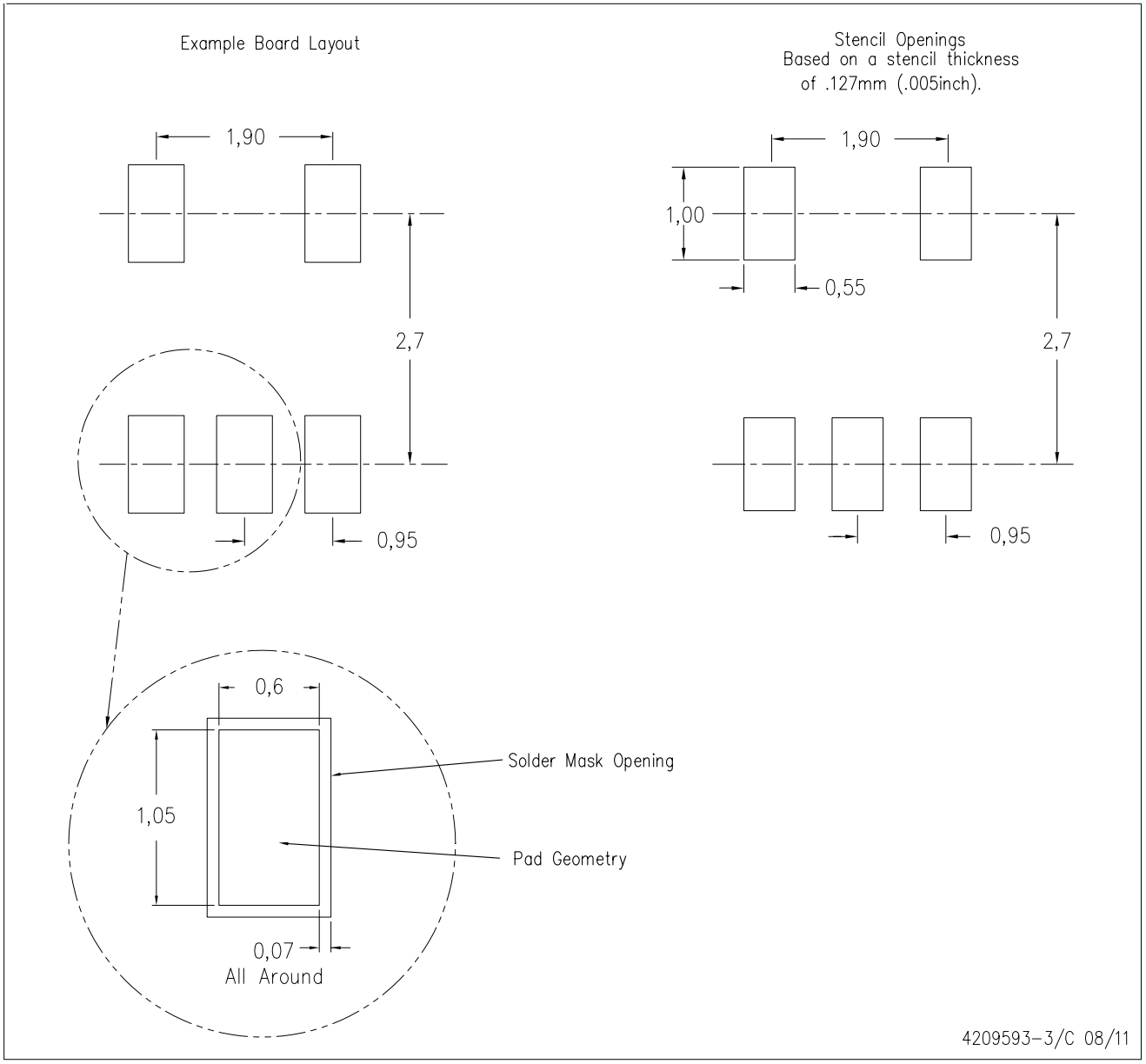
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

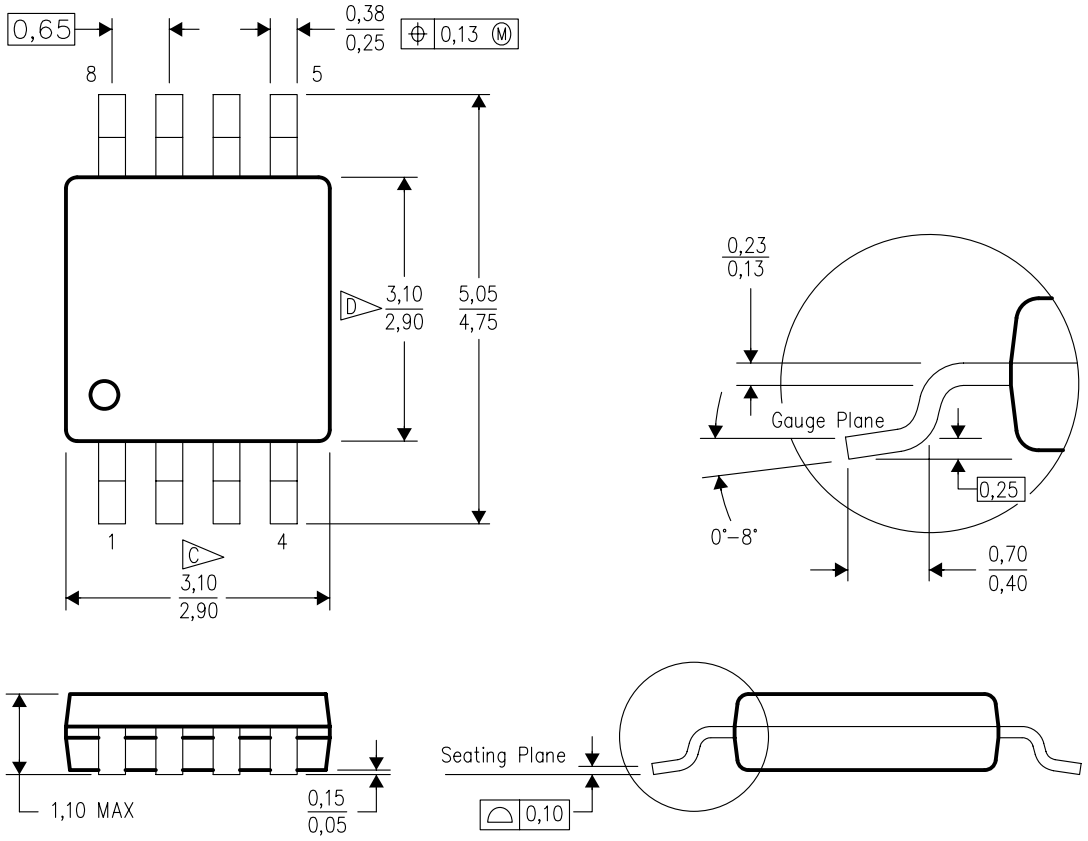
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

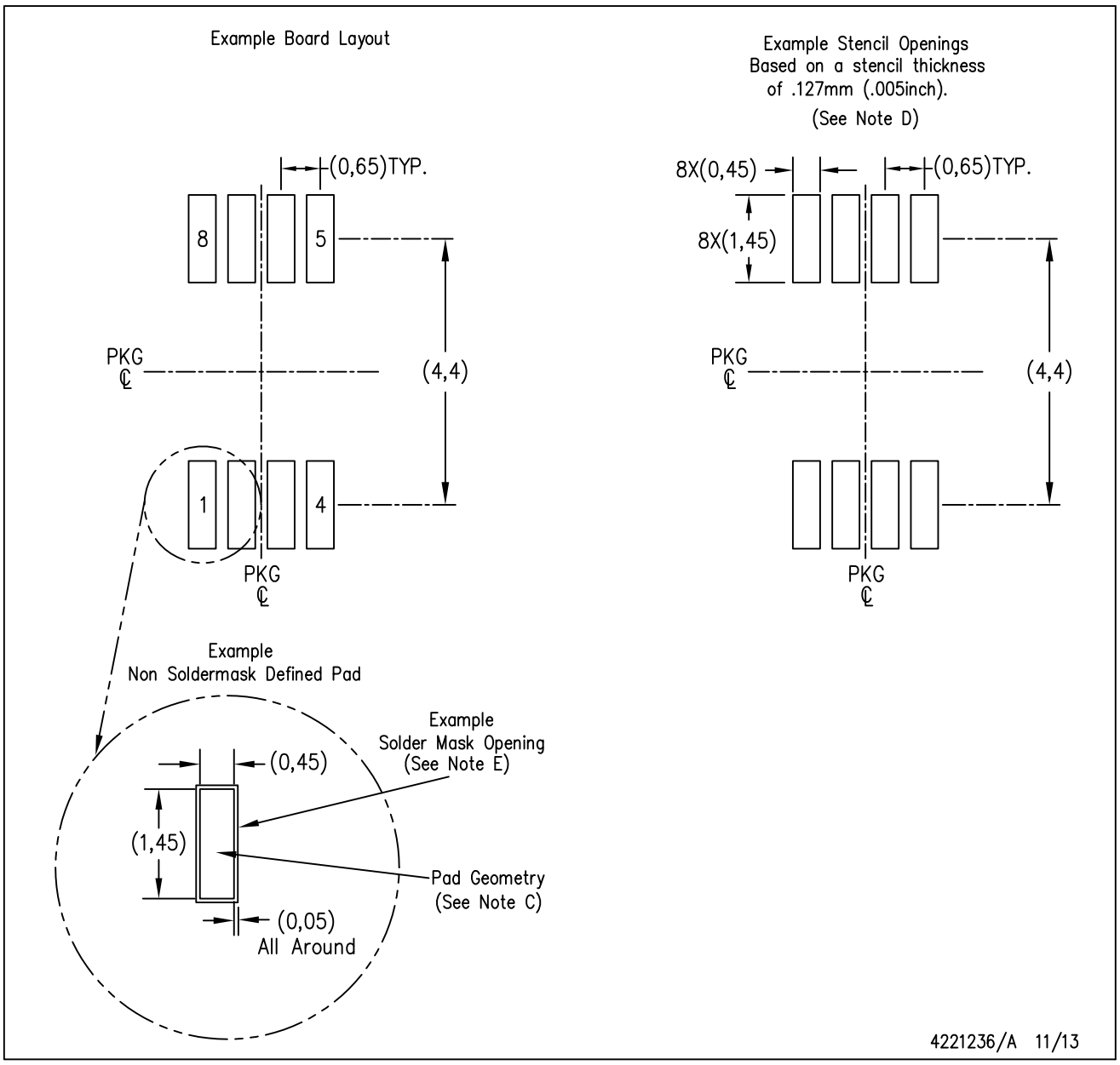
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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