

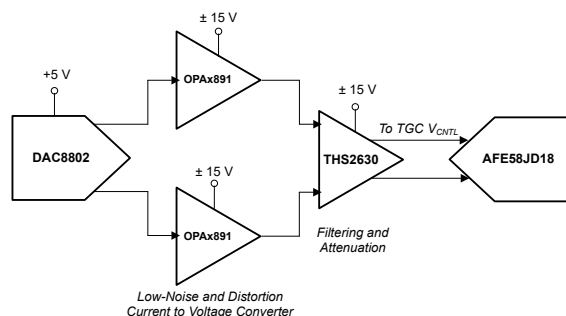
OPAx891, 180 MHz, 0.95 nV/√Hz, Ultra-low THD, Operational Amplifiers

1 Features

- Ultra-low 0.95 nV/√Hz voltage noise
- High Speed:
 - 180-MHz unity gain bandwidth
 - 140-MHz bandwidth [G = 2 (–1), –3 dB]
 - 105-V/μs slew rate
- Very low distortion
 - THD = –91 dBc (f = 1 MHz, R_L = 150 Ω)
 - THD = –100 dBc (f = 1 MHz, R_L = 1 kΩ)
 - THD+N = –137 dBc (f = 1 kHz, BW = 80 kHz)
- Low 0.2-mV (typical) and 1-mV (max) input offset voltage at 25°C
- 200-mA output current drive (typical)
- Typical operation from ±4.5 V to ±18 V
- Offset nulling pins on the OPA891

2 Applications

- Low-noise, wide-band amplifier for industrial applications
- Voltage-controlled oscillators
- Active filters
- Video amplifiers
- Cable drivers
- [Ultrasound Scanners](#)
- [Vector signal transceiver \(VST\)](#)
- [Professional audio mixer or control surface](#)
- [Professional microphones and wireless systems](#)
- [Professional speaker systems](#)
- [Professional audio amplifier](#)
- [Soundbar](#)
- [Turntable](#)
- [Professional video camera](#)
- [Guitar and other instrument amplifier](#)
- [Data acquisition \(DAQ\)](#)



Ultrasound Time-gain-control Circuit

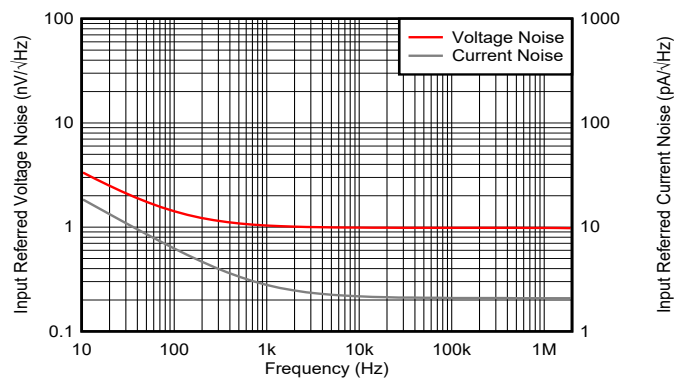
3 Description

The OPA891 and OPA2891 (OPAx891) are ultra-low voltage noise, high-speed voltage feedback amplifiers that are an excellent choice for applications requiring low voltage noise, including communications and imaging. The single-amplifier OPA891 and the dual-amplifier OPA2891 offer very good ac performance with 140-MHz bandwidth (G = 2), 105-V/μs slew rate, and 70-ns settling time (0.1%). The OPAx891 are unity-gain stable with 180-MHz bandwidth. These amplifiers have a high drive capability of 200 mA and draw only 7.5-mA supply current per channel. With –100 dBc of total harmonic distortion (THD) at f = 1 MHz and a very low noise of 0.95 nV/√Hz, the OPAx891 are designed for applications requiring low distortion and low noise such as buffering analog-to-digital converters.

Device Information

PART NUMBER	AMPLIFIERS	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
OPA891	One	D (SOIC, 8)	4.9 mm × 6 mm
		DGN (HVSSOP, 8)	3.0 mm × 4.9 mm
OPA2891 ⁽³⁾	Two	D (SOIC, 8)	4.9 mm × 6 mm
		DGN (HVSSOP, 8)	3.0 mm × 4.9 mm

- (1) For more information, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) Preview information (not Production Data).



Voltage and Current Noise vs Frequency



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4 Pin Configuration and Functions

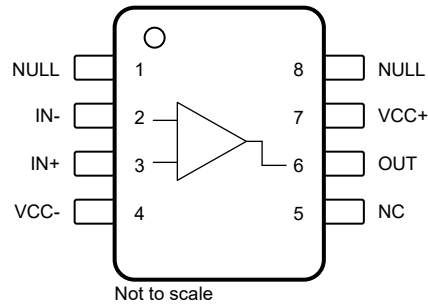


Figure 4-1. OPA891: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

Table 4-1. Pin Functions: OPA891

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN-	2	Input	Inverting input
IN+	3	Input	Non-inverting input
NC	5	—	No connection
NULL	1, 8	Input	Voltage offset adjust
OUT	6	Output	Output of amplifier
VCC-	4	—	Negative power supply
VCC+	7	—	Positive power supply

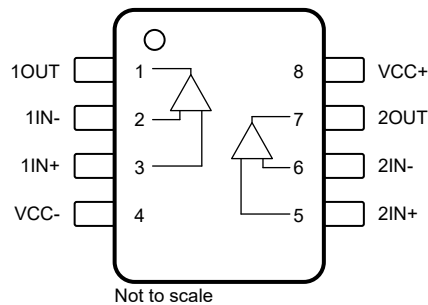


Figure 4-2. OPA2891: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

Table 4-2. Pin Functions: OPA2891

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN-	2	Input	Channel 1 inverting input
1IN+	3	Input	Channel 1 non-inverting input
1OUT	1	Output	Channel 1 output
2IN-	6	Input	Channel 2 inverting input
2IN+	5	Input	Channel 2 non-inverting input
2OUT	7	Output	Channel 2 output
VCC-	4	—	Negative power supply
VCC+	8	—	Positive power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage, V _{CC+} – V _{CC-}		37	V
V _I	Input Voltage		±V _{CC}	
I _O	Output current ⁽²⁾		240	mA
V _{IO}	Differential input voltage		±1.5	V
I _{IN}	Continuous input current		10	mA
T _A	Operating free-air temperature	–40	85	°C
T _J	Junction temperature	Any condition	150	°C
		Maximum junction temperature, continuous operation, long-term reliability ⁽³⁾	125	°C
	Storage temperature T _{stg}	–65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) When continuously operating at any output current, do not exceed the maximum junction temperature. Keep the output current less than the absolute maximum rating regardless of time interval.
- (3) The maximum junction temperature for continuous operation is limited by package constraints. Operation greater than this temperature can result in reduced reliability, lifetime of the device, or both.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±4000
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage	Dual-supply	±4.5	±15	±18	V
		Single-supply	9	30	36	V
T _A	Operating free-air temperature	–40	25	85	°C	

5.4 Thermal Information: OPA891

THERMAL METRIC ⁽¹⁾		OPA891		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	60.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.0	87.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	33	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.6	7.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.3	32.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	17.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Thermal Information: OPA2891

THERMAL METRIC ⁽¹⁾		OPA2891		UNIT
		D (SOIC)	DGN (HVSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.2	56.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.8	48.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.4	37.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.2	2.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61	37.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics: $R_L = 150 \Omega$

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15 \text{ V}$, and $R_L = 150 \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB)	Gain = –1 or 2	$V_{CC} = \pm 15 \text{ V}$		140		MHz
			$V_{CC} = \pm 5 \text{ V}$		135		
	Bandwidth for 0.1-dB flatness	Gain = –1 or 2	$V_{CC} = \pm 15 \text{ V}$		9		
			$V_{CC} = \pm 5 \text{ V}$		9		
SR	Slew rate ⁽¹⁾	Gain = –1	$V_{CC} = \pm 15 \text{ V}$, 20-V step		105		V/ μs
			$V_{CC} = \pm 5 \text{ V}$, 5-V step		90		
t_s	Settling time to 0.1%	Gain = –1	$V_{CC} = \pm 15 \text{ V}$, 5-V step		70		ns
			$V_{CC} = \pm 5 \text{ V}$, 2.5-V step		55		
	Settling time to 0.01%	Gain = –1	$V_{CC} = \pm 15 \text{ V}$, 5-V step		90		ns
			$V_{CC} = \pm 5 \text{ V}$, 2.5-V step		80		
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	Gain = 1, $R_L = 600 \Omega$, $f = 1 \text{ kHz}$, BW = 80 kHz	$V_{CC} = \pm 15 \text{ V}$, $V_O = 3 V_{RMS}$		–137		dB
					0.000014		%
			$V_{CC} = \pm 5 \text{ V}$, $V_O = 1 V_{RMS}$		–130		dB
		Gain = 2, $R_L = 600 \Omega$, $f = 1 \text{ kHz}$, BW = 80 kHz	$V_{CC} = \pm 15 \text{ V}$, $V_O = 3 V_{RMS}$		–133		dB
					0.000022		%
			$V_{CC} = \pm 5 \text{ V}$, $V_O = 1 V_{RMS}$		–124		dB
IMD	Intermodulation distortion	G = 1, $R_L = 600 \Omega$, SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)	$V_{CC} = \pm 15 \text{ V}$, $V_O = 3 V_{RMS}$		–130		dB
					0.000032		%
			$V_{CC} = \pm 5 \text{ V}$, $V_O = 1 V_{RMS}$		–126		dB
		G = 2, $R_L = 600 \Omega$, SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)	$V_{CC} = \pm 15 \text{ V}$, $V_O = 3 V_{RMS}$		–126		dB
					0.00005		%
			$V_{CC} = \pm 5 \text{ V}$, $V_O = 1 V_{RMS}$		–120		dB
		0.0001		%			
NOISE/DISTORTION PERFORMANCE							
THD	Total Harmonic Distortion	G = 2, $V_{CC} = \pm 5 \text{ V}$ or $\pm 15 \text{ V}$, $f = 1 \text{ MHz}$, $V_{O(pp)} = 2 \text{ V}$			–91		dBc
V_n	Input voltage noise	$V_{CC} = \pm 5 \text{ V}$ or $\pm 15 \text{ V}$, $f > 10 \text{ kHz}$			0.95		nV/ $\sqrt{\text{Hz}}$
I_n	Input current noise	$V_{CC} = \pm 5 \text{ V}$ or $\pm 15 \text{ V}$, $f > 10 \text{ kHz}$			2.3		pA/ $\sqrt{\text{Hz}}$
	Channel-to-channel crosstalk (OPA2891 only)	$V_{CC} = \pm 5 \text{ V}$ or $\pm 15 \text{ V}$, $f = 1 \text{ MHz}$			–80		dBc
DC PERFORMANCE							
V_{OS}	Input offset voltage	$V_{CC} = \pm 5 \text{ V}$ or $\pm 15 \text{ V}$	$T_A = 25^\circ\text{C}$		0.2	1	mV
	Offset voltage drift	$V_{CC} = \pm 5 \text{ V}$ or $\pm 15 \text{ V}$	$T_A = \text{full range}$		1		$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input bias current	$V_{CC} = \pm 5 \text{ V}$ or $\pm 15 \text{ V}$	$T_A = 25^\circ\text{C}$		9	20	μA
			$T_A = \text{full range}$			33	
I_{OS}	Input offset current	$V_{CC} = \pm 5 \text{ V}$ or $\pm 15 \text{ V}$	$T_A = 25^\circ\text{C}$		30	250	nA
			$T_A = \text{full range}$			400	
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	$V_{CC} = \pm 15 \text{ V}$		± 13.8	± 14.3		V
		$V_{CC} = \pm 5 \text{ V}$		± 3.8	± 4.3		V

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, and $R_L = 150\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	$V_{CC} = \pm 15\text{ V}$, $V_{ICR} = \pm 12\text{ V}$	$T_A = 25^\circ\text{C}$	85	104		dB
			$T_A = \text{full range}$	80			dB
		$V_{CC} = \pm 5\text{ V}$, $V_{ICR} = \pm 2.5\text{ V}$	$T_A = 25^\circ\text{C}$	90	106		dB
			$T_A = \text{full range}$	85			dB
	Input impedance	Common-mode		10 1.2			M Ω pF
		Differential-mode		6 1.8			k Ω pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	$V_{CC} = \pm 15\text{ V}$	$R_L = 250\ \Omega$	± 12	± 12.9		V
		$V_{CC} = \pm 5\text{ V}$		± 3	± 3.5		V
I_O	Output current ⁽²⁾	$R_L = 10\ \Omega$	$V_{CC} = \pm 15\text{ V}$	160	200		mA
			$V_{CC} = \pm 5\text{ V}$	120	160		mA
R_O	Output resistance	Open loop		5			Ω
POWER SUPPLY							
V_{CC}	Supply voltage operating range	Dual supply	Dual supply	± 4.5		± 18	V
		Single supply	Single supply	9		36	V
I_{CC}	Supply current (each amplifier)	$V_{CC} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$		7.5	10	mA
			$T_A = \text{full range}$			11	mA
		$V_{CC} = \pm 5\text{ V}$	$T_A = 25^\circ\text{C}$		6.5	9	mA
			$T_A = \text{full range}$			10	mA
PSRR	Power-supply rejection ratio	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	90	105		dB
		$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$	$T_A = \text{full range}$	85			dB

(1) Slew rate is measured from an output level range of 25% to 75%.

(2) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also [Section 5.1](#)

5.7 Electrical Characteristics: $R_L = 1\text{ k}\Omega$

at $T_A = \text{full range}$, $V_{CC} = \pm 15\text{ V}$, and $R_L = 1\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Unity gain bandwidth	$V_{CC} = \pm 15\text{ V}$, closed loop			180		MHz
	Small-signal bandwidth (-3 dB)	Gain = -1 or 2	$V_{CC} = \pm 15\text{ V}$		140		MHz
			$V_{CC} = \pm 5\text{ V}$		135		MHz
	Bandwidth for 0.1-dB flatness	Gain = -1 or 2	$V_{CC} = \pm 15\text{ V}$		9		MHz
			$V_{CC} = \pm 5\text{ V}$		9		MHz
Full power bandwidth ⁽¹⁾	$V_{CC} = \pm 15\text{ V}$, $V_{O(pp)} = 20\text{ V}$			1.7		MHz	
	$V_{CC} = \pm 5\text{ V}$, $V_{O(pp)} = 5\text{ V}$			5.7		MHz	
SR	Slew rate				105		V/ μs
t_s	Settling time to 0.1%	Gain = -1	$V_{CC} = \pm 15\text{ V}$, 5-V step		70		ns
			$V_{CC} = \pm 5\text{ V}$, 2.5-V step		55		
	Settling time to 0.01%	Gain = -1	$V_{CC} = \pm 15\text{ V}$, 5-V step		90		ns
			$V_{CC} = \pm 5\text{ V}$, 2.5-V step		80		
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	Gain = 1, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, BW = 80 kHz	$V_{CC} = \pm 15\text{ V}$, $V_O = 3\text{ V}_{RMS}$		-137		dB
					0.000014		%
			$V_{CC} = \pm 5\text{ V}$, $V_O = 1\text{ V}_{RMS}$		-130		dB
		Gain = 2, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, BW = 80 kHz	$V_{CC} = \pm 15\text{ V}$, $V_O = 3\text{ V}_{RMS}$		-133		dB
					0.000022		%
			$V_{CC} = \pm 5\text{ V}$, $V_O = 1\text{ V}_{RMS}$		-124		dB
			0.00006		%		

5.7 Electrical Characteristics: $R_L = 1\text{ k}\Omega$ (continued)

at $T_A = \text{full range}$, $V_{CC} = \pm 15\text{ V}$, and $R_L = 1\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IMD	Intermodulation distortion	G = 1, $R_L = 2\text{ k}\Omega$, $V_O = 1\text{ V}_{\text{RMS}}$, SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)	$V_{CC} = \pm 15\text{ V}$, $V_O = 3\text{ V}_{\text{RMS}}$	-130			dB
			$V_{CC} = \pm 5\text{ V}$, $V_O = 1\text{ V}_{\text{RMS}}$	0.000032			%
				-126			dB
		G = 2, $R_L = 2\text{ k}\Omega$, SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)	$V_{CC} = \pm 15\text{ V}$, $V_O = 3\text{ V}_{\text{RMS}}$	-126			dB
			$V_{CC} = \pm 5\text{ V}$, $V_O = 1\text{ V}_{\text{RMS}}$	0.00005			%
				-120			dB
			0.0001			%	
NOISE/DISTORTION PERFORMANCE							
THD	Total harmonic distortion	G = 2, $V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$, $f = 1\text{ MHz}$, $V_{O(\text{pp})} = 2\text{ V}$			-100		dBc
DC PERFORMANCE							
	Open loop gain	$V_{CC} = \pm 15\text{ V}$, $V_O = \pm 10\text{ V}$	$T_A = 25^\circ\text{C}$	93	100		dB
			$T_A = \text{full range}$	92			
		$V_{CC} = \pm 5\text{ V}$, $V_O = \pm 2.5\text{ V}$	$T_A = 25^\circ\text{C}$	92	98		
			$T_A = \text{full range}$	91			
V_{OS}	Input offset voltage	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$	$T_A = 25^\circ\text{C}$		0.2	1	mV
V_{OS}	Offset voltage drift	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$	$T_A = \text{full range}$			1	$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input bias current	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$	$T_A = 25^\circ\text{C}$		9	20	μA
			$T_A = \text{full range}$			33	
I_{OS}	Input offset current	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$	$T_A = 25^\circ\text{C}$		30	250	μA
			$T_A = \text{full range}$			400	
	Input offset current drift	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$	$T_A = \text{full range}$			0.2	$\text{nA}/^\circ\text{C}$
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	$V_{CC} = \pm 15\text{ V}$		± 13.8	± 14.3		V
		$V_{CC} = \pm 5\text{ V}$		± 3.8	± 4.3		
CMRR	Common-mode rejection ratio	$V_{CC} = \pm 15\text{ V}$, $V_{ICR} = \pm 12\text{ V}$	$T_A = 25^\circ\text{C}$	85	104		dB
			$T_A = \text{full range}$	80			
		$V_{CC} = \pm 5\text{ V}$, $V_{ICR} = \pm 2.5\text{ V}$	$T_A = 25^\circ\text{C}$	90	106		
			$T_A = \text{full range}$	85			
	Input impedance	Common-mode			$10 \parallel 1.2$		$\text{M}\Omega \parallel \text{pF}$
		Differential-mode				$6 \parallel 1.8$	
V_{ICR}	Common-mode input voltage range	$V_{CC} = \pm 15\text{ V}$		± 13.8	± 14.3		V
		$V_{CC} = \pm 5\text{ V}$		± 3.8	± 4.3		
CMRR	Common-mode rejection ratio	$V_{CC} = \pm 15\text{ V}$, $V_{ICR} = \pm 12\text{ V}$	$T_A = 25^\circ\text{C}$	85	104		dB
			$T_A = \text{full range}$	80			
		$V_{CC} = \pm 5\text{ V}$, $V_{ICR} = \pm 2.5\text{ V}$	$T_A = 25^\circ\text{C}$	90	106		
			$T_A = \text{full range}$	85			
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	$V_{CC} = \pm 15\text{ V}$		± 13	± 13.6		V
		$V_{CC} = \pm 5\text{ V}$		± 3.4	± 3.8		
POWER SUPPLY							
PSRR	Power-supply rejection ratio	$V_{CC} = \pm 5\text{ V}$ or $\pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	90	105		dB
			$T_A = \text{full range}$	85			

(1) Full power bandwidth = slew rate / $[\pi V_{O(\text{P-P})}]$.

5.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)

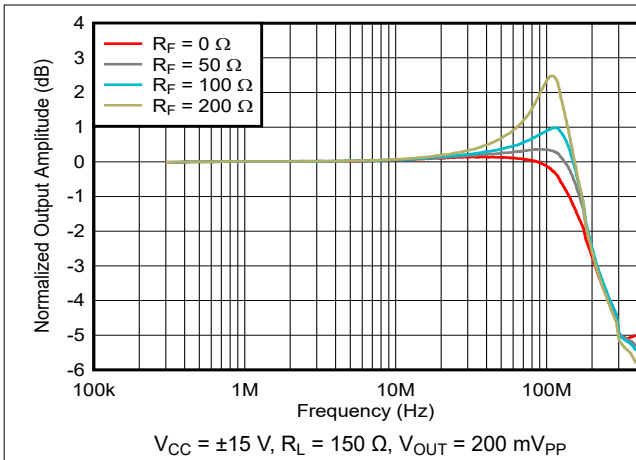


Figure 5-1. Frequency Response vs Feedback Resistance

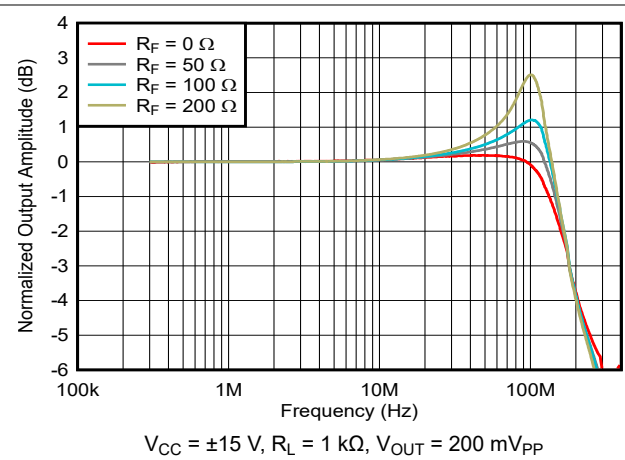


Figure 5-2. Frequency Response vs Feedback Resistance

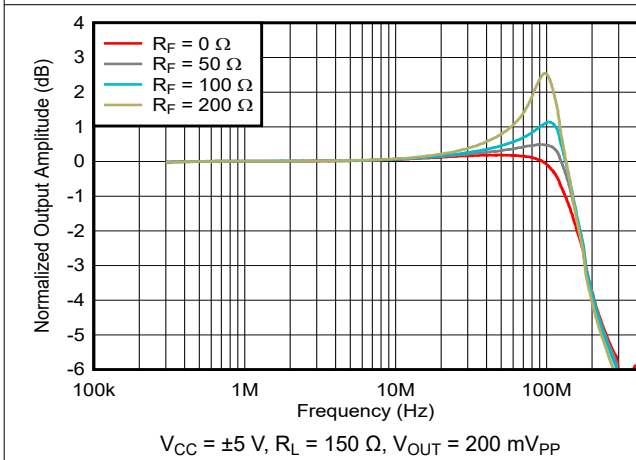


Figure 5-3. Frequency Response vs Feedback Resistance

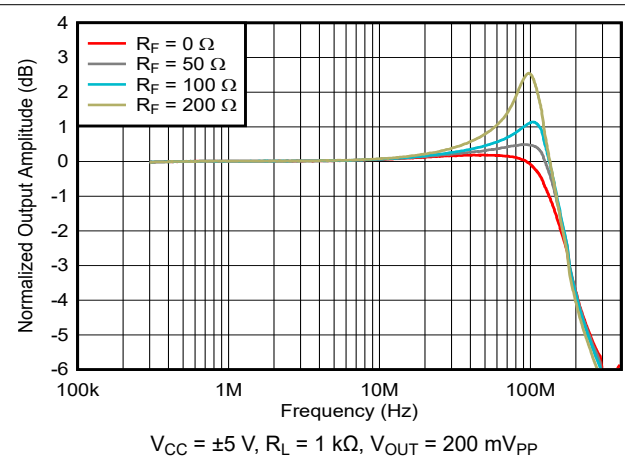


Figure 5-4. Frequency Response vs Feedback Resistance

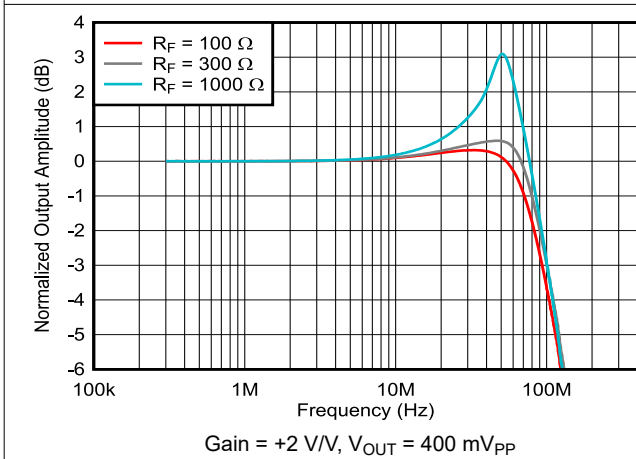


Figure 5-5. Frequency Response vs Feedback Resistance

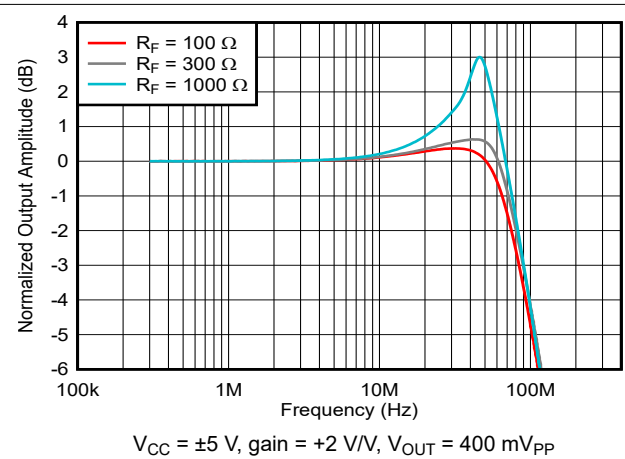


Figure 5-6. Frequency Response vs Feedback Resistance

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)

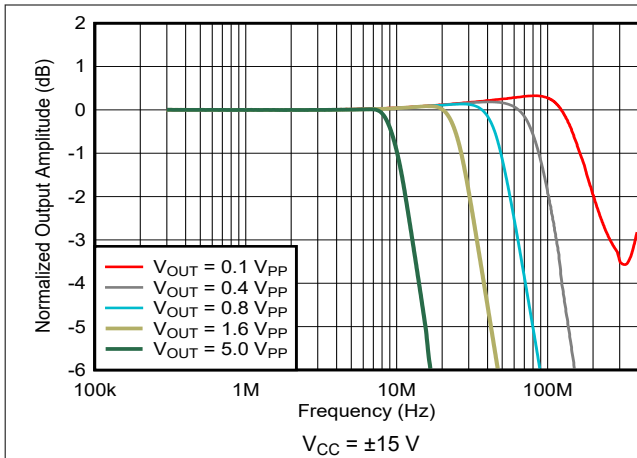


Figure 5-7. Large-signal Frequency Response

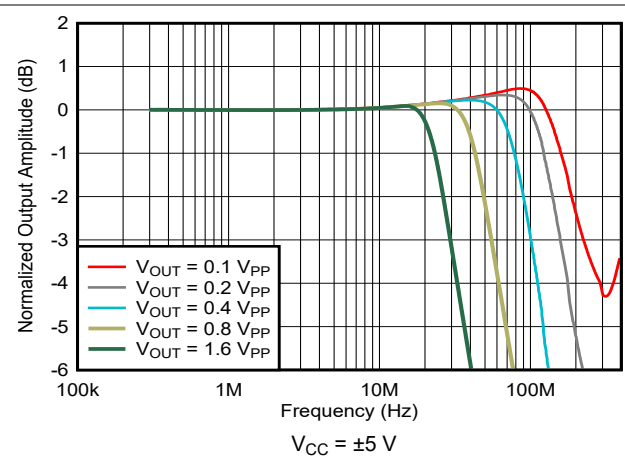


Figure 5-8. Large-signal Frequency Response

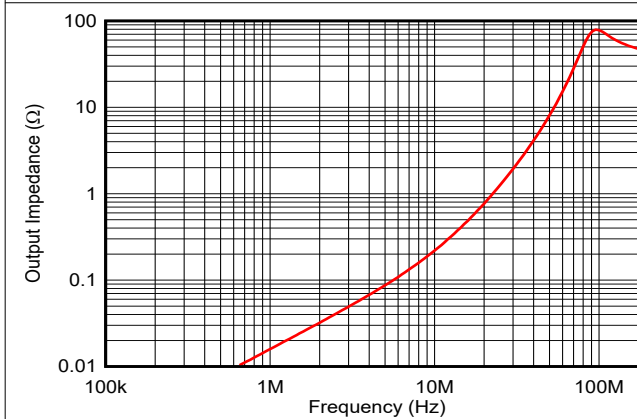


Figure 5-9. Closed-loop Output Impedance

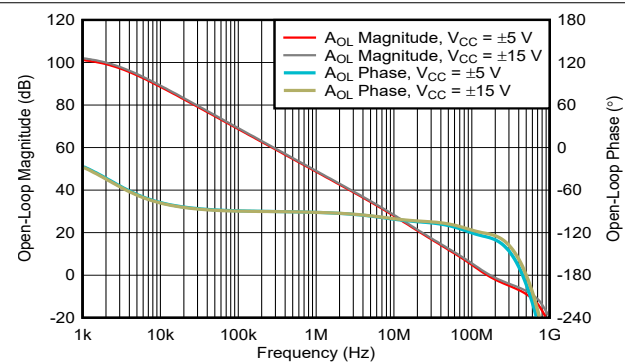


Figure 5-10. Open-loop Gain and Phase Response

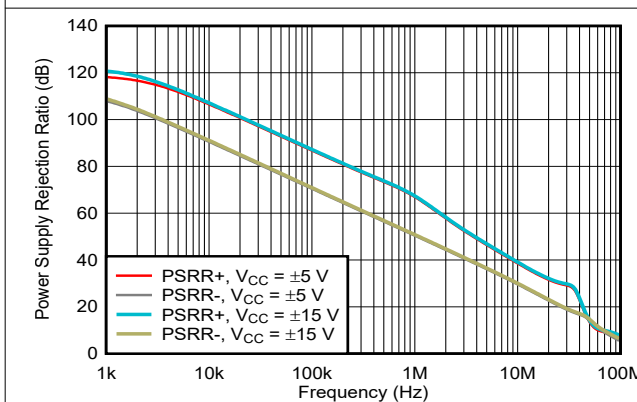


Figure 5-11. Power-supply Rejection Ratio vs Frequency

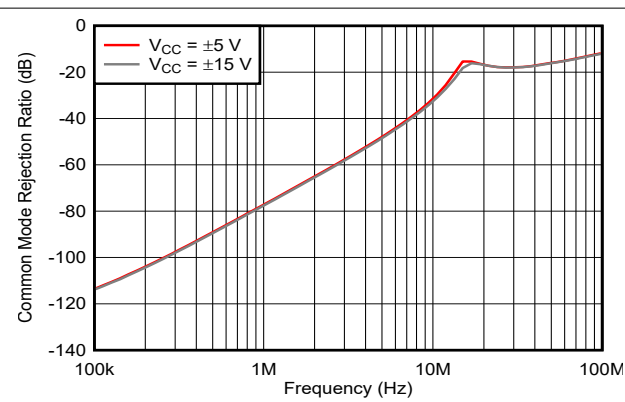


Figure 5-12. Common-mode Rejection Ratio vs Frequency

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)

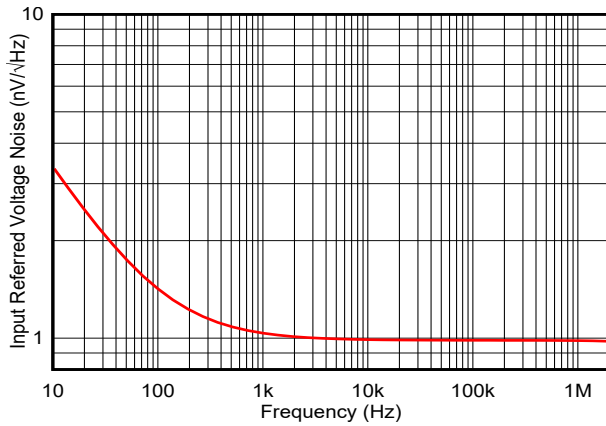


Figure 5-13. Input-referred Voltage Noise vs Frequency

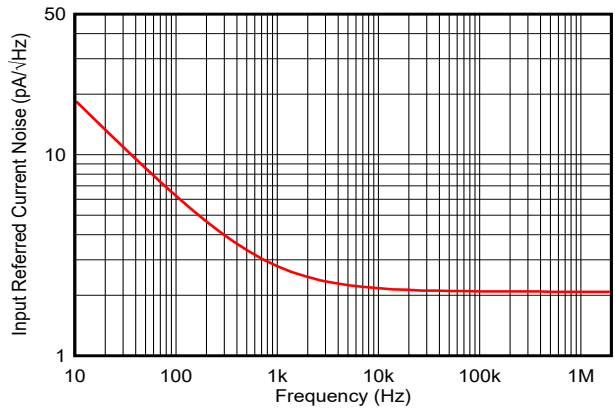
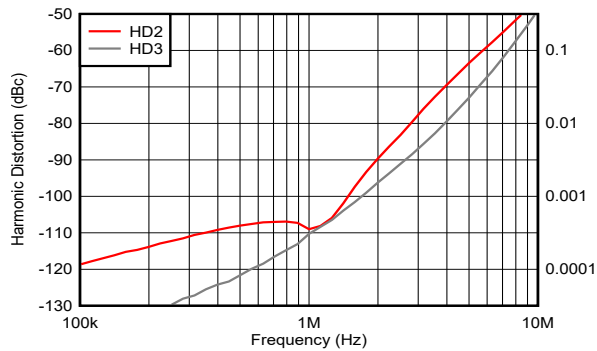
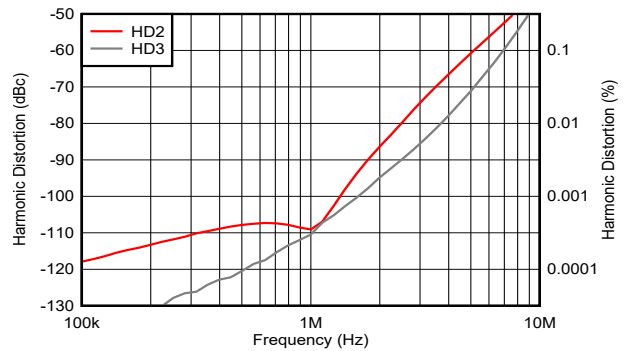


Figure 5-14. Input-referred Current Noise vs Frequency



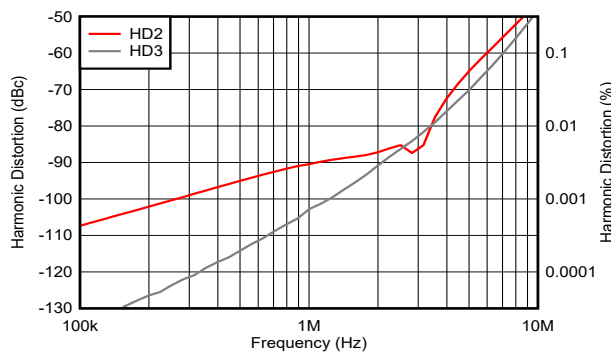
$V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 1\text{ k}\Omega$, $V_{OUT} = 2\text{ V}_{PP}$

Figure 5-15. Harmonic Distortion vs Frequency



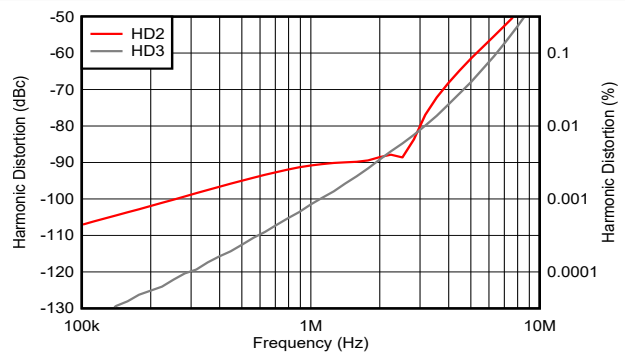
$V_{CC} = \pm 5\text{ V}$, gain = +2 V/V, $R_L = 1\text{ k}\Omega$, $V_{OUT} = 2\text{ V}_{PP}$

Figure 5-16. Harmonic Distortion vs Frequency



$V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, $V_{OUT} = 2\text{ V}_{PP}$

Figure 5-17. Harmonic Distortion vs Frequency

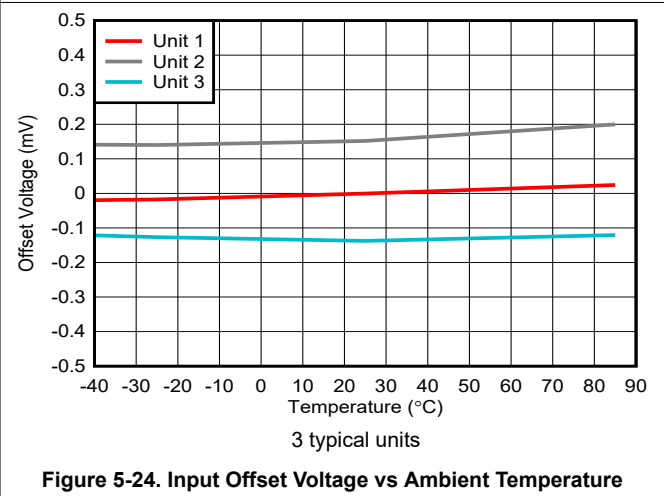
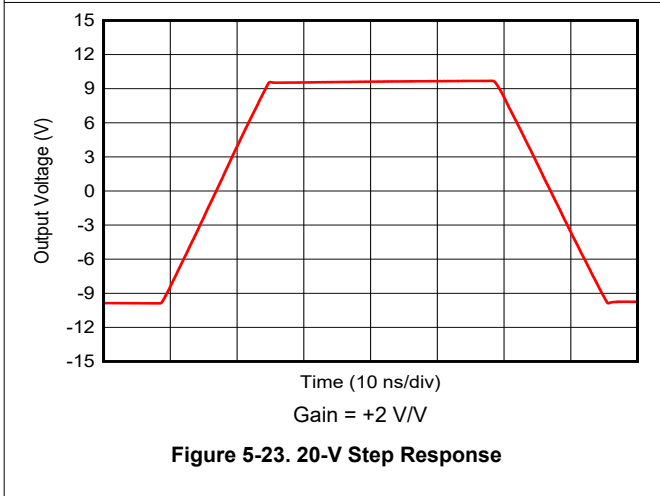
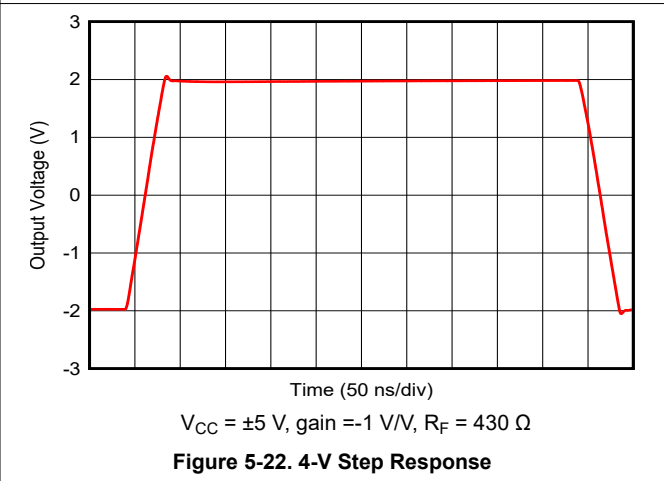
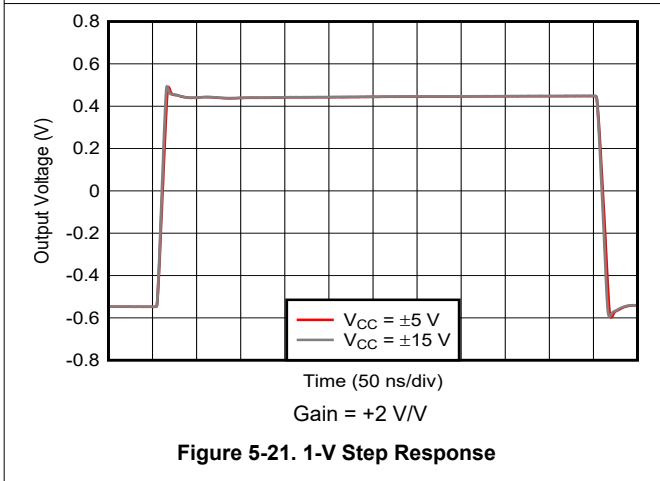
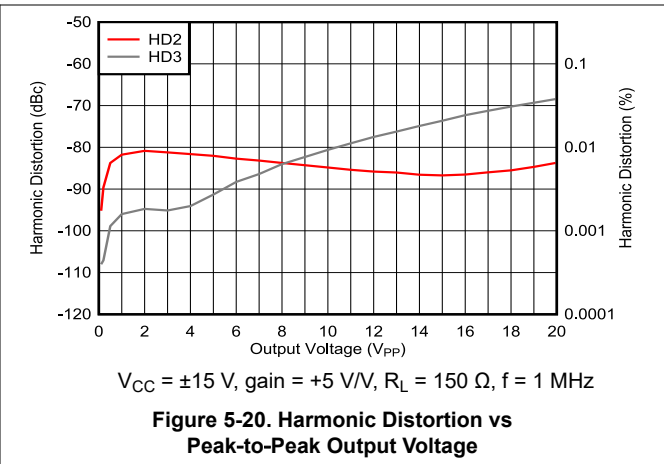
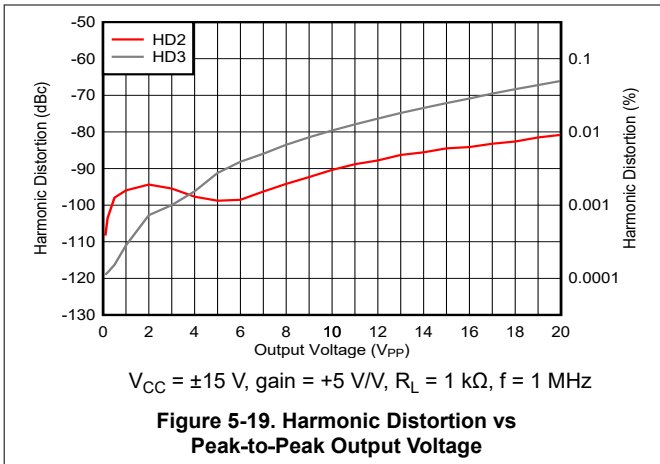


$V_{CC} = \pm 5\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, $V_{OUT} = 2\text{ V}_{PP}$

Figure 5-18. Harmonic Distortion vs Frequency

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)



5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)

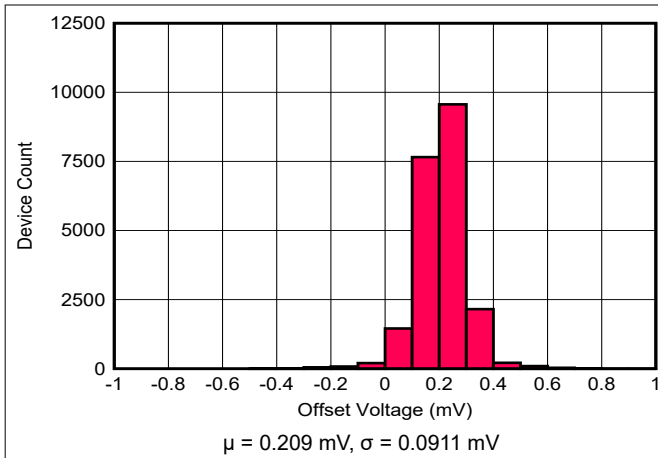


Figure 5-25. Voltage Offset Distribution

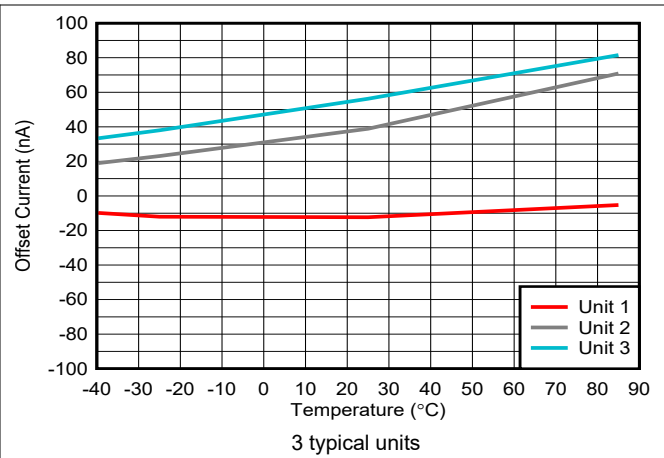


Figure 5-26. Input Offset Current vs Ambient Temperature

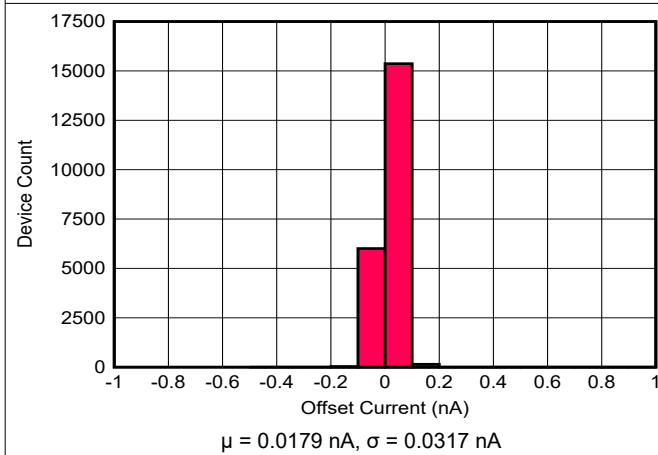


Figure 5-27. Input Offset Current vs Ambient Temperature

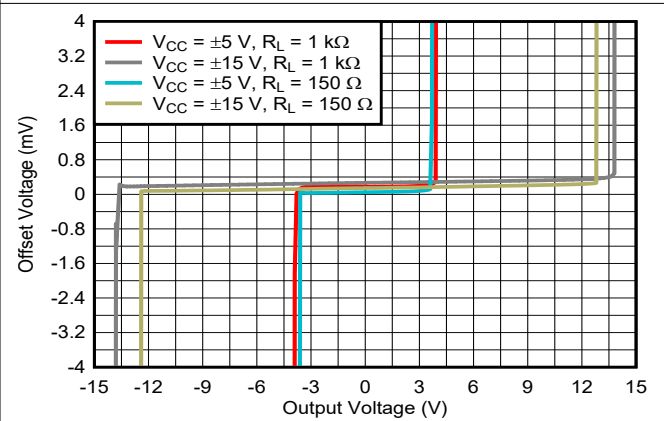


Figure 5-28. Offset Voltage vs Output Voltage

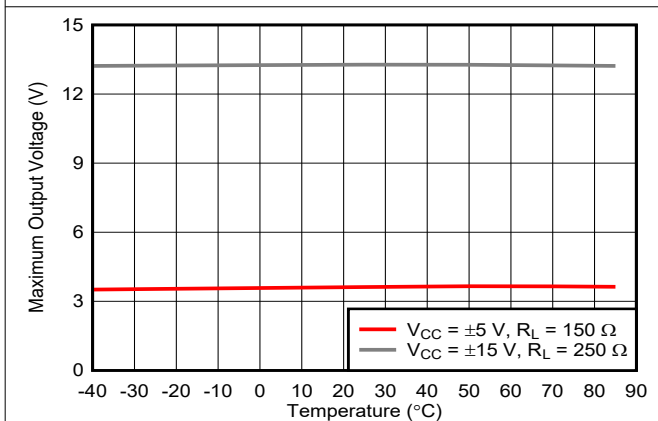


Figure 5-29. Maximum Output Voltage Swing vs Ambient Temperature

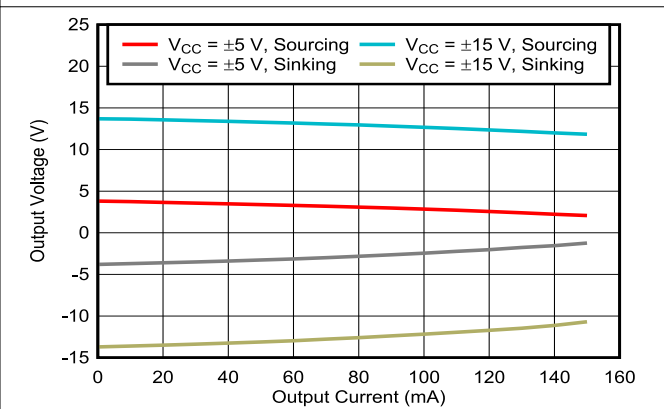


Figure 5-30. Output Swing vs Load Current

5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)

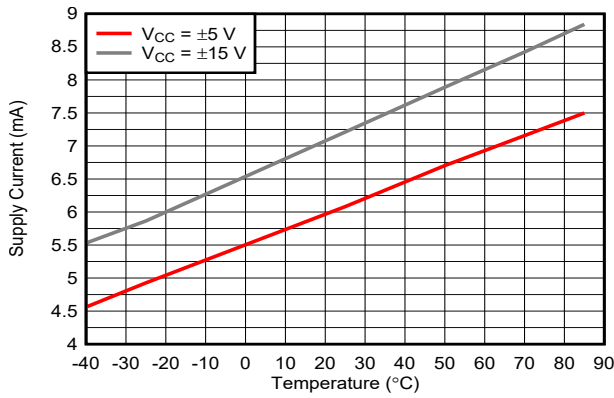
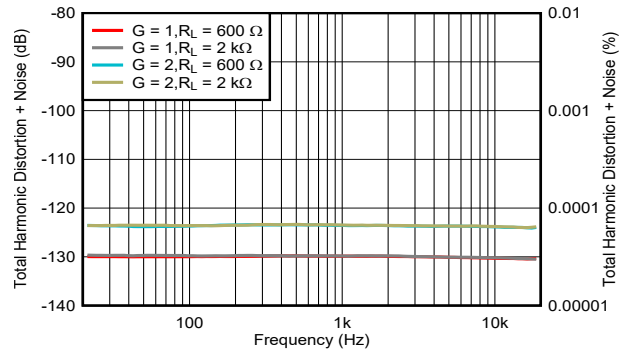
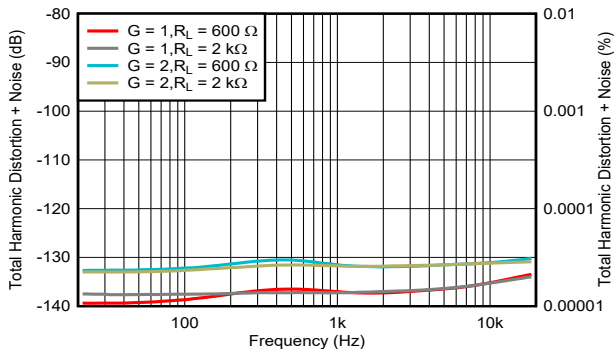


Figure 5-31. Supply Current vs Ambient Temperature



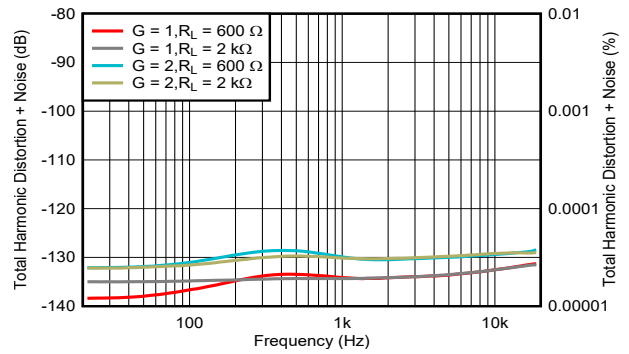
$V_{CC} = \pm 5\text{ V}$, $V_{OUT} = 1\text{ V}_{RMS}$, BW = 80 kHz

Figure 5-32. THD+N vs Frequency



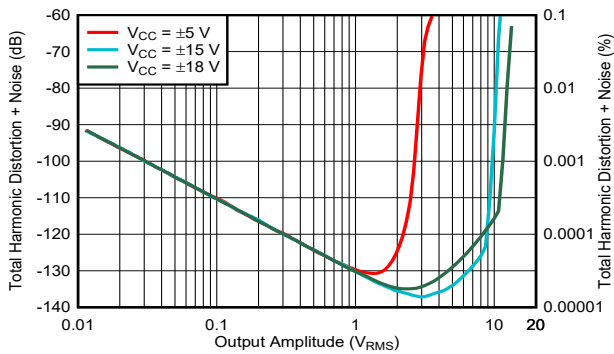
$V_{CC} = \pm 15\text{ V}$, $V_{OUT} = 3\text{ V}_{RMS}$, BW = 80 kHz

Figure 5-33. THD+N vs Frequency



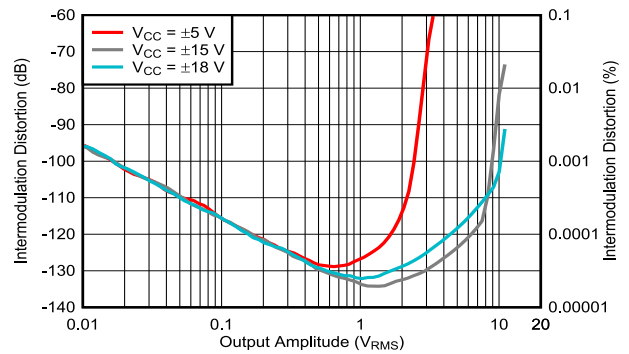
$V_{CC} = \pm 18\text{ V}$, $V_{OUT} = 3\text{ V}_{RMS}$, BW = 80 kHz

Figure 5-34. THD+N vs Frequency



Gain = +1 V/V, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, BW = 80 kHz

Figure 5-35. THD+N Ratio vs Output Amplitude

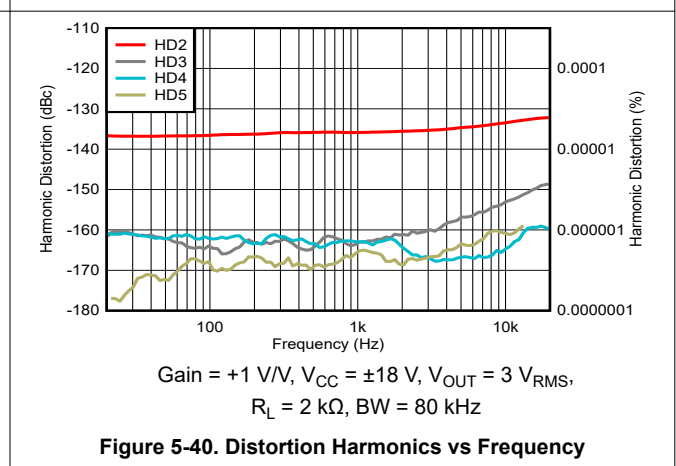
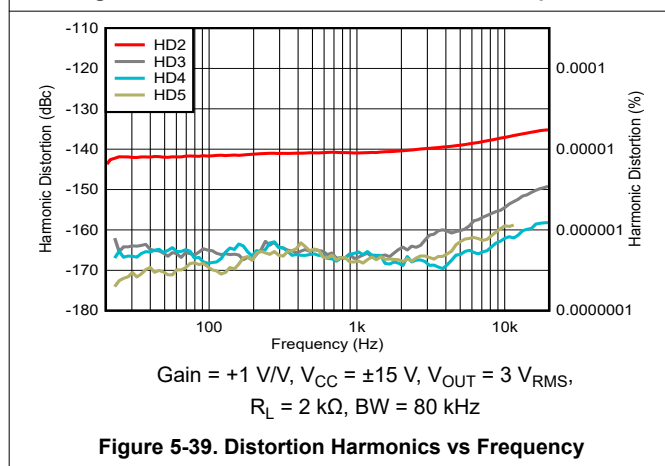
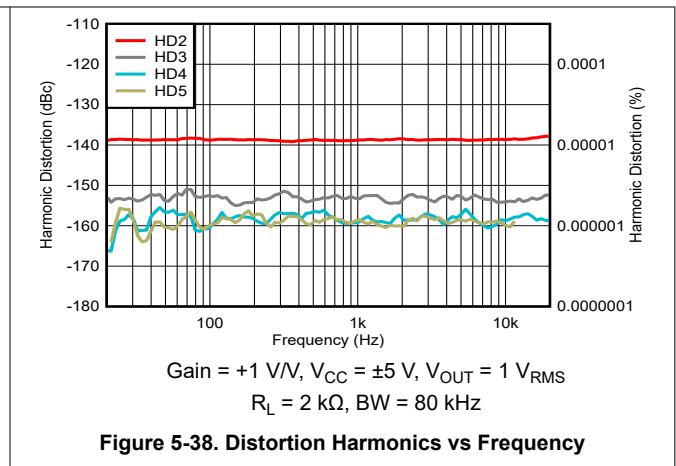
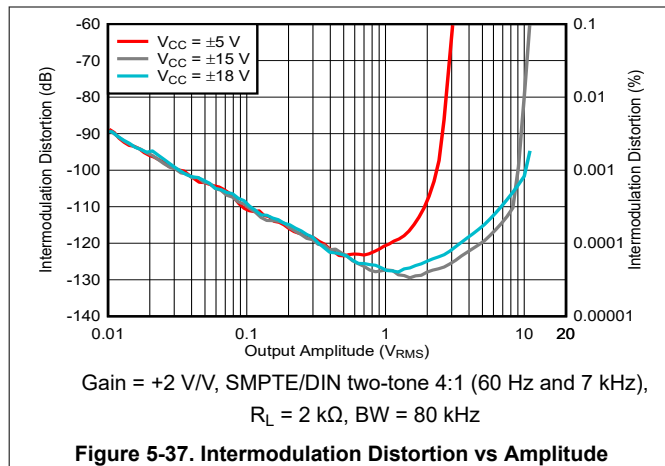


Gain = +1 V/V, SMPTE/DIN two-tone 4:1 (60 Hz and 7 kHz), $R_L = 2\text{ k}\Omega$, BW = 80 kHz

Figure 5-36. Intermodulation Distortion vs Amplitude

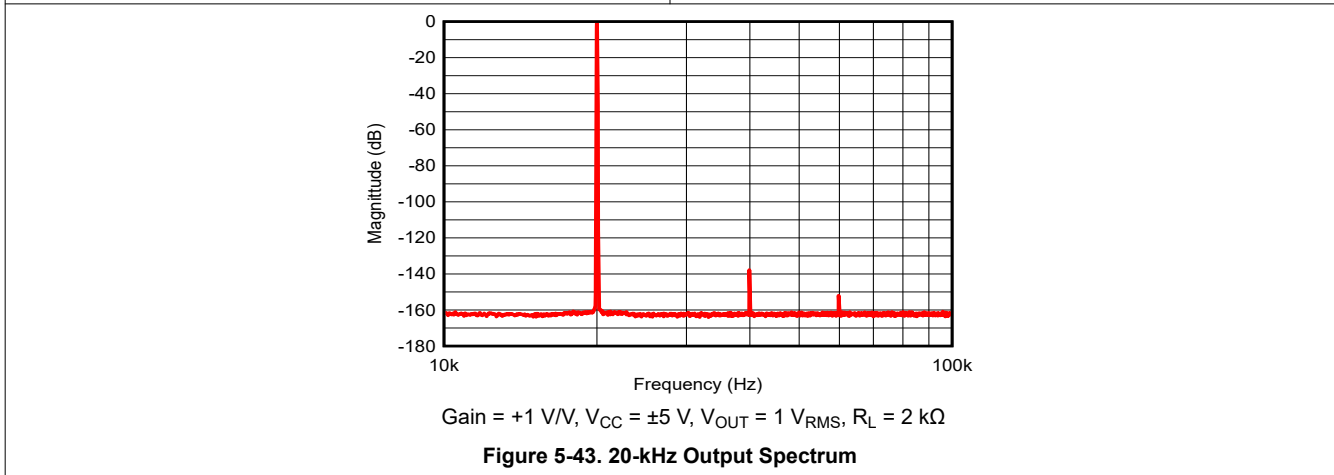
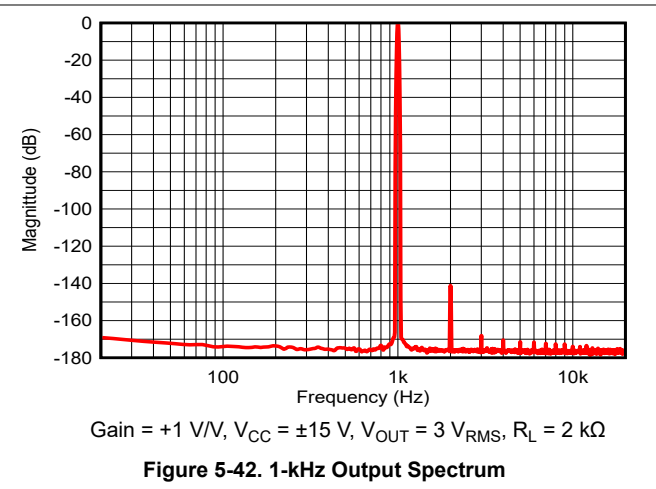
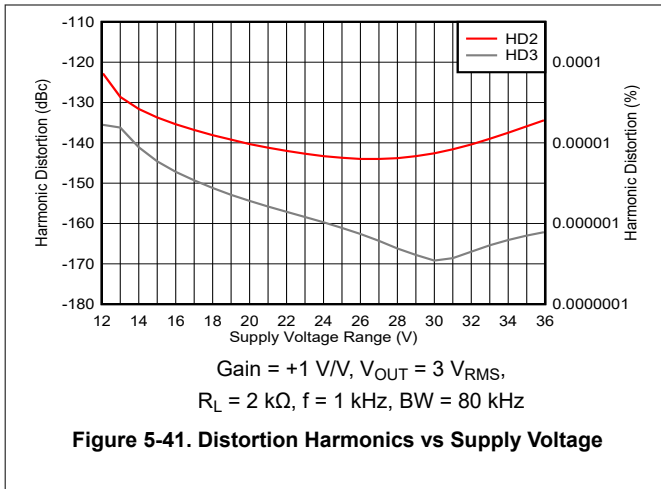
5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)



5.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, gain = +2 V/V, $R_L = 150\ \Omega$, and $R_F = 300\ \Omega$ (unless otherwise noted)



6 Detailed Description

6.1 Overview

The OPAx891 is a high-speed operational amplifier configured in a voltage feedback architecture. These amplifiers are built using a 36-V, complementary bipolar process with NPN and PNP transistors that possess an f_T of several GHz. This configuration results in exceptionally high-performance amplifiers with wide bandwidth, high slew rate, fast settling time, and low distortion.

6.2 Functional Block Diagrams

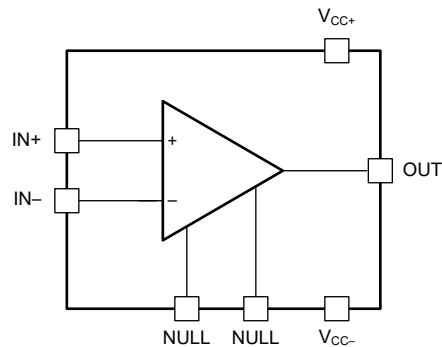


Figure 6-1. OPA891: Single Channel

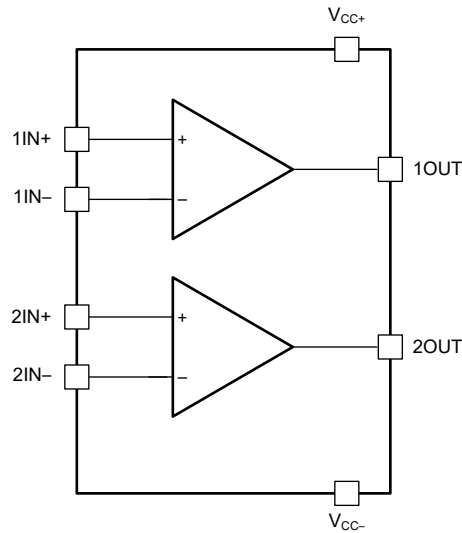


Figure 6-2. OPA2891: Dual Channel

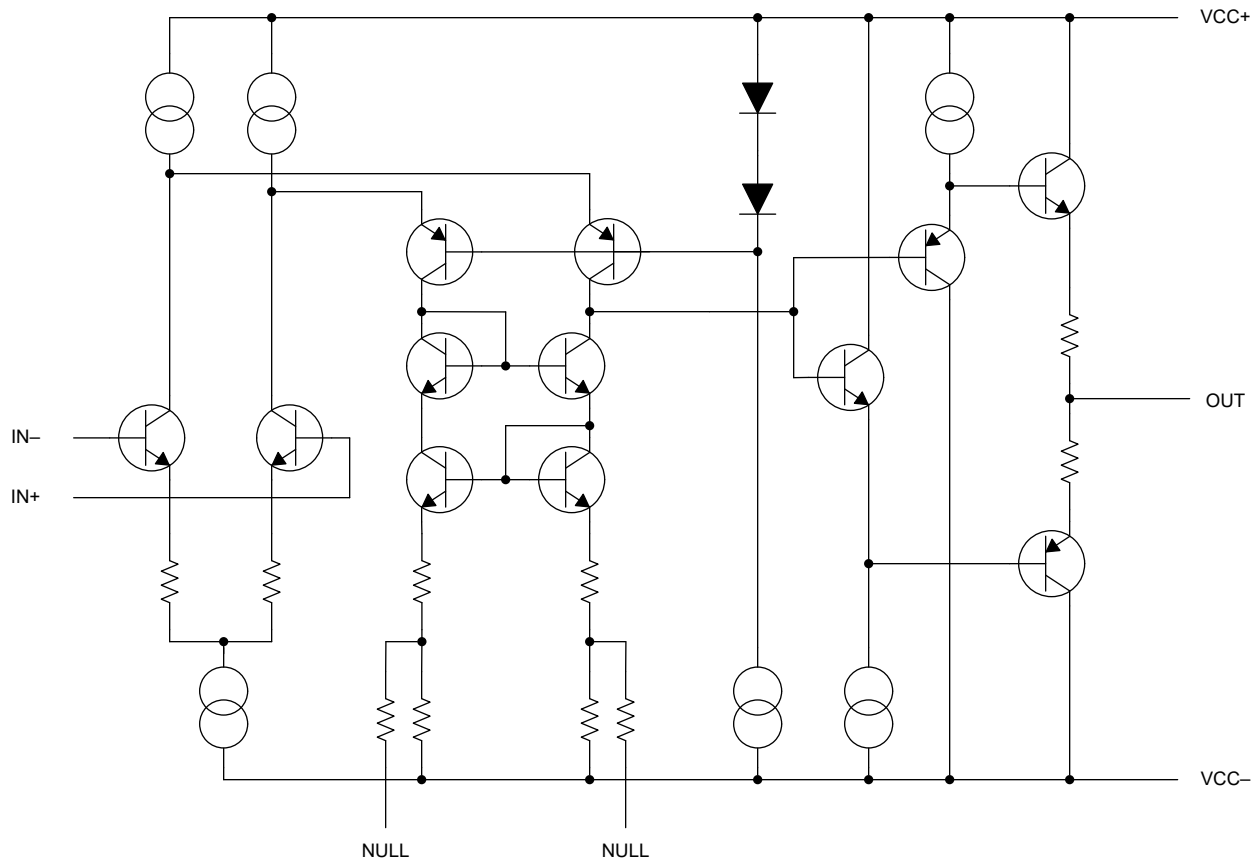


Figure 6-3. OPA891 Simplified Schematic

6.3 Feature Description

6.3.1 Offset Nulling

The OPAx891 have a very low input offset voltage for high-speed amplifiers. However, if additional correction is required, an offset nulling function is provided on the OPA891. To adjust the input offset voltage, place a potentiometer between pin 1 and pin 8 of the device, and tie the wiper to the negative supply. [Figure 6-4](#) shows this feature.

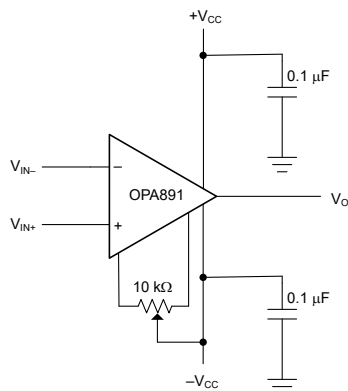


Figure 6-4. Offset Nulling Schematic

6.4 Device Functional Modes

The OPAx891 family has a single functional mode and can be used with both single-supply or split power-supply configurations. The power-supply voltage must be greater than 9 V (± 4.5 V) and less than 36 V (± 18 V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Driving a Capacitive Load

The OPAx891 are internally compensated to maximize bandwidth and slew-rate performance. To maintain stability, take additional precautions when driving capacitive loads with a high-performance amplifier. As a result of the internal compensation, significant capacitive loading directly on the output node decreases the device phase margin, and potentially lead to high-frequency ringing or oscillations. Therefore, for capacitive loads greater than 10 pF, place an isolation resistor in series with the output of the amplifier. [Figure 7-1](#) shows this configuration. For most applications, a minimum resistance of 20 Ω is recommended. In 75-Ω transmission systems, setting the series resistor value to 75 Ω is a beneficial choice because this value isolates any capacitance loading and provides source impedance matching.

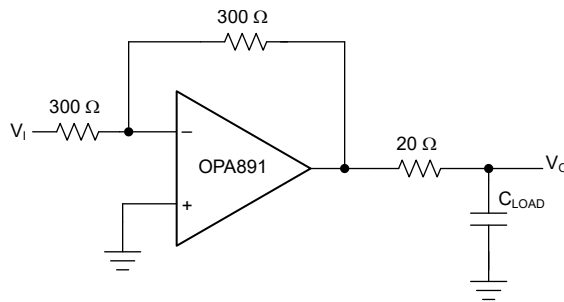


Figure 7-1. Driving a Capacitive Load

7.1.2 Low-pass Filter Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. [Figure 7-2](#) shows how the simplest way to accomplish this limiting is to place an RC filter at the noninverting pin of the amplifier.

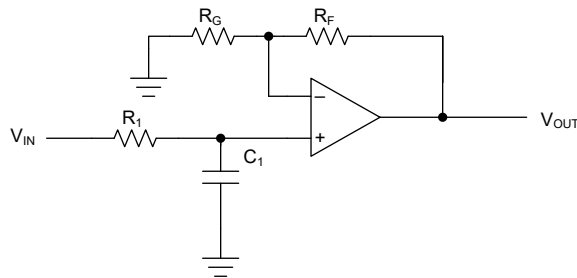


Figure 7-2. Single-pole Low-pass Filter

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + sR_1C_1}\right) \quad (1)$$

If more attenuation at higher frequencies is required, a multiple-pole filter is required. [Figure 7-3](#) shows a common implementation of a second-order filter called a Sallen-Key filter. When designing this type of filter,

choose an amplifier with a bandwidth that is approximately an order of magnitude larger than the desired filter bandwidth. See [Active Low-pass Filter Design](#) for more detailed active-filter design information.

Assuming $R_1 = R_2 = R$ and $C_1 = C_2 = C$, use [Equation 2](#) to set the bandwidth of the filter.

$$f_{3dB} = \frac{1}{2\pi RC} \quad (2)$$

The Q-factor of a filter controls the amount of peaking of the small-signal frequency response and the settling time of the pulse response. Set Q to 0.707 to provide a Butterworth response with a maximally-flat pass-band. Choose the ratio of R_F and R_G to obtain the desired Q value as shown in [Equation 3](#).

$$\frac{R_F}{R_G} = 2 - \frac{1}{Q} \quad (3)$$

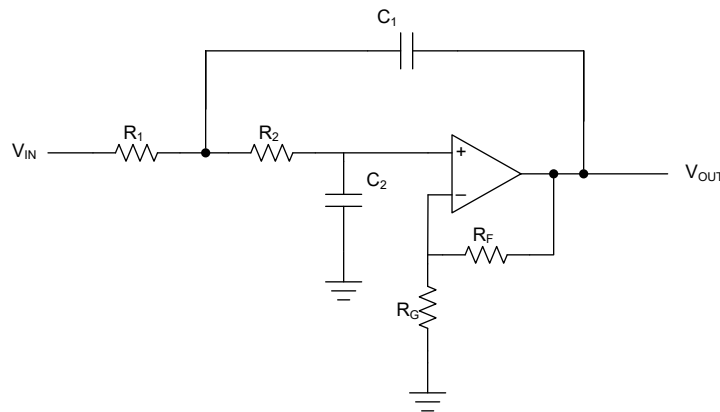


Figure 7-3. Two-pole Low-pass Sallen-Key Filter

7.2 Typical Application

This section demonstrates multiplexing several analog input signals to a high-performance driver amplifier which subsequently drives a single high-resolution, high-speed SAR analog-to-digital converter (ADC). This example uses the [ADS8411](#) and the [TS5A3159](#) or [TS5A3359](#) as the ADC and the multiplexer, respectively. This application uses the OPAx891 as the operational amplifier.

As detailed in [Figure 7-4](#), the example system consists of an ADC (ADS8411), a driving operational amplifier (OPA891), a multiplexer (TS5A3159), an AC source, a DC source, and two driving operational amplifiers.

The driving amplifiers OPA1 and OPA2 are shown as two OPA891 amplifiers. Alternatively, use a single OPA2891 to save on cost and board space. The purpose of these op-amps is to make the input sources present a low impedance to rest of the circuit. Additionally, to maintain signal fidelity, these operational amplifiers must have low noise and distortion. The third OPA891, labeled OPA3 in [Figure 7-4](#), is used to maintain switching speed and drive the ADC. The passive band-pass filter before the ADC reduces unwanted noise.

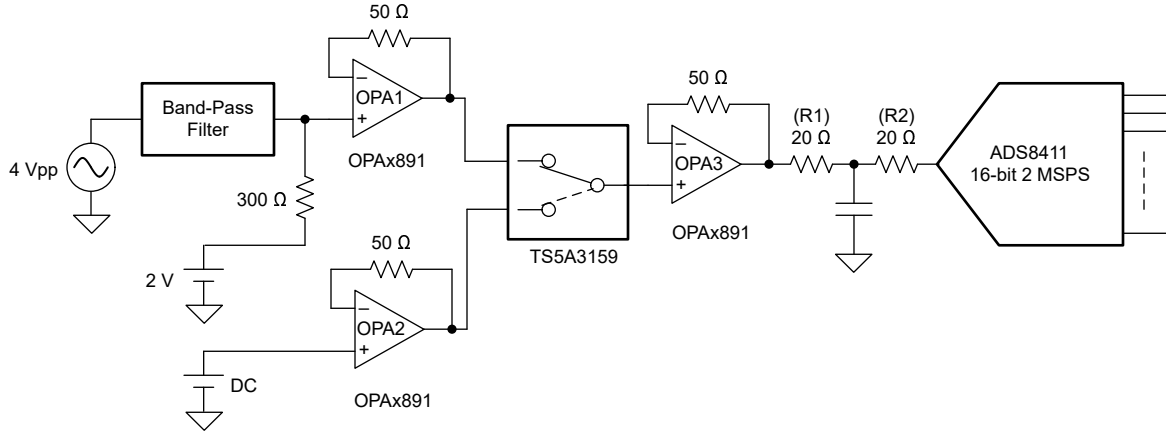


Figure 7-4. Multiplexing Set-up to Drive a High Performance ADC

7.2.1 Design Requirements

The objective is to design a multiplexed digitizer system with the dynamic performance shown in Table 7-1.

Table 7-1. Design Specifications

DEVICE SPEED (MSPS)	INPUT FREQUENCY (kHz)	SNR (dB)	THD (dB)	CROSSTALK (dB)
2	20	> 84	< -90	< -110
2	100	> 84	< -90	< -96

7.2.2 Detailed Design Procedure

The ADS8411 is a 16-bit, 2-MSPS analog-to-digital converter (ADC) with a 4-V reference. The ADS8411 has a unipolar single-ended input and includes a 16-bit capacitor-based SAR ADC, with inherent sample and hold. The output is a 16-bit parallel interface.

The TS5A3159 is a single-pole, double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The TS5A3159 offers a low ON state resistance and an excellent ON resistance matching with the break-before-make feature to prevent signal distortion during the transfer of a signal from one channel to another. Additionally, the TS5A3159 provides excellent total harmonic distortion (THD) performance and consumes low power. The TS5A3359 is a single-pole, triple-throw (SP3T) version of the same switch.

7.2.2.1 Selection of Multiplexer

Figure 7-5 shows an equivalent circuit diagram of one of the channels of a multiplexer. C_S is the input capacitance of the channel; C_D is the output capacitance of the channel. R_{ON} is the resistance of the channel when the channel is turned ON. C_L and R_L are the load capacitance and resistance, respectively. V_{IN} is the input voltage of the source. R_S is the resistance of the source. V_{OUT} is the output voltage of the multiplexer.

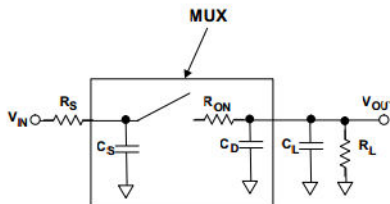


Figure 7-5. Multiplexer Equivalent Circuit

Settling time is improved when the values of R_S , R_{ON} , C_S , C_D , and C_L are small, and the value of R_L is large.

For TS5A3159:

- $R_{ON} = 1 \Omega$
- $C_S = C_D = 84 \text{ pF}$

Typical values for the extrinsic parameters are

- $R_S = 50 \Omega$
- $C_L = 5 \text{ pF}$
- $R_L = 10 \text{ k}\Omega$
- T_{RC} (time constant) = 8.65 ns

For a 16-bit system, at least 18-bit settling is desired to minimize distortion from settling artifacts. For a 18-bit settling, the circuit response time required is $(18 \times \ln 2) \times T_{RC} = 108 \text{ ns}$, which is less than 2 MSPS sampling time of 500 ns. If the settling time is more than the conversion time of the ADC, the output of the multiplexer does not settle to the required accuracy resulting in distortion.

One more important parameter to consider when selecting a multiplexer is the on-state resistance variation with voltage. This variation also affects distortion because R_{ON} and R_L act like a resistor divider circuit. Any variation of R_{ON} with voltage affects the output voltage.

7.2.2.2 Signal Source

The input signal source must be a low-noise, low-distortion source with low source resistance. As discussed in the earlier section, the source resistance also must be small to avoid impacting settling time. If the source is not a low-noise and low-distortion source, a passive band-pass filter can be added to improve the signal quality as shown in [Figure 7-4](#).

7.2.2.3 Driving Amplifier

The driving operational amplifier (OPA3 in [Figure 7-4](#)) in this application must have good slew rate, bandwidth, low noise, and distortion. The input of the operational amplifier can result in a maximum step of 4-V because of MUX switching. As a result, even if the signal bandwidth is low, the driving amplifier must settle from a 4-V step within one ADC sampling frame to avoid signal distortion. In this example, the settling requirement due to the ADC selection is 500 ns. The OPA891 is a good choice in this application due to the high slew rate and low distortion of this operational amplifier.

7.2.2.4 Driving Amplifier Bandwidth Restriction

Restricting excess bandwidth use by including a passive RC filter before the ADC results in better SNR and THD. However, restricting the bandwidth too much results in an excessive operational amplifier settling time. If the amplifier output does not settle quick enough, some residual charges from the previous channel remain in the next sampling interval and appear as crosstalk. One approach to solve this settling issue is to reduce the throughput of the ADC. However, the high sample rate ADC is often selected to meet the need to acquire higher frequency signals, limiting the freedom to reduce the ADC throughput. Due to these tradeoffs, the choice of the filter capacitor becomes critical. [Figure 7-6](#) and [Figure 7-7](#) show SNR and crosstalk as a function of the filter capacitor.

[Figure 7-8](#) shows input settling behavior with three different filter capacitor values. The value of the capacitor changes to filter bandwidth. As the filter bandwidth increases, the settling time improves as shown in [Equation 4](#).

$$\text{Filter Bandwidth} \cong \frac{1}{2\pi R_1 C_1} \quad (4)$$

7.2.3 Application Curves

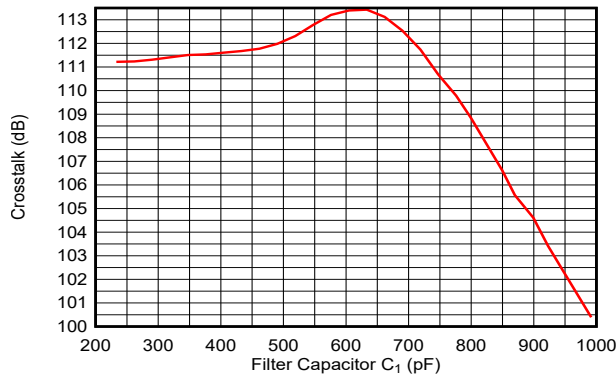


Figure 7-6. SNR vs Filter Capacitor

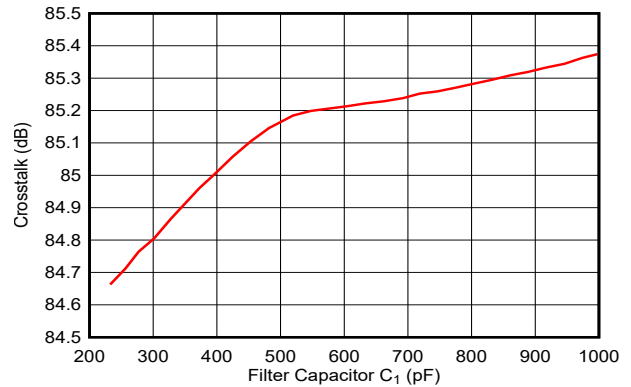


Figure 7-7. Crosstalk vs Filter Capacitor

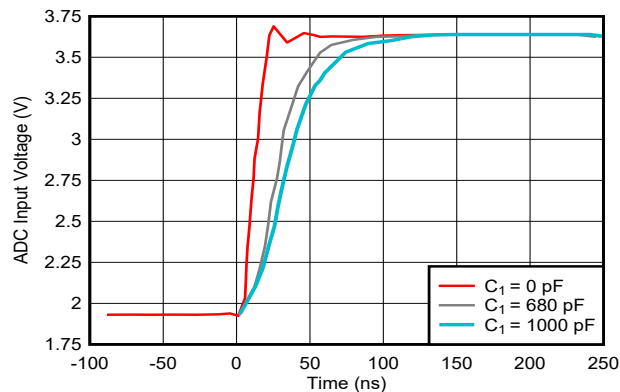


Figure 7-8. Input to ADC for Various Values of Filter Capacitors

7.3 Power Supply Recommendations

The OPAx891 family can operate with a single supply or with dual supplies. Choose supplies that provide for the required headroom to supply rails as specified by the common-mode input range (CMIR). Operating from a single supply can have numerous advantages. With the negative supply at ground, the dc errors due to the – PSRR term are minimized. Supplies must be decoupled as close to the amplifier as possible with low inductance capacitors decoupled to ground. When operating on a board with high-speed digital signals, provide isolation between digital signal noise and the analog input pins. When using a ground plane, removing the ground plane close to input sensitive pins reduces stray parasitics that adversely impact device performance. For split-supply operation, an optional supply decoupling capacitor across the two power supplies improves second harmonic distortion performance.

7.4 Layout

7.4.1 Layout Guidelines

To achieve the levels of high-frequency performance of the OPAx891, follow proper printed-circuit board (PCB), high-frequency design techniques. The following is a general set of guidelines. In addition, a OPAx891 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- **Ground planes**—make sure that the ground plane used on the board provides all components with a low-inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize stray capacitance.
- **Proper power-supply decoupling**—use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply pin. Sharing the tantalum capacitor among several amplifiers is possible depending on the application, but always use a 0.1- μ F ceramic capacitor on the supply pin of every amplifier. In addition, place the 0.1- μ F capacitor as close as possible to the supply pin. As this distance increases, the inductance

in the connecting trace makes the capacitor less effective. Strive for distances of less than 0.1 inch (2.54 mm) between the device power pins and the ceramic capacitors.

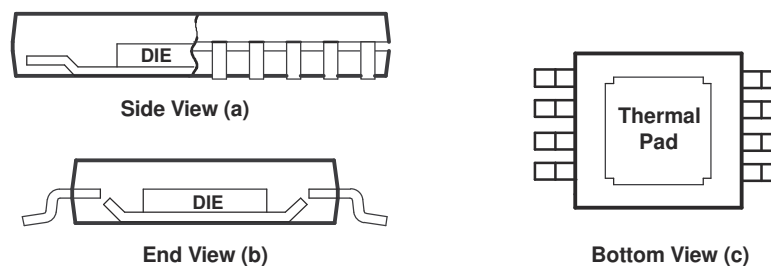
- **Short trace runs or compact part placements**—optimum high-frequency performance is achieved when stray series inductance has been minimized. To reduce stray series inductance, make the circuit layout as compact as possible, thereby minimizing the length of all trace runs. Focus attention on the inputs of the amplifier, keeping the trace lengths as short as possible. This layout helps to minimize stray capacitance at the input of the amplifier.
- **Sockets**—TI does not recommend sockets for high-speed operational amplifiers. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs and compact part placements**—Improved high-frequency performance is achieved when stray series inductance is minimized. To reduce stray series inductance, the circuit layout must be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention must be provided to the inverting input of the amplifier. The length must be kept as short as possible. This design decision helps minimize stray capacitance at the input of the amplifier.

7.4.1.1 General PowerPAD™ Design Considerations

The OPAx891 is available in a thermally-enhanced DGN package, which is a member of the PowerPAD™ family of integrated circuit packages. This package is constructed using a downset lead frame upon which the die is mounted [see Figure 7-9(a) and Figure 7-9(b)]. This arrangement results in the lead frame exposed as a thermal pad on the underside of the package [see Figure 7-9(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD™ integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into a ground plane or other heat-dissipating device.

The PowerPAD™ integrated circuit package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heat sinking.



- A. The thermal pad is electrically isolated from all pins in the package.

Figure 7-9. Views of Thermally-enhanced DGN Package

Although there are many ways to properly heat sink this device, the following steps show the recommended approach.

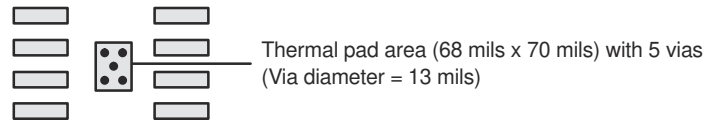
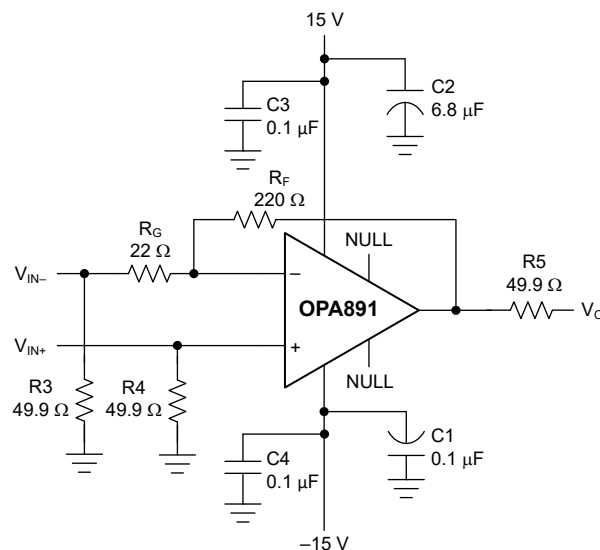


Figure 7-10. PowerPAD™ PCB Etch and Via Pattern

1. Prepare the PCB with a top-side etch pattern as shown in [Figure 7-10](#). There must be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes must be 13 mils (0.3302 mm) in diameter. The reason to keep the holes small is to discourage solder wicking through the holes during reflow.
3. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. This action helps dissipate the heat generated by the OPAx891 device. The additional vias can be of any diameter because wicking is not a concern outside of the thermal pad area.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPAx891 package must connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask must leave the pins of the package and the thermal pad area with the five holes exposed. The bottom-side solder mask must cover the five holes of the thermal pad area, which prevents solder from pulling away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and to all the device pins.
8. With these preparatory steps in place, the OPAx891 device is placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

7.4.2 Layout Example



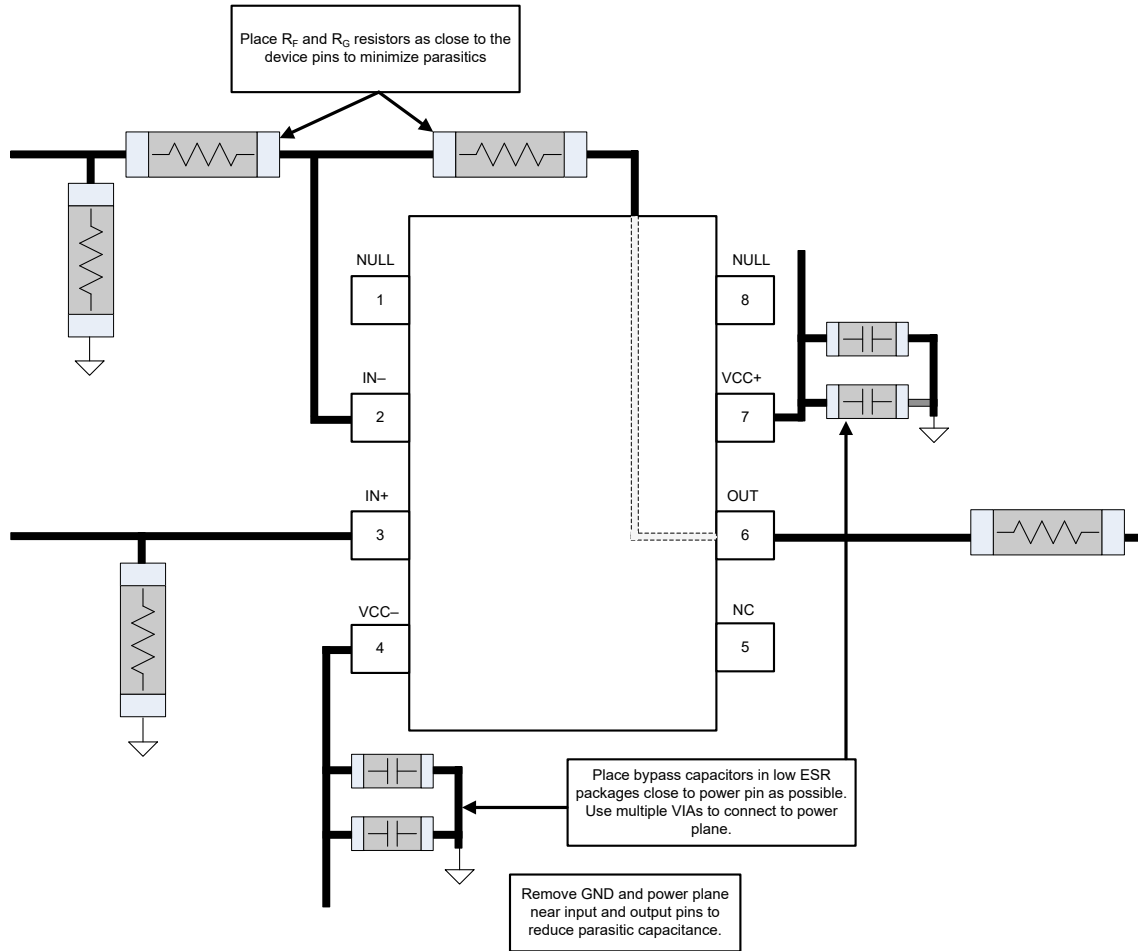


Figure 7-11. Layout Recommendations

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Noise Analysis for High-Speed Op Amps](#), application note
- Texas Instruments, [PowerPAD™ Thermally Enhanced Package](#), application note
- Texas Instruments, [DEM-OPA-SO-1A Demonstration Fixture](#), user's guide
- Texas Instruments, [DEM-OPA-SO-2A Demonstration Fixture](#), user's guide
- Texas Instruments, [DEM-OPA-MSOP-2A Demonstration Fixture](#), user's guide

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2023	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA891DGNR	ACTIVE	HVSSOP	DGN	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	O891	Samples
OPA891DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	O891	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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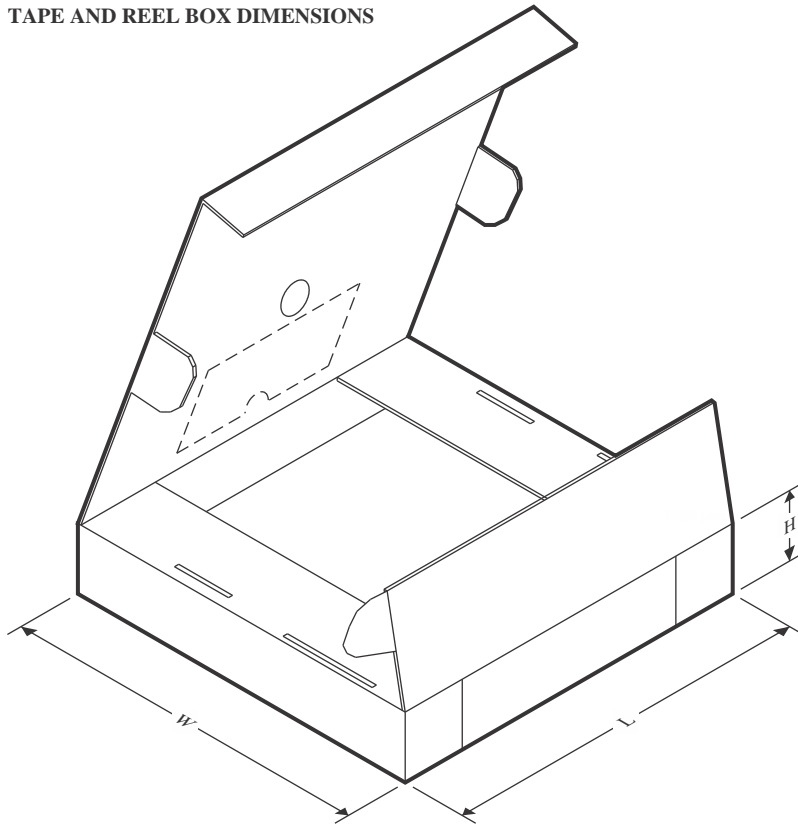
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA891DGNR	HVSSOP	DGN	8	3000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA891DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA891DGNR	HVSSOP	DGN	8	3000	356.0	356.0	35.0
OPA891DR	SOIC	D	8	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

DGN 8

PowerPAD VSSOP - 1.1 mm max height

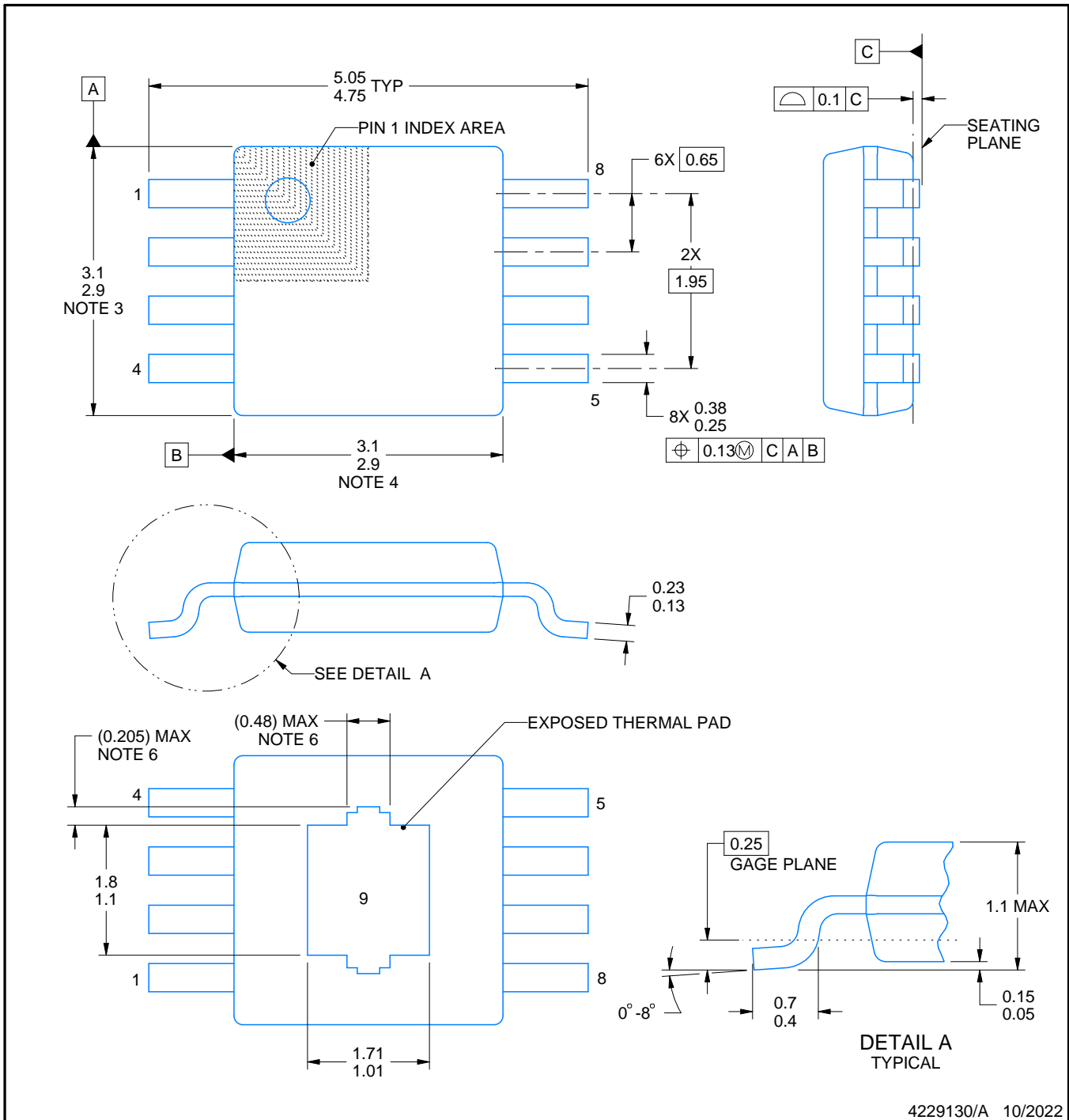
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A



4229130/A 10/2022

NOTES:

PowerPAD is a trademark of Texas Instruments.

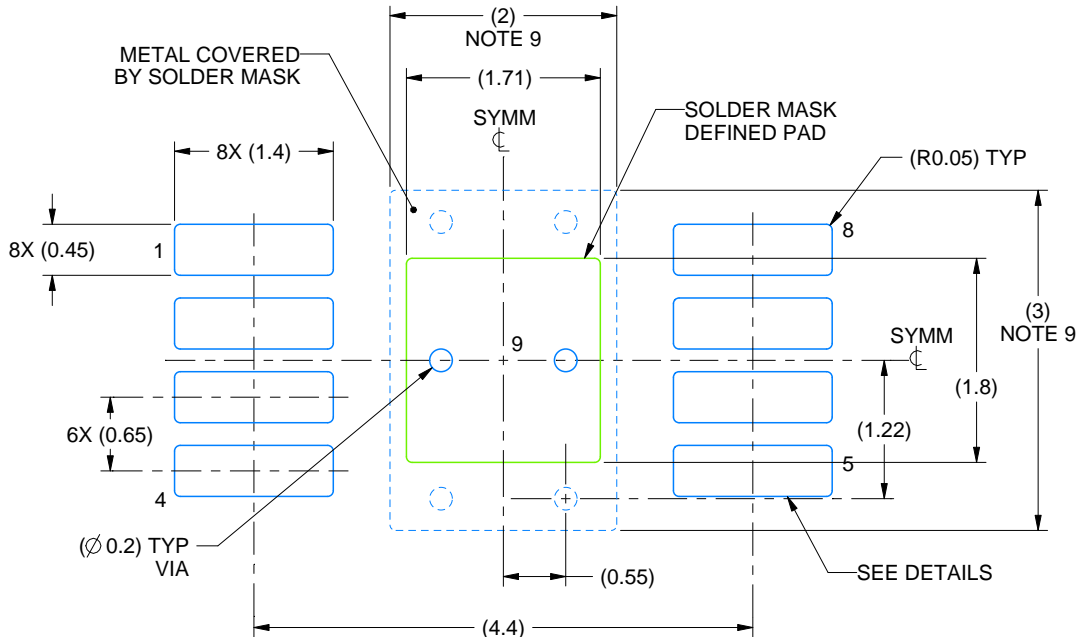
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

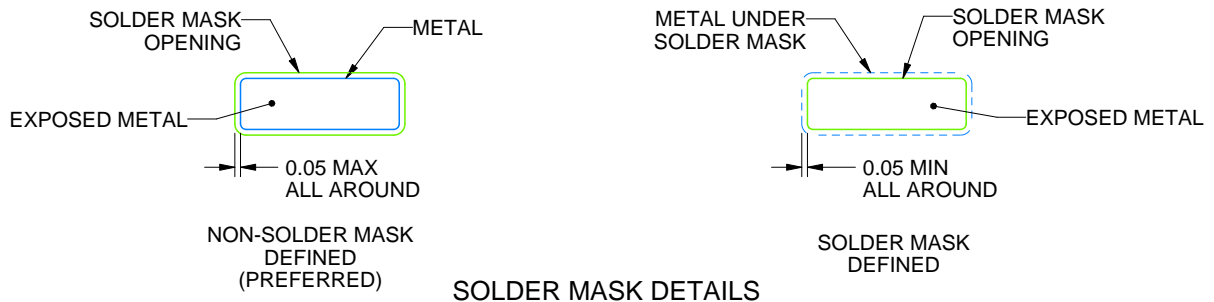
DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4229130/A 10/2022

NOTES: (continued)

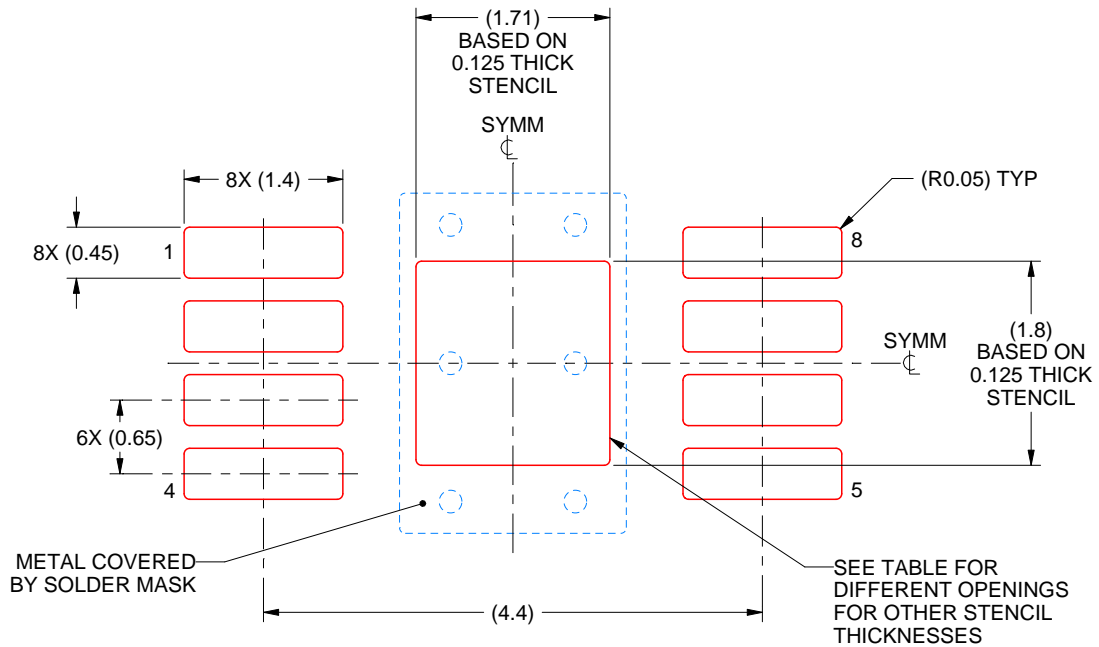
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
 EXPOSED PAD 9:
 100% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/A 10/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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[NJM2904CRB1-TE1](#) [UPC4570G2-E1-A](#) [UPC4741G2-E1-A](#) [UPC4574GR-9LG-E1-A](#) [NJM8532RB1-TE1](#) [EL2250CS](#) [EL5100IS](#) [EL5104IS](#)
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