

## REF60xx 集成 ADC 驱动器缓冲器的高精度电压基准

### 1 特性

- 出色的温度漂移性能
  - 40°C 至 +125°C 时为 5ppm/°C (最大值)
- 极低噪声
  - 总噪声: 5  $\mu\text{V}_{\text{RMS}}$  (使用 47 $\mu\text{F}$  电容时)
  - 1/f 噪声 (0.1Hz 至 10Hz): 3  $\mu\text{V}_{\text{PP}}/\text{V}$
- 集成 ADC 驱动器缓冲器
  - 低输出阻抗: < 50m $\Omega$  (0kHz-200kHz)
  - 首次使用 ADS8881 实现 18 位精确采样
  - 支持突发模式 DAQ 系统
- 低电源电流: 820 $\mu\text{A}$
- 低关断电流: 1 $\mu\text{A}$
- 高初始精度:  $\pm 0.05\%$
- 超低噪声和失真
  - 信噪比 (SNR): 100.5dB, 总谐波失真 (THD): -125dB (ADS8881)
  - 信噪比 (SNR): 106dB, 总谐波失真 (THD): -120dB (ADS127L01)
- 输出电流驱动能力:  $\pm 4\text{mA}$
- 可通过编程设定的短路电流
- 经验证用于驱动 ADS88xx 系列逐次逼近寄存器 (SAR) ADC 和 ADS127xx 系列宽频带  $\Delta$ - $\Sigma$  ADC 的 REF 引脚

### 2 应用

- 自动测试设备 (ATE) 测试器和示波器
- 测试和测量设备
- 可编程逻辑控制器 (PLC) 的模拟输入模块
- 医疗设备
- 精密数据采集系统

### 3 说明

REF6000 系列电压基准集成低输出阻抗缓冲器, 这使得用户能够直接驱动精密数据转换器的 REF 引脚, 同时维持线性度、失真和噪声性能。多数精密 SAR 和  $\Delta$ - $\Sigma$  ADC 在转换过程中会将二进制加权电容切换到 REF 引脚。为了支持这一动态负载, 必须通过一个低输出阻抗 (高带宽) 缓冲器缓冲电压基准的输出。REF6000 系列器件非常适合 (但不限于) 驱动 ADS88xx 系列 SAR ADC 和 ADS127xx 系列  $\Delta$ - $\Sigma$  ADC 以及其他数模转换器 (DAC) 的 REF 引脚。

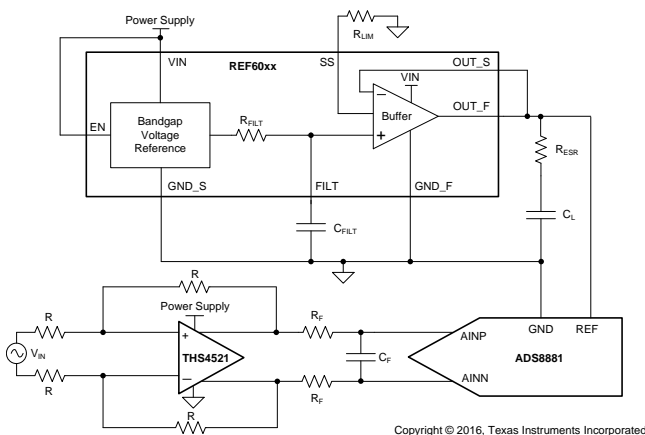
在驱动 ADS8881 的 REF 引脚时, 即使在首次转换过程中, REF6000 系列电压基准的输出电压也不会降至 1 LSB (18 位) 以下。该特性对于突发模式、事件触发的等时采样和可变采样率数据采集系统极为有用。REF6000 系列的 REF60xx 型号指定了最大温度漂移 (仅为 5ppm/°C), 可为电压基准与低输出阻抗缓冲器组合提供 0.05% 初始精度。关于 REF6000 系列中的多种温度漂移选项, 请参见 [器件比较表](#)。

器件信息<sup>(1)</sup>

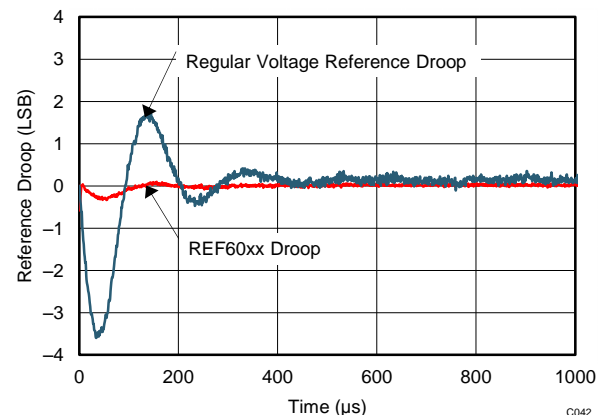
产品型号	封装	封装尺寸 (标称值)
REF60xx	VSSOP (8)	3.00mm x 3.00mm

(1) 要了解所有可用封装, 请参见数据表末尾的封装选项附录。

典型应用



基准压降比较  
(1 LSB = 19.07 $\mu\text{V}$ , ADS8881 的速率为 1MSPS)



## 目录

<b>1</b>	<b>特性</b> .....	<b>1</b>	9.1	Overview .....	19
<b>2</b>	<b>应用</b> .....	<b>1</b>	9.2	Functional Block Diagram .....	19
<b>3</b>	<b>说明</b> .....	<b>1</b>	9.3	Feature Description .....	20
<b>4</b>	<b>修订历史记录</b> .....	<b>2</b>	9.4	Device Functional Modes .....	23
<b>5</b>	<b>Device Comparison Table</b> .....	<b>3</b>	<b>10</b>	<b>Applications and Implementation</b> .....	<b>24</b>
<b>6</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	10.1	Application Information .....	24
<b>7</b>	<b>Specifications</b> .....	<b>4</b>	10.2	Typical Application .....	24
7.1	Absolute Maximum Ratings .....	4	<b>11</b>	<b>Power Supply Recommendations</b> .....	<b>27</b>
7.2	ESD Ratings .....	4	<b>12</b>	<b>Layout</b> .....	<b>28</b>
7.3	Recommended Operating Conditions .....	4	12.1	Layout Guidelines .....	28
7.4	Thermal Information .....	4	12.2	Layout Example .....	28
7.5	Electrical Characteristics .....	5	<b>13</b>	<b>器件和文档支持</b> .....	<b>29</b>
7.6	Typical Characteristics .....	7	13.1	文档支持 .....	29
<b>8</b>	<b>Parameter Measurement Information</b> .....	<b>14</b>	13.2	相关链接 .....	29
8.1	Solder Heat Shift .....	14	13.3	接收文档更新通知 .....	29
8.2	Thermal Hysteresis .....	15	13.4	社区资源 .....	29
8.3	Reference Droop Measurements .....	16	13.5	商标 .....	29
8.4	1/f Noise Performance .....	18	13.6	静电放电警告 .....	29
<b>9</b>	<b>Detailed Description</b> .....	<b>19</b>	13.7	Glossary .....	29
			<b>14</b>	<b>机械、封装和可订购信息</b> .....	<b>30</b>

## 4 修订历史记录

### Changes from Revision A (June 2016) to Revision B

**Page**

• 已更改 <i>说明</i> .....	1
• Changed the <i>Device Comparison Table</i> .....	3
• Changed list of devices for output current in Recommended Operating Conditions .....	4
• Changed load regulation max value for REF6050 at $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ from 30 to 50 .....	5
• Changed "second pass" to "final pass" in last paragraph of <i>Solder Heat Shift</i> section .....	14
• Added link to SLYY097 in <i>Overview</i> section .....	19

### Changes from Original (May 2016) to Revision A

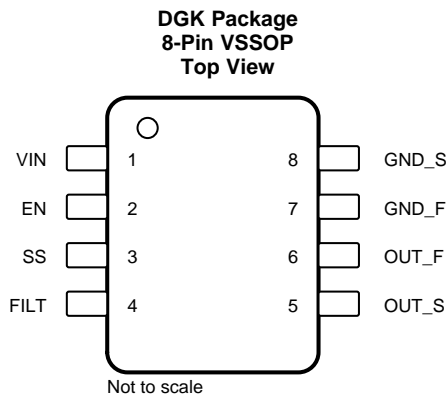
**Page**

• 已由“产品预览”更改为“量产数据” .....	1
---------------------------	---

## 5 Device Comparison Table

DEVICE FAMILY	TEMPERATURE DRIFT
REF60xx	5 ppm/°C from –40 to 125°C
REF61xx	8 ppm/°C from –40 to 125°C
REF62xx	3 ppm/°C from 0 to 70°C

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	2	Input	Enable pin
FILT	4	—	Filter capacitor pin. A capacitor ( $C_{\text{FILT}} \geq 1 \mu\text{F}$ ) must be connected between the FILT pin and ground for stability.
GND_F	7	Ground	Ground force pin
GND_S	8	Ground	Ground sense pin
OUT_F	6	Output	Output voltage force pin
OUT_S	5	Input	Output voltage sense pin
SS	3	—	Short circuit current limit pin. Connect a resistor to this pin to set the output short-circuit current limit. Connect to VIN pin for highest current limit
VIN	1	Power	Input supply voltage pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	$V_{IN}$	-0.3	6	V
	$V_{EN}$	-0.3	$V_{IN} + 0.3$	V
Operating temperature, $T_A$		-55	150	°C
Junction temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{IN}$ Supply input voltage ( $I_{OUT} = 0$ mA)	REF6025	3		5.5	V
	REF6030, REF6033, REF6041, REF6045	$V_{OUT} + 0.25$		5.5	
	REF6050	5.3		5.5	
$V_{EN}$ Enable voltage		0		$V_{IN}$	V
$I_L$ Output current	REF6025, REF6030, REF6033, REF6041	-4		4	mA
	REF6045	-3.5		3.5	
	REF6050	-3		3	
$T_A$ Operating temperature		-40	25	125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		REF60xx	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.5	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	5.2	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	78.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{ V}$  for all devices except REF6050,  $V_{IN} = 5.4\text{ V}$  for REF6050,  $I_L = 0\text{ mA}$ ,  $C_L = 22\text{ }\mu\text{F}$ ,  $C_{FILT} = 1\text{ }\mu\text{F}$ , and  $V_{EN} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>ACCURACY AND DRIFT</b>							
Output voltage accuracy				-0.05%		0.05%	
Output voltage temperature coefficient <sup>(1)</sup>						5	ppm/ $^\circ\text{C}$
<b>LINE AND LOAD REGULATION</b>							
$\Delta V_{O(\Delta V_I)}$ Line regulation	REF6025	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$T_A = 25^\circ\text{C}$		4	20	ppm/V
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			30	
	REF6030, REF6033, REF6041, REF6045	$V_{OUT} + 0.25\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$T_A = 25^\circ\text{C}$		4	20	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			30	
	REF6050	$V_{OUT} + 0.3\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$T_A = 25^\circ\text{C}$		7	60	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			120	
$\Delta V_{O(\Delta I_L)}$ Load regulation, sourcing and sinking	REF6025, REF6030, REF6033, REF6041	$I_L = 0\text{ mA}$ to $4\text{ mA}$ , $V_{IN} = V_{OUT} + 600\text{ mV}$	$T_A = 25^\circ\text{C}$		2	20	ppm/mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			30	
	REF6045	$I_L = 0\text{ mA}$ to $3.5\text{ mA}$ , $V_{IN} = V_{OUT} + 600\text{ mV}$	$T_A = 25^\circ\text{C}$		2	20	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			30	
	REF6050	$I_L = 0\text{ mA}$ to $3\text{ mA}$ , $V_{IN} = V_{OUT} + 400\text{ mV}$	$T_A = 25^\circ\text{C}$		2	20	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			50	
$I_{SC}$ Short-circuit current	SS = open				10.5		mA
<b>NOISE</b>							
Total integrated noise	$C_L = 22\text{ }\mu\text{F}$				5		$\mu\text{V}_{RMS}$
	$C_L = 47\text{ }\mu\text{F}$				5		
Low frequency noise	$0.1\text{ Hz} \leq f \leq 10\text{ Hz}$				3		$\mu\text{V}_{PP}/\text{V}$
<b>OUTPUT IMPEDANCE</b>							
Output impedance	$f = \text{DC}$ to $200\text{ kHz}$ , $C_L = 47\text{ }\mu\text{F}$				50		m $\Omega$
<b>TURN-ON TIME</b>							
$t_{on}$ Turn-on time	0.1% settling, $C_L = 47\text{ }\mu\text{F}$ , SS = open, REF6025				100		ms
<b>HYSTERESIS AND LONG TERM DRIFT</b>							
Long term stability	0 to 1000h at $25^\circ\text{C}$				80		ppm
	1000h to 2000h at $25^\circ\text{C}$				20		
Output voltage hysteresis <sup>(2)</sup>	25 $^\circ\text{C}$ , -40 $^\circ\text{C}$ , 125 $^\circ\text{C}$ , 25 $^\circ\text{C}$ (cycle 1)				33		ppm
	25 $^\circ\text{C}$ , -40 $^\circ\text{C}$ , 125 $^\circ\text{C}$ , 25 $^\circ\text{C}$ (cycle 2)				8		
<b>CAPACITIVE LOAD</b>							
$C_L$ Stable output capacitor value					10	47	$\mu\text{F}$

(1) Temperature drift is specified according to the box method. See the [Feature Description](#) section for more details.

(2) See the [Thermal Hysteresis](#) section.

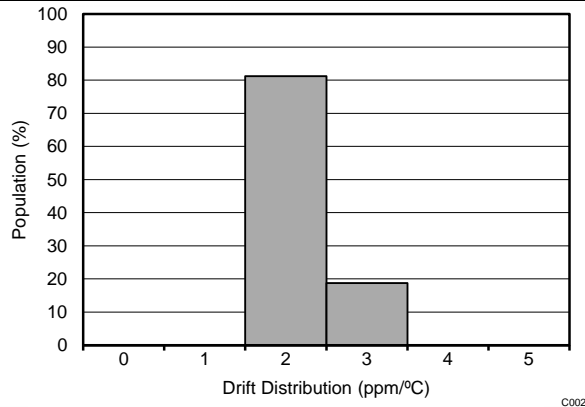
**Electrical Characteristics (continued)**

at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{ V}$  for all devices except REF6050,  $V_{IN} = 5.4\text{ V}$  for REF6050,  $I_L = 0\text{ mA}$ ,  $C_L = 22\text{ }\mu\text{F}$ ,  $C_{FILT} = 1\text{ }\mu\text{F}$ , and  $V_{EN} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>OUTPUT VOLTAGE</b>							
$V_{OUT}$	Output voltage	REF6025		2.5		V	
		REF6030		3			
		REF6033		3.3			
		REF6041		4.096			
		REF6045		4.5			
		REF6050		5			
<b>POWER SUPPLY</b>							
$I_{CC}$	Supply current	REF6025, REF6030, REF6033, REF6041	Active mode, $V_{EN} = 5\text{ V}$	$T_A = 25^\circ\text{C}$	0.82	0.90	mA
				$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	1.1		
		REF6045, REF6050	Active mode, $V_{EN} = 5\text{ V}$	$T_A = 25^\circ\text{C}$	0.83	0.95	
				$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	1.15		
			Shutdown mode, $V_{EN} = 0\text{ V}$	$T_A = 25^\circ\text{C}$	1	3	$\mu\text{A}$
				$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	15		
Enable pin voltage	Voltage reference in active mode ( $EN = 1$ )			1.6		V	
	Voltage reference in shutdown mode ( $EN = 0$ )			0.6			
Enable pin current	$V_{EN} = 5\text{ V}$			100	150	nA	
Dropout voltage	REF6025	$I_L = 0\text{ mA}$		500	500	mV	
		$I_L = 4\text{ mA}$		600			
	REF6030, REF6033, REF6041	$I_L = 0\text{ mA}$		50	250		
		$I_L = 4\text{ mA}$		600			
	REF6045	$I_L = 0\text{ mA}$		50	250		
		$I_L = 3.5\text{ mA}$		600			
	REF6050	$I_L = 0\text{ mA}$		100	300		
		$I_L = 3\text{ mA}$		400			

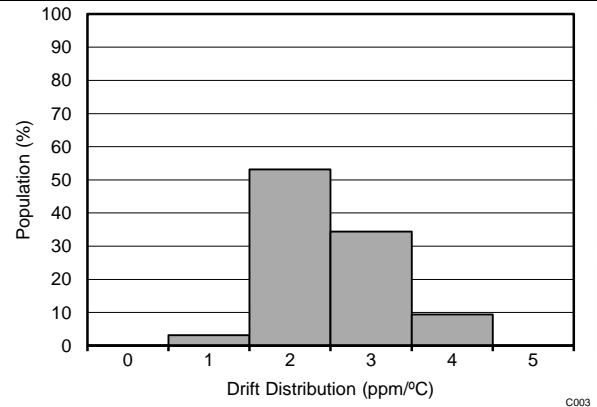
## 7.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , using REF6025 (unless otherwise noted)



$T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$

Figure 1. Drift Distribution



$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Figure 2. Drift Distribution

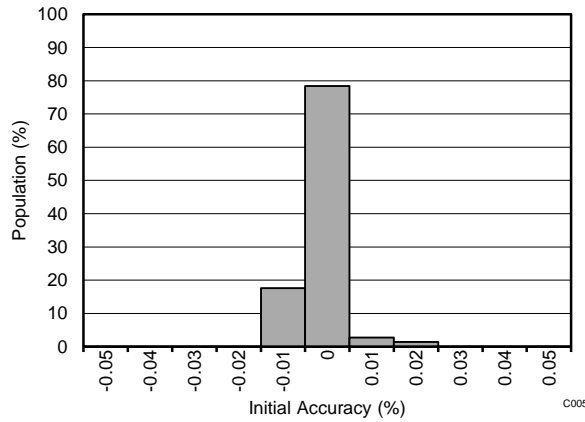


Figure 3. Initial Accuracy Distribution

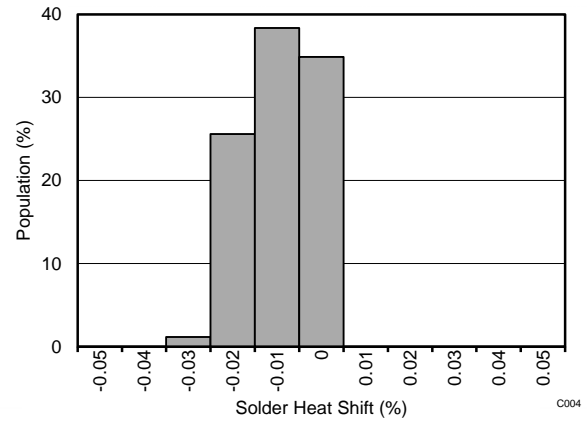


Figure 4. Solder-Heat Shift Distribution

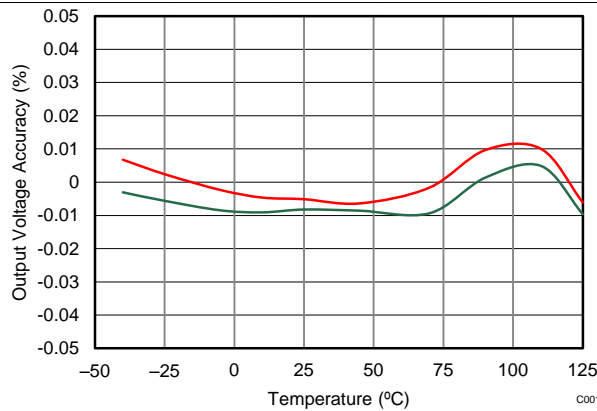


Figure 5. Output Voltage Accuracy vs Temperature

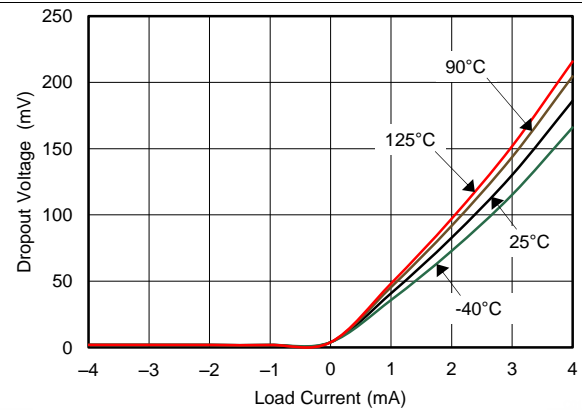
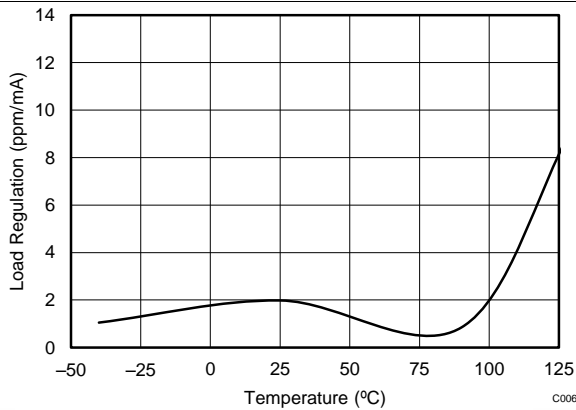


Figure 6. Dropout Voltage vs Load Current

### Typical Characteristics (continued)

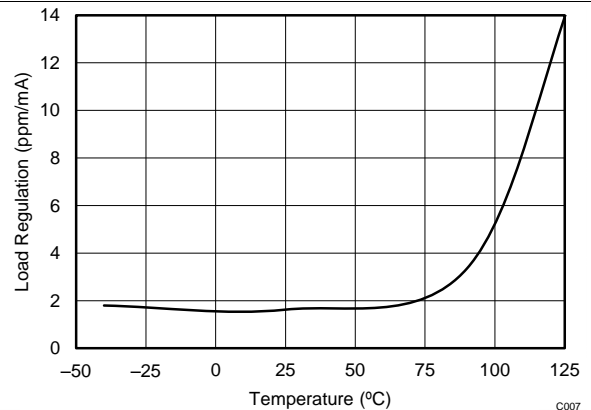
at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , using REF6025 (unless otherwise noted)



$$V_{IN} = V_{OUT} + 600\text{ mV},$$

$$I_L = 0\text{ mA to } 4\text{ mA}$$

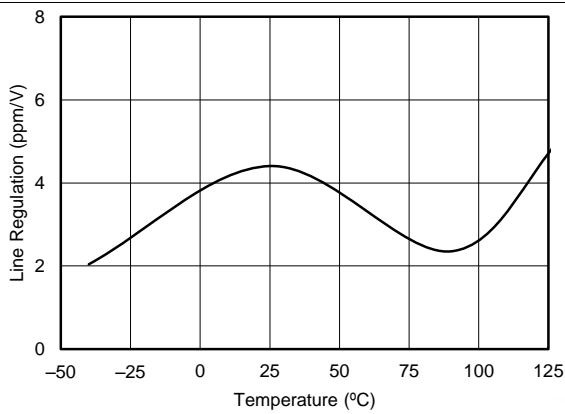
Figure 7. Load Regulation Sourcing vs Temperature



$$V_{IN} = V_{OUT} + 600\text{ mV},$$

$$I_L = 0\text{ mA to } 4\text{ mA}$$

Figure 8. Load Regulation Sinking vs Temperature



$$V_{OUT} + 0.25\text{ V} \leq V_{IN} \leq 5.5\text{ V}$$

Figure 9. Line Regulation vs Temperature

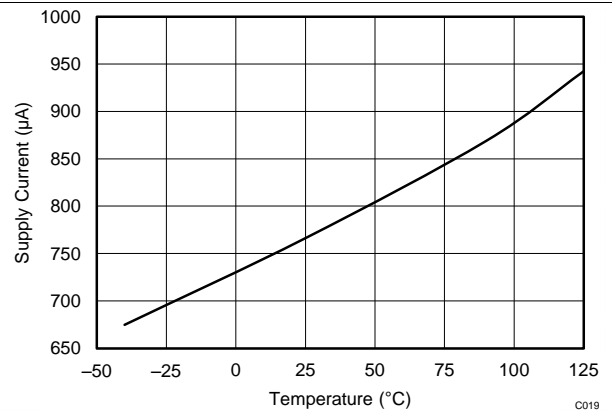


Figure 10. Supply Current vs Temperature

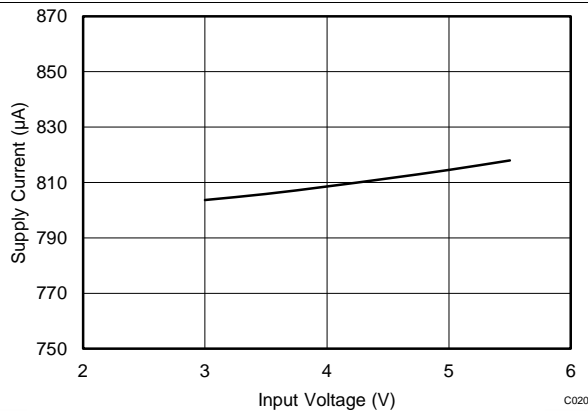


Figure 11. Supply Current vs Input Voltage

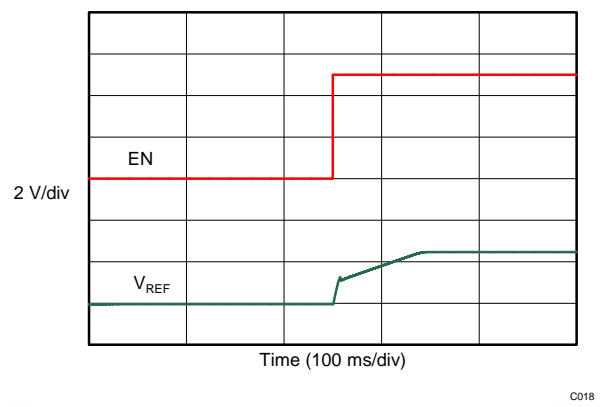
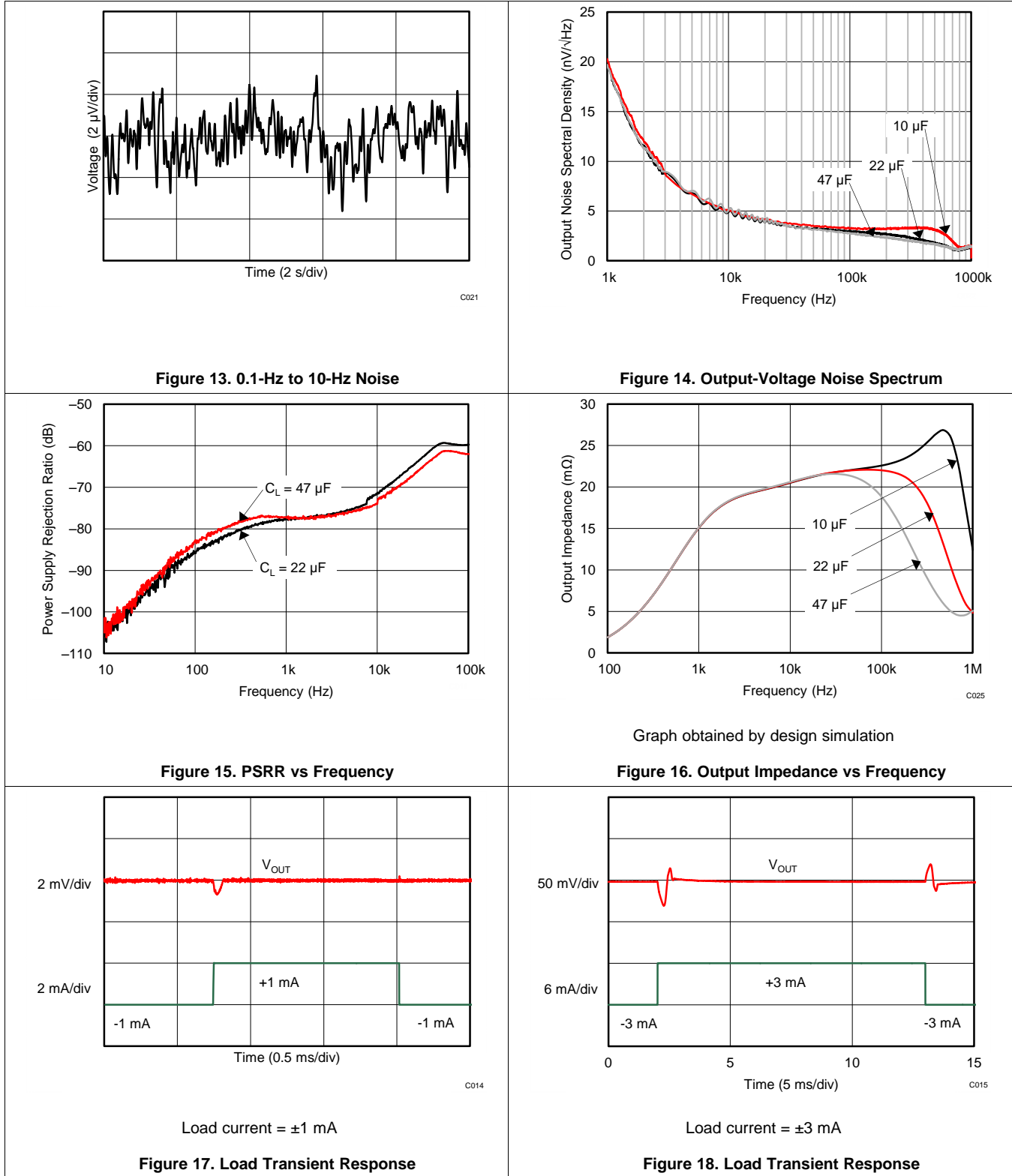


Figure 12. Turn-On Settling Time



Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , using REF6025 (unless otherwise noted)



Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , using REF6025 (unless otherwise noted)

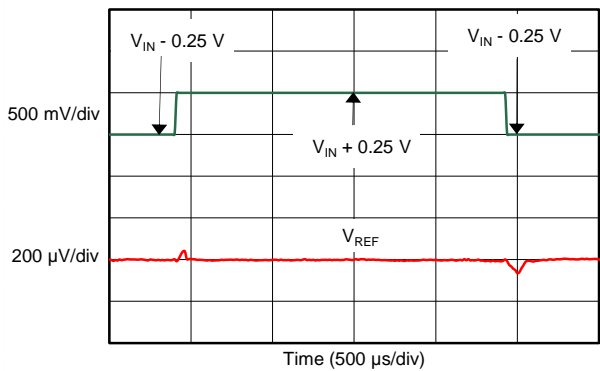


Figure 19. Line Transient Response

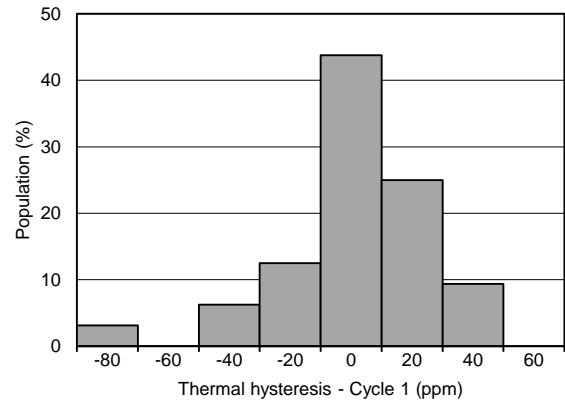


Figure 20. Thermal Hysteresis Distribution (Cycle 1)

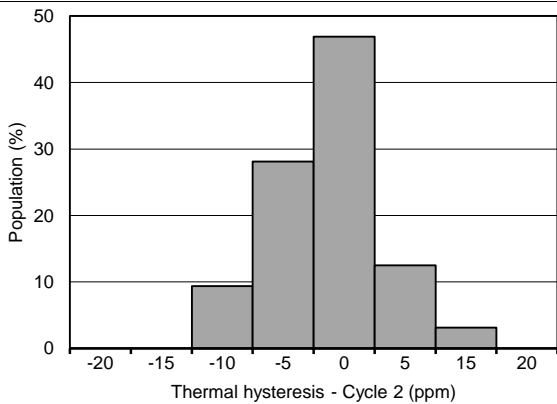


Figure 21. Thermal Hysteresis Distribution (Cycle 2)

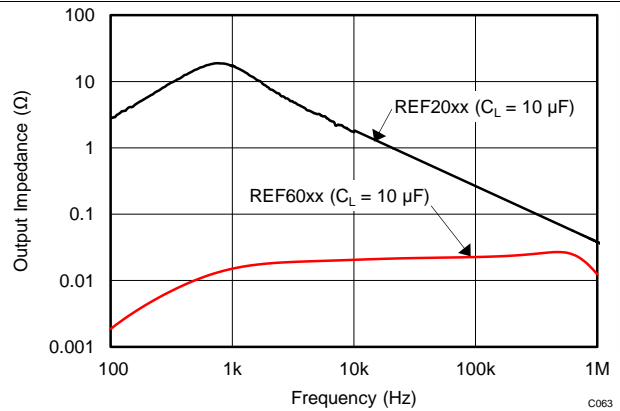


Figure 22. Output Impedance Comparison

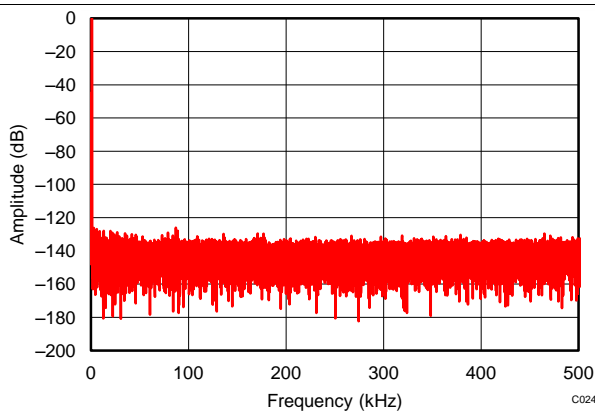


Figure 23. Typical FFT Plot

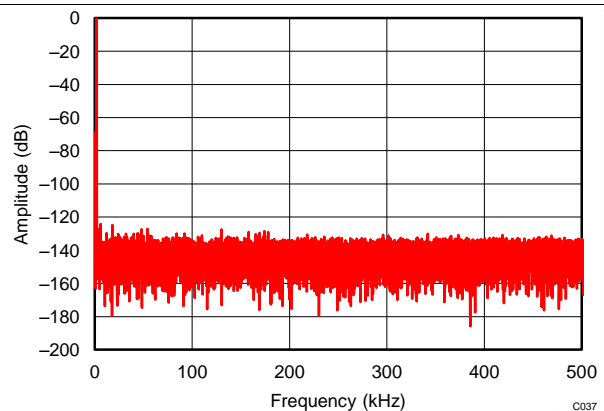
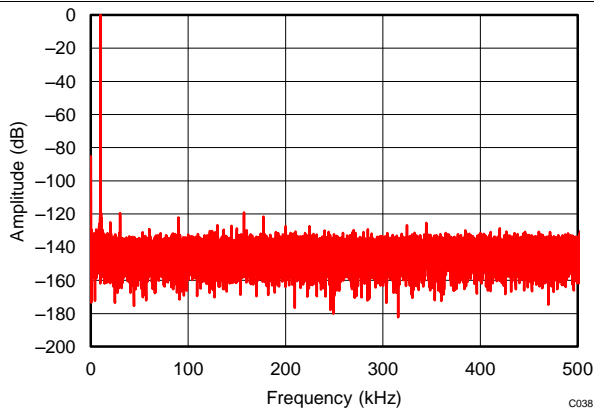


Figure 24. Typical FFT Plot

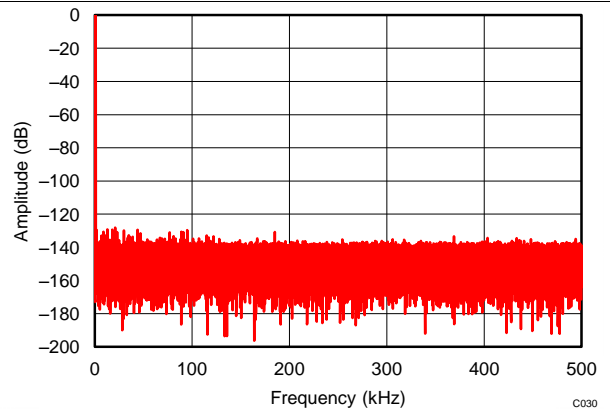
Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , using REF6025 (unless otherwise noted)



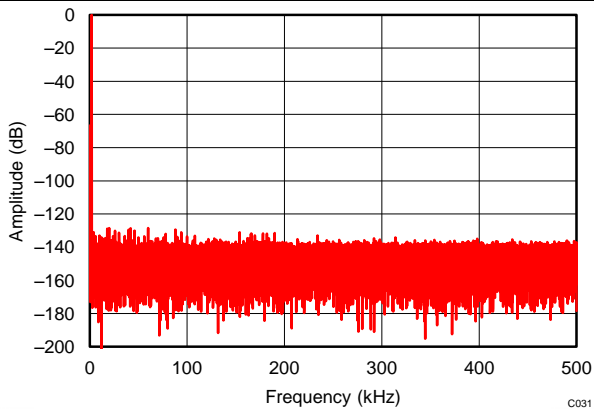
REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 10\text{ kHz}$ , SNR = 99.2 dB, THD = -119.4 dB

Figure 25. Typical FFT Plot



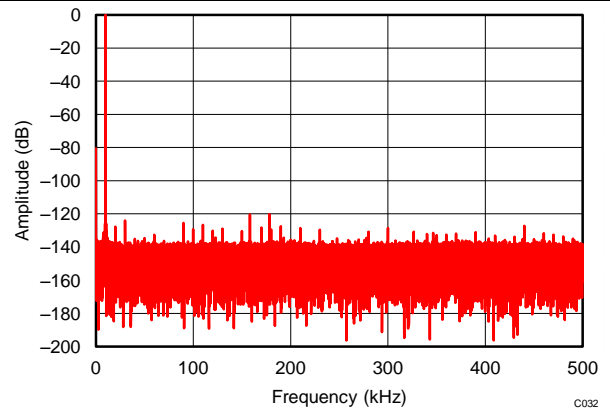
REF6041 driving REF pin of ADS8881,  
 $f_{IN} = 1\text{ kHz}$ , SNR = 99 dB, THD = -124.4 dB

Figure 26. Typical FFT Plot



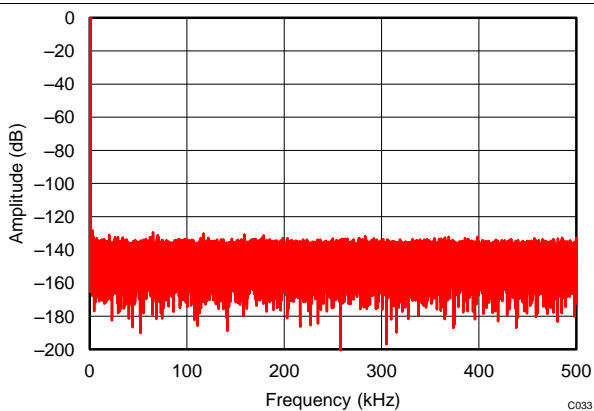
REF6041 driving REF pin of ADS8881,  
 $f_{IN} = 2\text{ kHz}$ , SNR = 99 dB, THD = -123.6 dB

Figure 27. Typical FFT Plot



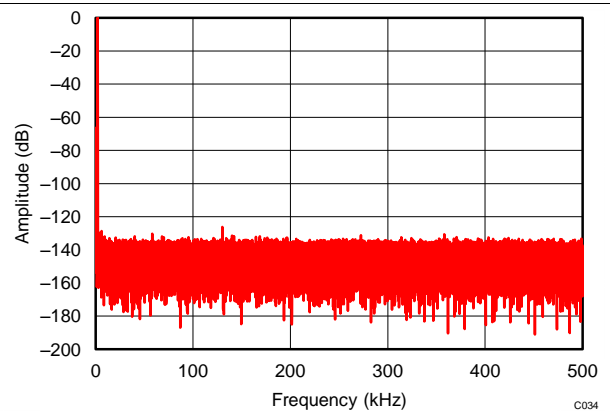
REF6041 driving REF pin of ADS8881,  
 $f_{IN} = 10\text{ kHz}$ , SNR = 97.2 dB, THD = -119.7 dB

Figure 28. Typical FFT Plot



REF6025 driving REF pin of ADS8881,  
 $f_{IN} = 1\text{ kHz}$ , SNR = 95.4 dB, THD = -124 dB

Figure 29. Typical FFT Plot

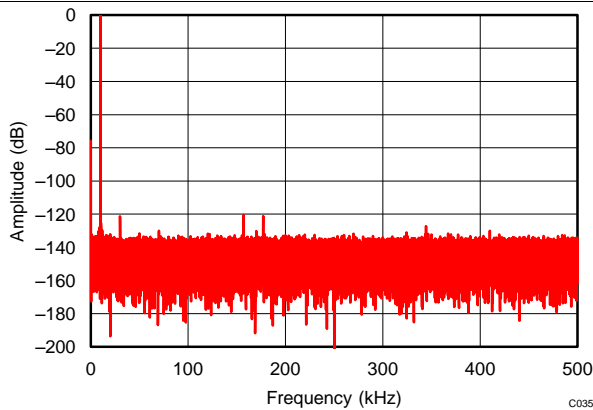


REF6025 driving REF pin of ADS8881,  
 $f_{IN} = 2\text{ kHz}$ , SNR = 95.4 dB, THD = -123.5 dB

Figure 30. Typical FFT Plot

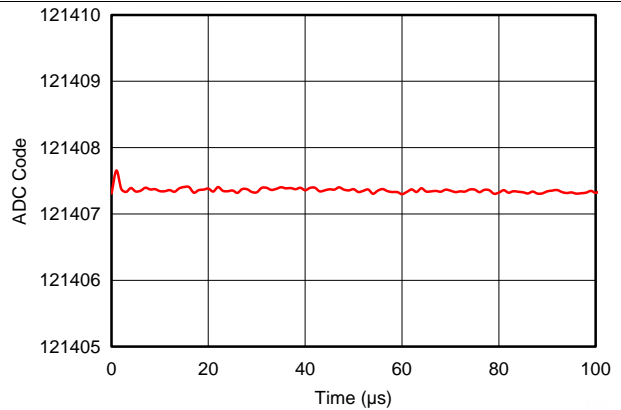
Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , using REF6025 (unless otherwise noted)



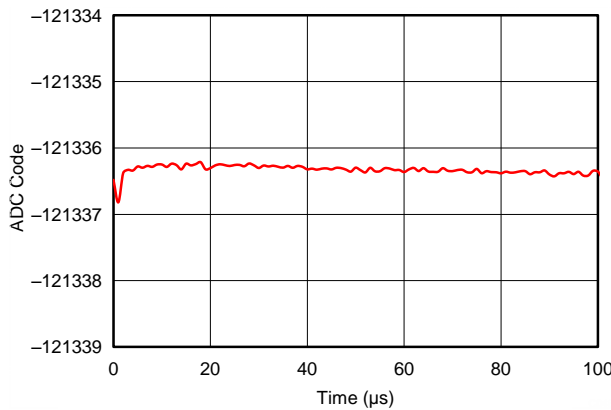
REF6025 driving REF pin of ADS8881,  
 $f_{IN} = 10\text{ kHz}$ , SNR = 94.0 dB, THD = -119.3 dB

Figure 31. Typical FFT Plot



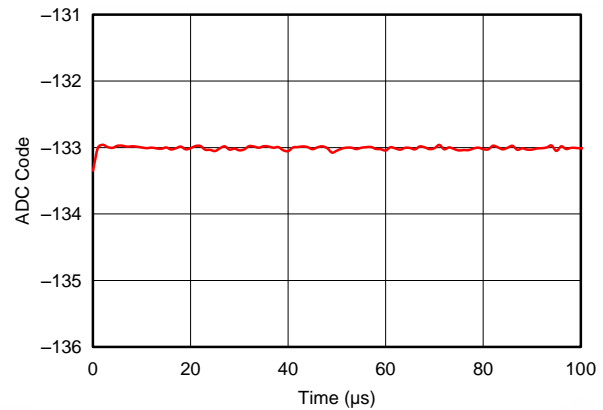
REF6050 driving REF pin of ADS8881 operating at 1 MSPS,  
positive full-scale input to ADS8881

Figure 32. Reference Droop



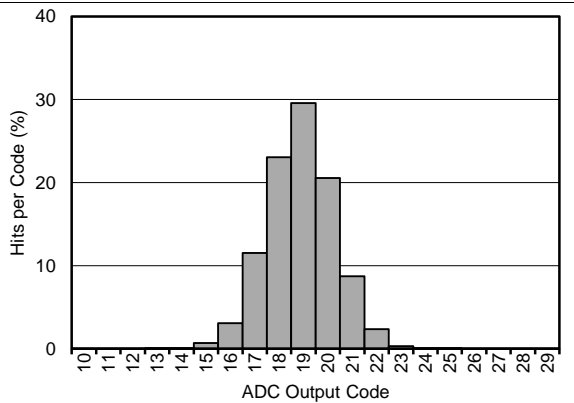
REF6050 driving REF pin of ADS8881 operating at 1 MSPS,  
negative full-scale input to ADS8881

Figure 33. Reference Droop



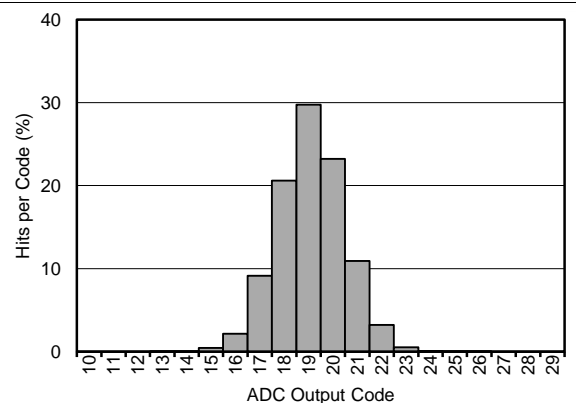
REF6050 driving REF pin of ADS8881 operating at 1 MSPS,  
 $A_{INP} = A_{INN} = V_{REF} / 2$  for ADS8881

Figure 34. Reference Droop



$A_{INP} = A_{INN} = V_{REF} / 2$  for ADS8881,  
sampling rate = 1 MSPS

Figure 35. DC Input Histogram

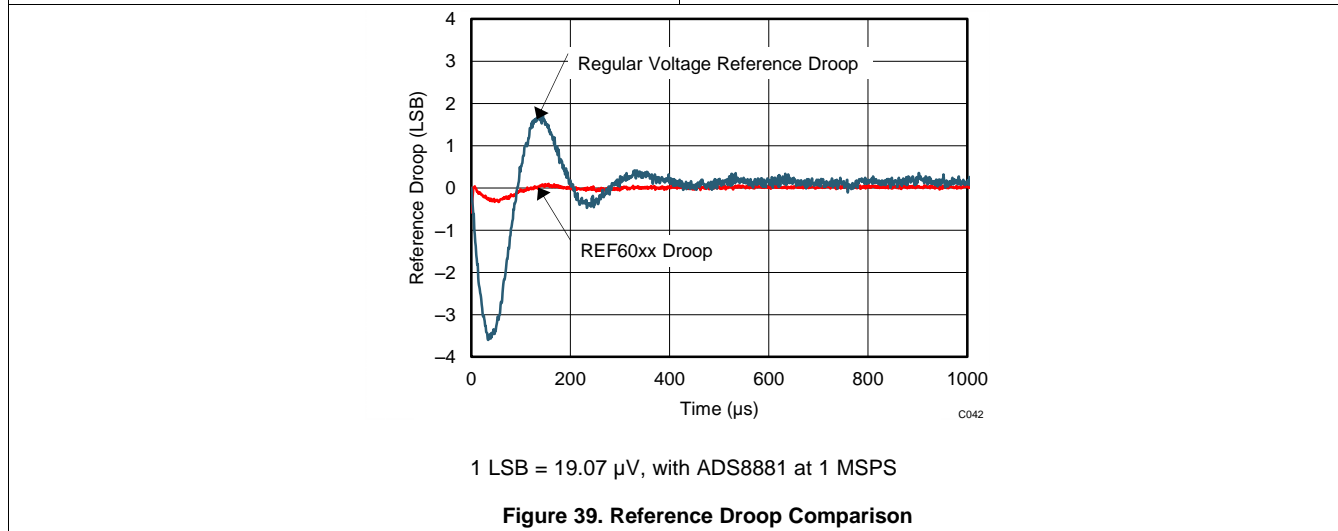
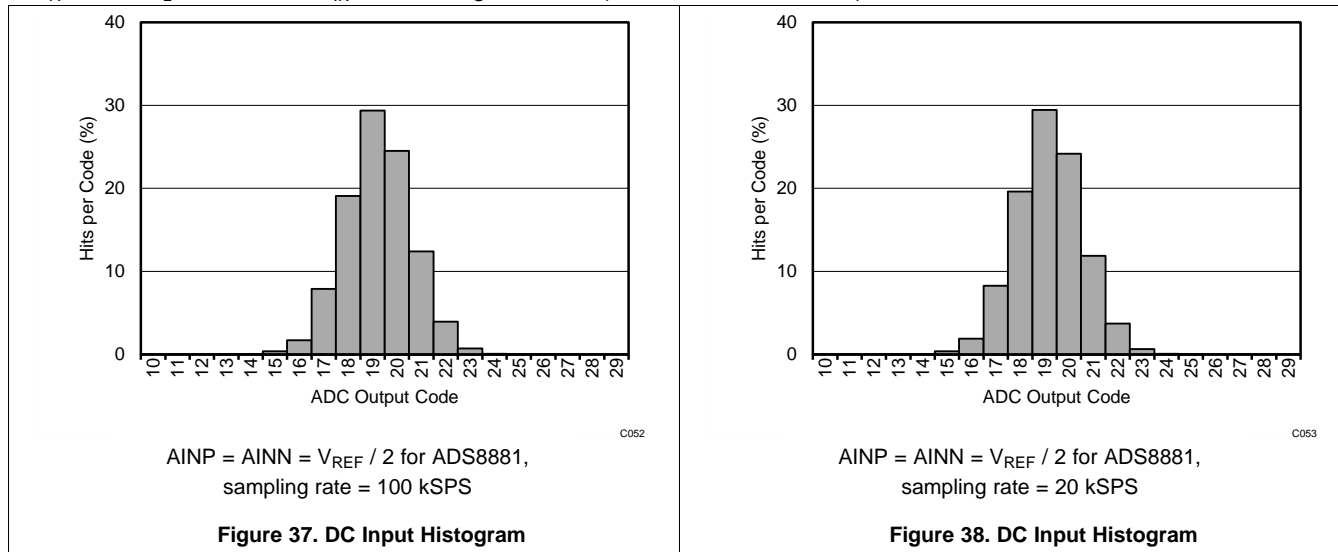


$A_{INP} = A_{INN} = V_{REF} / 2$  for ADS8881,  
sampling rate = 500 kSPS

Figure 36. DC Input Histogram

**Typical Characteristics (continued)**

at  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , using REF6025 (unless otherwise noted)



## 8 Parameter Measurement Information

### 8.1 Solder Heat Shift

The materials used in the manufacture of the REF60xx have differing coefficients of thermal expansion, and result in stress on the device die when the part is heated. Mechanical and thermal stress on the device die sometimes causes the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 128 devices were soldered on eight printed circuit boards (PCBs), with 16 devices on each PCB, using lead-free solder paste, and the manufacturer-suggested reflow profile. The reflow profile is as shown in Figure 40. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 101.6 mm × 127 mm.

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in Figure 41. Although all tested units exhibit very low shifts (< 0.03%), higher shifts are also possible depending on the size, thickness, and material of the PCB.

The histogram displays the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, solder the device in the final pass to minimize exposure to thermal stress.

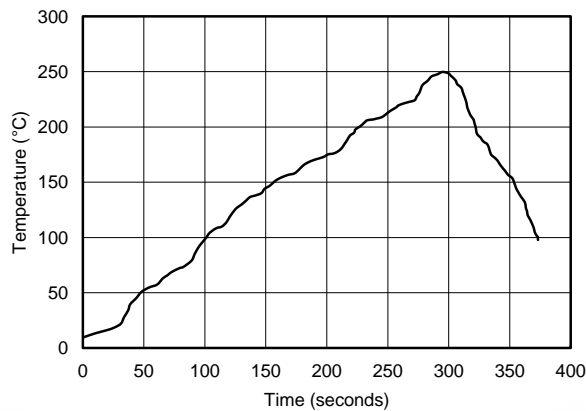


Figure 40. Reflow Profile

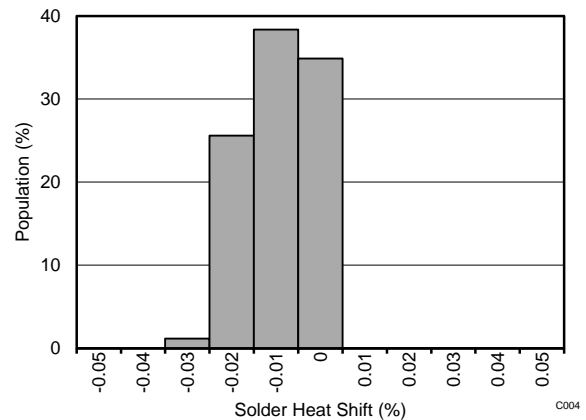


Figure 41. Solder Heat Shift Distribution

## 8.2 Thermal Hysteresis

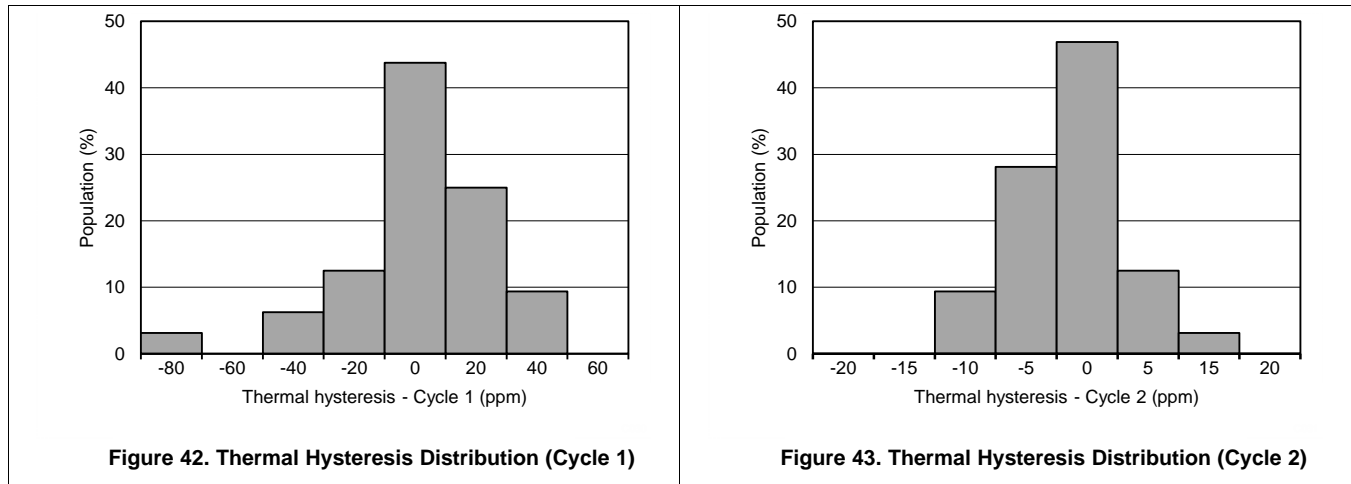
Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Thermal hysteresis was measured with the REF60xx soldered to a PCB, similar to a real-world application. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Thermal hysteresis is expressed as:

$$V_{\text{HYST}} = \left( \frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \cdot 10^6 \text{ (ppm)}$$

where

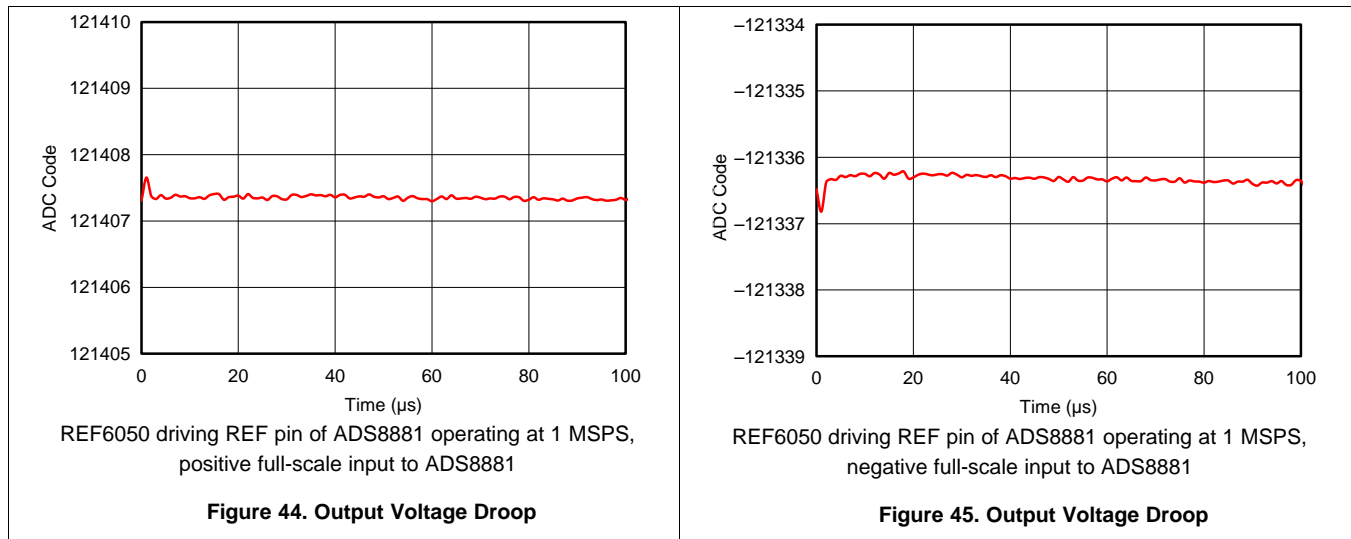
- $V_{\text{HYST}}$  = thermal hysteresis (in units of ppm).
- $V_{\text{NOM}}$  = the specified output voltage.
- $V_{\text{PRE}}$  = output voltage measured at 25°C pretemperature cycling.
- $V_{\text{POST}}$  = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C. (1)

Typical thermal hysteresis distribution is shown in [Figure 42](#) and [Figure 43](#).



### 8.3 Reference Droop Measurements

Many applications, such as event-triggered and multiplexed data-acquisition systems, require the very first conversion of the ADC to have 18-bit or greater precision. These types of data-acquisition systems capture data in bursts, and are also called burst-mode, data-acquisition systems. Achieving 18-bit precision for the first sample is a very difficult using a conventional voltage reference because the voltage reference droop limits the accuracy of the first few conversions. The REF60xx have an integrated ADC drive buffer that makes sure the reference droop is less than 1 LSB at 18-bit precision when used with the ADS8881, even at full throughput. [Figure 44](#) and [Figure 45](#) show the REF60xx output voltage droop when driving the REF pin of the ADS8881 at positive and negative full-scale inputs, respectively.



Direct measurement of the reference droop to 18-bit accuracy can be a challenging process. Therefore, the plots in [Figure 44](#) and [Figure 45](#) were obtained by processing the output code of the ADC. The ADC output code is given by:

$$C = (\text{Input Voltage} / V_{\text{REF}}) \times 2^N \quad (2)$$

If the input voltage is kept constant,  $V_{\text{REF}}$  is computed by monitoring the ADC output code  $C$ . The ADC code usually has six to seven LSBs of code spread due to the inherent noise of the ADC. In order to measure reference droop, this noise must be reduced drastically. Noise reduction is done by averaging the output code multiple times, as described in the next paragraph.



## Reference Droop Measurements (continued)

Figure 46 shows the setup that was used to measure the reference droop. The output ADC code was captured using a field-programmable gate array (FPGA), and post-processing was done on a personal computer. The input to the THS4521, and hence in turn to the ADS8881, is a constant dc voltage (close to positive or negative full-scale because this condition is the worst-case for charge drawn from the REF pin). The dc source must have extremely low noise. After the REF60xx device is powered up and stable, the FPGA sends commands to the ADS8881 to capture data in bursts. The ADS8881 is initially in idle mode for 100 ms. The FPGA then sends a command to the ADS8881 to perform 100 conversions at 1 MSPS. The ADC code corresponding to these 100 conversions (one burst of data) is stored as the first row in a 1000 × 100 dimensional array. This operation is repeated 1000 times, and the data corresponding to each burst is stored in a new row of the 1000 × 100 dimensional array. Finally, each column in this array is averaged to get a final data-set of 100 elements. This final data-set now has code spread that is much less than 1 LSB because most of the noise has now been removed through averaging. This data-set was plotted on a graph with X axis = column number (each column number corresponds to 1 μs of time because the sampling rate is 1 MSPS), and Y axis = ADC output code to obtain reference-droop measurements.

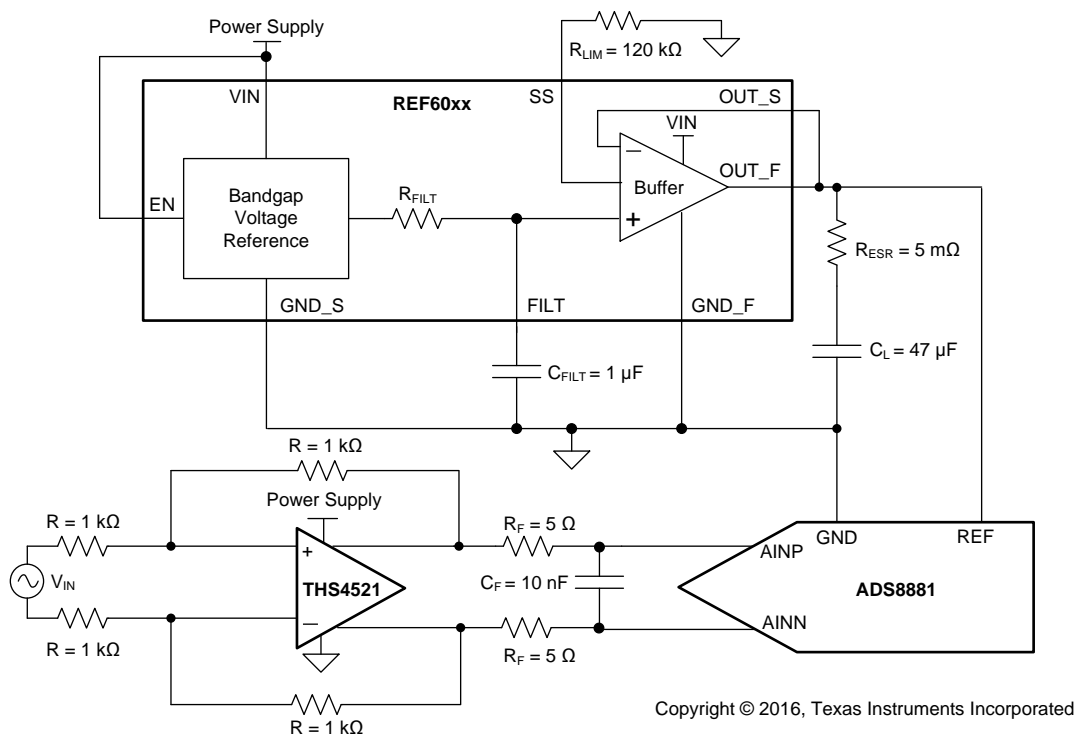
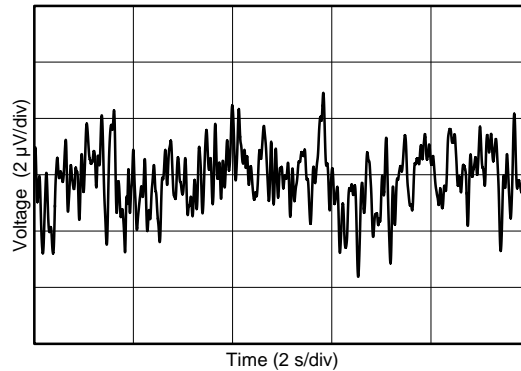


Figure 46. Burst-Mode Measurement Setup

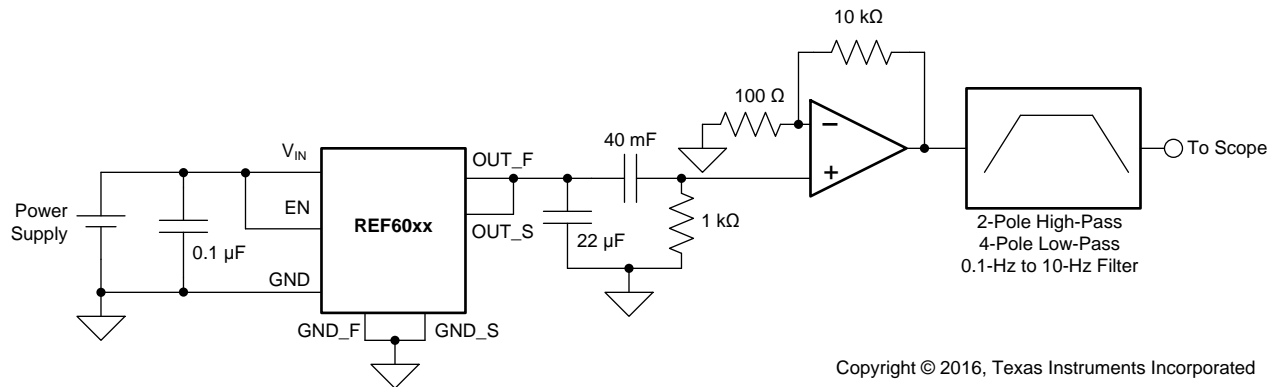
### 8.4 1/f Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise for the REF6025 is shown in Figure 47. The 1/f noise scales with output voltage, but remains  $3 \mu\text{V}_{\text{pp}}/\text{V}$  for all the variants. Peak-to-peak noise measurement setup is shown in Figure 48.



C021

**Figure 47. 0.1-Hz to 10-Hz Noise**



**Figure 48. 0.1-Hz to 10-Hz Noise Measurement Setup**

## 9 Detailed Description

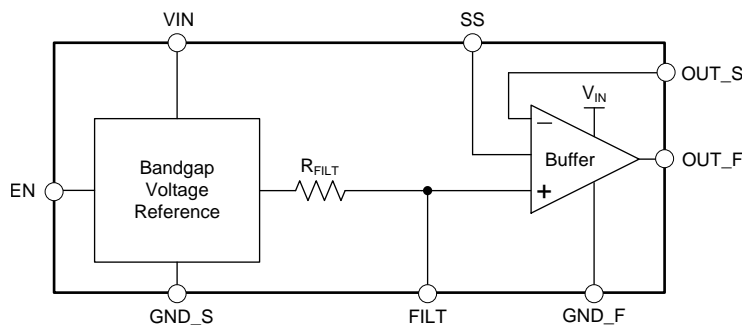
### 9.1 Overview

Most SAR ADCs, and a few delta-sigma ADCs, switch binary-weighted capacitors onto the REF pin during the conversion process. The magnitude of the capacitance switched onto the REF pin during each conversion depends on the input signal to the ADC. If a voltage reference is directly connected to the REF pin of these ADCs, the reference voltage droops because of the dynamic input signal dependent load of the binary-weighted capacitors. Because the reference voltage droop now has input signal dependence, significant degradation in THD and linearity for the system occurs.

In order to support this dynamic load and preserve the ADC linearity, distortion and noise performance, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF60xx family of voltage references have an integrated low output impedance buffer that enables the user to directly drive the REF pin of a SAR ADC, while preserving ADC linearity and distortion. In addition, the total noise in the full bandwidth of the REF60xx is extremely low, thus preserving the noise performance of the ADC. [Voltage-Reference Impact on Total Harmonic Distortion \(SLYY097\)](#) correlates the effect of reference settling to ADC distortion, and how the REF60xx achieves lowest distortion with minimal components and lowest power consumption.

The output voltage of the REF60xx does not droop below 1 LSB (18-bit), even during the first conversion while driving the REF pin of the ADS8881. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems. [Functional Block Diagram](#) shows a simplified schematic of the REF60xx.

### 9.2 Functional Block Diagram

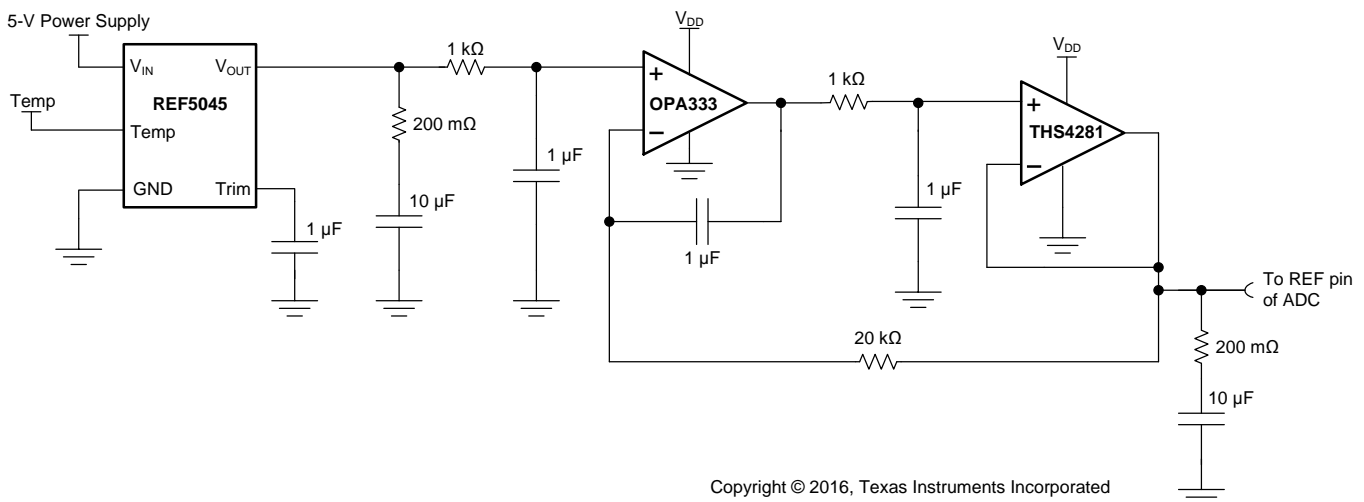


## 9.3 Feature Description

### 9.3.1 Integrated ADC Drive Buffer

Many ADC data sheets specify a few microamps of average current draw from the REF pin. Almost all voltage references provide these few microamps of average current; but not all voltage references are practical for driving a high-resolution, high-throughput SAR ADC because the peak current drawn can be very high when the capacitors are switched on the REF pin. The worst-case demand for the voltage reference is during a burst-mode conversion, when the ADC is idle for a very long time, before a conversion is initiated, and the first sample converted is expected to be precise. Usually, a large capacitor is connected between the REF pin and ground pin (or sometimes between the REFP and REFM pins) of the ADC to smoothen the current load and reduce the burden on the voltage reference. The voltage reference must then be capable of providing the average current required to completely charge the reference capacitor, but without causing the reference voltage to droop significantly. Most voltage references lack the ability to completely charge the reference capacitor, and settle when the binary-weighted capacitors are being switched onto the REF pin because of the large output impedance. Usually, voltage references have output impedances in the range of 10's of ohms at frequencies higher than 100 Hz. The output voltage of the voltage reference must be buffered with a low output impedance (usually high bandwidth) amplifier to achieve excellent linearity and distortion performance.

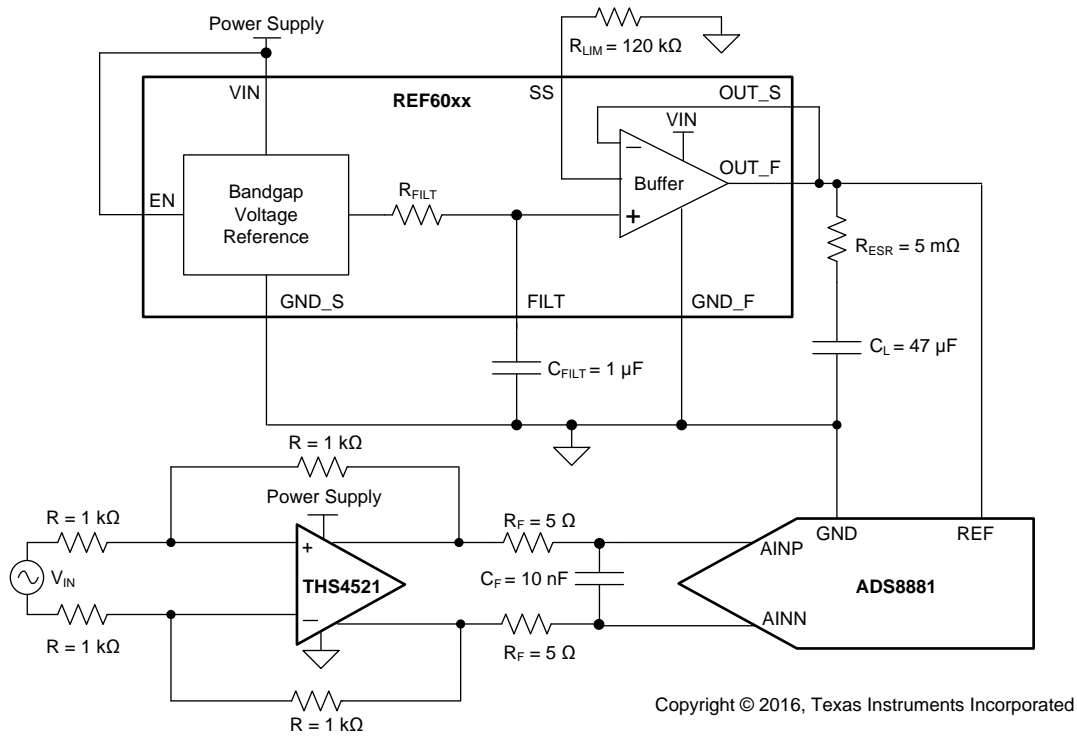
The key amplifier specifications to be considered when designing a reference buffer for a high-precision ADC are: low offset, low drift, wide bandwidth, and low output impedance. While it is possible to select an amplifier that sufficiently meets all these requirements, the amplifier comes at a cost of excessive power consumption. For example, the [OPA350](#) is a 38-MHz bandwidth amplifier with a maximum offset of 0.5 mV, and low offset drift of 4  $\mu\text{V}/^\circ\text{C}$ , but consumes a quiescent current of 5.2mA. This is because (from an amplifier design perspective) offset and drift are dc specifications, whereas bandwidth, low output impedance, and high capacitive drive capability are high-frequency specifications. Therefore, achieving all the performance in one amplifier requires power. However, a more efficient design to meet the low power budget is to use a composite reference buffer, which uses an amplifier with superior high-frequency specifications in the feedback loop of a dc precision amplifier to get the overall performance at much lower power consumption. [Figure 49](#) shows such a composite amplifier design with the [OPA333](#) (dc precision amplifier) and [THS4281](#) (high-bandwidth amplifier). This reference buffer design requires three devices, and a large number of external components. This solution still consumes close to 2 mA of quiescent current.



**Figure 49. Composite Amplifier Reference Buffer**

Feature Description (continued)

The REF60xx family of voltage references have an integrated low output impedance buffer (ADC drive buffer); therefore, there is no need for an external buffer while driving the REF pin of high-precision, high-throughput SAR ADCs, as shown in Figure 50. The ADC drive buffer of the REF60xx is capable of replenishing a charge of 70 pC on a 47-μF capacitor in 1 μs, without allowing the voltage on the capacitor to droop more than 1 LSB at 18-bit precision. The REF60xx are trimmed at multiple temperatures in production, achieving a max drift of just 5 ppm/°C for both the voltage reference and the buffer combined, while operating at a typical quiescent current of 820 μA. Figure 51 compares the output impedance of a regular voltage reference (REF20xx) and a voltage reference with integrated ADC drive buffer (REF60xx). Figure 52 compares the burst-mode, reference-setting performance of a regular voltage reference and the REF60xx.



Copyright © 2016, Texas Instruments Incorporated

Figure 50. REF60xx Driving REF Pin of ADS8881 SAR ADC

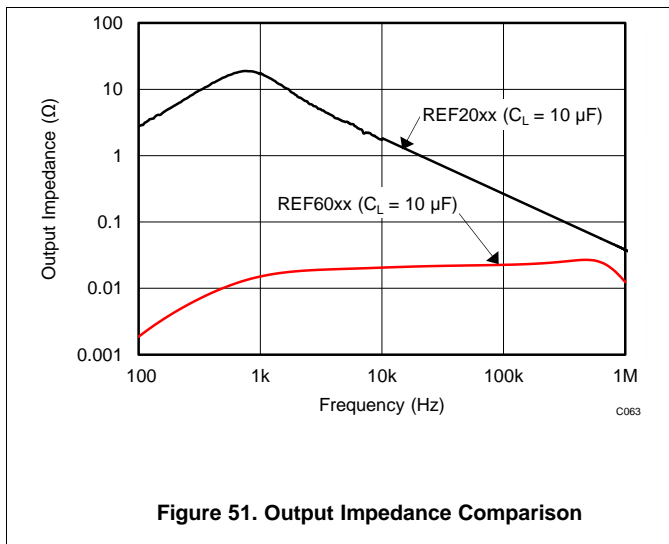
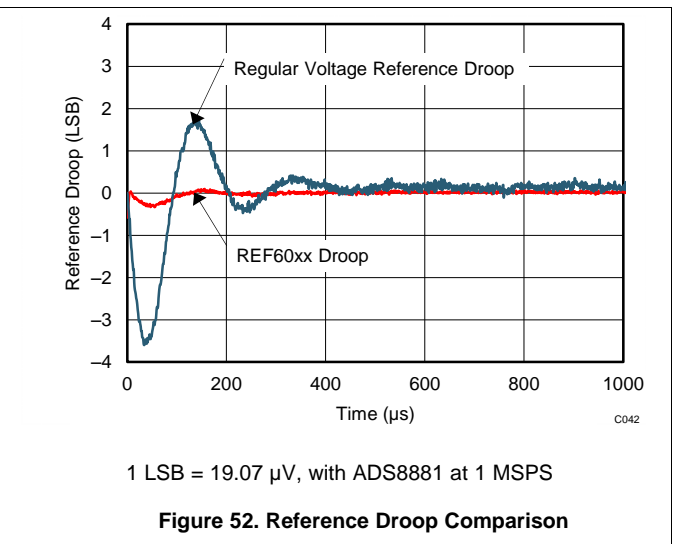


Figure 51. Output Impedance Comparison



1 LSB = 19.07 μV, with ADS8881 at 1 MSPS

Figure 52. Reference Droop Comparison

## Feature Description (continued)

### 9.3.2 Temperature Drift

The REF60xx family is designed for minimal drift error, defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left( \frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF}} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm}) \quad (3)$$

### 9.3.3 Load Current

The REF6025, REF6030, REF6033 and REF6041 are specified to deliver current load of  $\pm 4$  mA. The REF6045 is specified to deliver  $\pm 3.5$  mA, and the REF6050 is specified to deliver  $\pm 3$  mA. The REF60xx are protected from short circuits at the output by limiting the output short-circuit current.

The short-circuit current limit ( $I_{\text{SC}}$ ) of the REF60xx family of devices is adjusted by connecting a resistor ( $R_{\text{SS}}$ ) on the SS pin. The short-circuit current limit when the REF60xx device is sourcing current can be calculated as shown in [Equation 4](#):

$$I_{\text{SC}} = (80 \cdot 10^{-9}) \cdot R_{\text{SS}} + (3 \cdot 10^{-3}) \quad (4)$$

The short circuit current limit when the REF60xx device is sinking is calculated as shown in [Equation 5](#):

$$I_{\text{SC}} = (115 \cdot 10^{-9}) \cdot R_{\text{SS}} + (4.6 \cdot 10^{-3}) \quad (5)$$

The recommended output current of the REF60xx also depends on the resistor connected to the SS pin. The recommended output current (sourcing and sinking) for the REF6025, REF6030, REF6033 and REF6041 is given by [Equation 6](#):

$$I_{\text{L}} = (31.25 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.25 \cdot 10^{-3}) \quad (6)$$

The recommended output current (sourcing and sinking) for the REF6045 is given by [Equation 7](#):

$$I_{\text{L}} = (27.08 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.25 \cdot 10^{-3}) \quad (7)$$

The recommended output current (sourcing and sinking) for the REF6050 is given by [Equation 8](#):

$$I_{\text{L}} = (23.75 \cdot 10^{-9}) \cdot R_{\text{SS}} + (0.15 \cdot 10^{-3}) \quad (8)$$

The temperature of the device increases according to [Equation 9](#):

$$T_{\text{J}} = T_{\text{A}} + P_{\text{D}} \cdot R_{\theta\text{JA}}$$

where:

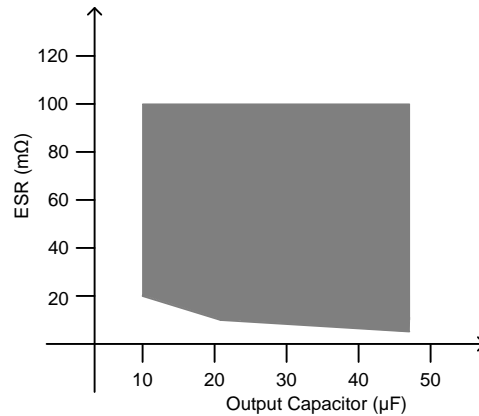
- $T_{\text{J}}$  = junction temperature ( $^{\circ}\text{C}$ ).
  - $T_{\text{A}}$  = ambient temperature ( $^{\circ}\text{C}$ ).
  - $P_{\text{D}}$  = power dissipated (W).
  - $R_{\theta\text{JA}}$  = junction-to-ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ ).
- (9)

The REF60xx maximum junction temperature must not exceed the absolute maximum rating of  $150^{\circ}\text{C}$ .

## Feature Description (continued)

### 9.3.4 Stability

The REF60xx family of voltage references are stable with output capacitor values ranging from 10  $\mu\text{F}$  to 47  $\mu\text{F}$ . At a low output-capacitor value of 10  $\mu\text{F}$ , an effective series resistance (ESR) of 20 m $\Omega$  to 100 m $\Omega$  is required for stability; whereas, at a higher value of 47  $\mu\text{F}$ , an ESR of 5 m $\Omega$  to 100 m $\Omega$  is required. The shaded region in [Figure 53](#) shows the stable region of operation for the REF60xx devices.



**Figure 53. Stable Output Capacitor Range**

A capacitor of value 1  $\mu\text{F}$  is required at the FILT pin for stability and noise performance. A low ESR (5 m $\Omega$  to 20 m $\Omega$ ) is easily achieved by increasing the PCB trace length, thus eliminating the need for a discrete resistor. Higher values of ESR (greater than 20 m $\Omega$ , but lesser than 100 m $\Omega$ ) can be intentionally added to increase the output bandwidth of the REF60xx. This higher ESR improves the transient performance of the REF60xx, but worsens noise performance because of increased bandwidth.

## 9.4 Device Functional Modes

When the EN pin of the REF60xx is pulled high, the device is in active mode. The device must be in active mode for normal operation.

To place the REF60xx into a shutdown mode, pull the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 1  $\mu\text{A}$  (typ). See the enable pin voltage parameter in the [Electrical Characteristics](#) table for logic high and logic low voltage levels.

## 10 Applications and Implementation

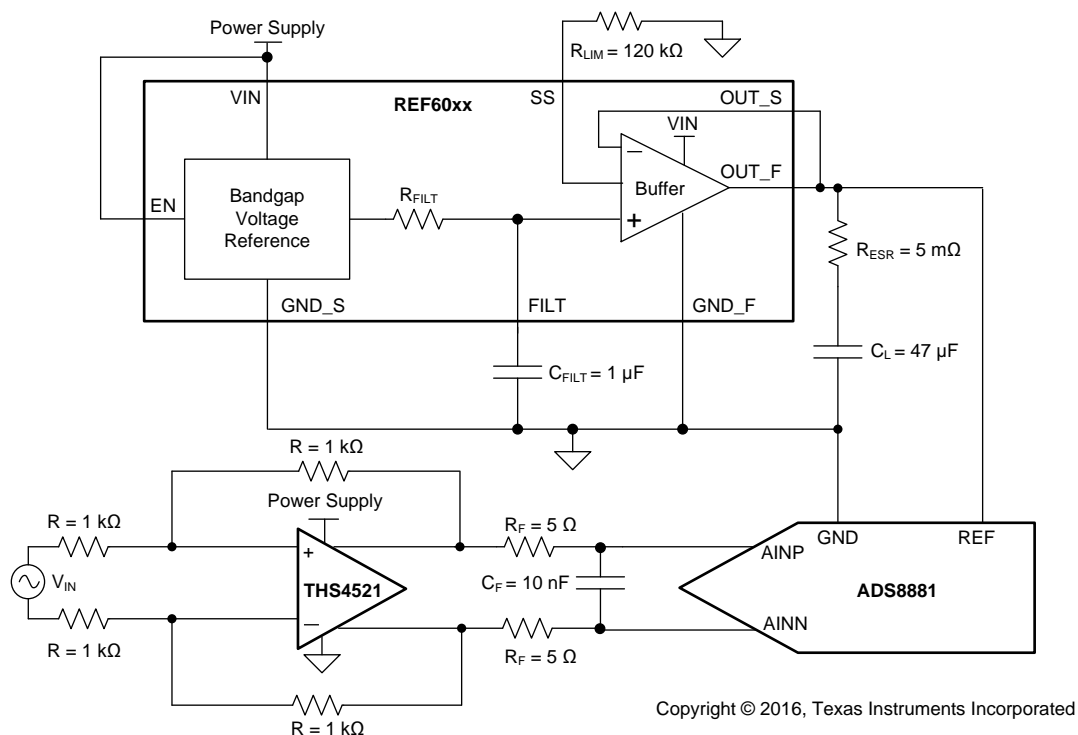
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

Many applications, such as event-triggered and multiplexed data-acquisition systems, require the very first conversion of the ADC to have 18-bit or greater precision. These types of data acquisition systems capture data in bursts, and are also called burst-mode, data-acquisition systems. Achieving 18-bit precision for the first sample is very difficult using a conventional voltage reference because the voltage reference droop limits the accuracy of the first few conversions. Furthermore, variable-sampling-rate systems require that the gain error of the system does not vary with sampling rate. The primary objective of this design example is to demonstrate the lowest distortion and noise, burst-mode data-acquisition block with low power consumption, using an 18-bit SAR ADC operating at a throughput of 1 MSPS, for a 1-kHz, full-scale, pure sine-wave input.

### 10.2 Typical Application



**Figure 54. 18-bit, 1-MSPS, Burst-Mode Data Acquisition system**

#### 10.2.1 Design Requirements

1. Burst-mode support (see [Reference Droop Measurements](#) section for more details)
2. ENOB > 16 bits
3. THD < -120 dB
4. Power consumption < 50 mW
5. Throughput = 1 MSPS



## Typical Application (continued)

### 10.2.2 Detailed Design Procedure

The data acquisition system shown in [Figure 54](#) has three major contributors to the noise and accuracy in the system: the input driver, the reference with driver, and the data converter. Each analog block is carefully designed so that the data converter specifications limit the system specifications. The [THS4551](#), a fully differential operational amplifier is used to drive the 18-bit ADC ([ADS8881](#)). The charge-kickback RC filter at the output of the THS4551 is used to reduce the charge kickback created by the opening and closing of the sampling switch inside the ADC. Design the RC filter so that the voltage at the sampling capacitor settles to 18-bit accuracy within the acquisition time of the ADC.

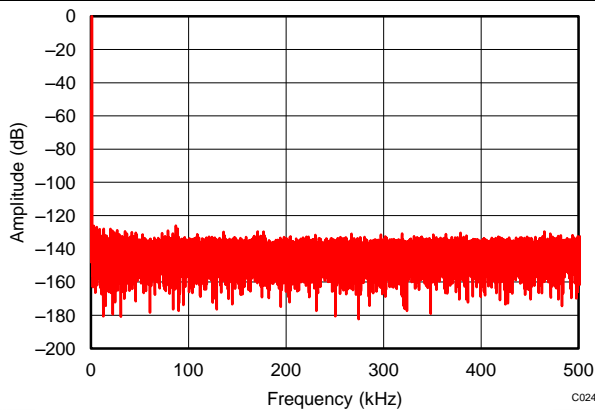
Data-acquisition systems require stable and accurate voltage references in order to perform the most accurate data conversion. The REF60xx family of voltage references have integrated an ADC drive buffer, and can therefore drive the REF pin of the ADS8881 directly, without the need for an external reference buffer. See the [Integrated ADC Drive Buffer](#) section for more details about reference-buffer requirements. Correct output capacitor selection for the REF60xx is very important in this design. The [Stability](#) section describes the ESR requirements of the output capacitor for stability and burst-mode requirements. A capacitance of 1  $\mu$ F is connected to the FILT pin to reduce broadband noise of the REF60xx.

#### 10.2.2.1 Results

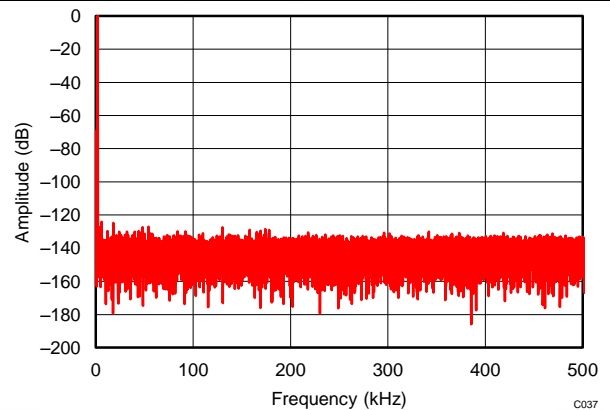
[Table 1](#) summarizes the measured results.

**Table 1. Measured Results**

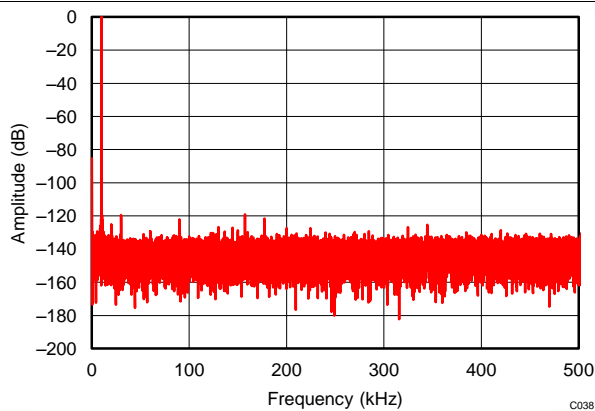
SPECIFICATION	MEASURED RESULT
SNR	100.5 dB
ENOB	16.4
THD	-125.9 dB
Throughput	1 MSPS
Burst mode	First sample > 18-bit precision
Power consumption	40 mW

**10.2.3 Application Curves**


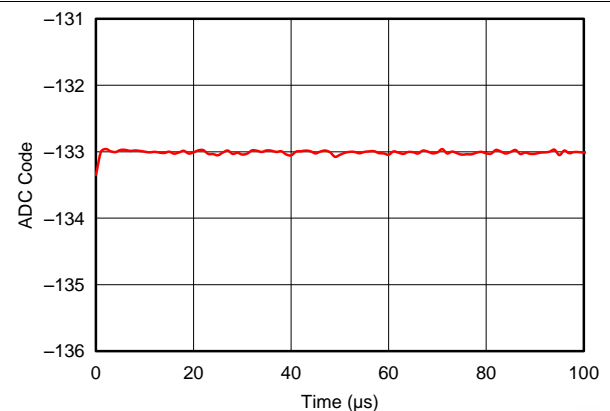
REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 1 \text{ kHz}$ , SNR = 100.5 dB, THD = -125.9 dB

**Figure 55. Typical FFT Plot**


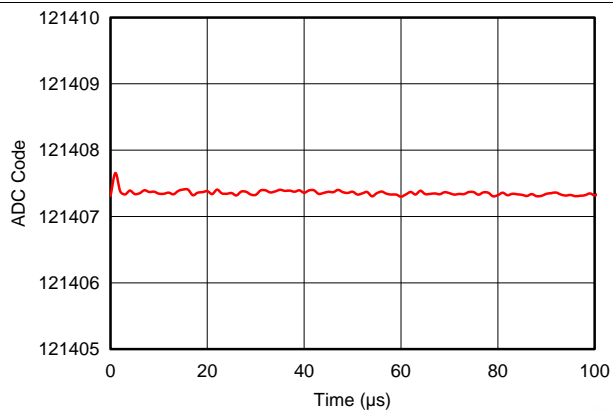
REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 2 \text{ kHz}$ , SNR = 100.4 dB, THD = -123.9 dB

**Figure 56. Typical FFT Plot**


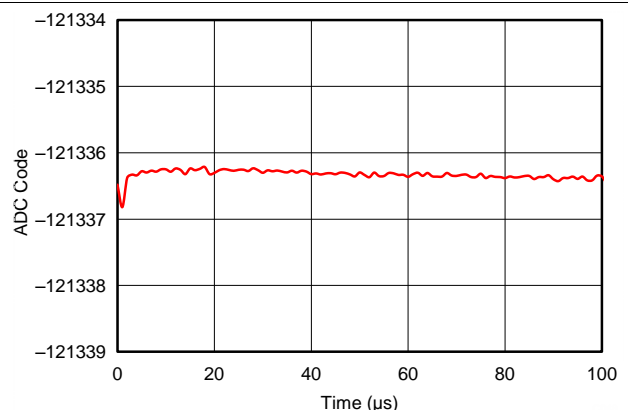
REF6050 driving REF pin of ADS8881,  
 $f_{IN} = 10 \text{ kHz}$ , SNR = 99.2 dB, THD = -119.4 dB

**Figure 57. Typical FFT Plot**


REF6050 driving REF pin of ADS8881 operating at 1 MSPS,  
 $A_{INP} = A_{INN} = V_{REF} / 2$  for ADS8881

**Figure 58. Reference Droop**


REF6050 driving REF pin of ADS8881 operating at 1 MSPS,  
 positive full-scale input to ADS8881

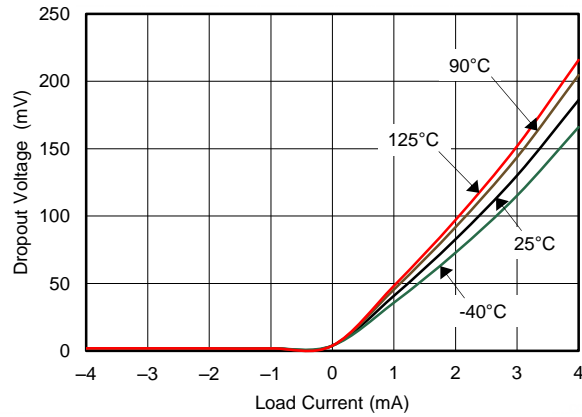
**Figure 59. Reference Droop**


REF6050 driving REF pin of ADS8881 operating at 1 MSPS,  
 negative full-scale input to ADS8881

**Figure 60. Reference Droop**

## 11 Power Supply Recommendations

The REF60xx family of references have extremely low dropout voltage. The dropout specifications can be found in the [Electrical Characteristics](#) section. A minimum 0.1  $\mu\text{F}$  decoupling capacitor must be connected between the VIN and GND\_F pins of the REF60xx. A typical dropout voltage versus load is shown in [Figure 61](#).



**Figure 61. Dropout Voltage vs Load Current**

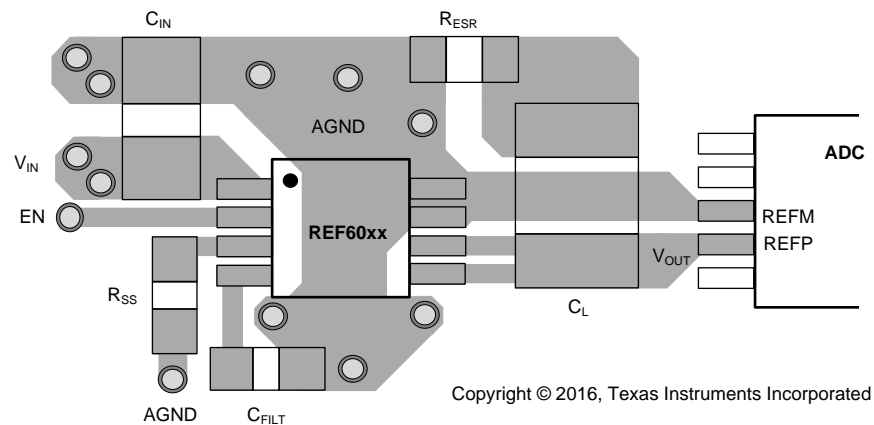
## 12 Layout

### 12.1 Layout Guidelines

Figure 62 illustrates an example of a PCB layout for a data-acquisition system using the REF60xx. Some key considerations are:

- Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between the VIN pin and ground.
- Place the REF60xx output capacitor ( $C_L$ ) and the ADC as close to each other as possible.
- Run two separate traces between VOUT\_F, VOUT\_S and the output capacitor, as shown in Figure 62.
- Short the GND\_F and GND\_S pins with a solid plane, and extend this plane to connect to the output capacitor  $C_L$ , as shown in Figure 62.
- Use a solid ground plane to help distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

### 12.2 Layout Example



**Figure 62. Layout Example**

## 13 器件和文档支持

### 13.1 文档支持

#### 13.1.1 相关文档

相关文档如下:

- 《[ADS8881x 18 位、1MSPS、串行接口、低功耗、微型、真正的差分输入、SAR 模数转换器数据表](#)》（文献编号: SBAS547）
- 《[ADS127L01 24 位、高速、高带宽模数转换器数据表](#)》（文献编号: SBAS607）
- 《[REF6025EVM-PDK 用户指南](#)》（文献编号: SBAU258）
- 《[电压基准对总谐波失真的影响](#)》（文献编号: SLYY097）

### 13.2 相关链接

下面的表格中列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
REF6025	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
REF6030	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
REF6033	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
REF6041	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
REF6045	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
REF6050	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 13.3 接收文档更新通知

如需接收文档更新通知，请访问 [www.ti.com.cn](http://www.ti.com.cn) 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

### 13.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 商标

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## 重要声明

德州仪器(TI)及其下属子公司有权根据 JESD46 最新标准,对所提供的产品和服务进行更正、修改、增强、改进或其它更改,并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息,并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内,且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定,否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险,客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息,不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可,或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分,仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时,如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分,则会失去相关 TI 组件或服务的所有明示或暗示授权,且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意,尽管任何应用相关信息或支持仍可能由 TI 提供,但他们将独立负责满足与其产品及其在应用中使用的 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意,他们具备制定与实施安全措施所需的全部专业技术和知识,可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中,为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此,此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备)的授权许可,除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意,对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用,其风险由客户单独承担,并且由客户独立负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品,这些产品主要用于汽车。在任何情况下,因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122  
Copyright © 2016, 德州仪器半导体技术(上海)有限公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF6025IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV	<a href="#">Samples</a>
REF6025IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV	<a href="#">Samples</a>
REF6030IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV	<a href="#">Samples</a>
REF6030IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV	<a href="#">Samples</a>
REF6033IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV	<a href="#">Samples</a>
REF6033IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV	<a href="#">Samples</a>
REF6041IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV	<a href="#">Samples</a>
REF6041IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV	<a href="#">Samples</a>
REF6045IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG	<a href="#">Samples</a>
REF6045IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG	<a href="#">Samples</a>
REF6050IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV	<a href="#">Samples</a>
REF6050IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.



- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF6025IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6025IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6030IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6030IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6033IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6033IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6045IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6045IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF6025IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6025IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6030IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6030IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6033IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6033IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6041IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6041IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6045IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6045IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6050IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6050IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0





- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明和免责声明

TI 均以“原样”提供技术性及其可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

Copyright © 2020 德州仪器半导体技术（上海）有限公司

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Voltage References](#) category:*

*Click to view products by [Texas Instruments](#) manufacturer:*

Other Similar products are found below :

[5962-8686103XC](#) [LT1021DCS8-5PBF](#) [LT1236AIS8-10PBF](#) [LTC6655CHMS8-2.048PBF](#) [MSB-T](#) [REF01J/883](#) [LM4040B25QFTA](#)  
[NJM2823F-TE1](#) [EL5226IR](#) [EL5326IR](#) [EL5326IRZ](#) [ISL21007DFB825Z](#) [ISL21009BFB812Z](#) [ISL21009CFB812Z](#) [ISL60002BIH312](#)  
[TS3320AMR](#) [TS3325AMR](#) [TS3330AMR](#) [TS3333AMR](#) [X60003CIG3-41](#) [X60003DIG3Z-41T1](#) [X60250V8I](#) [REF3025TB-GT3](#)  
[SC432BVSNT1G](#) [TL431CPG](#) [ADR4520ARZ-R7](#) [ADR4533BRZ-R7](#) [LT1027CCS8-5#TRPBF](#) [REF35102QDBVR](#) [AD587KRZ-REEL](#)  
[ADR425ARZ-REEL7](#) [CA-HP6025S](#) [CA-HP6041S](#) [JTL431A](#) [TLVH431NAQDBZRR](#) [REF2033QDDCRQ1](#) [REF35330QDBVR](#)  
[ADR4530BRZ-R7](#) [LT1236BCS8-5#TRPBF](#) [ADR435BRMZ-REEL7](#) [CA-HP6050S](#) [TL431](#) [BR431RM](#) [MSR025](#) [MC1403BN](#) [LM285Z-2.5](#)  
[LM385B-ADJ](#) [LM385B-2.5](#) [HT385R-1.2](#) [HT336R-2.5](#)