REF60xx 集成 ADC 驱动器缓冲器的高精度电压基准

1 特性

- 出色的温度漂移性能
  - -40℃ 至 +125°C 时为 5ppm/°C（最大值）
- 极低噪声
  - 总噪声：5 μV_{RMS}（使用 47µF 电容时）
  - 1/f 噪声（0.1Hz 至 10Hz）：3 μV_{PP}/V
- 集成 ADC 驱动器缓冲器
  - 低输出阻抗：< 50mΩ (0kHz-200kHz)
  - 首次使用 ADS8881 实现 18 位精确采样
  - 支持突发模式 DAQ 系统
- 低电源电流：820µA
- 低关断电流：1µA
- 高初始精度：±0.05%
- 超低噪声和失真
  - 信噪比 (SNR)：100.5dB，总谐波失真 (THD)：-125dB (ADS8881)
  - 信噪比 (SNR)：106dB，总谐波失真 (THD)：-120dB (ADS127L01)
- 输出电流驱动能力：±4mA
- 可通过编程设定的短路电流
- 经验证用于驱动 ADS88xx 系列逐次逼近寄存器 (SAR) ADC 和 ADS127xx 系列宽频带 Δ-Σ ADC 的 REF 引脚

2 应用

- 自动测试设备 (ATE) 测试器和示波器
- 测试和测量设备
- 可编程逻辑控制器 (PLC) 的模拟输入模块
- 医疗设备
- 精密数据采集系统

3 说明

REF6000 系列电压基准集成低输出阻抗缓冲器，这使得用户能够直接驱动精密数据转换器的 REF 引脚，同时维持线性度、失真和噪声性能。多数精密 SAR 和 Δ-Σ ADC 在转换过程中会将二进制加权电容切换到 REF 引脚。为了支持这一动态负载，必须通过一个低输出阻抗（高带宽）缓冲器缓冲电压基准的输出。REF6000 系列器件非常适合（但不限于）驱动 ADS88xx 系列 SAR ADC 和 ADS127xx 系列 Δ-Σ ADC 以及其他数模转换器 (DAC) 的 REF 引脚。

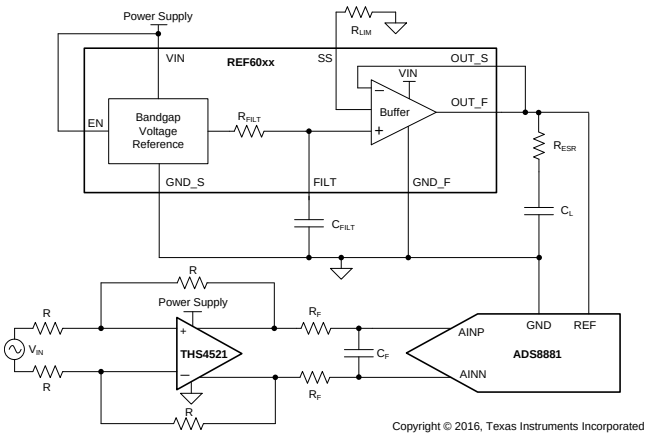
在驱动 ADS8881 的 REF 引脚时，即使在首次转换过程中，REF6000 系列电压基准的输出电压也不会降至 1 LSB（18 位）以下。该特性对于突发模式、事件触发的等时采样和可变采样率数据采集系统极为有用。REF6000 系列的 REF60xx 型号指定了最大温度漂移（仅为 5ppm/°C），可为电压基准与低输出阻抗缓冲器组合提供 0.05% 初始精度。关于 REF6000 系列中的多种温度漂移选项，请参见 *器件比较表*。

器件信息(1)

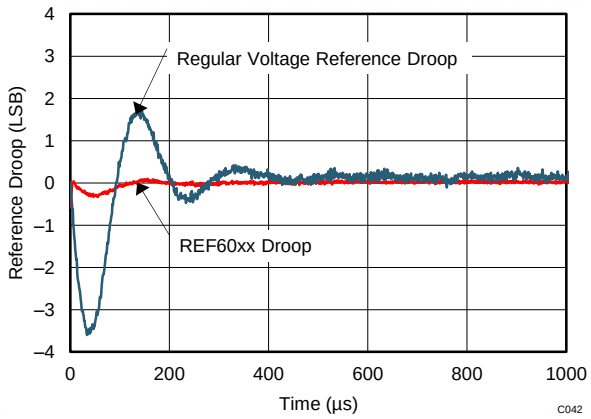
产品型号	封装	封装尺寸（标称值）
REF60xx	VSSOP (8)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

典型应用



基准压降比较
（1 LSB = 19.07µV，ADS8881 的速率为 1MSPS）



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4 修订历史记录

Changes from Revision A (June 2016) to Revision B **Page**

- 已更改 *说明* ... 1
- Changed the *Device Comparison Table* ... 3
- Changed list of devices for output current in Recommended Operating Conditions ... 4
- Changed load regulation max value for REF6050 at T_A = –40°C to +125°C from 30 to 50 ... 5
- Changed "second pass" to "final pass" in last paragraph of *Solder Heat Shift* section ... 14
- Added link to SLYY097 in *Overview* section ... 19

Changes from Original (May 2016) to Revision A **Page**

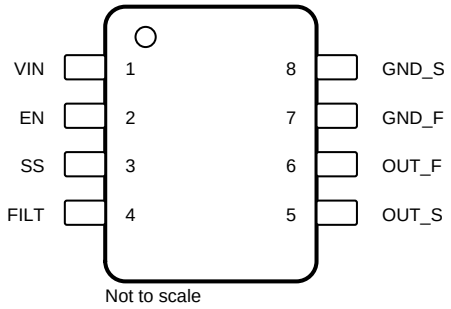
- 已由“产品预览”更改为“量产数据” ... 1

5 Device Comparison Table

DEVICE FAMILY	TEMPERATURE DRIFT
REF60xx	5 ppm/°C from –40 to 125°C
REF61xx	8 ppm/°C from –40 to 125°C
REF62xx	3 ppm/°C from 0 to 70°C

6 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	2	Input	Enable pin
FILT	4	—	Filter capacitor pin. A capacitor (C_{FILT}) ≥ 1 µF must be connected between the FILT pin and ground for stability.
GND_F	7	Ground	Ground force pin
GND_S	8	Ground	Ground sense pin
OUT_F	6	Output	Output voltage force pin
OUT_S	5	Input	Output voltage sense pin
SS	3	—	Short circuit current limit pin. Connect a resistor to this pin to set the output short-circuit current limit. Connect to VIN pin for highest current limit
VIN	1	Power	Input supply voltage pin

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	6	V
	V_{EN}	–0.3	V_{IN} + 0.3	V
Operating temperature, T_A		–55	150	°C
Junction temperature, T_j			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage (I_{OUT} = 0 mA)	REF6025	3		5.5	V
		REF6030, REF6033, REF6041, REF6045	V_{OUT} + 0.25		5.5	
		REF6050	5.3		5.5	
V_{EN}	Enable voltage		0		V_{IN}	V
I_L	Output current	REF6025, REF6030, REF6033, REF6041	–4		4	mA
		REF6045	–3.5		3.5	
		REF6050	–3		3	
T_A	Operating temperature		–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		REF60xx DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_{IN} = 5 V for all devices except REF6050, V_{IN} = 5.4 V for REF6050, I_L = 0 mA, C_L = 22 µF, C_{FILT} = 1 µF, and V_{EN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT								
	Output voltage accuracy				-0.05%		0.05%	
	Output voltage temperature coefficient(1)						5	ppm/°C
LINE AND LOAD REGULATION								
$\Delta V_{O(\Delta VI)}$	Line regulation	REF6025	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V	T_A = 25°C		4	20	ppm/V
				T_A = –40°C to +125°C			30	
		REF6030, REF6033, REF6041, REF6045	V_{OUT} + 0.25 V ≤ V_{IN} ≤ 5.5 V	T_A = 25°C		4	20	
				T_A = –40°C to +125°C			30	
		REF6050	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 5.5 V	T_A = 25°C		7	60	
				T_A = –40°C to +125°C			120	
$\Delta V_{O(\Delta IL)}$	Load regulation, sourcing and sinking	REF6025, REF6030, REF6033, REF6041	I_L = 0 mA to 4 mA, V_{IN} = V_{OUT} + 600 mV	T_A = 25°C		2	20	ppm/mA
				T_A = –40°C to +125°C			30	
		REF6045	I_L = 0 mA to 3.5 mA, V_{IN} = V_{OUT} + 600 mV	T_A = 25°C		2	20	
				T_A = –40°C to +125°C			30	
		REF6050	I_L = 0 mA to 3 mA, V_{IN} = V_{OUT} + 400 mV	T_A = 25°C		2	20	
				T_A = –40°C to +125°C			50	
I_{SC}	Short-circuit current	SS = open				10.5		mA
NOISE								
	Total integrated noise	C_L = 22 µF				5		μV_{RMS}
		C_L = 47 µF				5		
	Low frequency noise	0.1 Hz ≤ f ≤ 10 Hz				3		μV_{PP}/V
OUTPUT IMPEDANCE								
	Output impedance	f = DC to 200 kHz, C_L= 47 µF				50		mΩ
TURN-ON TIME								
t_{on}	Turn-on time	0.1% settling, C_L = 47 µF, SS = open, REF6025				100		ms
HYSTERESIS AND LONG TERM DRIFT								
	Long term stability	0 to 1000h at 25°C				80		ppm
		1000h to 2000h at 25°C				20		
	Output voltage hysteresis(2)	25°C, –40°C,125°C, 25°C (cycle 1)				33		ppm
		25°C, –40°C,125°C, 25°C (cycle 2)				8		
CAPACITIVE LOAD								
C_L	Stable output capacitor value				10		47	µF

(1) Temperature drift is specified according to the box method. See the Feature Description section for more details.
(2) See the *Thermal Hysteresis* section.

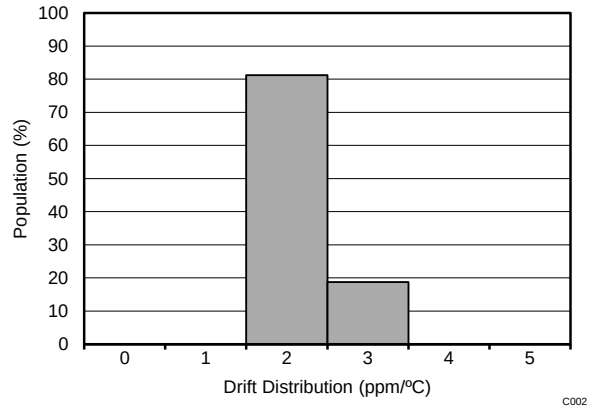
Electrical Characteristics (continued)

at T_A = 25°C, V_{IN} = 5 V for all devices except REF6050, V_{IN} = 5.4 V for REF6050, I_L = 0 mA, C_L = 22 µF, C_{FILT} = 1 µF, and V_{EN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE								
V_{OUT}	Output voltage	REF6025				2.5		V
		REF6030				3		
		REF6033				3.3		
		REF6041				4.096		
		REF6045				4.5		
		REF6050				5		
POWER SUPPLY								
I_{CC}	Supply current	REF6025, REF6030, REF6033, REF6041	Active mode, V_{EN} = 5 V	T_A = 25°C		0.82	0.90	mA
				T_A = –40°C to +125°C			1.1	
		REF6045, REF6050	Active mode, V_{EN} = 5 V	T_A = 25°C		0.83	0.95	
				T_A = –40°C to +125°C			1.15	
		Shutdown mode, V_{EN} = 0 V		T_A = 25°C		1	3	µA
				T_A = –40°C to +125°C			15	
	Enable pin voltage	Voltage reference in active mode (EN = 1)			1.6			V
		Voltage reference in shutdown mode (EN = 0)					0.6	
	Enable pin current	V_{EN} = 5 V				100	150	nA
	Dropout voltage	REF6025		I_L = 0 mA		500	500	mV
				I_L = 4 mA			600	
		REF6030, REF6033, REF6041		I_L = 0 mA		50	250	
				I_L = 4 mA			600	
		REF6045		I_L = 0 mA		50	250	
				I_L = 3.5 mA			600	
		REF6050		I_L = 0 mA		100	300	
				I_L = 3 mA			400	

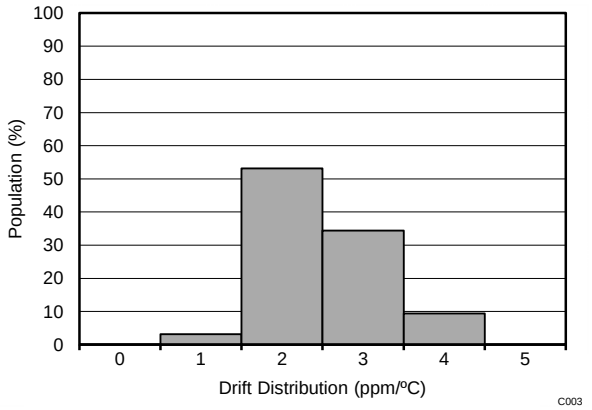
7.6 Typical Characteristics

at T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, using REF6025 (unless otherwise noted)



T_A = –40°C to +125°C

Figure 1. Drift Distribution



T_A = –40°C to +85°C

Figure 2. Drift Distribution

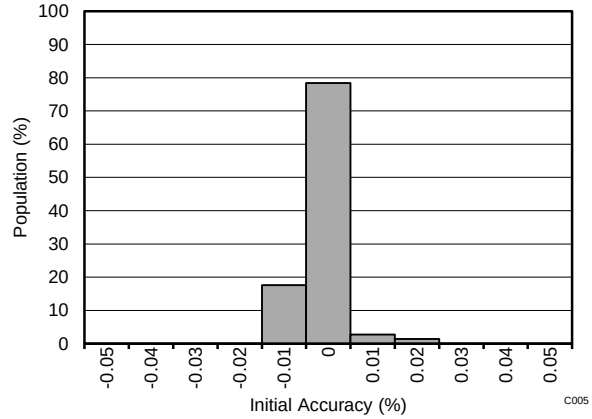


Figure 3. Initial Accuracy Distribution

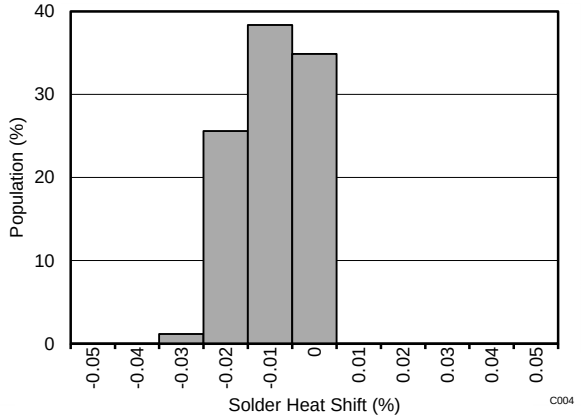


Figure 4. Solder-Heat Shift Distribution

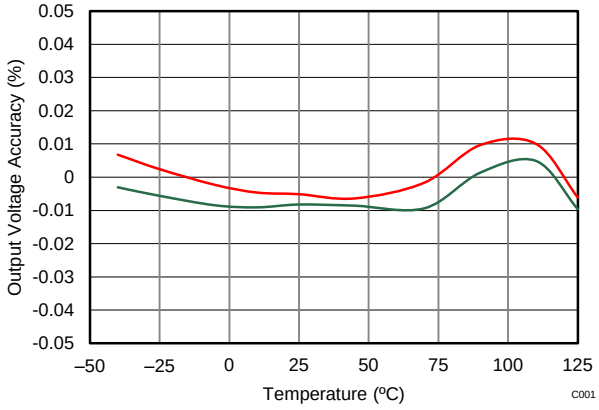


Figure 5. Output Voltage Accuracy vs Temperature

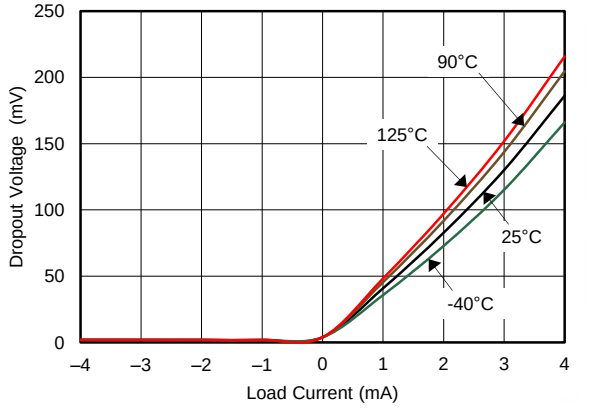
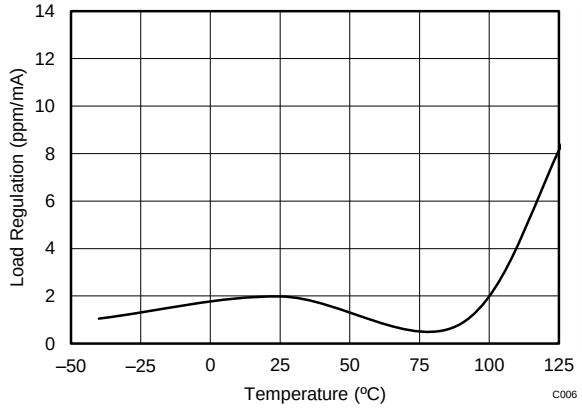


Figure 6. Dropout Voltage vs Load Current

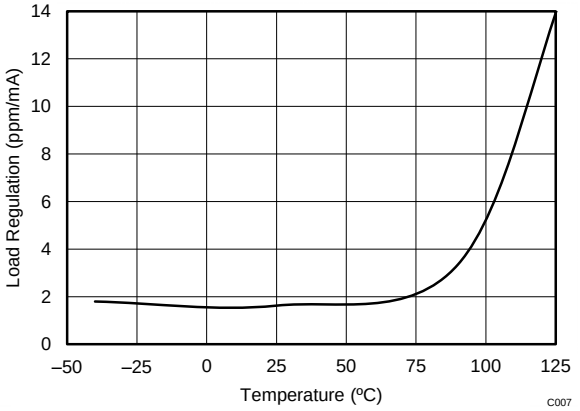
Typical Characteristics (continued)

at T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, using REF6025 (unless otherwise noted)



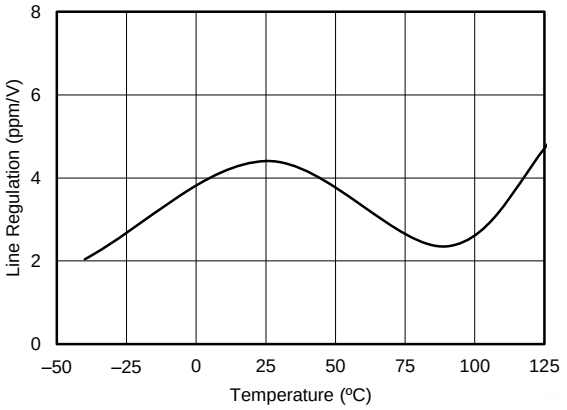
$V_{IN} = V_{OUT}$ + 600 mV,
I_L = 0 mA to 4 mA

Figure 7. Load Regulation Sourcing vs Temperature



$V_{IN} = V_{OUT}$ + 600 mV,
I_L = 0 mA to 4 mA

Figure 8. Load Regulation Sinking vs Temperature



V_{OUT} + 0.25 V ≤ V_{IN} ≤ 5.5 V

Figure 9. Line Regulation vs Temperature

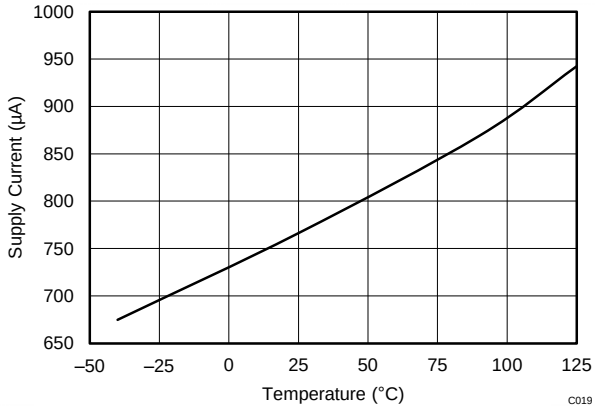


Figure 10. Supply Current vs Temperature

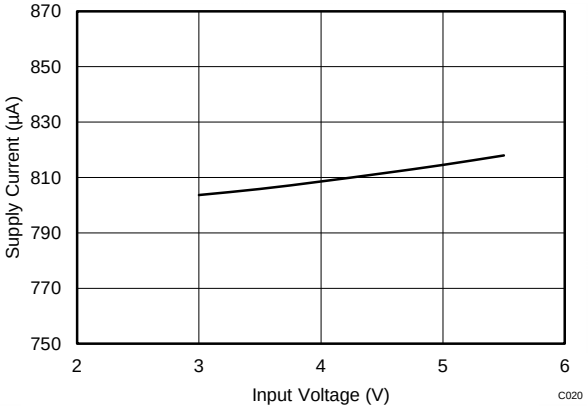


Figure 11. Supply Current vs Input Voltage

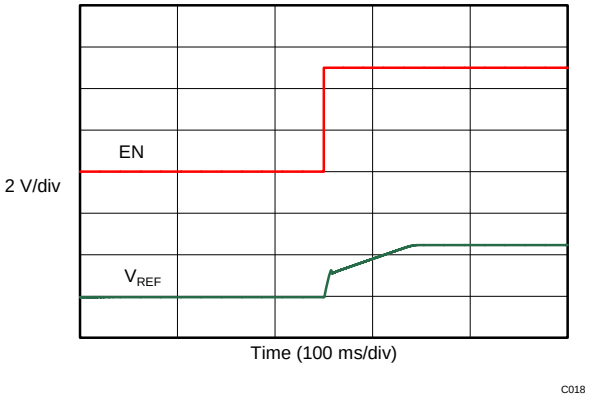


Figure 12. Turn-On Settling Time

Typical Characteristics (continued)

at T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, using REF6025 (unless otherwise noted)

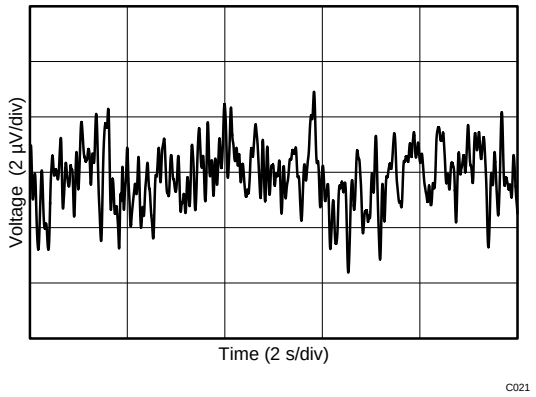


Figure 13. 0.1-Hz to 10-Hz Noise

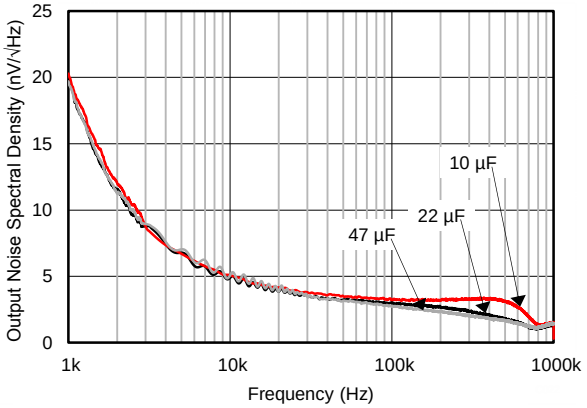


Figure 14. Output-Voltage Noise Spectrum

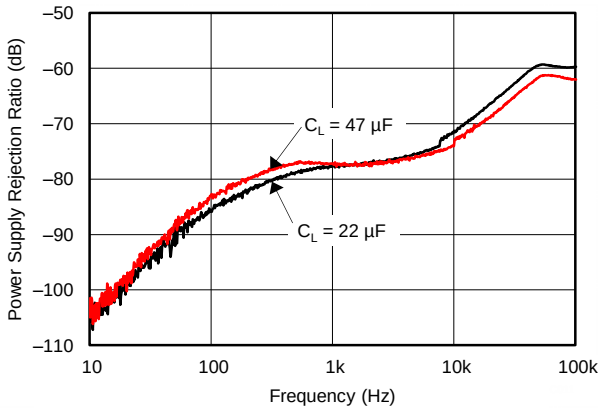
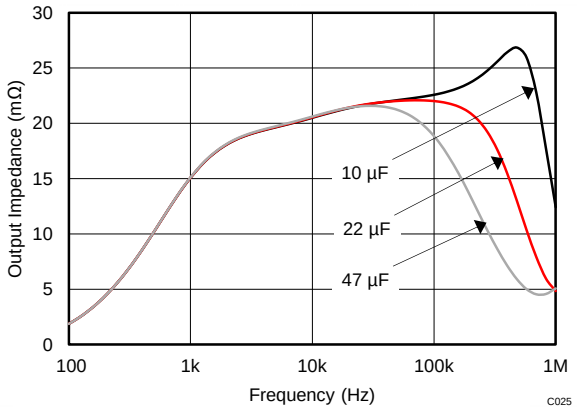
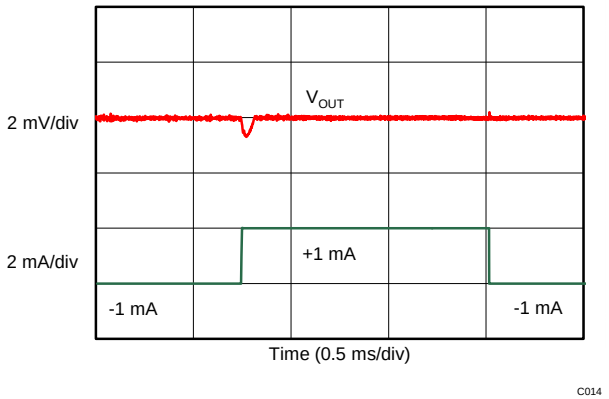


Figure 15. PSRR vs Frequency



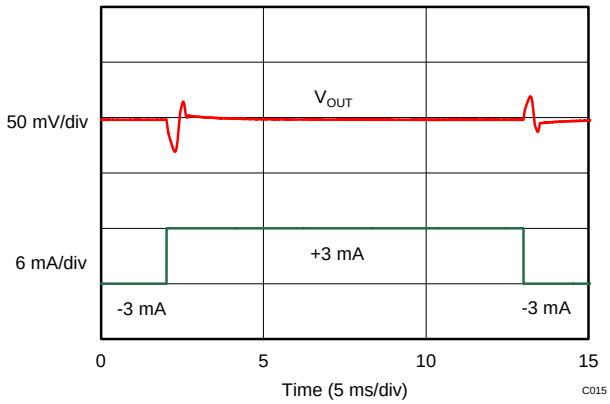
Graph obtained by design simulation

Figure 16. Output Impedance vs Frequency



Load current = ±1 mA

Figure 17. Load Transient Response



Load current = ±3 mA

Figure 18. Load Transient Response

Typical Characteristics (continued)

at T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, using REF6025 (unless otherwise noted)

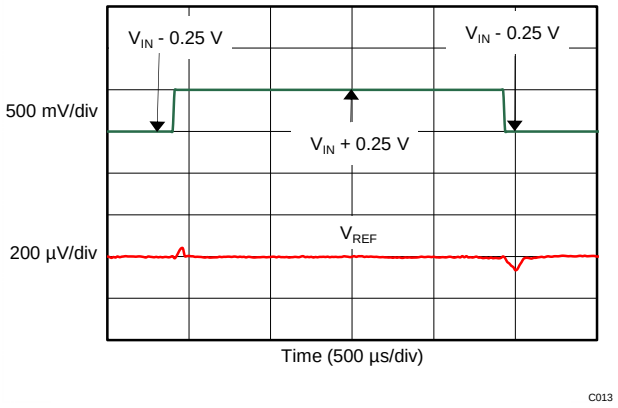


Figure 19. Line Transient Response

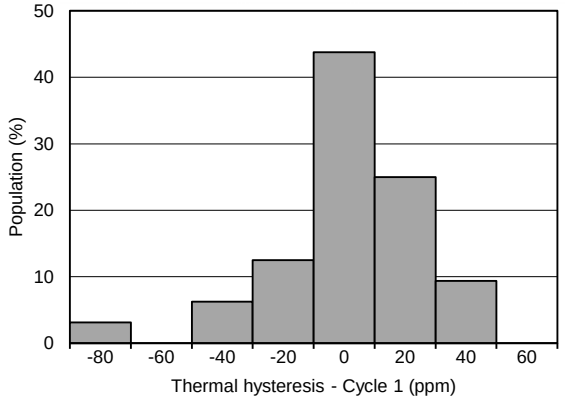


Figure 20. Thermal Hysteresis Distribution (Cycle 1)

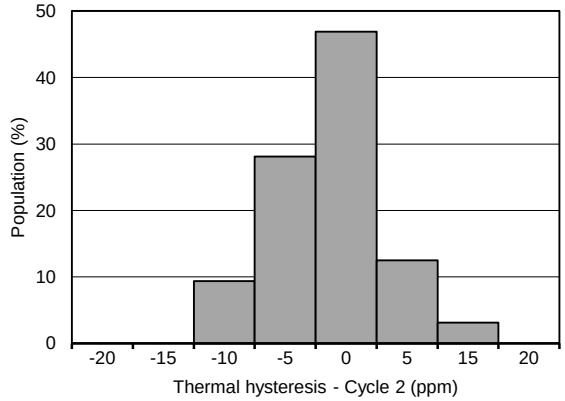


Figure 21. Thermal Hysteresis Distribution (Cycle 2)

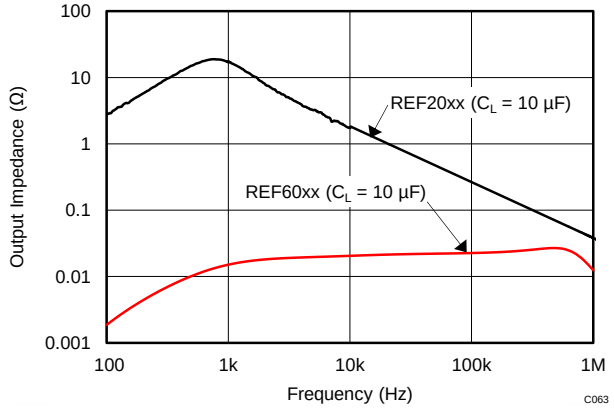
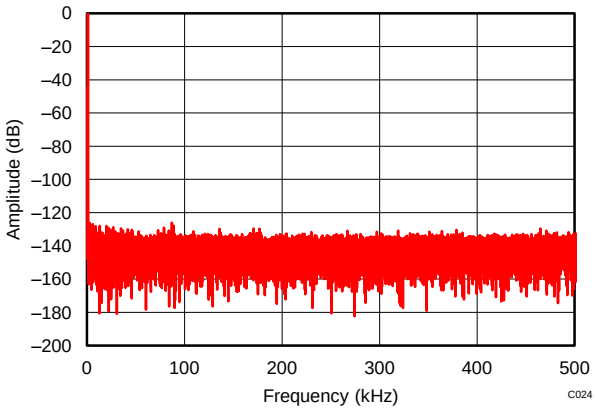
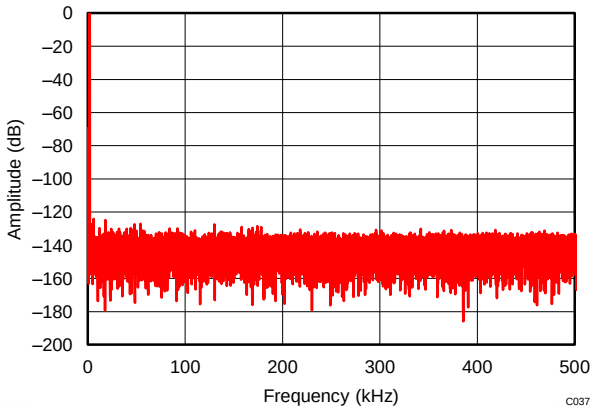


Figure 22. Output Impedance Comparison



REF6050 driving REF pin of ADS8881,
f_{IN} = 1 kHz, SNR = 100.5 dB, THD = –125.9 dB

Figure 23. Typical FFT Plot

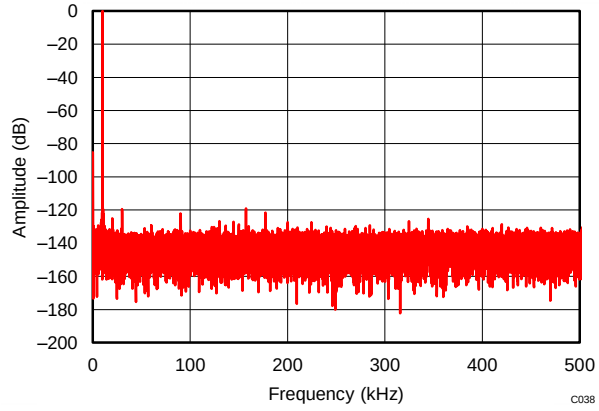


REF6050 driving REF pin of ADS8881,
f_{IN} = 2 kHz, SNR = 100.4 dB, THD = –123.9 dB

Figure 24. Typical FFT Plot

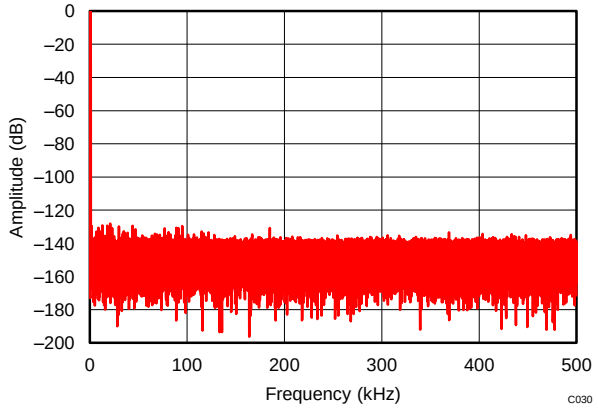
Typical Characteristics (continued)

at T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, using REF6025 (unless otherwise noted)



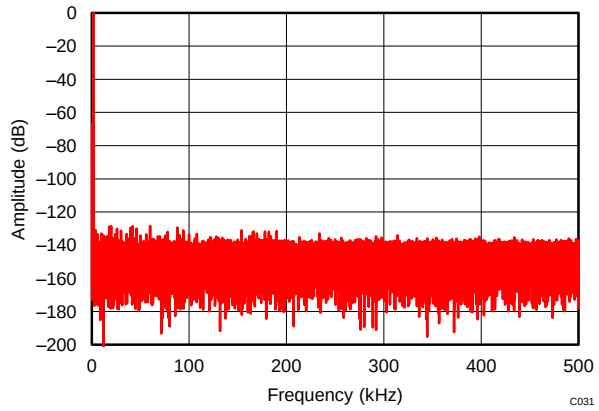
REF6050 driving REF pin of ADS8881,
f_{IN} = 10 kHz, SNR = 99.2 dB, THD = –119.4 dB

Figure 25. Typical FFT Plot



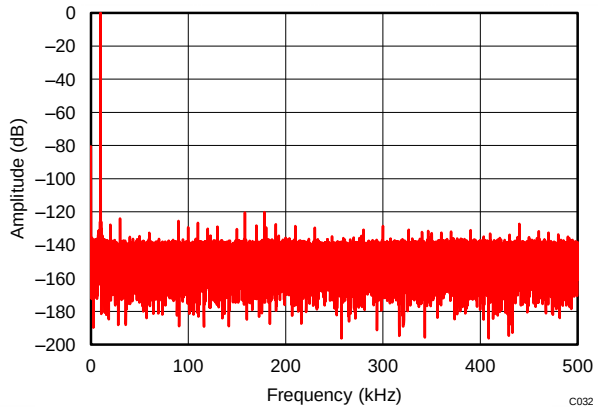
REF6041 driving REF pin of ADS8881,
f_{IN} = 1 kHz, SNR = 99 dB, THD = –124.4 dB

Figure 26. Typical FFT Plot



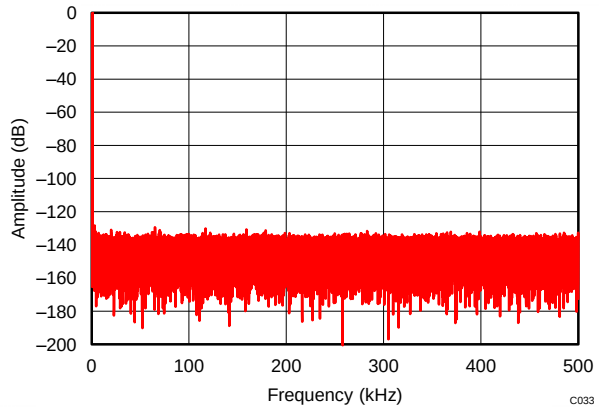
REF6041 driving REF pin of ADS8881,
f_{IN} = 2 kHz, SNR = 99 dB, THD = –123.6 dB

Figure 27. Typical FFT Plot



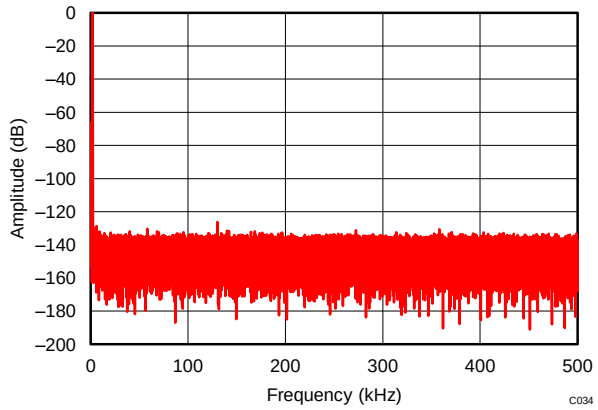
REF6041 driving REF pin of ADS8881,
f_{IN} = 10 kHz, SNR = 97.2 dB, THD = –119.7 dB

Figure 28. Typical FFT Plot



REF6025 driving REF pin of ADS8881,
f_{IN} = 1 kHz, SNR = 95.4 dB, THD = –124 dB

Figure 29. Typical FFT Plot

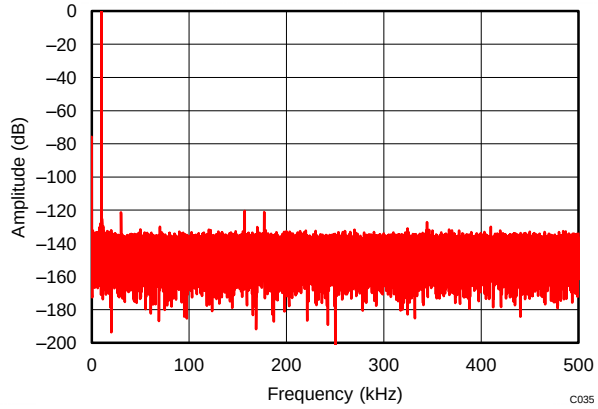


REF6025 driving REF pin of ADS8881,
f_{IN} = 2 kHz, SNR = 95.4 dB, THD = –123.5 dB

Figure 30. Typical FFT Plot

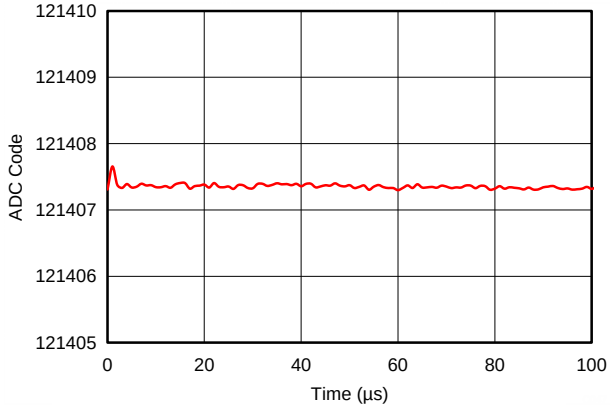
Typical Characteristics (continued)

at T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, using REF6025 (unless otherwise noted)



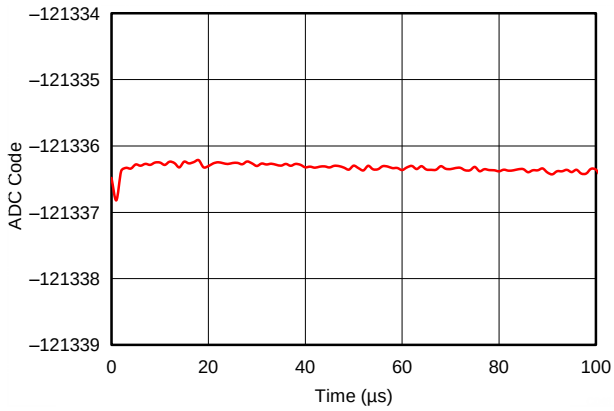
REF6025 driving REF pin of ADS8881,
f_{IN} = 10 kHz, SNR = 94.0 dB, THD = –119.3 dB

Figure 31. Typical FFT Plot



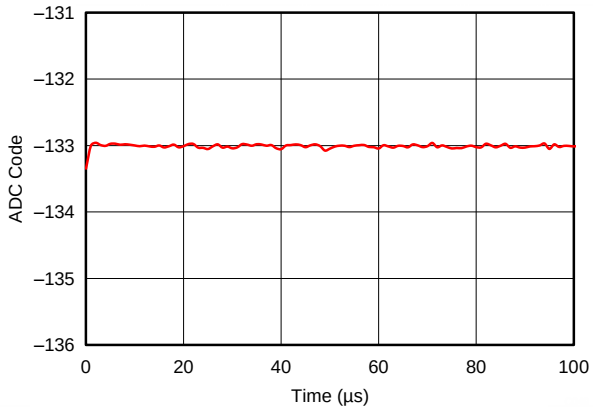
REF6050 driving REF pin of ADS8881 operating at 1 MSPS,
positive full-scale input to ADS8881

Figure 32. Reference Droop



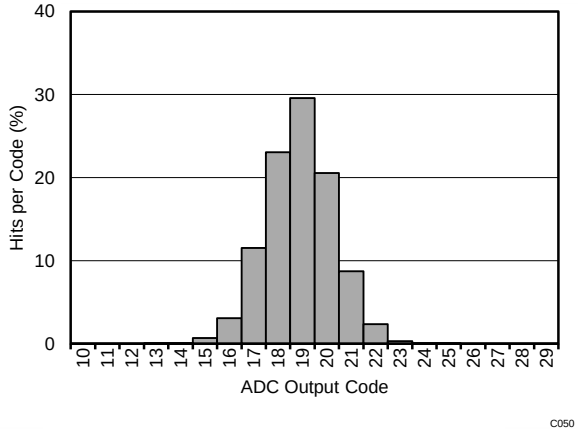
REF6050 driving REF pin of ADS8881 operating at 1 MSPS,
negative full-scale input to ADS8881

Figure 33. Reference Droop



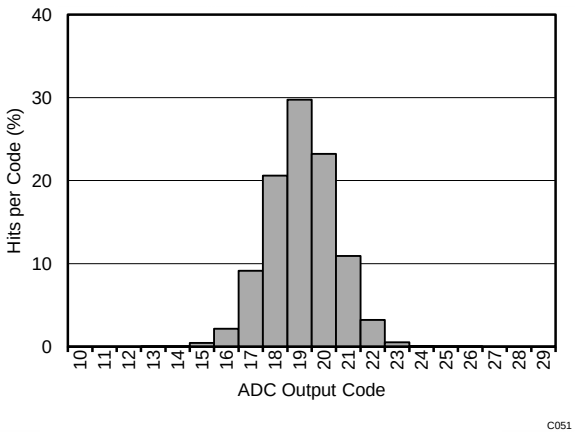
REF6050 driving REF pin of ADS8881 operating at 1 MSPS,
AINP = AINN = V_{REF} / 2 for ADS8881

Figure 34. Reference Droop



AINP = AINN = V_{REF} / 2 for ADS8881,
sampling rate = 1 MSPS

Figure 35. DC Input Histogram

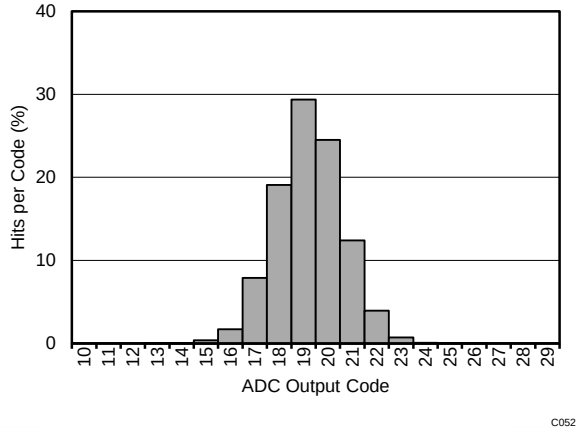


AINP = AINN = V_{REF} / 2 for ADS8881,
sampling rate = 500 kSPS

Figure 36. DC Input Histogram

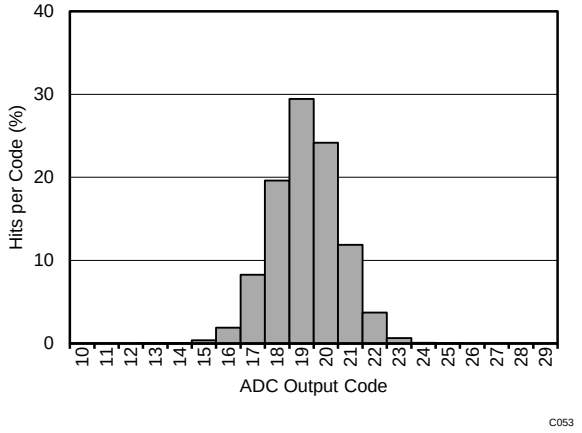
Typical Characteristics (continued)

at T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, using REF6025 (unless otherwise noted)



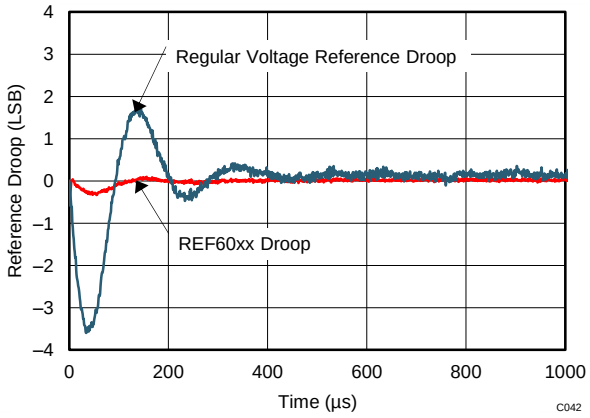
AINP = AINN = V_{REF} / 2 for ADS8881,
sampling rate = 100 kSPS

Figure 37. DC Input Histogram



AINP = AINN = V_{REF} / 2 for ADS8881,
sampling rate = 20 kSPS

Figure 38. DC Input Histogram



1 LSB = 19.07 µV, with ADS8881 at 1 MSPS

Figure 39. Reference Droop Comparison

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF60xx have differing coefficients of thermal expansion, and result in stress on the device die when the part is heated. Mechanical and thermal stress on the device die sometimes causes the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 128 devices were soldered on eight printed circuit boards (PCBs), with 16 devices on each PCB, using lead-free solder paste, and the manufacturer-suggested reflow profile. The reflow profile is as shown in Figure 40. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 101.6 mm × 127 mm.

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in Figure 41. Although all tested units exhibit very low shifts (< 0.03%), higher shifts are also possible depending on the size, thickness, and material of the PCB.

The histogram displays the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, solder the device in the final pass to minimize exposure to thermal stress.

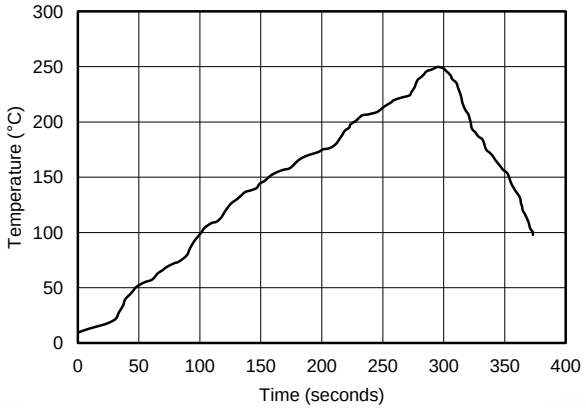


Figure 40. Reflow Profile

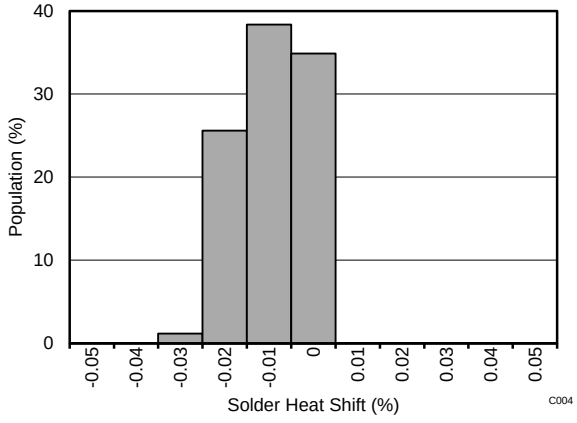


Figure 41. Solder Heat Shift Distribution

8.2 Thermal Hysteresis

Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Thermal hysteresis was measured with the REF60xx soldered to a PCB, similar to a real-world application. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Thermal hysteresis is expressed as:

$$V_{HYST} = \left(\frac{\left| V_{PRE} - V_{POST} \right|}{V_{NOM}} \right) \bullet 10^{6} \quad (ppm) \tag{1}$$

where

- V_{HYST} = thermal hysteresis (in units of ppm).
- V_{NOM} = the specified output voltage.
- V_{PRE} = output voltage measured at 25°C pretemperature cycling.
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C.

Typical thermal hysteresis distribution is shown in Figure 42 and Figure 43.

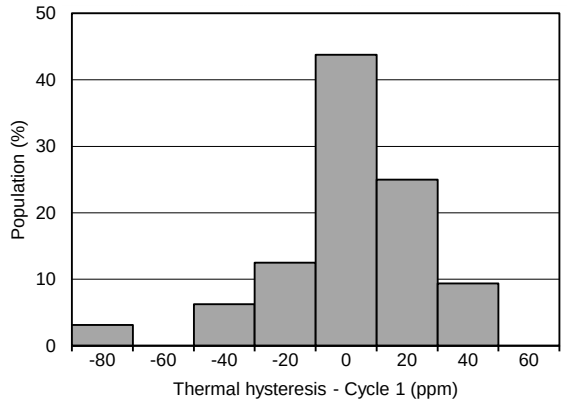


Figure 42. Thermal Hysteresis Distribution (Cycle 1)

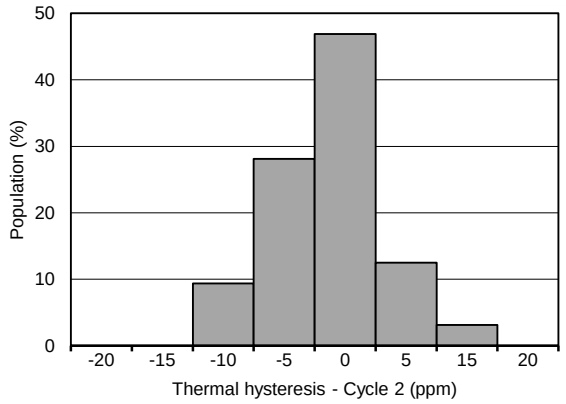
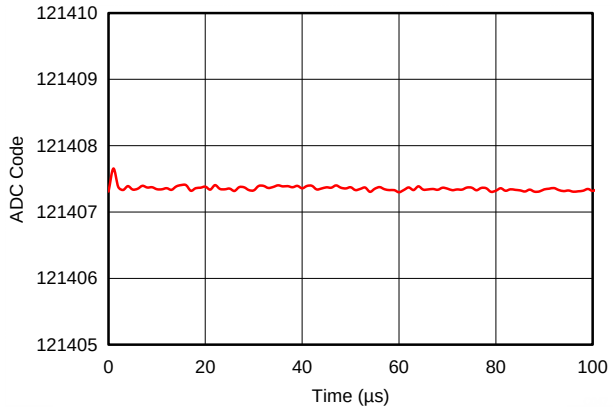


Figure 43. Thermal Hysteresis Distribution (Cycle 2)

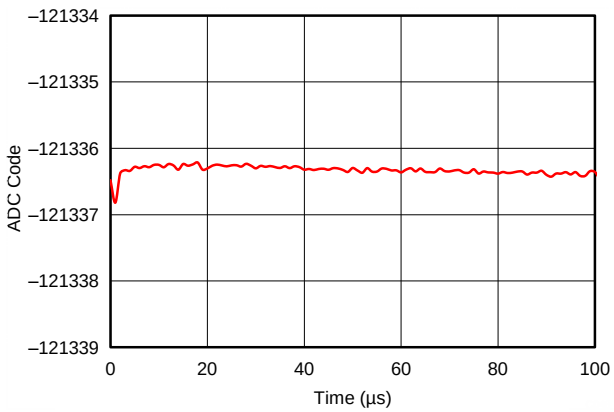
8.3 Reference Droop Measurements

Many applications, such as event-triggered and multiplexed data-acquisition systems, require the very first conversion of the ADC to have 18-bit or greater precision. These types of data-acquisition systems capture data in bursts, and are also called burst-mode, data-acquisition systems. Achieving 18-bit precision for the first sample is a very difficult using a conventional voltage reference because the voltage reference droop limits the accuracy of the first few conversions. The REF60xx have an integrated ADC drive buffer that makes sure the reference droop is less than 1 LSB at 18-bit precision when used with the ADS8881, even at full throughput. Figure 44 and Figure 45 show the REF60xx output voltage droop when driving the REF pin of the ADS8881 at positive and negative full-scale inputs, respectively.



REF6050 driving REF pin of ADS8881 operating at 1 MSPS, positive full-scale input to ADS8881

Figure 44. Output Voltage Droop



REF6050 driving REF pin of ADS8881 operating at 1 MSPS, negative full-scale input to ADS8881

Figure 45. Output Voltage Droop

Direct measurement of the reference droop to 18-bit accuracy can be a challenging process. Therefore, the plots in Figure 44 and Figure 45 were obtained by processing the output code of the ADC. The ADC output code is given by:

$$C = (\text{Input Voltage} / V_{REF}) \times 2^N \quad (2)$$

If the input voltage is kept constant, V_{REF} is computed by monitoring the ADC output code C. The ADC code usually has six to seven LSBs of code spread due to the inherent noise of the ADC. In order to measure reference droop, this noise must be reduced drastically. Noise reduction is done by averaging the output code multiple times, as described in the next paragraph.

Reference Droop Measurements (continued)

Figure 46 shows the setup that was used to measure the reference droop. The output ADC code was captured using a field-programmable gate array (FPGA), and post-processing was done on a personal computer. The input to the THS4521, and hence in turn to the ADS8881, is a constant dc voltage (close to positive or negative full-scale because this condition is the worst-case for charge drawn from the REF pin). The dc source must have extremely low noise. After the REF60xx device is powered up and stable, the FPGA sends commands to the ADS8881 to capture data in bursts. The ADS8881 is initially in idle mode for 100 ms. The FPGA then sends a command to the ADS8881 to perform 100 conversions at 1 MSPS. The ADC code corresponding to these 100 conversions (one burst of data) is stored as the first row in a 1000 × 100 dimensional array. This operation is repeated 1000 times, and the data corresponding to each burst is stored in a new row of the 1000 × 100 dimensional array. Finally, each column in this array is averaged to get a final data-set of 100 elements. This final data-set now has code spread that is much less than 1 LSB because most of the noise has now been removed through averaging. This data-set was plotted on a graph with X axis = column number (each column number corresponds to 1 µs of time because the sampling rate is 1 MSPS), and Y axis = ADC output code to obtain reference-droop measurements.

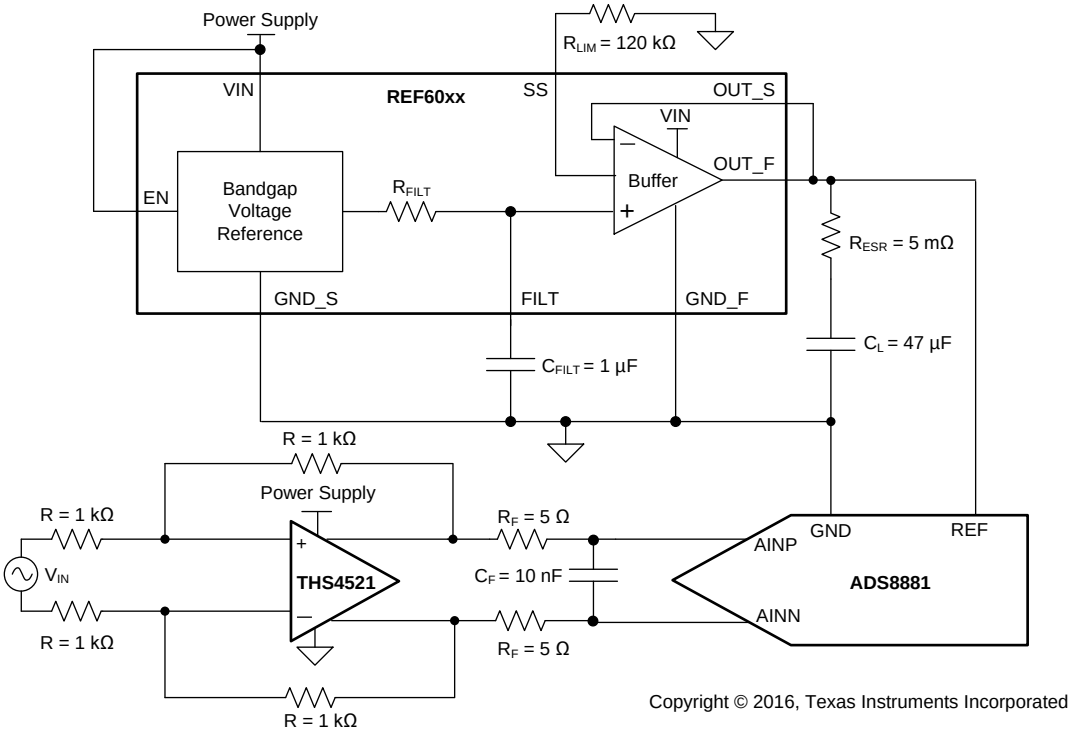


Figure 46. Burst-Mode Measurement Setup

8.4 1/f Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise for the REF6025 is shown in Figure 47. The 1/f noise scales with output voltage, but remains 3 $\mu V_{PP}/V$ for all the variants. Peak-to-peak noise measurement setup is shown in Figure 48.

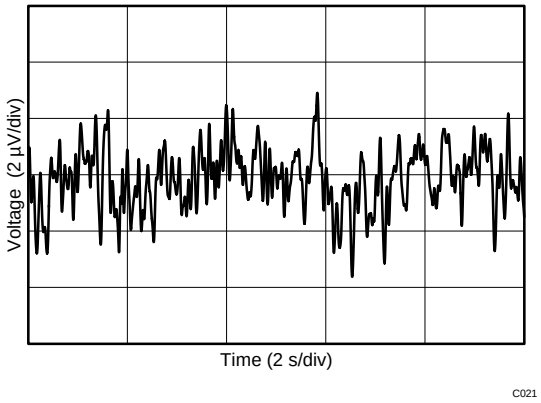


Figure 47. 0.1-Hz to 10-Hz Noise

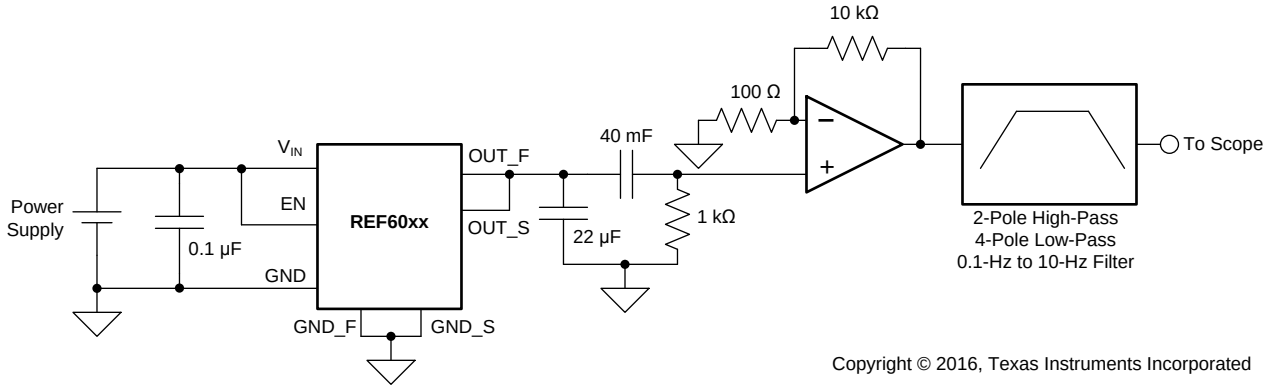


Figure 48. 0.1-Hz to 10-Hz Noise Measurement Setup

9 Detailed Description

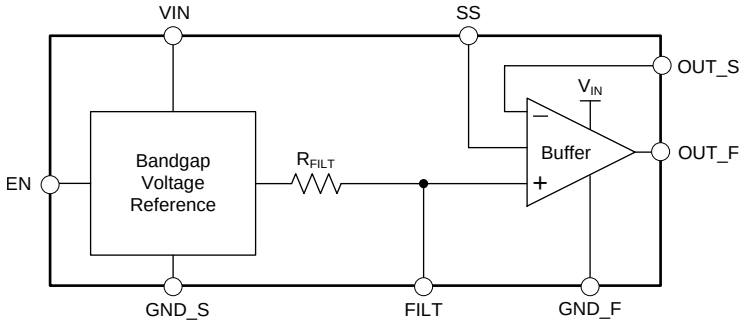
9.1 Overview

Most SAR ADCs, and a few delta-sigma ADCs, switch binary-weighted capacitors onto the REF pin during the conversion process. The magnitude of the capacitance switched onto the REF pin during each conversion depends on the input signal to the ADC. If a voltage reference is directly connected to the REF pin of these ADCs, the reference voltage droops because of the dynamic input signal dependent load of the binary-weighted capacitors. Because the reference voltage droop now has input signal dependance, significant degradation in THD and linearity for the system occurs.

In order to support this dynamic load and preserve the ADC linearity, distortion and noise performance, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF60xx family of voltage references have an integrated low output impedance buffer that enables the user to directly drive the REF pin of a SAR ADC, while preserving ADC linearity and distortion. In addition, the total noise in the full bandwidth of the REF60xx is extremely low, thus preserving the noise performance of the ADC. *Voltage-Reference Impact on Total Harmonic Distortion* (SLYY097) correlates the effect of reference settling to ADC distortion, and how the REF60xx achieves lowest distortion with minimal components and lowest power consumption.

The output voltage of the REF60xx does not droop below 1 LSB (18-bit), even during the first conversion while driving the REF pin of the ADS8881. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems. *Functional Block Diagram* shows a simplified schematic of the REF60xx.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Integrated ADC Drive Buffer

Many ADC data sheets specify a few microamps of average current draw from the REF pin. Almost all voltage references provide these few microamps of average current; but not all voltage references are practical for driving a high-resolution, high-throughput SAR ADC because the peak current drawn can be very high when the capacitors are switched on the REF pin. The worst-case demand for the voltage reference is during a burst-mode conversion, when the ADC is idle for a very long time, before a conversion is initiated, and the first sample converted is expected to be precise. Usually, a large capacitor is connected between the REF pin and ground pin (or sometimes between the REFP and REFM pins) of the ADC to smoothen the current load and reduce the burden on the voltage reference. The voltage reference must then be capable of providing the average current required to completely charge the reference capacitor, but without causing the reference voltage to droop significantly. Most voltage references lack the ability to completely charge the reference capacitor, and settle when the binary-weighted capacitors are being switched onto the REF pin because of the large output impedance. Usually, voltage references have output impedances in the range of 10's of ohms at frequencies higher than 100 Hz. The output voltage of the voltage reference must be buffered with a low output impedance (usually high bandwidth) amplifier to achieve excellent linearity and distortion performance.

The key amplifier specifications to be considered when designing a reference buffer for a high-precision ADC are: low offset, low drift, wide bandwidth, and low output impedance. While it is possible to select an amplifier that sufficiently meets all these requirements, the amplifier comes at a cost of excessive power consumption. For example, the OPA350 is a 38-MHz bandwidth amplifier with a maximum offset of 0.5 mV, and low offset drift of 4 µV/ºC, but consumes a quiescent current of 5.2mA. This is because (from an amplifier design perspective) offset and drift are dc specifications, whereas bandwidth, low output impedance, and high capacitive drive capability are high-frequency specifications. Therefore, achieving all the performance in one amplifier requires power. However, a more efficient design to meet the low power budget is to use a composite reference buffer, which uses an amplifier with superior high-frequency specifications in the feedback loop of a dc precision amplifier to get the overall performance at much lower power consumption. Figure 49 shows such a composite amplifier design with the OPA333 (dc precision amplifier) and THS4281 (high-bandwidth amplifier). This reference buffer design requires three devices, and a large number of external components. This solution still consumes close to 2 mA of quiescent current.

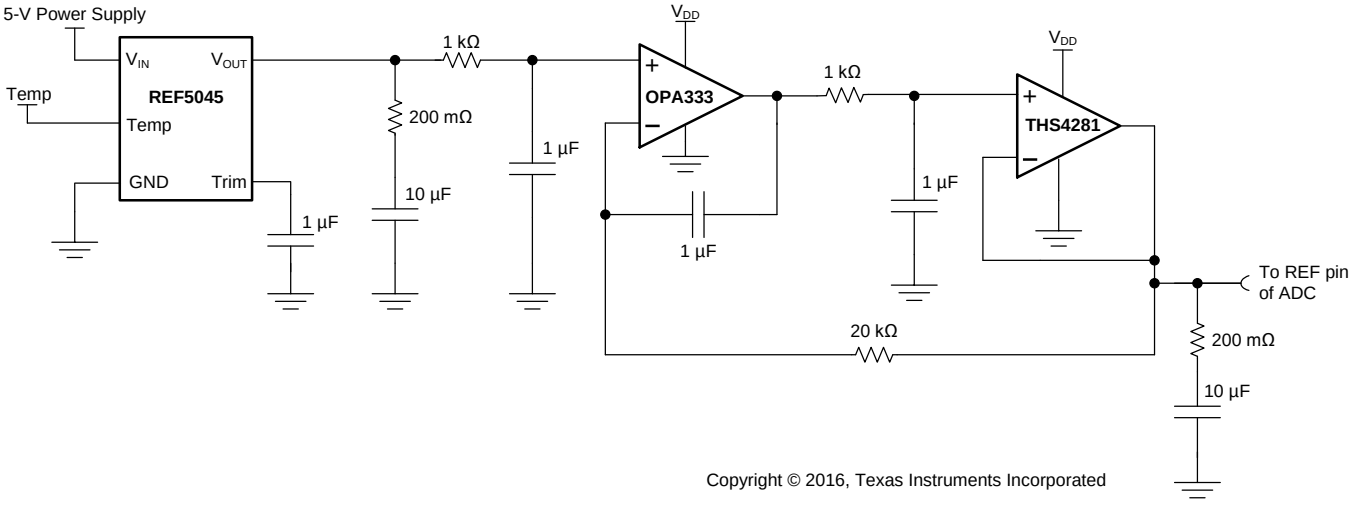


Figure 49. Composite Amplifier Reference Buffer

Feature Description (continued)

The REF60xx family of voltage references have an integrated low output impedance buffer (ADC drive buffer); therefore, there is no need for an external buffer while driving the REF pin of high-precision, high-throughput SAR ADCs, as shown in Figure 50. The ADC drive buffer of the REF60xx is capable of replenishing a charge of 70 pC on a 47-µF capacitor in 1 µs, without allowing the voltage on the capacitor to droop more than 1 LSB at 18-bit precision. The REF60xx are trimmed at multiple temperatures in production, achieving a max drift of just 5 ppm/°C for both the voltage reference and the buffer combined, while operating at a typical quiescent current of 820 µA. Figure 51 compares the output impedance of a regular voltage reference (REF20xx) and a voltage reference with integrated ADC drive buffer (REF60xx). Figure 52 compares the burst-mode, reference-settling performance of a regular voltage reference and the REF60xx.

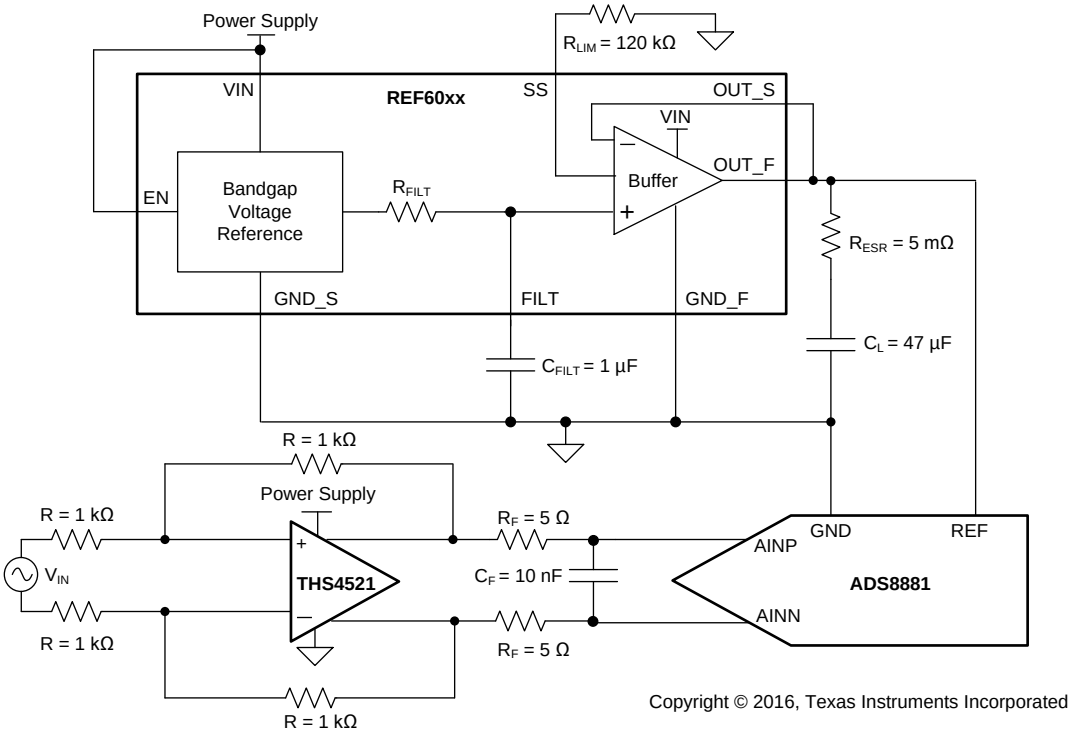


Figure 50. REF60xx Driving REF Pin of ADS8881 SAR ADC

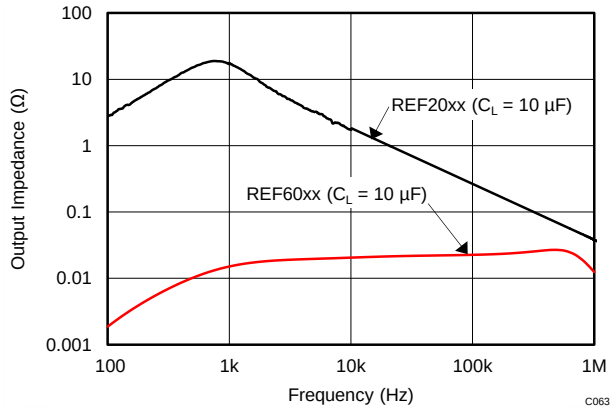
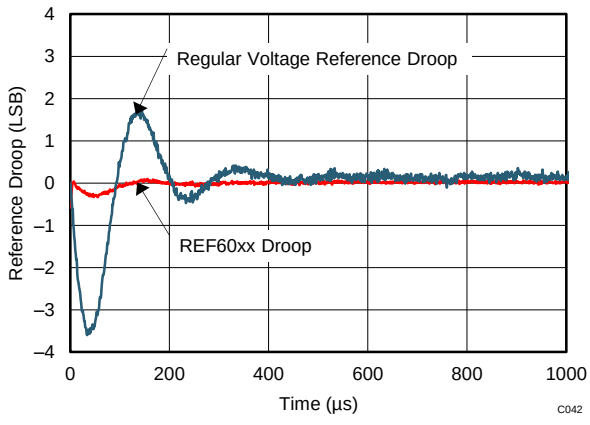


Figure 51. Output Impedance Comparison



1 LSB = 19.07 µV, with ADS8881 at 1 MSPS

Figure 52. Reference Droop Comparison

Feature Description (continued)

9.3.2 Temperature Drift

The REF60xx family is designed for minimal drift error, defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \bullet \text{Temperature Range}} \right) \bullet 10^6 \quad \text{(ppm)} \tag{3}$$

9.3.3 Load Current

The REF6025, REF6030, REF6033 and REF6041 are specified to deliver current load of ±4 mA. The REF6045 is specified to deliver ±3.5 mA, and the REF6050 is specified to deliver ±3 mA. The REF60xx are protected from short circuits at the output by limiting the output short-circuit current.

The short-circuit current limit (I_{SC}) of the REF60xx family of devices is adjusted by connecting a resistor (R_{SS}) on the SS pin. The short-circuit current limit when the REF60xx device is sourcing current can be calculated as shown in Equation 4:

$$I_{SC} = (80 * 10^{-9}) * R_{SS} + (3 * 10^{-3}) \tag{4}$$

The short circuit current limit when the REF60xx device is sinking is calculated as shown in Equation 5:

$$I_{SC} = (115 * 10^{-9}) * R_{SS} + (4.6 * 10^{-3}) \tag{5}$$

The recommended output current of the REF60xx also depends on the resistor connected to the SS pin. The recommended output current (sourcing and sinking) for the REF6025, REF6030, REF6033 and REF6041 is given by Equation 6:

$$I_L = (31.25 * 10^{-9}) * R_{SS} + (0.25 * 10^{-3}) \tag{6}$$

The recommended output current (sourcing and sinking) for the REF6045 is given by Equation 7:

$$I_L = (27.08 * 10^{-9}) * R_{SS} + (0.25 * 10^{-3}) \tag{7}$$

The recommended output current (sourcing and sinking) for the REF6050 is given by Equation 8:

$$I_L = (23.75 * 10^{-9}) * R_{SS} + (0.15 * 10^{-3}) \tag{8}$$

The temperature of the device increases according to Equation 9:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

where:

- T_J = junction temperature (°C).
- T_A = ambient temperature (°C).
- P_D = power dissipated (W).
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W). (9)

The REF60xx maximum junction temperature must not exceed the absolute maximum rating of 150°C.

Feature Description (continued)

9.3.4 Stability

The REF60xx family of voltage references are stable with output capacitor values ranging from 10 µF to 47 µF. At a low output-capacitor value of 10 µF, an effective series resistance (ESR) of 20 mΩ to 100 mΩ is required for stability; whereas, at a higher value of 47 µF, an ESR of 5 mΩ to 100 mΩ is required. The shaded region in Figure 53 shows the stable region of operation for the REF60xx devices.

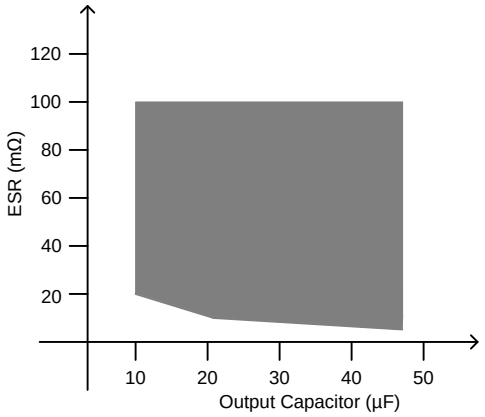


Figure 53. Stable Output Capacitor Range

A capacitor of value 1 µF is required at the FILT pin for stability and noise performance. A low ESR (5 mΩ to 20 mΩ) is easily achieved by increasing the PCB trace length, thus eliminating the need for a discrete resistor. Higher values of ESR (greater than 20 mΩ, but lesser than 100 mΩ) can be intentionally added to increase the output bandwidth of the REF60xx. This higher ESR improves the transient performance of the REF60xx, but worsens noise performance because of increased bandwidth.

9.4 Device Functional Modes

When the EN pin of the REF60xx is pulled high, the device is in active mode. The device must be in active mode for normal operation.

To place the REF60xx into a shutdown mode, pull the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 1 µA (typ). See the enable pin voltage parameter in the *Electrical Characteristics* table for logic high and logic low voltage levels.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Many applications, such as event-triggered and multiplexed data-acquisition systems, require the very first conversion of the ADC to have 18-bit or greater precision. These types of data acquisition systems capture data in bursts, and are also called burst-mode, data-acquisition systems. Achieving 18-bit precision for the first sample is very difficult using a conventional voltage reference because the voltage reference droop limits the accuracy of the first few conversions. Furthermore, variable-sampling-rate systems require that the gain error of the system does not vary with sampling rate. The primary objective of this design example is to demonstrate the lowest distortion and noise, burst-mode data-acquisition block with low power consumption, using an 18-bit SAR ADC operating at a throughput of 1 MSPS, for a 1-kHz, full-scale, pure sine-wave input.

10.2 Typical Application

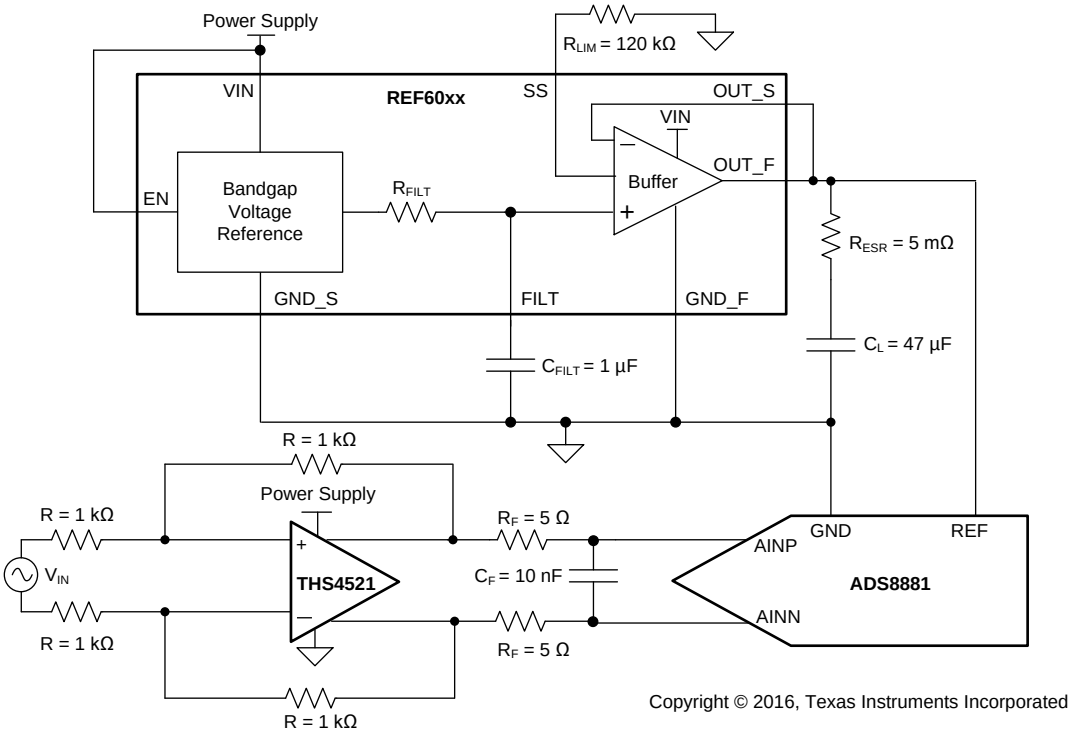


Figure 54. 18-bit, 1-MSPS, Burst-Mode Data Acquisition system

10.2.1 Design Requirements

1. Burst-mode support (see *Reference Droop Measurements* section for more details)
2. ENOB > 16 bits
3. THD < –120 dB
4. Power consumption < 50 mW
5. Throughput = 1 MSPS

Typical Application (continued)

10.2.2 Detailed Design Procedure

The data acquisition system shown in Figure 54 has three major contributors to the noise and accuracy in the system: the input driver, the reference with driver, and the data converter. Each analog block is carefully designed so that the data converter specifications limit the system specifications. The THS4551, a fully differential operational amplifier is used to drive the 18-bit ADC (ADS8881). The charge-kickback RC filter at the output of the THS4551 is used to reduce the charge kickback created by the opening and closing of the sampling switch inside the ADC. Design the RC filter so that the voltage at the sampling capacitor settles to 18-bit accuracy within the acquisition time of the ADC.

Data-acquisition systems require stable and accurate voltage references in order to perform the most accurate data conversion. The REF60xx family of voltage references have integrated an ADC drive buffer, and can therefore drive the REF pin of the ADS8881 directly, without the need for an external reference buffer. See the *Integrated ADC Drive Buffer* section for more details about reference-buffer requirements. Correct output capacitor selection for the REF60xx is very important in this design. The *Stability* section describes the ESR requirements of the output capacitor for stability and burst-mode requirements. A capacitance of 1 μF is connected to the FILT pin to reduce broadband noise of the REF60xx.

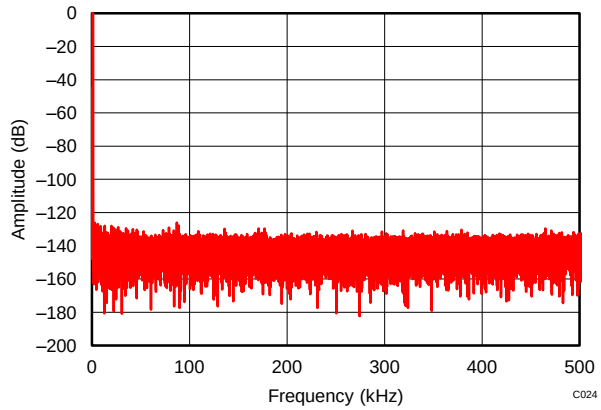
10.2.2.1 Results

Table 1 summarizes the measured results.

Table 1. Measured Results

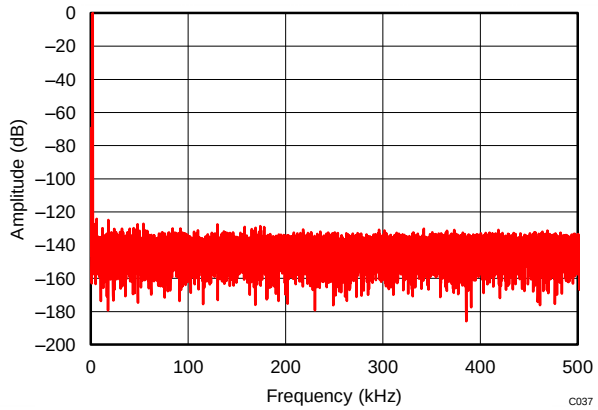
SPECIFICATION	MEASURED RESULT
SNR	100.5 dB
ENOB	16.4
THD	–125.9 dB
Throughput	1 MSPS
Burst mode	First sample > 18-bit precision
Power consumption	40 mW

10.2.3 Application Curves



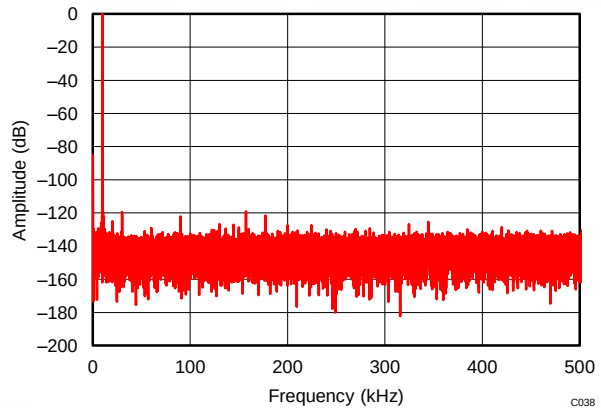
REF6050 driving REF pin of ADS8881,
f_{IN} = 1 kHz, SNR = 100.5 dB, THD = –125.9 dB

Figure 55. Typical FFT Plot



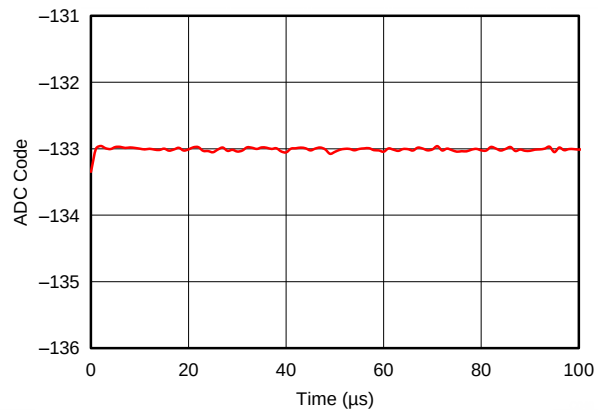
REF6050 driving REF pin of ADS8881,
f_{IN} = 2 kHz, SNR = 100.4 dB, THD = –123.9 dB

Figure 56. Typical FFT Plot



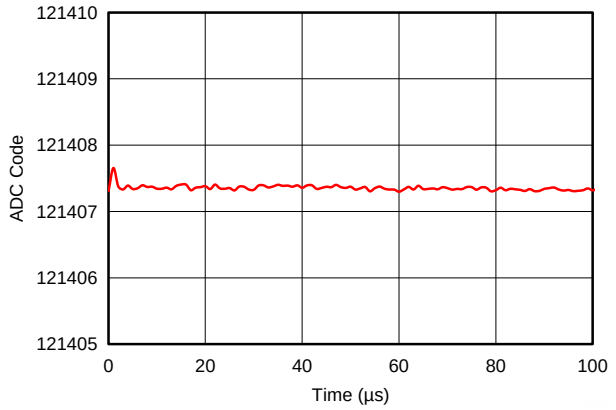
REF6050 driving REF pin of ADS8881,
f_{IN} = 10 kHz, SNR = 99.2 dB, THD = –119.4 dB

Figure 57. Typical FFT Plot



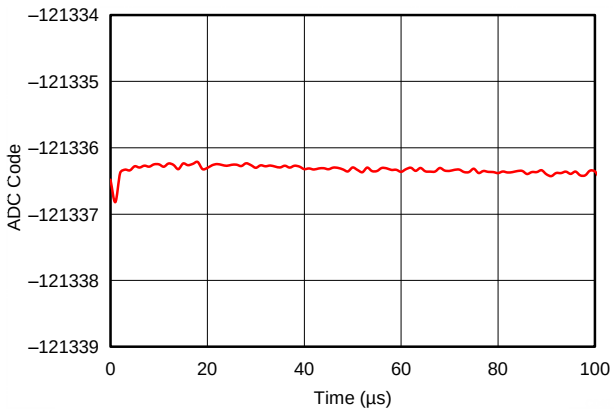
REF6050 driving REF pin of ADS8881 operating at 1 MSPS,
AINP = AINN = V_{REF} / 2 for ADS8881

Figure 58. Reference Droop



REF6050 driving REF pin of ADS8881 operating at 1 MSPS,
positive full-scale input to ADS8881

Figure 59. Reference Droop



REF6050 driving REF pin of ADS8881 operating at 1 MSPS,
negative full-scale input to ADS8881

Figure 60. Reference Droop

11 Power Supply Recommendations

The REF60xx family of references have extremely low dropout voltage. The dropout specifications can be found in the *Electrical Characteristics* section. A minimum 0.1 µF decoupling capacitor must be connected between the VIN and GND_F pins of the REF60xx. A typical dropout voltage versus load is shown in Figure 61.

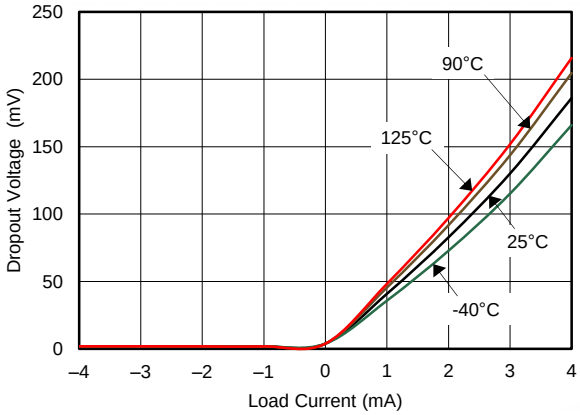


Figure 61. Dropout Voltage vs Load Current

12 Layout

12.1 Layout Guidelines

Figure 62 illustrates an example of a PCB layout for a data-acquisition system using the REF60xx. Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between the VIN pin and ground.
- Place the REF60xx output capacitor (C_L) and the ADC as close to each other as possible.
- Run two separate traces between VOUT_F, VOUT_S and the output capacitor, as shown in Figure 62.
- Short the GND_F and GND_S pins with a solid plane, and extend this plane to connect to the output capacitor C_L, as shown in Figure 62.
- Use a solid ground plane to help distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

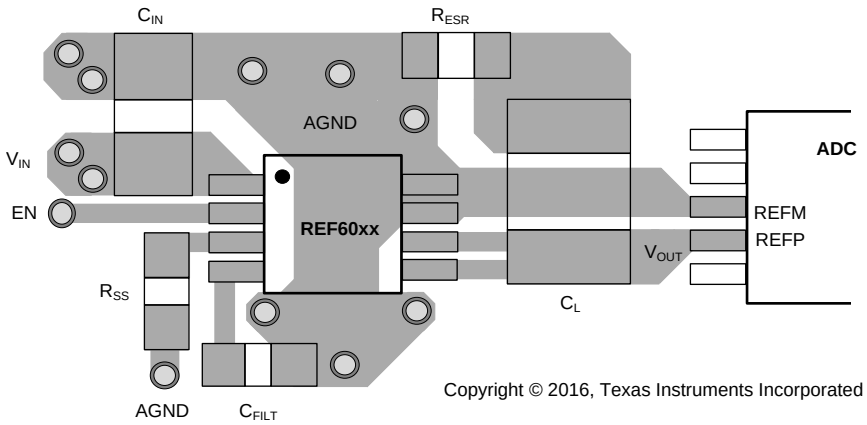


Figure 62. Layout Example

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

相关文档如下：

- *《ADS8881x 18 位、1MSPS、串行接口、微功耗、微型、真正的差分输入、SAR 模数转换器数据表》*（文献编号：SBAS547）
- *《ADS127L01 24 位、高速、高带宽模数转换器数据表》*（文献编号：SBAS607）
- *《REF6025EVM-PDK 用户指南》*（文献编号：SBAU258）
- *《电压基准对总谐波失真的影响》*（文献编号：SLYY097)

13.2 相关链接

下面的表格中列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **2.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
REF6025	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6030	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6033	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6041	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6045	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
REF6050	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

13.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
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RFID 系统	www.ti.com.cn/rfidsys		
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邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF6025IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV	Samples
REF6025IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11KV	Samples
REF6030IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV	Samples
REF6030IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11LV	Samples
REF6033IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV	Samples
REF6033IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11MV	Samples
REF6041IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV	Samples
REF6041IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11NV	Samples
REF6045IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG	Samples
REF6045IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13SG	Samples
REF6050IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV	Samples
REF6050IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13QV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

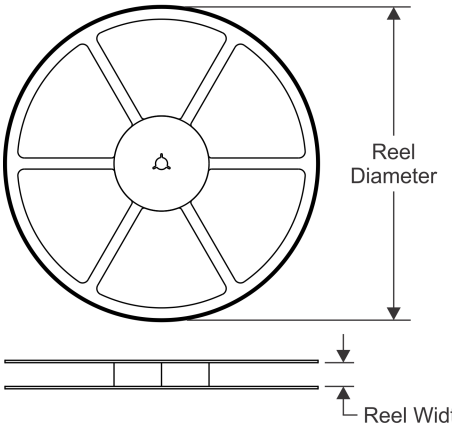
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

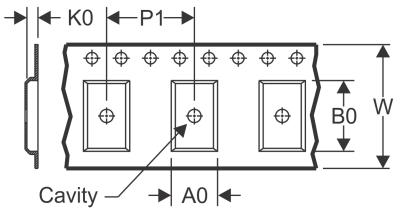
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

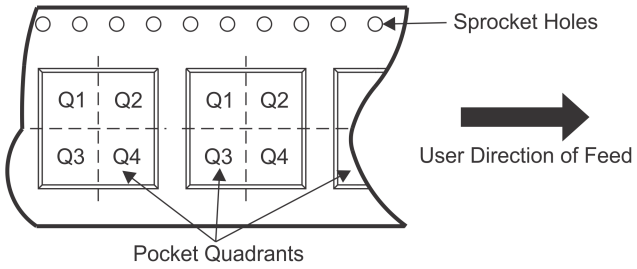


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

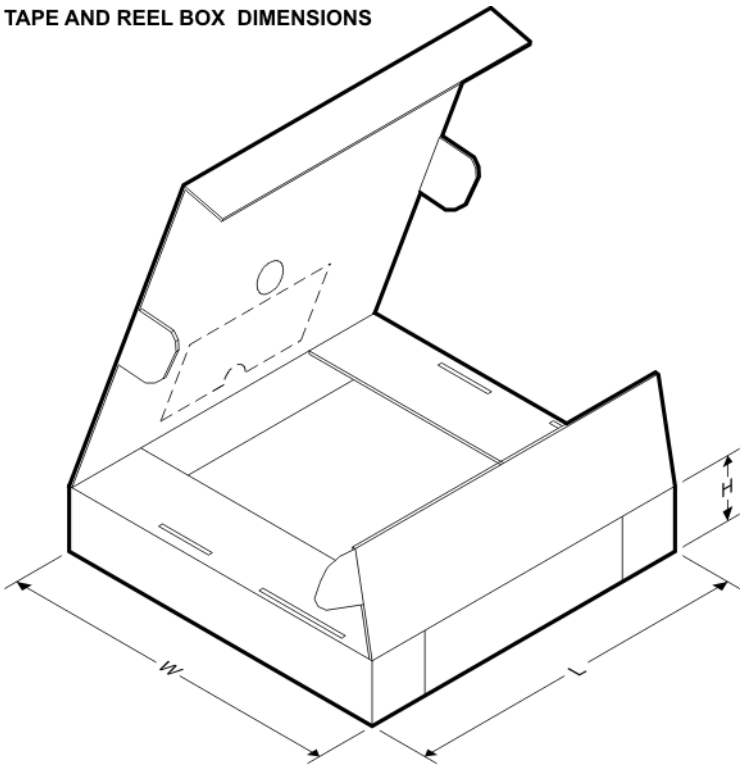
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF6025IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6025IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6030IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6030IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6033IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6033IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6041IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6045IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6045IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF6050IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

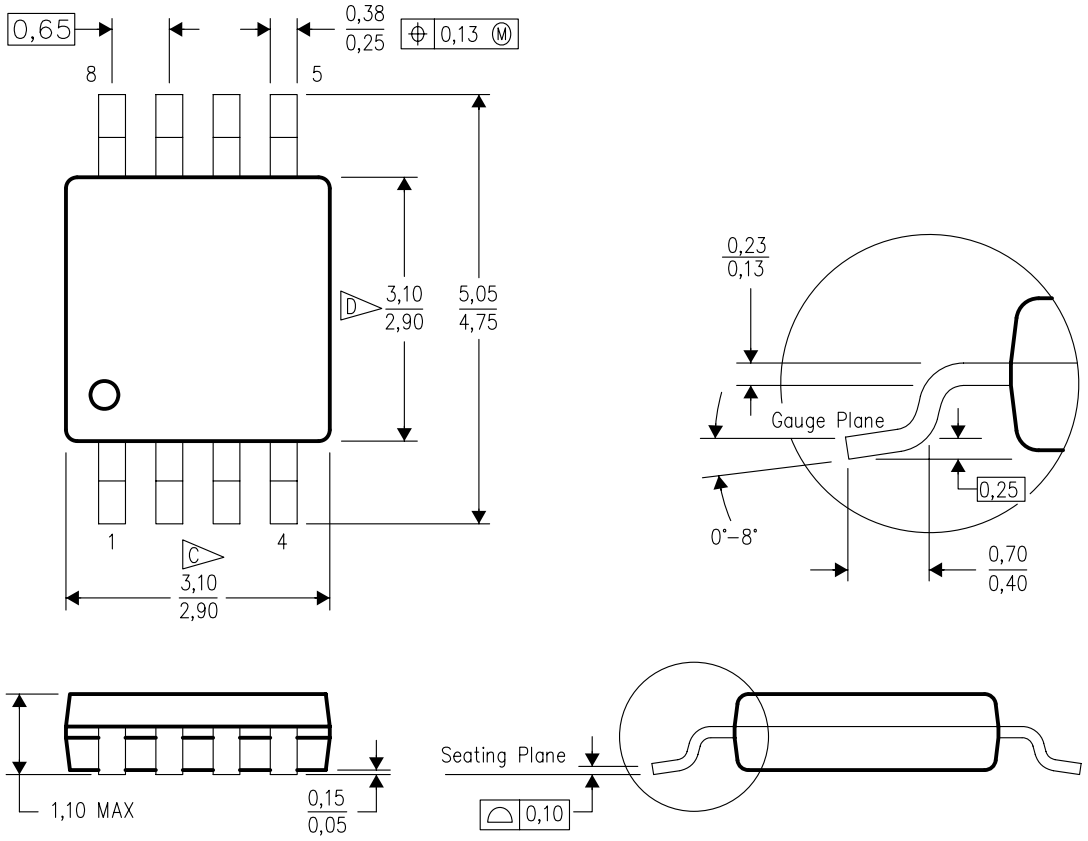
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF6025IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6025IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6030IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6030IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6033IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6033IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6041IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6041IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6045IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6045IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
REF6050IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
REF6050IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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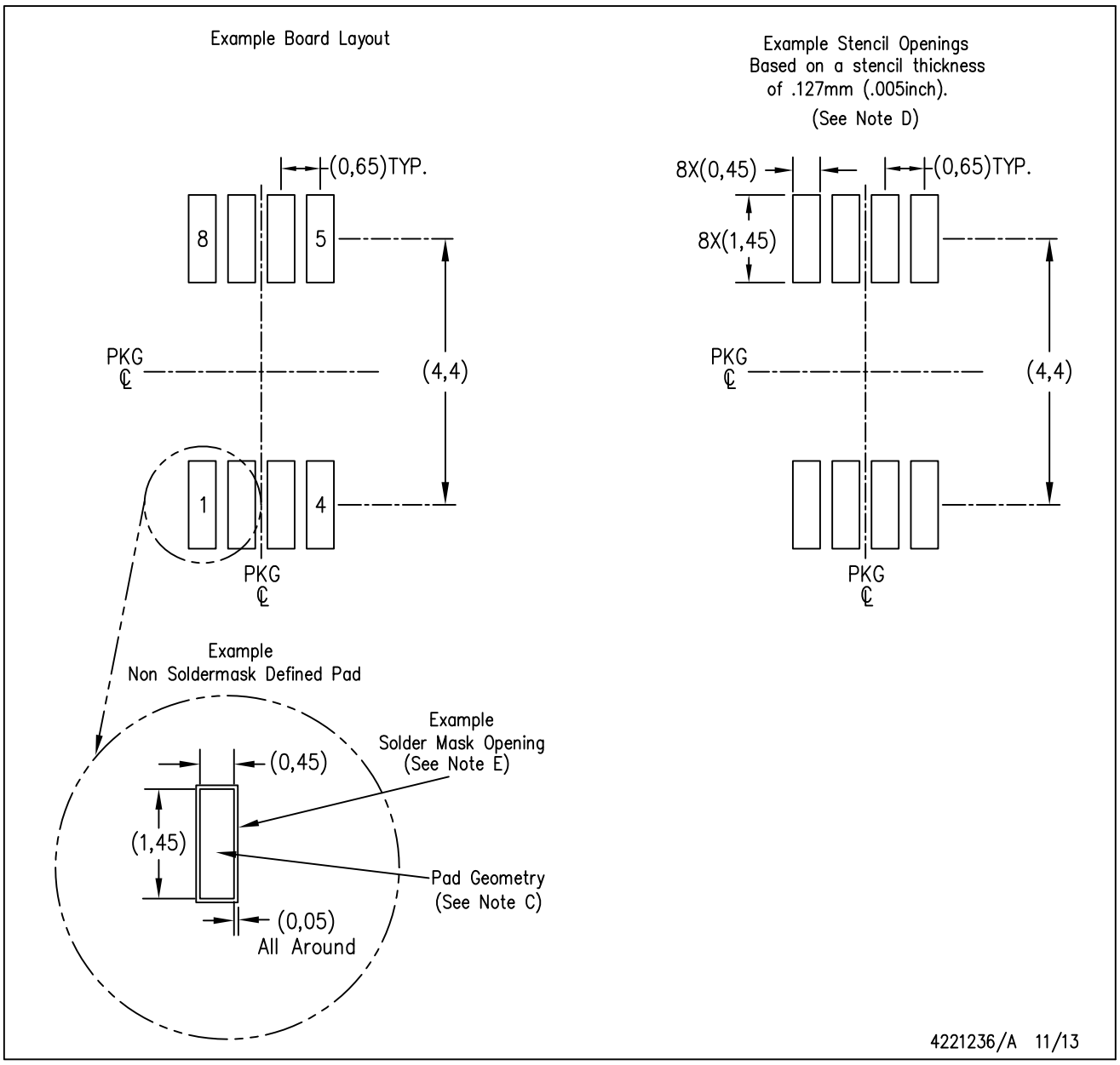
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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