TMS470MF04207/TMS470MF03107 16/32 位精简指令集 (RISC) 闪存微控制器

查询样片: TMS470MF04207, TMS470MF03107

1 特性

- 带有安全特性的高性能汽车级微控制器
  - 完全车用温度范围
  - 闪存和 **SRAM** 上的错误校正码 **(ECC)**
  - **CPU** 和内存 **BIST**（内置自检）
- **ARM Cortex™-M3 32** 位 **RISC CPU**
  - 高效 **1.2DMIPS/MHz**
  - 优化的 **Thumb2** 指令集
  - 内存保护单元 **(MPU)**
  - 带有第三方支持的开放式架构
  - 内置调试模块
- 操作特性
  - 高达 **80Mhz** 系统时钟
  - 单个 **3.3V** 电源
- 集成内存
  - 带有 **ECC** 的 **448KB** 总程序闪存
  - 支持闪存 **EEPROM** 仿真
  - 带有 **ECC** 的 **24K** 字节静态 **RAM (SRAM)**
- 关键外设
  - 高端定时器，多缓冲模数转换器 **(MibADC)**，控制器局域网络 **(CAN)**，多缓冲串行外设接口 **(MibSPI)**
- 通用 **TMS470M/570** 平台架构
  - 系列产品上的一致内存映射
  - 实时中断定时器 **(RTI)**
  - 数字安全装置
  - 矢量中断模块 **(VIM)**
  - 循环冗余校验器 **(CRC)**
- 基于调频零引脚锁相环路 **(FMzPLL)** 的时钟模块
  - 振荡器和 **PLL** 时钟模块
- 高达 **49** 个外设 **IO** 引脚
  - **4** 个专用 **GIO -** 带有外部中断
- 两个外部时钟前置分频器 **(ECP)** 模块
  - 可编程低频外部时钟 **(ECLK)**
  - 一个专用引脚和一个复用 **ECLK/HET** 引脚
- 通信接口
  - 两个 **CAN** 控制器
    - 一个有 **32** 个邮箱，另外一个有 **16** 个邮箱
    - 邮箱 **RAM** 上的奇偶校验
  - 两个多缓冲串行外设接口 **(MibSPI)**
    - 总数为 **12** 的芯片选择
    - **64** 个缓冲器，每个缓冲器上均有奇偶校验
  - 两个通用异步收发器 **(UART) (SCI)** 接口
    - 针对本地互连网络（**LIN 2.1** 主控模式）的硬件支持
- 高端定时器 **(HET)**
  - 多达 **16** 个可编程 **I/O** 通道
  - 带有奇偶校验的 **128** 字高端定时器 **RAM**
- **16** 通道 **10** 位多缓冲 **ADC (MibADC)**
  - 带有奇偶校验的 **64** 字 **FIFO** 缓冲器
  - 单一或者连续转换模式
  - **1.55μs** 最小采样/转换时间
  - 校准模式和自检特性
- 片载基于扫描的仿真逻辑电路
  - **IEEE** 标准 **1149.1 (JTAG)** 测试-访问端口和边界扫描
- 支持的数据包
  - **100** 引脚塑料四方扁平封装（**PZ** 后缀）
  - 绿色环保/无铅
- 可用的开发工具
  - 开发板
  - **Code Composer Studio** 集成开发环境 **(IDE)**
  - **HET** 汇编程序和模拟器
  - **nowFlash™** 闪存编程工具
- 社区资源
  - **TI E2E** 社区

1.1 PZ 封装视图

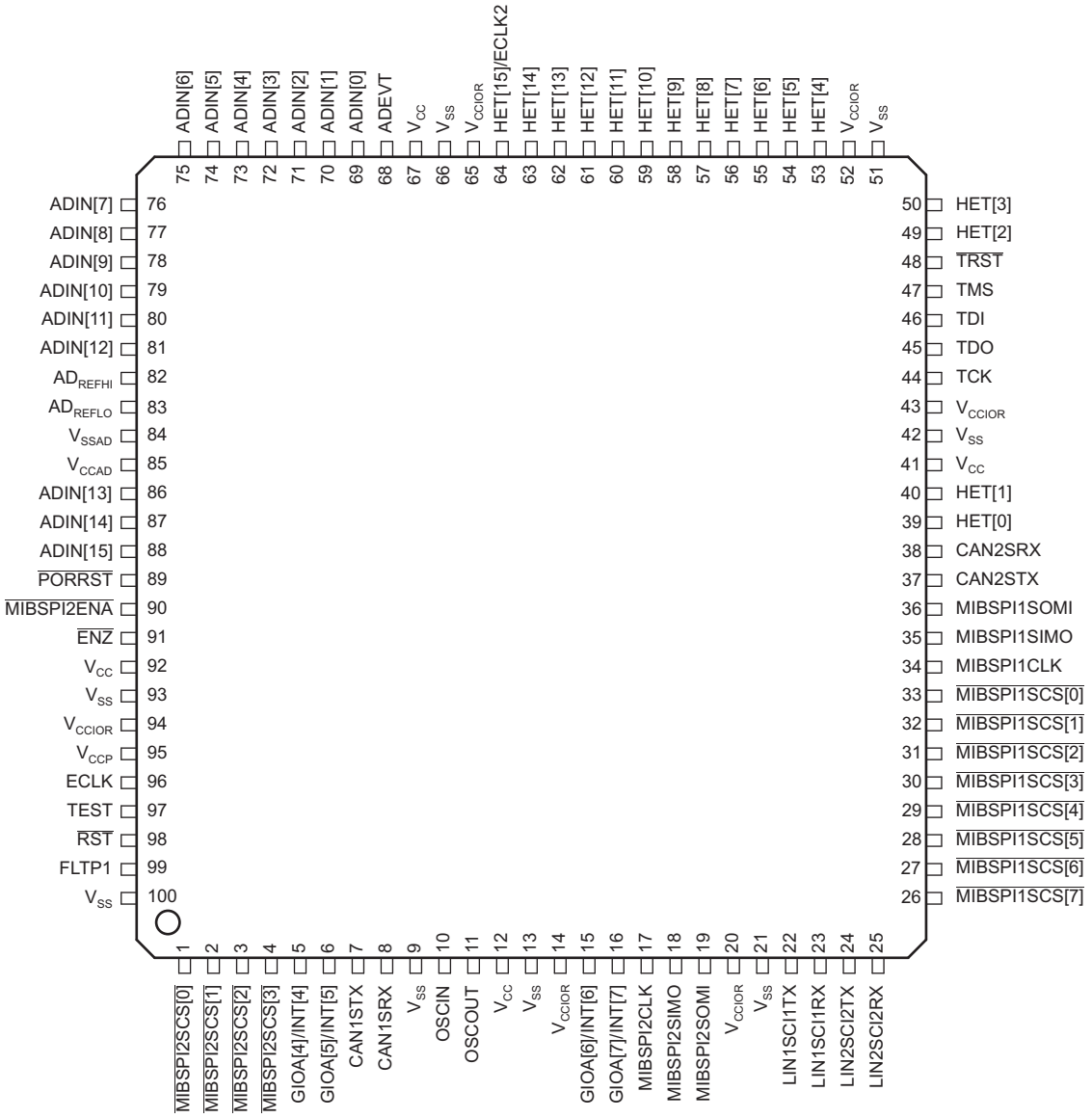


图 **1-1. TMS470MF04207** 和 **TMS470MF03107 100** 引脚 **PZ** 封装（顶视图）

1.2 说明

TMS470MF04207/03107 器件隶属于德州仪器 (TI) 的 TMS470M 汽车级 16/32 位精简指令集计算机 (RISC) 微控制器系列。 TMS470M 微控制器利用高效率的 Cortex™–M3 16/32 位 RISC 中央处理单元 (CPU) 提供了高性能，由此实现了很高的指令吞吐量并保持了更加出色的代码效率。 TMS470M 器件运用了大端字节序格式，在该格式中，一个字的最高有效字节被存储于编号最小的字节中，而最低有效字节则存储在编号最大的字节中。

高端嵌入式控制应用要求其控制器提供更多的性能并保持低成本。 TMS470M 微控制器架构提供了针对这些性能和成本需求的解决方案，并保持了低功耗。

TMS470MF04207/03107 器件的组成如下：

- 16/32 位 RISC CPU 内核
- TMS470MF04207 高达 448K 字节的程序闪存（具有 SECDED ECC）
- TTMS470MF03107 高达 320K 字节的程序闪存（具有SECDED ECC）
- 具有 SECDED ECC 的 64K 字节闪存 （用于获得额外的程序空间或进行 EEPROM 仿真）
- 高达 24K 字节的静态 RAM (SRAM) （具有 SECDED ECC）
- 实时中断定时器 (RTI)
- 矢量中断模块 (VIM)
- 硬件内置自测试 (BIST) 校验器，用于SRAM (MBIST) 和 CPU (LBIST)
- 64 位循环冗余校验器 (CRC)
- 基于调频零引脚锁相环 (FMzPLL) 的时钟模块（带前置分频器）
- 两个多缓冲串行外设接口 (MibSPI)
- 两个具有本地互连网络接口 (LIN) 的 UART (SCI)
- 两个 CAN 控制器 (DCAN)
- 高端定时器 (HET)
- 外部时钟前置分频器 (ECP) 模块
- 一个 16 通道 10 位多缓冲 ADC (MibADC)
- 错误信令模块 (ESM)
- 4 个专用的通用 I/O (GIO) 引脚和 45 个附加外设 I/O (100 引脚封装)

TMS470M 内存包括通用 SRAM，可支持字节模式、半字模式及字模式的单周期读/写存取。 可以利用 ECC 对 TMS470M 器件上的 SRAM 加以保护。 此项特性运用单错纠正和双错检测电路（SECDED 电路）来检测并选择性地校正单位错误以及检测所有的双位错误和某些多位错误。 这是通过将一个用于内存空间的每个 64 位双字的 8 位 ECC 校验和/代码保存在一个单独的 ECC RAM 内存空间中实现的。

该器件上的闪存是一种非易失性、电可擦且可编程的存储器。 它是采用一个 144 位宽的数据字 （128 位，无 ECC） 和一个 64 位宽的闪存模块接口实现的。 该闪存在高达 28MHz 的系统时钟频率条件下运行。 可提供闪存数据线性预读取的流水线模式实现了一个高达 80MHz 的系统时钟。

TMS470M 器件上的增强型实时中断 (RTI) 模块可选择由振荡器时钟进行驱动。 数字安全装置 (DWD) 是一个 25 位的可复位递减计数器，当安全装置计数器终止计数时，该计数器将提供系统复位。

TMS470M 器件具有 6 个通信接口：两个 LIN/SCI、两个 DCAN 和两个 MibSPI。 LIN 是本地互连网络标准，而且还支持一种 SCI 模式。 SCI 可被用在一个用于 CPU 与其他采用标准不归零制 (NRZ) 格式外设之间的异步通信的全双工、串行 I/O 接口中。 DCAN 采用一种串行、多主机通信协议，此协议可高效支持分布式实时控制及高达 1 兆位每秒 (Mbps) 的稳健通信速率。 DCAN 非常适合于工作于嘈杂和严酷环境中的应用（例如：汽车和工业领域），此类应用需要可靠的串行通信或多路复用线路。 MibSPI 为相似的移位寄存器型器件之间的高速通信提供了一种便捷的串行交互方法。 MibSPI 提供了标准的 SOMI、SIMO 和 SPI 时钟接口以及多达 8 条芯片选择线路。

HET 是一种先进的智能定时器，可为实时应用提供精密的定时功能。 该定时器为软件控制型，采用一个精简指令集，并具有一个专用的微级机定时器和一个连接的 I/O 端口。 这种 HET 可用于比较、捕获或通用型 I/O。它特别适合于那些需要带有复杂和准确的时间脉冲的多种传感器信息和驱动传动器的应用。 TMS470M HET 外设包含 “异或 (XOR) 共享” 功能。 该功能允许对两个相邻的 HET 高分辨率通道进行 “异或” 运算，从而可以输出一个小于标准 HET 的脉冲。

TMS470M 器件具有一个 10 位分辨率的采样及保持 MibADC。 可利用软件对每个 MibADC 通道进行分组，以用于顺序转换序列。 有三个单独的分组，它们均可以由一个外部事件触发。 每个序列可在被触发时执行一次转换，或者通过配置以执行连续转换模式。

调频零引脚锁相环 (FMzPLL) 时钟模块包含一个锁相环、一个时钟监视器电路、一个时钟启用电路和一个前置分频器。 FMzPLL 的功能是将外部频率基准倍频至一个较高的频率，以供内部使用。 FMzPLL 提供了全局时钟模块 (GCM) 的输入。 GCM 模块接着向所有其他的 TMS470M 器件模块提供系统时钟 (HCLK)、实时中断时钟 (RTICLK)、CPU 时钟 (GCLK)、HET 时钟 (VCLK2)、DCAN 时钟 (AVCLK1) 及外设接口时钟 (VCLK)。

另外，TMS470MF04207/TMS470MF03107 器件还具有两个外部时钟前置分频器 (ECP) 模块，该模块在被启用时将输出一个连续外部时钟 (ECLK)。 ECLK1 频率是外设接口时钟 (VCLK) 频率的一个用户可编程比值。 可以选择第二个 ECLK 输出来取代 HET15 输出。 它与 ECLK1 共用同一个信源时钟，但可以针对一个产生自 ECLK1 的单独输出频率进行独立设置。

错误信令模块 (ESM) 在器件内部提供了一个用于错误报告的共用位置，从而实现了高效的错误检查和识别。

1.3 功能方框图

图 1-2显示了 TMS470M 器件的功能方框图。

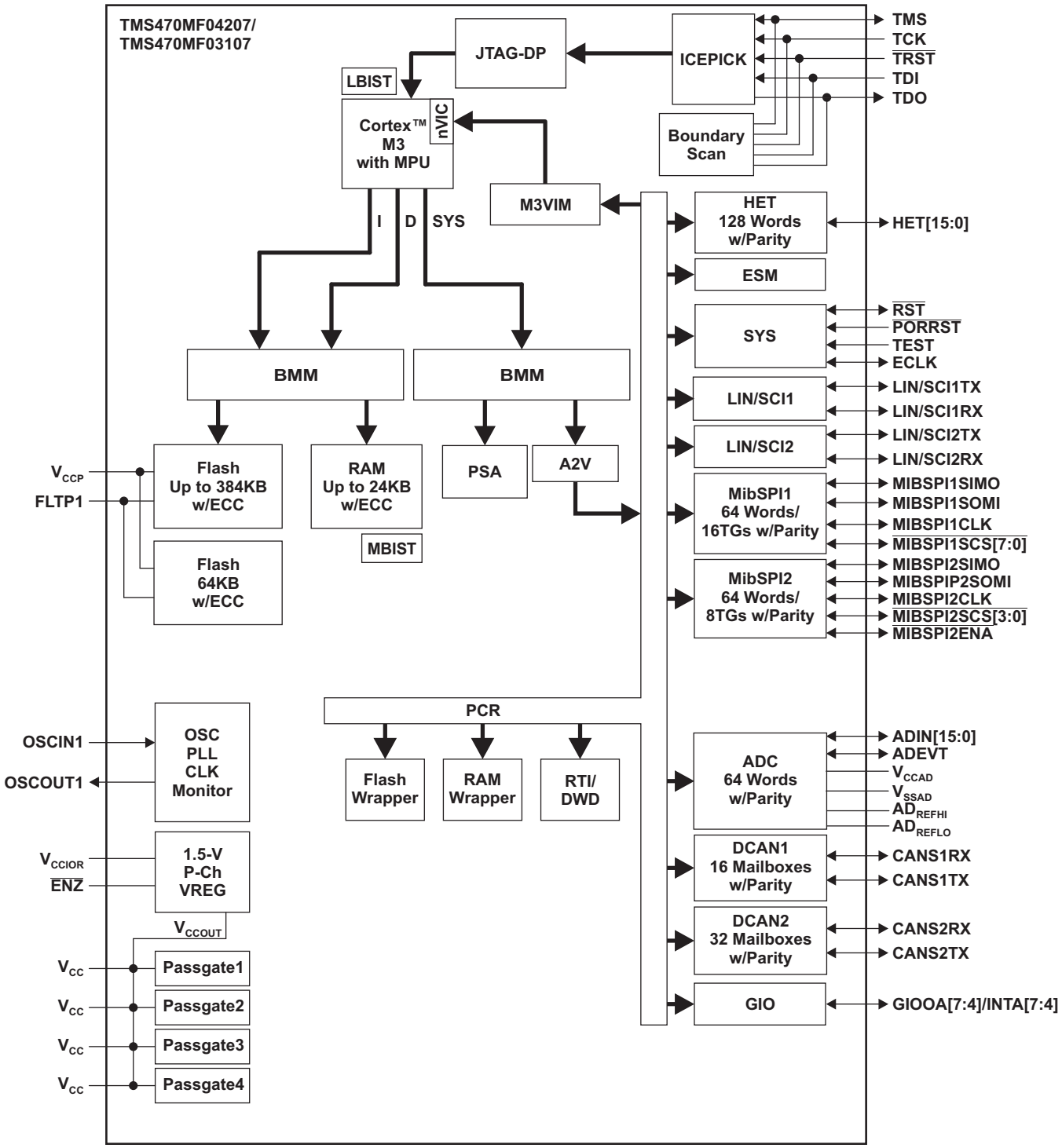


图 **1-2. TMS470M** 系列方框图

1.4 术语和首字母缩略词

表 1-1. 术语和首字母缩略词

术语和首字母缩略词	描述	注释
A2V	AHB 至 VBUSP 桥接	A2V 桥接提供私有 TI VBUSP 和 TMS470M 平台器件中 ARM AHB 总线间的内存接口。
ADC	模数转换器	
AHB	高级高性能总线	M3 内核的部件
BMM	总线矩阵主控	BMM 提供不同总线受控模块到不同总线主控模块的连接性。 如果没有发生资源冲突或者如果主控模块在仲裁过程中保持并行的话，来自不同总线模块的访问可并行执行。
CRC	循环冗余校验控制器	
DAP	调试访问端口	DAP 是一个 ARM 调试接口的工具。
DCAN	控制器局域网	
DWD	数字安全装置	
ECC	错误校正码	
ESM	错误信令模块	
GIO	通用输入/输出	
HET	高端定时器	
ICEPICK	处于电路仿真 TAP（测试访问端口）选择模块	ICEPick 能够连接或者隔离一个模块级 TAP 到一个更高级芯片 TAP 的数据通信。 ICEPick 设计时充分考虑了仿真和测试需要。
JTAG	联合测试访问组	负责测试访问端口的 IEEE 委员会
JTAG-DP	JTAG 调试端口	JTAG-DP 包含一个调试端口状态机 (JTAG)，此状态机控制 JTAG-DP 运行，包括控制扫描链路接口，此接口提供到 JTAG-DP 的外部物理接口。 它基于 JTAG TAP 状态机，请见 IEEE 标准 1149.1-2001。
LBIST	逻辑内置自检	测试 M3 CPU 的完整性
LIN	本地互连网络	
M3VIM	Cortex-M3 矢量中断管理器	
MBIST	存储器内置自检	测试 SRAM 的完整性
MibSPI	多缓冲串行外设接口	
MPU	保护单元	
NVIC	嵌套矢量中断控制器	M3 内核的部件
OSC	振荡器	
PCR	外设中心资源	
PLL	锁相环路	
PSA	并行签名分析	
RTI	实时中断	
SCI	串行通信接口	
SECDED	单一错误校正和双错误校正	
STC	自检控制器	
SYS	系统模块	
VBUS	虚拟总线	包括 CBA（通用总线架构）的协议中的一个
VBUSP	虚拟管道型总线	包括 CBA（通用总线架构）的协议中的一个
VREG	电压稳压器	

2 Device Overview

The TMS470MF04207/03107 device is a TMS470M Platform Architecture implemented in F035 130-nm TI technology. Table 2-1 identifies all the characteristics of the TMS470MF04207/03107 device except the SYSTEM and CPU, which are generic.

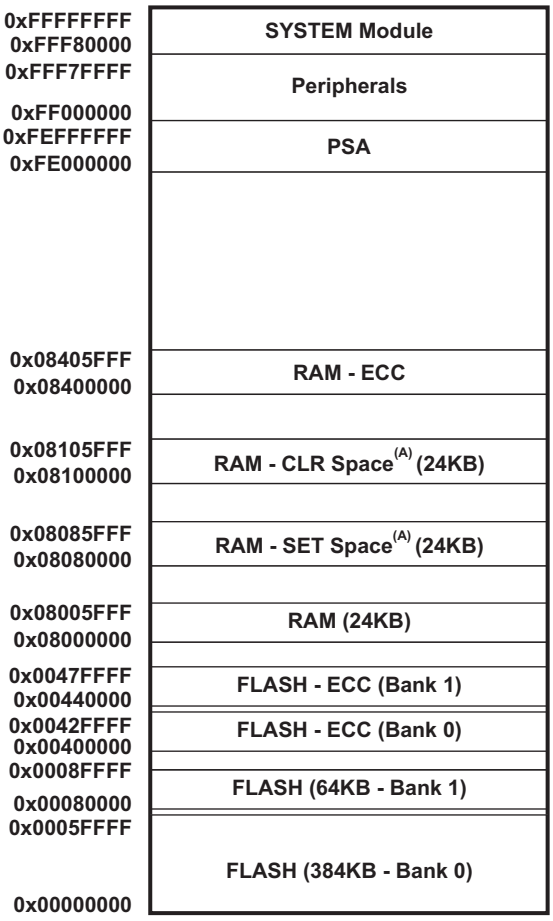
Table 2-1. Device Characteristics

CHARACTERISTICS	DEVICE DESCRIPTION TMS470MF04207/03107	COMMENTS FOR TMS470M
MEMORY		
INTERNAL MEMORY	Pipeline/Non-Pipeline 2 Banks with up to 448K-Byte Flash with ECC Up to 24K-Byte SRAM with ECC CRC, 1-channel	Flash is pipeline-capable
PERIPHERALS		
For the device-specific interrupt priority configurations, see Table 3-4. For the peripheral address ranges and their peripheral selects, see Table 2-7.		
CLOCK	FMzPLL	Frequency-modulated zero-pin PLL has no external loop filter pins.
GENERAL-PURPOSE I/Os	4 I/O	The GIOA port has up to four (4) external pins with external interrupt capability.
LIN/SCI	2 LIN/SCI	
DCAN	2 DCAN	Each with 16/32 mailboxes, respectively.
MibSPI	2 MibSPI	One MibSPI with eight chip select pins, 16 transfer groups, and a 64 word buffer with parity. A second MibSPI with four chip select pins, 1 enable pin, 8 transfer groups, and a 64 word buffer with parity.
HET with XOR Share	16 I/O	The high-resolution (HR) SHARE feature allows even-numbered HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. HET RAM with parity checking capability.
HET RAM	128-Instruction Capacity	
MibADC	10-bit, 16-channel 64-word FIFO	MibADC RAM includes parity support.
CORE VOLTAGE	1.55 V	The core voltage is supplied and regulated by the device's internal voltage regulator. There is not need for an externally supplied core voltage.
I/O VOLTAGE	3.3 V	
PINS	100	Available in a 100-pin package.
PACKAGE	PZ (100 pin)	The 100-pin package designator is PZ.

2.1 Memory Map Summary

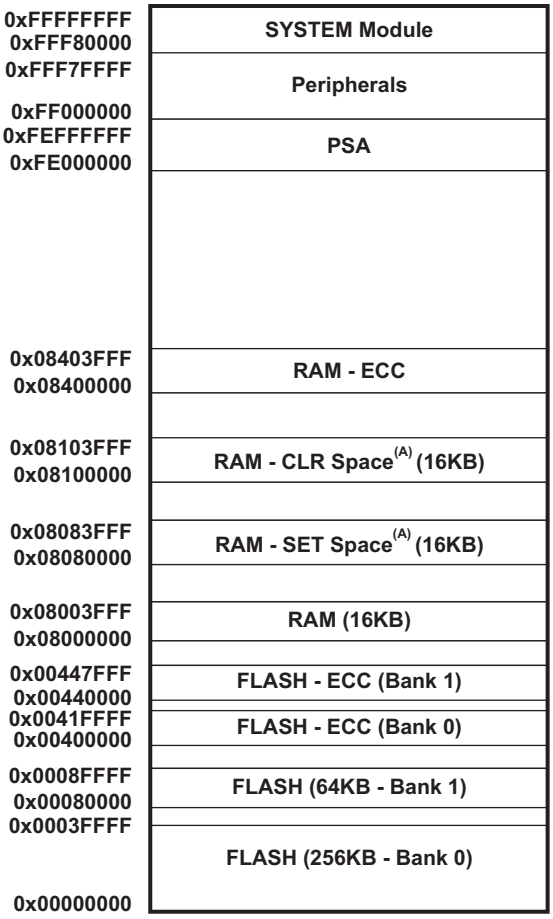
2.1.1 Memory Map

Figure 2-1 and Figure 2-2 show the TMS470MF04207 and TMS470MF03107 memory maps.



A. The RAM supports bit access operation which allows set/clear to dedicated bits without disturbing the other bits; for detailed description, see the Architecture Specification.

Figure 2-1. TMS470MF04207 Memory Map



A. The RAM supports bit access operation which allows set/clear to dedicated bits without disturbing the other bits; for detailed description, see the Architecture Specification.

Figure 2-2. TMS470MF03107 Memory Map

2.1.2 Memory Selects

Memories in the TMS470M devices are located at fixed addresses. Table 2-2 through Table 2-7 detail the mapping of the memory regions.

Table 2-2. TMS470MF04207-Specific Memory Frame Assignment

MEMORY FRAME NAME	START ADDRESS	ENDING ADDRESS	MEMORY TYPE	ACTUAL MEMORY
nCS0(1)	0x0000 0000	0x0005 FFFF	Flash	384K Bytes
	0x0008 0000	0x0008 FFFF	Flash	64K Bytes
RAM-CLR	0x0810 0000	0x0810 5FFF	Internal RAM	24K Bytes
RAM-SET	0x0808 0000	0x0808 5FFF	Internal RAM	24K Bytes
CSRAM0(1)	0x0800 0000	0x0800 5FFF	Internal RAM	24K Bytes
	0x0840 0000	0x0840 5FFF	Internal RAM-ECC	24K Bytes

(1) Additional address mirroring could be present resulting in invalid but addressable locations beyond those listed above. TI recommends the use of the MPU for protecting access to addresses outside the intended range of use.

Table 2-3. TMS470MF03107-Specific Memory Frame Assignment

MEMORY FRAME NAME	START ADDRESS	ENDING ADDRESS	MEMORY TYPE	ACTUAL MEMORY
nCS0(1)	0x0000 0000	0x0003 FFFF	Flash	256K Bytes
	0x0008 0000	0x0008 FFFF	Flash	64K Bytes
RAM-CLR	0x0810 0000	0x0810 3FFF	Internal RAM	16K Bytes
RAM-SET	0x0808 0000	0x0808 3FFF	Internal RAM	16K Bytes
CSRAM0(1)	0x0800 0000	0x0800 3FFF	Internal RAM	16K Bytes
	0x0840 0000	0x0840 3FFF	Internal RAM-ECC	16K Bytes

(1) Additional address mirroring could be present resulting in invalid but addressable locations beyond those listed above. TI recommends the use of the MPU for protecting access to addresses outside the intended range of use.

Table 2-4. Memory Initialization and MBIST

CONNECTING MODULE	ADDRESS RANGE		MEMORY INITIALIZATION CHANNEL	MBIST CONTROLLER ENABLE CHANNEL
	BASE ADDRESS	ENDING ADDRESS		
System RAM (TMS470MF04207)	0x0800 0000	0x0800 5FFF	0	0
System RAM (TMS470MF03107)	0x0800 0000	0x0800 3FFF	0	0
MibSPI1 RAM	0xFF0E 0000	0xFF0F FFFF	1	1 or 2(1)
MibSPI2 RAM	0xFF0C 0000	0xFF0D FFFF	2	
DCAN1 RAM	0xFF1E 0000	0xFF1F FFFF	3	3 or 4(1)
DCAN2 RAM	0xFF1C 0000	0xFF1D FFFF	4	
ADC RAM	0xFF3E 0000	0xFF3F FFFF	5	5
HET RAM	0xFF46 0000	0xFF47 FFFF	Not Available	6
STC ROM	Not Applicable	Not Applicable	Not Applicable	7

(1) There are single MBIST controllers for both MibSPI RAMs and both DCAN RAMs. The MBIST controller for both MibSPI RAMs is mapped to channels 1 and 2 and the MBIST controller for both DCAN RAMs is mapped to channels 3 and 4. MBIST on these modules can be initiated by selecting one of the 2 channels or both.

Table 2-5. Peripheral Memory Chip Select Assignment

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
MibSPI1 RAM	0xFF0E 0000	0xFF0F FFFF	PCS[7]
MibSPI2 RAM	0xFF0C 0000	0xFF0D FFFF	PCS[6]
DCAN1 RAM	0xFF1E 0000	0xFF1F FFFF	PCS[14]
DCAN2 RAM	0xFF1C 0000	0xFF1D FFFF	PCS[15]

Table 2-5. Peripheral Memory Chip Select Assignment (continued)

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
ADC RAM	0xFF3E 0000	0xFF3F FFFF	PCS[31]
HET RAM	0xFF46 0000	0xFF47 FFFF	PCS[35]

NOTE

All used peripheral memory chip selects should decode down to the smallest possible address for this particular peripheral configuration, starting from 4kB upwards. Unused addresses should generate an illegal address error when accessed.

Table 2-6. System Peripheral Registers

FRAME NAME	ADDRESS RANGE	
	FRAME START ADDRESS	FRAME ENDING ADDRESS
PSA	0xFE00 0000	0xFEFF FFFF
Flash Wrapper Registers	0xFFF8 7000	0xFFF8 7FFF
PCR Register	0xFFFF E000	0xFFFF E0FF
System Frame 2 Registers	0xFFFF E100	0xFFFF E1FF
CPU STC (LBIST)	0xFFFF E400	0xFFFF E4FF
ESM Register	0xFFFF F500	0xFFFF F5FF
RAM ECC Register	0xFFFF F900	0xFFFF F9FF
RTI Register	0xFFFF FC00	0xFFFF FCFF
VIM Register	0xFFFF FE00	0xFFFF FEFF
System Registers	0xFFFF FF00	0xFFFF FFFF

Table 2-7. Peripheral Select Map with Address Range

CONNECTING MODULE	BASE ADDRESS	END ADDRESS	PERIPHERAL SELECTS
MibSPI2	0xFFF7 F600	0xFFF7 F7FF	PS[2]
MibSPI1	0xFFF7 F400	0xFFF7 F5FF	
LIN/SCI1	0xFFF7 E500	0xFFF7 E5FF	PS[6]
LIN/SCI2	0xFFF7 E400	0xFFF7 E4FF	
DCAN2	0xFFF7 DE00	0xFFF7 DFFF	PS[8]
DCAN1	0xFFF7 DC00	0xFFF7 DDFF	
ADC	0xFFF7 C000	0xFFF7 C1FF	PS[15]
GIO	0xFFF7 BC00	0xFFF7 BCFF	PS[16]
HET	0xFFF7 B800	0xFFF7 B8FF	PS[17]

2.1.3 Flash Memory

When in pipeline mode, the Flash operates with a system clock frequency of up to 80 MHz (versus a system clock in non-pipeline mode of up to 28 MHz). Flash in pipeline mode is capable of accessing 128-bit words and provides four 32-bit pipelined words to the CPU.

NOTE

1. After a system reset, pipeline mode is **disabled** [FRDCNTL[2:0] is 000b, see the Flash chapter in the *TMS470M Series Technical Reference Manual* (literature number SPNU495)]. In other words, the device powers up and comes out of reset in **non-pipeline mode**.
2. **The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).**

2.1.4 Flash Program and Erase

The TMS470MF04207/TMS470MF03107 devices flash contain one 384/256K-byte memory array (or bank) and one 64K-byte bank for a total of up to 12 sectors. Table 2-8 and Table 2-9 show the TMS470MF04207 and TMS470MF03107 flash memory banks and sectors.

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 32-bit word.

Table 2-8. TMS470MF04207 Flash Memory Banks and Sectors

SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS	MEMORY ARRAYS (OR BANKS)
0	16k	0x0000 0000	0x0000 3FFF	BANK 0 (384K Bytes)
1	16k	0x0000 4000	0x0000 7FFF	
2	32k	0x0000 8000	0x0000 FFFF	
3	64k	0x0001 0000	0x0001 FFFF	
4	64k	0x0002 0000	0x0002 FFFF	
5	64k	0x0003 0000	0x0003 FFFF	
6	64k	0x0004 0000	0x0004 FFFF	
7	64k	0x0005 0000	0x0005 FFFF	
0	16k	0x0008 0000	0x0008 3FFF	BANK 1 (1) (64K Bytes)
1	16k	0x0008 4000	0x0008 7FFF	
2	16k	0x0008 8000	0x0008 BFFF	
3	16k	0x0008 C000	0x0008 FFFF	

(1) Bank 1 can be used as either EEPROM emulation space or as program space.

Table 2-9. TMS470MF03107 Flash Memory Banks and Sectors

SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS	MEMORY ARRAYS (OR BANKS)
0	16k	0x0000 0000	0x0000 3FFF	BANK 0 (256K Bytes)
1	16k	0x0000 4000	0x0000 7FFF	
2	32k	0x0000 8000	0x0000 FFFF	
3	64k	0x0001 0000	0x0001 FFFF	
4	64k	0x0002 0000	0x0002 FFFF	
5	64k	0x0003 0000	0x0003 FFFF	
0	16k	0x0008 0000	0x0008 3FFF	BANK 1 (1) (64K Bytes)
1	16k	0x0008 4000	0x0008 7FFF	
2	16k	0x0008 8000	0x0008 BFFF	
3	16k	0x0008 C000	0x0008 FFFF	

(1) Bank 1 can be used as either EEPROM emulation space or as program space.

2.2 Terminal Functions

The terminal functions table (Table 2-10) identifies the pin names, the associated pin numbers, input voltage, output voltage, whether the pin has any internal pullup/pulldown resistors and a functional pin description. The TMS470MF04207 and TMS470MF03107 devices have the same pin out.

Table 2-10. Terminal Functions

TERMINAL		INPUT VOLTAGE(1) (2)	OUTPUT CURRENT(3)	IPU/IPD(4)	DESCRIPTION
NAME	100 PIN				
HIGH-END TIMER (HET)					
HET[0]	39	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPD (100 µA)	Timer input capture or output compare. The HET[15:0] applicable pins can be programmed as general-purpose input/output (GIO) pins. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structure. The next higher odd HR pin structure is always implemented, even if the next higher odd HR pad and/or pin itself is not. **Note:** HET[15] is muxed with ECLK2 output. If ECLK2 output is enabled (through SYSPC1 register at 0xFFFFFF00), ECLK2 is output on this pin and HET[15] becomes an internal only HET channel. **Note:** ECLK2 source select must be programmed the same as ECLK1 due to device specific implementation details. **Note:** ECLK2 is enabled and ECLK2 divider is programmed through ECP control register 1 in System Frame 2 Registers (0xFFFFE128).
HET[1]	40				
HET[2]	49				
HET[3]	50				
HET[4]	53				
HET[5]	54				
HET[6]	55				
HET[7]	56				
HET[8]	57				
HET[9]	58				
HET[10]	59				
HET[11]	60				
HET[12]	61				
HET[13]	62				
HET[14]	63				
HET[15]/ECLK2	64				
CAN CONTROLLER 1 (DCAN1)					
CAN1STX	7	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	DCAN1 transmit pin or GIO pin.
CAN1SRX	8				DCAN1 receive pin or GIO pin.
CAN CONTROLLER 2 (DCAN2)					
CAN2STX	37	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	DCAN2 transmit pin or GIO pin
CAN2SRX	38				DCAN2 receive pin or GIO pin
GENERAL-PURPOSE I/O (GIO)					
GIOA[4]/INT[4]	5	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPD (100 µA)	General-purpose input/output pins. They are interrupt-capable pins.
GIOA[5]/INT[5]	6				
GIOA[6]/INT[6]	15				
GIOA[7]/INT[7]	16				

(1) PWR = power, GND = ground, REF = reference voltage, NC = no connect
(2) All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
(3) The TMS470M device utilizes adaptive impedance 4 mA buffers that default to an adaptive impedance mode of operation. As a fail-safe, the adaptive impedance features of the buffer may be disabled and revert the buffer to a standard buffer mode.
(4) IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are inactive on input pins when $\overline{\text{PORRST}}$ is asserted)

Table 2-10. Terminal Functions (continued)

TERMINAL		INPUT VOLTAGE(1) (2)	OUTPUT CURRENT(3)	IPU/IPD(4)	DESCRIPTION
NAME	100 PIN				
MULTI-BUFFERED SERIAL PERIPHERAL INTERFACE 1 (MIBSPI1)					
MIBSPI1CLK	34	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	MIBSPI1 clock. MIBSPI1CLK can be programmed as a GIO pin.
$\overline{\text{MIBSPI1SCS[0]}}$	33				MIBSPI1 slave chip select. $\overline{\text{MIBSPI1SCS[7:0]}}$ can be programmed as a GIO pins.
$\overline{\text{MIBSPI1SCS[1]}}$	32				
$\overline{\text{MIBSPI1SCS[2]}}$	31				
$\overline{\text{MIBSPI1SCS[3]}}$	30				
$\overline{\text{MIBSPI1SCS[4]}}$	29				
$\overline{\text{MIBSPI1SCS[5]}}$	28				
$\overline{\text{MIBSPI1SCS[6]}}$	27				
$\overline{\text{MIBSPI1SCS[7]}}$	26				
MIBSPI1SIMO	35				MIBSPI1 data stream. Slave in/master out. MIBSPI1SIMO can be programmed as a GIO pin.
MIBSPI1SOMI	36				MIBSPI1 data stream. Slave out/master in. MIBSPI1SOMI can be programmed as a GIO pin.
MULTI-BUFFERED SERIAL PERIPHERAL INTERFACE 2 (MibSPI2)					
MibSPI2CLK	17	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	MibSPI2 clock. MibSPI2CLK can be programmed as a GIO pin.
$\overline{\text{MibSPI2SCS[0]}}$	1				MibSPI2 slave chip select $\overline{\text{MibSPI2SCS[3:0]}}$ can be programmed as GIO pins.
$\overline{\text{MibSPI2SCS[1]}}$	2				
$\overline{\text{MibSPI2SCS[2]}}$	3				
$\overline{\text{MibSPI2SCS[3]}}$	4				
$\overline{\text{MibSPI2ENA}}$	90				MibSPI2 enable pin. $\overline{\text{MibSPI2ENA}}$ can be programmed as a GIO pin.
MibSPI2SIMO[0]	18				MibSPI2 data stream. Slave in/master out. MibSPI2SIMO pins can be programmed as a GIO pins.
MibSPI2SOMI[0]	19				MibSPI2 data stream. Slave out/master in. MibSPI2SOMI pins can be programmed as GIO pins.
LOCAL INTERCONNECT NETWORK/SERIAL COMMUNICATIONS INTERFACE (LIN/SCI)					
LIN/SCI1RX	23	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	LIN/SCI1 data receive. Can be programmed as a GIO pin.
LIN/SCI1TX	22				LIN/SCI1 data transmit. Can be programmed as a GIO pin.
LIN/SCI2RX	25	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	LIN/SCI2 data receive. Can be programmed as a GIO pin.
LIN/SCI2TX	24				LIN/SCI2 data transmit. Can be programmed as a GIO pin.
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MIBADC)					
ADEVT	68	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPD (100 µA)	MibADC event input. Can be programmed as a GIO pin.

Table 2-10. Terminal Functions (continued)

TERMINAL		INPUT VOLTAGE(1) (2)	OUTPUT CURRENT(3)	IPU/IPD(4)	DESCRIPTION
NAME	100 PIN				
ADIN[0]	69	3.3 V			MibADC analog input pins.
ADIN[1]	70				
ADIN[2]	71				
ADIN[3]	72				
ADIN[4]	73				
ADIN[5]	74				
ADIN[6]	75				
ADIN[7]	76				
ADIN[8]	77				
ADIN[9]	78				
ADIN[10]	79				
ADIN[11]	80				
ADIN[12]	81				
ADIN[13]	86				
ADIN[14]	87				
ADIN[15]	88				
AD_{REFHI}	82	3.3-V REF			MibADC module high-voltage reference input.
AD_{REFLO}	83	GND REF			MibADC module low-voltage reference input.
V_{CCAD}	85	3.3-V PWR			MibADC analog supply voltage.
V_{SSAD}	84	GND			MibADC analog ground reference.
OSCILLATOR (OSC)					
OSCIN	10	1.55-V I			Crystal connection pin or external clock input.
OSCOUT	11	1.55-V O			External crystal connection pin.
SYSTEM MODULE (SYS)					
$\overline{PORRST}$	89	3.3-V I		IPD (100 µA)	Input master chip power-up reset. External V_{CC} monitor circuitry must assert a power-on reset.
$\overline{RST}$	98	3.3-V I/O	Adaptive impedance 4 mA	IPU (100 µA)	Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On this pin, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to this pin.
ECLK	96	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPD (100 µA)	Bidirectional pin. ECLK can be programmed as a GIO pin.
TEST/DEBUG (T/D)					
TCK	44	3.3-V I		IPD (100 µA)	Test clock. TCK controls the test hardware (JTAG).
TDI	46	3.3-V I/O	Adaptive impedance 4 mA	IPU (100 µA)	Test data in pin. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG).
TDO	45			IPD (100 µA)	Test data out pin. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG).
TMS	47			IPU (100 µA)	Serial input pin for controlling the state of the CPU test access port (TAP) controller (JTAG).
$\overline{TRST}$	48	3.3-V I		IPD (100 µA)	Test hardware reset to TAP. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic.

Table 2-10. Terminal Functions (continued)

TERMINAL		INPUT VOLTAGE[1] [2]	OUTPUT CURRENT[3]	IPU/IPD[4]	DESCRIPTION
NAME	100 PIN				
TEST	97	3.3-V I		IPD (100 µA)	Test enable. Reserved for internal use only. TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.
$\overline{ENZ}$	91	3.3-V I		IPD (100 µA)	Enables/disables the internal voltage regulator. 0V - Enables internal voltage regulator. 3.3V-Disables internal voltage regulator. **Note: The ENZ pin is provided to facilitate testing across the core voltage range and is not intended for disabling the on chip voltage regulator during application use.**
FLASH					
FLTP1	99				Flash Test Pad 1 pin. **For proper operation, this pin must connect only to a test pad or not be connected at all [no connect (NC)]. The test pad must not be exposed in the final product where it might be subjected to an ESD event.**
V_{CCP1}	95	3.3-V PWR			Flash external pump voltage (3.3 V). This pin is required for both Flash read and Flash program and erase operations. **V_{CCP1} and V_{CCP2} are double bonded to the same pin.**
V_{CCP2}	95				
SUPPLY VOLTAGE CORE (1.55 V)					
V_{CC}	12	1.55-V PWR			Vreg output voltage when Vreg is enabled. V_{CC} input when Vreg is disabled.
	41				
	67				
	92				
SUPPLY VOLTAGE DIGITAL I/O AND REGULATOR (3.3 V)					
V_{CCIOR}	14	3.3-V PWR			Digital I/O and internal regulator supply voltage.
	20				
	43				
	52				
	65				
	94				
SUPPLY GROUND					
V_{SS}	9	GND			Digital I/O and core supply ground reference.
	13				
	21				
	42				
	51				
	66				
	93				
	100				

2.3 Device Support

2.3.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices and support tools. Each commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g.,TMS470MF04207). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

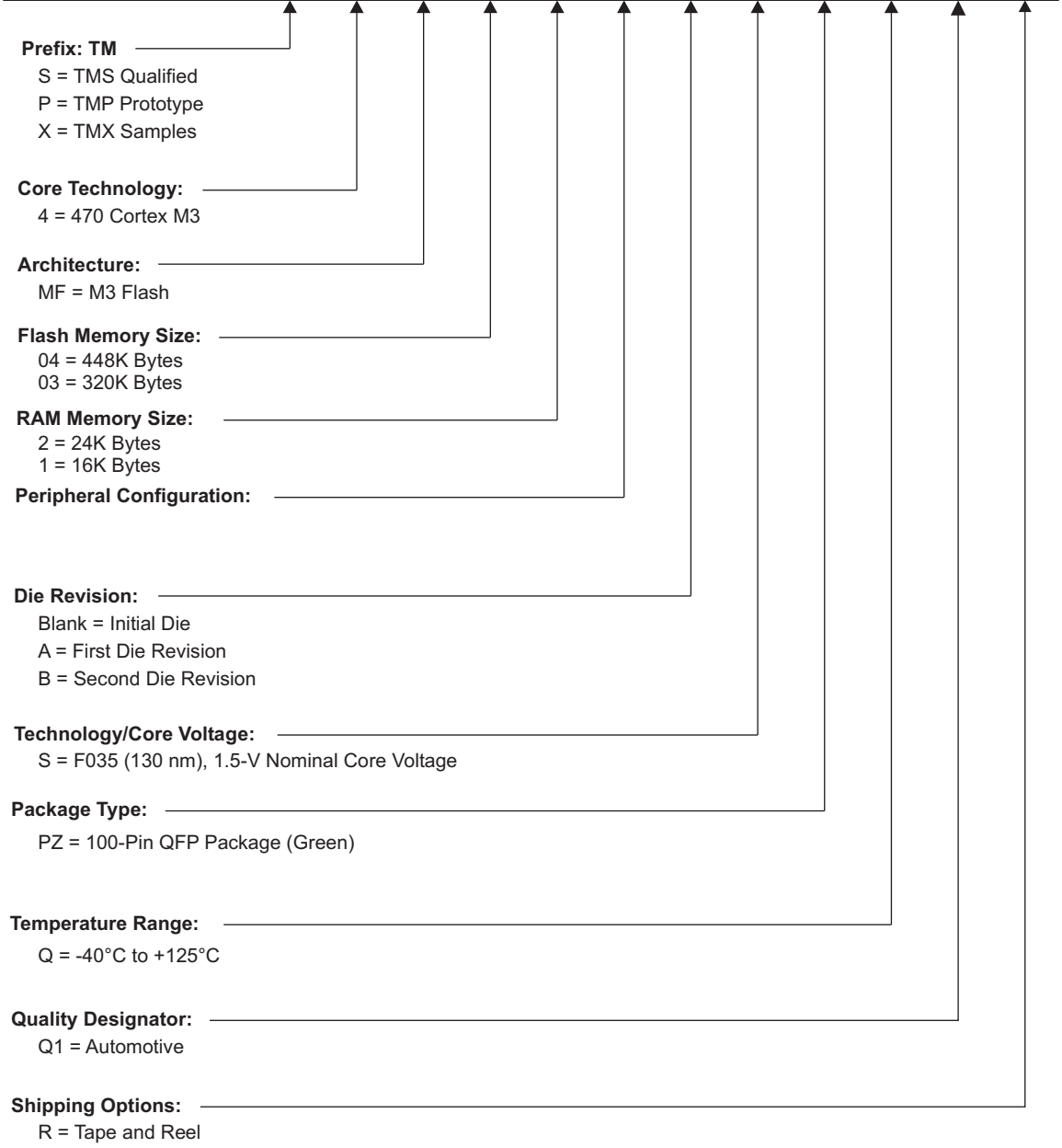
TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZ), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz.

Figure 2-3 illustrates the numbering and symbol nomenclature for the TMS470M family.

Full Part Number	TMS	470	MF	04	2	07	B	S	PZ	Q	Q1	R
Orderable Part Number	S	4	MF	04	2	07	B	S	PZ	Q	Q1	R



NOTE: The part number given above is for illustrative purposes only and does not necessarily represent the specific part number or silicon revision to which this document applies.

Figure 2-3. TMS470M Device Numbering Conventions

3 Device Configurations

3.1 Reset/Abort Sources

Resets/aborts are handled as shown in Table 3-1.

Table 3-1. Reset/Abort Sources

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP, GROUP.CHANNEL
1) CPU TRANSACTIONS			
Precise write error (NCNB/Strongly Ordered)	User/Privilege	Precise Abort (CPU)	n/a
Precise read error (NCB/Device or Normal)	User/Privilege	Precise Abort (CPU)	n/a
Imprecise write error (NCB/Device or Normal)	User/Privilege	Imprecise Abort (CPU)	n/a
External imprecise error (Illegal transaction with ok response)	User/Privilege	ESM	2.17
Illegal instruction	User/Privilege	Undefined Instruction Trap (CPU)(1)	n/a
M3 Lockup	User/Privilege	ESM => NMI	2.16
MPU access violation	User/Privilege	Abort (CPU)	n/a
2) SRAM			
ECC single error (correctable)	User/Privilege	ESM	1.26
ECC double error (uncorrectable)	User/Privilege	ESM => NMI	2.6
3) FLASH WITH ECC			
ECC single error (correctable)	User/Privilege	ESM	1.6
ECC double error (uncorrectable)	User/Privilege	ESM => NMI	2.4
8) HET			
HET Memory parity error	User/Privilege	ESM	1.7
9) MIBSPI			
MibSPI1 memory parity error	User/Privilege	ESM	1.17
MibSPI2 memory parity error	User/Privilege	ESM	1.18
10) MIBADC			
Memory parity error	User/Privilege	ESM	1.19
11) DCAN/CAN			
DCAN1 memory parity error	User/Privilege	ESM	1.21
DCAN2 memory parity error	User/Privilege	ESM	1.23
13) PLL			
PLL slip error	User/Privilege	ESM	1.10
14) CLOCK MONITOR			
Clock monitor interrupt	User/Privilege	ESM	1.11
19) VOLTAGE REGULATOR			
Vcc out of range	n/a	Reset	n/a
20) CPU SELFTEST (LBIST)			
CPU Selftest (LogicBIST) error	User/Privilege	ESM	1.27
21) ERRORS REFLECTED IN THE SYSESR REGISTER			
Power-Up Reset/Vreg out of voltage(2)	n/a	Reset	n/a

(1) The undefined instruction trap is NOT detected outside of the CPU. The trap is taken only if the code reaches the execute stage of the CPU.
(2) Both a power-on reset and Vreg out-of-range reset are indicated by the PORST bit in the SYSESR register.

Table 3-1. Reset/Abort Sources (continued)

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP, GROUP.CHANNEL
Oscillator fail / PLL slip(3)	n/a	Reset	n/a
M3 Lockup/LRM	n/a	Reset	n/a
Watchdog time limit exceeded	n/a	Reset	n/a
CPU Reset	n/a	Reset	n/a
Software Reset	n/a	Reset	n/a
External Reset	n/a	Reset	n/a

(3) Oscillator fail/PLL slip can be configured in the system register (SYS.PLLCTL1) to generate a reset.

3.2 Lockup Reset Module

The lockup reset module (LRM) is implemented to communicate a lockup condition by the core. The LRM provides a small watchdog timer which can generate a system reset in case a lockup condition that is identified by the core cannot be cleared by software.

3.3 ESM Assignments

The ESM module is intended for the communication critical system failures in a central location. The error indication is by an error interrupt when the failure is recognized from any detection unit. The ESM module consist of three error groups with 32 inputs each. The generation of the interrupts is shown in Table 3-2. ESM assignments are listed in Table 3-3.

Table 3-2. ESM Groups

ERROR GROUP	INTERRUPT, LEVEL
Group1	maskable, low/high
Group2	non-maskable, high
Group3	Not Used

Table 3-3. ESM Assignments

ERROR SOURCES	CHANNEL
GROUP 1	
Reserved	0 - 5
Flash - ECC Single Bit	6
HET memory parity error	7
Reserved	8-9
PLL Slip Error	10
Clock Monitor interrupt	11
Reserved	12-16
MibSPI1 memory parity error	17
MibSPI2 memory parity error	18
MibADC memory parity error	19
Reserved	20
DCAN1 memory parity error	21
Reserved	22
DCAN2 memory parity error	23
Reserved	24-25
SRAM - single bit	26
CPU LBIST - selftest error	27

Table 3-3. ESM Assignments (continued)

ERROR SOURCES	CHANNEL
Reserved	28-31
GROUP 2	
Reserved	0-3
Flash - Double-Bit Error (uncorrectable)	4
Reserved	5
SRAM - Double-Bit Error (uncorrectable)	6
Reserved	7-15
M3 Lockup	16
M3 External Imprecise Abort	17
Reserved	18-31

3.4 Interrupt Priority (M3VIM)

The TMS470M platform interrupt architecture includes a vectored interrupt manager (M3VIM) that provides hardware assistance for prioritizing and controlling the many interrupt sources present on a device. Table 3-4 communicates the default interrupt request assignments.

Table 3-4. Interrupt Request Assignments

MODULES	INTERRUPT SOURCES	DEFAULT VIM INTERRUPT REQUEST
ESM	ESM High level interrupt (NMI)	0
Reserved	(NMI)	1
ESM	ESM Low level interrupt	2
SYSTEM	Software interrupt (SSI)	3
RTI	RTI compare interrupt 0	4
RTI	RTI compare interrupt 1	5
RTI	RTI compare interrupt 2	6
RTI	RTI compare interrupt 3	7
RTI	RTI overflow interrupt 0	8
RTI	RTI overflow interrupt 1	9
Reserved	Reserved	10
GIO	GIO Interrupt A	11
GIO	GIO Interrupt B	12
HET	HET level 0 interrupt	13
HET	HET level 1 interrupt	14
MibSPI1	MibSPI1 level 0 interrupt	15
MibSPI1	MibSPI1 level 1 interrupt	16
Reserved	Reserved	17
LIN/SCI2	LIN/SCI2 level 0 interrupt	18
LIN/SCI2	LIN/SCI2 level 1 Interrupt	19
LIN/SCI1	LIN/SCI1 level 0 interrupt	20
LIN/SCI1	LIN/SCI1 level 1 Interrupt	21
DCAN1	DCAN1 level 0 Interrupt	22
DCAN1	DCAN1 level 1 Interrupt	23
ADC	ADC event group interrupt	24
ADC	ADC sw group 1 interrupt	25
ADC	ADC sw group 2 interrupt	26

Table 3-4. Interrupt Request Assignments (continued)

MODULES	INTERRUPT SOURCES	DEFAULT VIM INTERRUPT REQUEST
MibSPI2	MibSPI2 level 0 interrupt	27
MibSPI2	MibSPI2 level 1 interrupt	28
DCAN2	DCAN2 level 0 interrupt	29
DCAN2	DCAN2 level 1 interrupt	30
ADC	ADC magnitude threshold interrupt	31
Reserved	Reserved	32
Reserved	Reserved	33
DCAN1	DCAN1 IF3 interrupt	34
DCAN2	DCAN2 IF3 interrupt	35
Reserved	Reserved	36-47

3.5 MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The TMS470M MibADC module stores its digital results in one of three FIFO buffers. There is one FIFO buffer for each conversion group [event, group1 (G1), and group2 (G2)], and the total MibADC FIFO on the device is divided amongst these three regions. The size of the individual group buffers are software programmable. MibADC buffers can be serviced by interrupts.

3.5.1 MibADC Event Triggers

All three conversion groups can be configured for event-triggered operation, providing up to three event-triggered groups.

The trigger source and polarity can be selected individually for group 1, group 2 and the event group from the options identified in Table 3-5.

Table 3-5. MibADC Event Hookup Configuration

EVENT NO.	SOURCE SELECT BITS for G1 or EVENT (G1SRC[2:0] or EVSRC[2:0])	SIGNAL PIN NAME
1	000	ADEVT
2	001	HET[1]
3	010	HET[3]
4	011	HET[16](1)
5	100	HET[18](1)
6	101	HET[24](1)
7	110	HET[26](1)
8	111	HET[28](1)

(1) These channels are available as internal signals even if they are not included as pins (节 1.1).

3.6 MibSPI

The multi-buffered serial peripheral interface module allows CPU independent SPI communications with system peripherals.

The MibSPI1 module can support up to 16 transfer groups and 8 chip selects. In addition, up to 4 data formats can be supported allowing assignment of various formats to each transfer group.

The MibSPI2 module can support up to 8 transfer groups, 4 chip selects, and up to 4 data formats.

3.6.1 MibSPI Event Trigger

The MibSPI module has the ability to automatically trigger SPI events based on internal and external event triggers.

The trigger sources can be selected individually for each transfer group from the options identified in Table 3-6.

Table 3-6. MibSPI1 and MibSPI2 Event Hookup Configuration

EVENT NO.	SOURCE SELECT BITS FOR MIBSPI EVENTS TGXCTRL TRIGSRC[3:0]	SIGNAL PIN NAME
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0](1)
EVENT1	0010	GIOA[1](1)
EVENT2	0011	GIOA[2](1)
EVENT3	0100	GIOA[3](1)
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	HET[20](1)
EVENT7	1000	HET[21](1)
EVENT8	1001	HET[22](1)

(1) These channels are available as internal signals even if they are not included as pins (节 1.1).

Table 3-6. MibSPI1 and MibSPI2 Event Hookup Configuration (continued)

EVENT NO.	SOURCE SELECT BITS FOR MIBSPI EVENTS TGXCTRL TRIGSRC[3:0]	SIGNAL PIN NAME
EVENT9	1010	HET[23](1)
EVENT10	1011	HET[28](1)
EVENT11	1100	HET[29](1)
EVENT12	1101	HET[30](1)
EVENT13	1110	HET[31](1)
EVENT14	1111	Internal Tick Counter

3.7 JTAG ID

The 32-bit JTAG ID code for this device is 0x0B8D802F.

3.8 Scan Chains

The device contains an ICEPICK module to access the debug scan chains; see Figure 3-1. Debug scan chain #0 handles the access to the CPU. The ICEPICK scan ID is 0x00366D05, which is the same as the device ID.

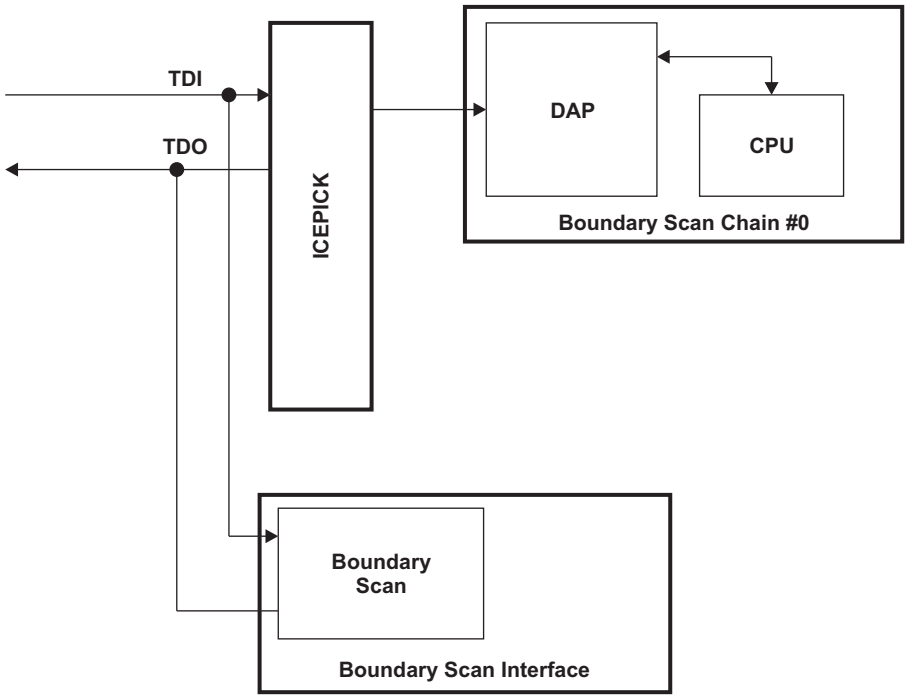


Figure 3-1. Debug Scan Chains

3.9 Adaptive Impedance 4 mA IO Buffer

The adaptive impedance 4 mA buffer is a buffer that has been explicitly designed to address the issue of decoupling EMI sources from the pins which they drive. This is accomplished by adaptively controlling the impedance of the output buffer and should be particularly effective with capacitive loads.

The adaptive impedance 4 mA buffer features two modes of operation: Impedance Control Mode, and Low-Power Mode/Standard Buffer Mode as defined below:

- **Impedance Control Mode** is enabled in the design by default. This mode adaptively controls the impedance of the output buffer.

- **Standard Buffer Mode** is used to configure the buffer back into a generic configuration. This buffer mode is used when it is necessary to drive the output at very high speeds, or when EMI reduction is not a concern.

Table 3-7. Adaptive Impedance 4 mA Buffer Mode Availability

MODULE OR PIN NAME	STANDARD BUFFER ENABLE (SBEN)(1)
SYS.ECLK	GPREG1.0
SYS.nRST	GPREG1.1
SYS.TDI/TDO	Standard Buffer Enabled
SYS.TMSC	Standard Buffer Enabled
HET	GPREG1.2
SCI1	GPREG1.3
LIN/SCI2	GPREG1.4
MIBSPI1	GPREG1.5
MibSPI2	GPREG1.6
Reserved	GPREG1.7
MIBADC.ADEVT	GPREG1.8
DCAN1	GPREG1.9
DCAN2	GPREG1.10
GIOA	GPREG1.11

(1) SBEN configuration can be achieved using the GPREG register within the system frame(0xFFFFFFA0).

3.9.1 Standard Buffer Enable Register (GPREG1)

A general purpose register with the system frame has been utilized to control the enabling of standard buffer mode. This register is shown in Figure 3-2 and described in Table 3-8

NOTE

In general, all device registers are defined within the TRM (SPNU450); however, in cases where the register definition is device specific, the register is defined within the device specific datasheet.

31							16
Reserved							
R-0							

15			12	11	10	9	8
Reserved				GIOA_SBEN	DCAN2_SBEN	DCAN1_SBEN	ADC.ADEVT_SBEN
R-0				RW-0	RW-0	RW-0	RW-0

7	6	5	4	3	2	1	0
Reserved	MibSPI2_SBEN	MIBSPI1_SBEN	LIN2SCI2_SBEN	LIN1SCI1_SBEN	HET_SBEN	$\overline{\text{RST}}$_SBEN	ECLK_SBEN
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-2. General-Purpose Register 1 (GPREG1)

Table 3-8. General-Purpose Register 1 (GPREG1) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved		These bits are reserved. Reads return 0 and writes have no effect.
11	GIOA_SBEN		GIOA port standard buffer enable bit. This bit enables/disables standard buffer mode for all GIOA pins
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
10	DCAN2_SBEN		DCAN2 standard buffer enable bit. This bit enables/disables standard buffer mode for all DCAN2 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
9	DCAN1_SBEN		DCAN1 standard buffer enable bit. This bit enables/disables standard buffer mode for all DCAN1 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
8	ADC.ADEVT_SBEN		ADC.ADEVT standard buffer enable bit. This bit enables/disables standard buffer mode for the ADC.ADEVT pin.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for the ADEVT pin.
7	Reserved		These bits are reserved. Reads return 0 and writes have no effect.
6	MibSPI2_SBEN		MibSPI2 standard buffer enable bit. This bit enables/disables standard buffer mode for all MibSPI2 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
5	MIBSPI1		MIBSPI1 standard buffer enable bit. This bit enables/disables standard buffer mode for all MIBSPI1 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.

Table 3-8. General-Purpose Register 1 (GPREG1) Field Descriptions (continued)

Bit	Field	Value	Description
4	LIN2SCI2_SBEN		LIN/SCI2 standard buffer enable bit. This bit enables/disables standard buffer mode for all LIN/SCI2 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
3	LIN1SCI1_SBEN		LIN/SCI1 standard buffer enable bit. This bit enables/disables standard buffer mode for all LIN/SCI1 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
2	HET_SBEN		HET standard buffer enable bit. This bit enables/disables standard buffer mode for all HET pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
1	$\overline{\text{RST}}$_SBEN		$\overline{\text{RST}}$ standard buffer enable bit. This bit enables/disables standard buffer mode for the $\overline{\text{RST}}$ pin.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for the $\overline{\text{RST}}$ pin.
0	ECLK_SBEN		ECLK standard buffer enable bit. This bit enables/disables standard buffer mode for the ECLK pin.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for the ECLK pin.

3.9.2 Coresight Components/Debug ROM

Coresight registers are memory-mapped and accessible via the CPU and JTAG.

Table 3-9. Debug Component Memory Map

COMPONENT	FRAME START ADDRESS	FRAME END ADDRESS	FRAME SIZE	MEMORY TYPE
M3 INTEGRATION FRAME				
DWT	0xE000_1000	0xE000_1FFF	4K	Control Registers for debug and trace modules
FPB	0xE000_2000	0xE000_2FFF	4K	
NVIC	0xE000_E000	0xE000_EFFF	4K	
Debug ROM 1	0xE00F_F000	0xE00F_FFFF	4K	

Table 3-10. Debug ROM contents for Debug ROM 1 (M3 ROM)

ADDRESS OFFSET see Table 3-9	DESCRIPTION	VALUE
0x000	NVIC	0xFFF0_F003
0x004	DWT	0xFFF0_2003
0x008	FPB	0xFFF0_3003
0x00C	ITM	0xFFF0_1003
0x010	TPIU(1)	0xFFF4_1002
0x014	ETM(1)	0xFFF4_2002
0x018	End of Table	0x0000_0000

(1) Cortex™-M3 debug ROM always will have entries for optional components TPIU and ETM. Whether or not these components are present is determined by bit number 0 of the entry value.

3.10 Built-In Self Test (BIST) Features

3.10.1 STC/LBIST

The TMS470M family supports a logic built-in self test (LBIST or CPUBIST) of the M3 CPU.

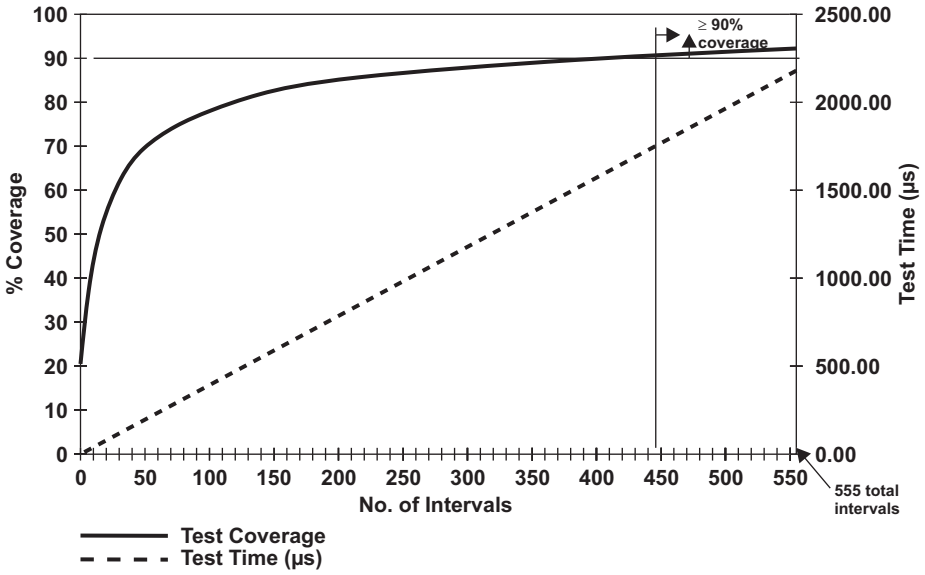
LBIST testing can be performed in two modes of operation:

- **Full Execution.** In this mode, the full suite of test patterns is run without interruption. This test is started via CPU control and is well suited for use at device start up.
- **Cyclic Execution.** During cyclic execution, a small percentage of time will be dedicated to running a subset of the self-test (STC Intervals). This mode is well suited for executing on a periodic basis to minimize the bandwidth use. After all STC intervals are executed, all test patterns will have been run.

NOTE

1. The application will need to disable peripherals and or interrupts to avoid missing interrupts.
2. No debugger interaction is possible with the CPU during self test. This includes access to memory and registers since access is through the CPU.

The default value of the LBIST clock prescaler (STCDIV) is *divide-by-1* and the device will support STC frequencies up to and including HCLK frequency. In order to minimize the current consumption during LBIST execution, the LBIST clock prescalar (STCDIV) may be configured to reduce the LBIST frequency.



A. A single LBIST interval is 158 STC CLK cycles in duration, excluding clock transition timing of 20 cycles.
B. This device has 555 total intervals.

Figure 3-3. CPU BIST Intervals vs Coverage

3.10.2 MBIST

The TMS470M supports memory built-in self test (MBIST) of the SRAM. The MBIST is accessible via the application in order to facilitate memory self test by the application by enabling the MBIST controllers associated with the specific RAMs to be tested. (For device-specific MBIST controller assignments, see Table 2-4.)

The MBIST controller:

- Supports testing of all system and peripheral RAM.
- Captures the MBIST results in the MBIST status register (MSTFAIL).
- Supports execution of each Memory BIST controller in parallel (MSINENA).
  For MSIENA bit assignments, see Table 2-4
- Supports execution of each Memory BIST controller individually (MSINENA).
  For MSIENA bit assignments, see Table 2-4

The MBIST controller selection is mapped to the MBIST controller/memory initialization enable register (MSIENA) within the SYS register frame. Each MBIST controller is enabled by setting the corresponding bit within this register and then enabling memory self-test via the memory self-test global enable within the global control register (MSTGCR.MSTGENA[3:0]).

The MBIST controllers support execution of the following tests:

Table 3-11. MBIST Algorithms and Cycle Counts(1)

Module	Algorithm (Cycle Counts)					
	Checker Board	March13N Background 0	March11N Background A	March13N Background 3/0F/69	PMOS Open Address Decode	ROM2
ADC RAM	1427	1555	1089	4033	4225	-
DCAN RAM	1503	1503	1057	3745	3265	-
SRAM	26835	26835	22529	79873	147457	-
HET RAM	7539	8307	6529	24193	29185	-
MibSPI RAM	3583	3583	2817	9985	10753	-
STC ROM	-	-	-	-	-	18433

(1) Cycle times provided are for the execution of the specific algorithms and do not include overhead from the BIST statemachine.

NOTE

The algorithm to be applied is selectable via the memory self-test global control register algo selection field (MSTGCR.MBIST_ALGSEL[7:0]).

3.11 Device Identification Code Register

The device identification code register identifies the coprocessor status, an assigned device-specific part number, the technology family (TF), the I/O voltage, whether or not parity is supported, the levels of flash and RAM error detection, and the device version. The TMS470M device identification code base register value is 0X00366D05 and is subject to change based on the silicon version.

31	30	17	16
CP15	PART NUMBER		TF
R-0	R-00000000011011		R-0

15	13	12	11	10	9	8
TF		I/O VOLT	PP	FLASHECC		RAMECC
R-011		R-0	R-1	R-10		R-1

7	3	2	1	0
VERSION		1	0	1
R-0000		R-1	R-0	R-1

LEGEND: R = Read only; -*n* = value after reset

Figure 3-4. TMS470 Device ID Bit Allocation Register

Table 3-12. TMS470 Device ID Bit Allocation Register Field Descriptions

Bit	Field	Value	Description
31	CP15		This bit indicates the presence of coprocessor (CP15).
		0	No coprocessor present in the device.
		1	Coprocessor present in the device.
30-17	PART NUMBER		These bits indicate the assigned device-specific part number. The assigned device-specific part number for the TMS470M device is 00000000011011.
16-13	TF		Technology family bit. These bits indicate the technology family (C05, F05, F035, C035).
		0011	F035
12	I/O VOLT		I/O voltage bit. This bit identifies the I/O power supply.
		0	3.3 V
		1	5 V
11	PP		Peripheral parity bit. This bit indicates whether parity is supported.
		0	No parity on peripheral.
		1	Parity on peripheral.
10	FLASHECC		Flash ECC bits. These bits indicate the level of error detection and correction on the flash memory.
		00	No error detection/correction.
		01	Program memory with parity.
		10	Program memory with ECC.
		11	Reserved
8	RAMECC		RAM ECC bits. This bit indicates the presence of error detection and correction on the CPU RAM.
		0	RAM ECC not present.
		1	RAM ECC present.
7-3	VERSION		These bits identify the silicon version of the device.
2-0	101		Bits 2:0 are set to 101 by default to indicate a platform device.

3.12 Device Part Numbers

Table 3-13 lists all the available TMS470MF04207/TMS470MF03107 device configurations.

Table 3-13. Device Part Numbers

DEVICE PART NUMBER	SAP PART NUMBER	PROGRAM MEMORY	PACKAGE TYPE	TEMPERATURE RANGE	PbFREE/ GREEN(1)
		FLASH EEPROM	100-PIN LQFP	-40°C to 125°C	
TMS470MF04207PZQ	S4MF04207SPZQQ1	X	X	X	X
TMS470MF03107PZQ	S4MF03107SPZQQ1	X	X	X	X

(1) RoHS compliant products are compatible with the current RoHS requirements for all six substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials, unless exempt. Pb-Free products are RoHS Compliant, plus suitable for use in higher temperature lead-free solder processes (typically 245 to 260°C). Green products are RoHS and Pb-Free, plus also free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

4 Device Operating Conditions

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range, Q Version(1)

Supply voltage range:	V_{CC} (2)	-0.5 V to 2.1 V
	V_{CCIOR}, V_{CCAD}, V_{CC} (Flash pump) (2)	-0.5 V to 4.1 V
Input voltage range:	All input pins	-0.5 V to 4.1 V
Input clamp current:	I_{IK} (V_I < 0 or V_I > V_{CCIOR}) All pins, except ADIN[0:15]	±20 mA
	I_{IK} (V_I < 0 or V_I > V_{CCIOR}) ADIN[0:15]	±10 mA
Operating free-air temperature range, T_A:	Q version	-40°C to 125°C
Operating junction temperature range, T_J:	Standard	-40°C to 150°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to their associated grounds.

4.2 Device Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
V_{CCIOR}	Digital I/O and internal regulator supply voltage		3	3.3	3.6	V
V_{CC}	Voltage regulator output voltage		1.40	1.55	1.70	V
V_{CCAD}	MibADC supply voltage		3	3.3	3.6	V
V_{CCP}	Flash pump supply voltage		3	3.3	3.6	V
V_{SS}	Digital logic supply ground			0		V
V_{SSAD}	MibADC supply ground		-0.1		0.1	V
T_A	Operating free-air temperature	Q version	-40		125	°C
T_J	Operating junction temperature		-40		150	°C

(1) All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}.

4.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, Q Version[1][2]

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis			150			mV
V_{IL}	Low-level input voltage	All inputs[3]		-0.3		0.8	V
		OSCIN				0.2 V_{CC}	V
V_{IH}	High-level input voltage	All inputs[3]		2		V_{CCIOR} + 0.3	V
		OSCIN		0.8 V_{CC}			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.2 V_{CCIOR}	V
			I_{OL} = 50 µA Standard mode			0.2	
			I_{OL} = 50 µA Impedance Control mode			0.2 V_{CCIOR}	
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MAX	0.8 V_{CCIOR}			V
			I_{OH} = 50 µA Standard mode	V_{CCIOR} -0.2			
			I_{OH} = 50 µA Impedance Control mode	0.8 V_{CCIOR}			
I_{IC}	Input clamp current (I/O pins)[4]		V_I < V_{SSIO} - 0.3 or V_I > V_{CCIOR} + 0.3	-2		2	mA
I_I	Input current (I/O pins)	I_{IH} Pulldown	V_I = V_{CCIOR}	40		190	µA
		I_{IL} Pullup	V_I = V_{SS}	-190		-40	
		All other pins	No pullup or pulldown	-1		1	
I_{OL}	Low-level output tcurrent	Adaptive impedance 4 mA Buffer	V_{OL} = V_{OL} MAX			4	mA
I_{OH}	High-level output current	Adaptive impedance 4 mA Buffer	V_{OH} = V_{OH} MIN	-4			mA
I_{CC}	V_{CC} digital supply current (operating mode, internal regulator disabled)		HCLK = 80 MHz, VCLK = 80 MHz, V_{CC} = 1.70 V[5]			110	mA
I_{CCIOR}	V_{CCIOR} IO and digital supply current (operating mode, internal regulator enabled)		HCLK = 80 MHz, VCLK = 80 MHz, No DC load, V_{CCIOR} = 3.6 V[5][6]			115	mA
	V_{CCIOR} IO and digital supply current (LBIST execution, internal regulator enabled)[7]		HCLK = 80 MHz, VCLK = 80 MHz, STCCLK = 80 MHz, No DC load, V_{CCIOR} = 3.6 V[6]			155	
	V_{CCIOR} IO and digital supply current (MBIST execution, internal regulator enabled)[8]		HCLK = 80 MHz, VCLK = 80 MHz, No DC load, V_{CCIOR} = 3.6 V[6]			130	

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) "All frequencies" will include all specified device configuration frequencies.
(3) The V_{IL} here does not apply to the OSCIN, OSCOUT and $\overline{\text{PORRST}}$ pins; the V_{IH} here does not apply to the OSCIN, OSCOUT and $\overline{\text{RST}}$ pins; For $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ exceptions, see Section 5.1.
(4) Parameter does not apply to input-only or output-only pins.
(5) Maximum currents are measured using a system-level test case. This test case exercises all of the device peripherals concurrently (excluding MBIST and STC LBIST).
(6) I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} - 0.2 V. ECLK output ≤ 2 MHz.
(7) LBIST current specified is peak current for the maximum supported operating clock (HCLK = 80 MHz) and STC CLK = HCLK. Lower current consumption can be achieved by configuring a slower STC Clock frequency. The current peak duration can last for the duration of 1 LBIST test interval.
(8) MBIST currents specified are for execution of MBIST on all RAMs in parallel. Lower current consumption can be achieved by sequenced execution of MBIST on each of the RAM spaces available.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, Q Version[1][2] *(continued)*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCAD}	V_{CCAD} supply current (operating mode)	All frequencies, V_{CCAD} = 3.6 V			8	mA
I_{CCP}	V_{CCP} pump supply current	V_{CCP} = 3.6 V read operation[5]			10	mA
		V_{CCP} = 3.6 V program[9]			75	
		V_{CCP} = 3.6 V erase			75	
$I_{CCTOTAL}$ (10)	V_{CCIOR} + V_{CCAD} + V_{CCP} total digital supply current (operating mode, internal regulator enabled)	HCLK = 80 MHz, VCLK = 80 MHz, No DC load, V_{CCIOR} = 3.6 V[5][6]			125	mA
C_I	Input capacitance		6			pF
C_O	Output capacitance		7			pF

(9) Assumes reading from one bank while programming a different bank.
(10) Total device operating current is derived from the total I_{CCIOR}, I_{CCAD}, and I_{CCP} in normal operating mode excluding MBIST and LBIST execution. It is expected that the total will be less than the sums of the values of the individual components due to statistical calculations involved in producing the specification values.

5 Peripheral Information and Electrical Specifications

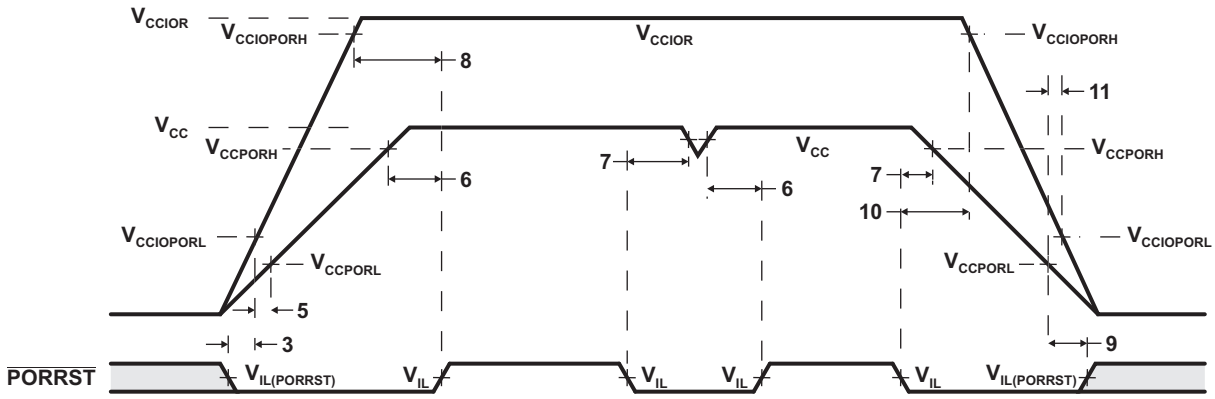
5.1 $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ Timings

Table 5-1. Timing Requirements for $\overline{\text{PORRST}}$[1]

(see Figure 5-1)

NO.			MIN	MAX	UNIT
	V_{CCPORL}	V_{CC} low supply level when $\overline{\text{RST}}$ becomes active	1.30		V
	V_{CCPORH}	V_{CC} high supply level when $\overline{\text{RST}}$ becomes active		1.80	V
	$V_{CCIOPORL}$	V_{CCIO} low supply level when $\overline{\text{PORRST}}$ must be active during power up		1.1	V
	$V_{CCIOPORH}$	V_{CCIO} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	3.0		V
	V_{IL} (2)	Low-level input voltage after V_{CCIOR} > $V_{CCIOPORH}$		0.2 V_{CCIOR}	V
	V_{OH} (3)	High-level output voltage after V_{CCIOR} > $V_{CCIOPORH}$	0.8 V_{CCIOR}		V
	$V_{IL(PORRST)}$	Low-level input voltage of $\overline{\text{PORRST}}$ before V_{CCIOR} > $V_{CCIOPORL}$		0.5	V
3	$t_{su(PORRST)r}$	Setup time, $\overline{\text{PORRST}}$ active before V_{CCIOR} > $V_{CCIOPORL}$ during power up	0		ms
5	$t_{su(VCCIOR)r}$	Setup time, V_{CCIOR} > $V_{CCIOPORL}$ before V_{CC} > V_{CCPORL}	0		ms
6	$t_{h(PORRST)r}$	Hold time, $\overline{\text{PORRST}}$ active after V_{CC} > V_{CCPORH}	1		ms
7	$t_{su(PORRST)f}$	Setup time, $\overline{\text{PORRST}}$ active before V_{CC} ≤ V_{CCPORH} during power down	8		µs
8	$t_{h(PORRST)rio}$	Hold time, $\overline{\text{PORRST}}$ active after V_{CCIOR} > $V_{CCIOPORH}$	1		ms
9	$t_{h(PORRST)d}$	Hold time, $\overline{\text{PORRST}}$ active after V_{CCIOR} < $V_{CCIORPORL}$	0		ms
10	$t_{su(PORRST)fio}$	Setup time, $\overline{\text{PORRST}}$ active before V_{CC} ≤ $V_{CCIOPORH}$ during power down	0		ns
11	$t_{su(VCCIO)f}$	Setup time, V_{CC} < V_{CCPORE} before V_{CCIO} < $V_{CCIOPORL}$	0		ns
	$t_{f(PORRST)}$	Filter time $\overline{\text{PORRST}}$, pulses less than MIN get filtered out; pulses greater than MAX generate a reset.	30	185	ns
	$t_{f(RST)}$	Filter time $\overline{\text{RST}}$, pulses less than MIN get filtered out; pulses greater than MAX generate a reset.	40	150	ns

(1) When the V_{CC} timing requirements for $\overline{\text{PORRST}}$ are satisfied, there are no timing requirements for V_{CCP}.
(2) Corresponds to $\overline{\text{PORRST}}$.
(3) Corresponds to $\overline{\text{RST}}$.



V_{CC} (1.55 V)
V_{CCP}/V_{CCIOR} (3.3 V)

Note: V_{CC} is provided by the on-chip voltage regulator during normal application run time. It is not recommended to use the device in an application with the Vreg disabled due to potential glitching issues; however, if used in this mode, the application should ensure that the specified voltage ranges for V_{CC} are maintained.

Figure 5-1. $\overline{\text{PORRST}}$ Timing Diagram

Table 5-2. Switching Characteristics Over Recommended Operating Conditions for $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ (1)

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, $\overline{\text{RST}}$ active after $\overline{\text{PORRST}}$ inactive	$1024t_{c(OSC)}$		ns
	Valid time, $\overline{\text{RST}}$ active (all others)	$8t_{c(VCLK)}$		
$V_{CCIOPORL}$	Vccio low supply level when $\overline{\text{PORRST}}$ must be active during power-up and power-down		1.1	V

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see Table 5-13.

Table 5-3. Internal Voltage Regulator Specifications

PARAMETER		MIN	MAX	UNIT
$t_{D(VCCIOR)0-3}$	Delay time, input supply to ramp from 0 V to 3 V	12	1000	µs
$t_{V(PORRST)L}$	Valid time, $\overline{\text{PORRST}}$ active after input supply becomes ≥ 3.0 V	1		ms
$V_{CCIORmin(PORRST)f}$	Minimum input voltage, when $\overline{\text{PORRST}}$ must be made active during power down or brown out	3.0		V
$C_{(VCC)core}$	Capacitance distributed over core V_{CC} pins for voltage regulator stability	1.2	6.0	µF
$ESR_{(max)core}$	Total combined ESR of stabilization capacitors on core V_{CC} pins	0	0.75	Ω

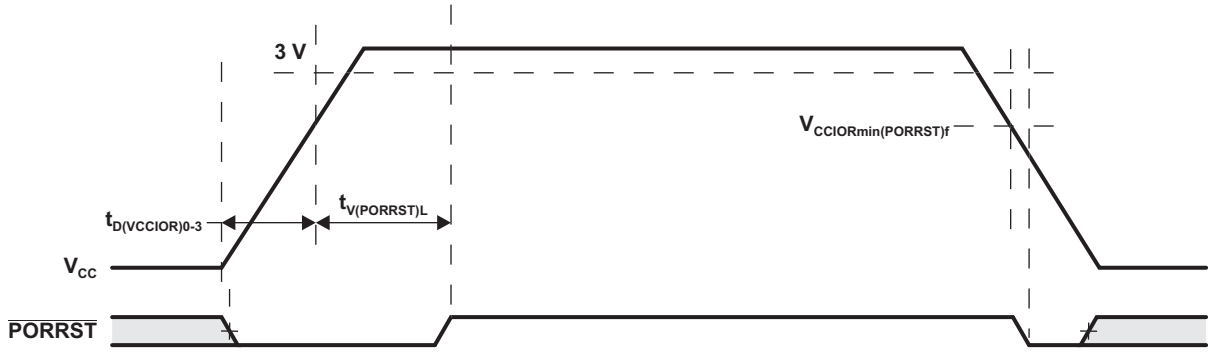


Figure 5-2. $\overline{\text{PORRST}}$ Timing Requirements

Table 5-4. VREG Recommended Operation Conditions

PARAMETER		CONDITIONS	MIN	MAX	UNIT
I_{CC}	V_{CC} Load Rating	Normal mode, regulator active	0	200	mA
		Off, enable forced off	-	-	µA

5.2 PLL and Clock Specifications

Table 5-5. Timing Requirements for PLL Circuits Enabled or Disabled

PARAMETER		MIN	MAX	UNIT
$f_{(OSC)}$	Input clock frequency	5	20	MHz
$t_{c(OSC)}$	Cycle time, OSCIN	50		ns
$t_{w(OSCIL)}$	Pulse duration, OSCIN low	15		ns
$t_{w(OSCIH)}$	Pulse duration, OSCIN high	15		ns

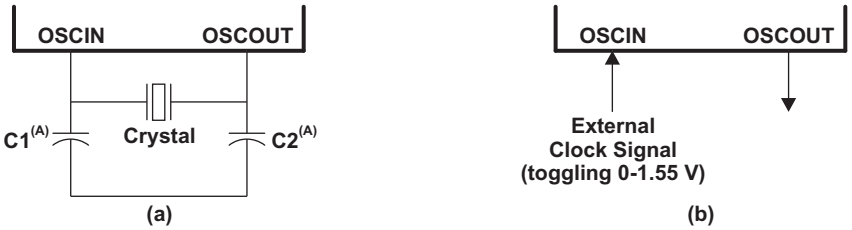
5.2.1 External Reference Resonator/Crystal Oscillator Clock Option

The oscillator is enabled by connecting the appropriate fundamental 5-20 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 5-3(a). The oscillator is a single stage inverter held in bias by an integrated bias resistor.

TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. Vendors are equipped to determine which load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

5.2.2 External Clock Source

An external oscillator source can be used by connecting a 1.55-V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 5-3(b).



A. The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 5-3. Recommended Crystal/Clock Connection

5.2.3 Validated FMPLL Settings

The following table includes the validated FMPLL settings.

Table 5-6. Validated FMPLL Settings

Mode	OSCIN Frequency (MHz)	PLLCTL1[1]	PLLCTL2[1]	FMPLL Output Frequency (MHz)	Modulation Bandwidth (KHz)	Modulation Depth
Non-Modulated[2]	10	0x20048B00	0x00007800	56	-	-
	12	0x20026100	0x00007C00			
		0x20058B00	0x00007800			
	14	0x20055F00	0x00007600			
		0x20068B00	0x00007800			
	16	0x20036100	0x00007C00			
		0x20078B00	0x00007800			
	20	0x20098B00	0x00007800			
Non-Modulated[2]	10	0x20049F00	0x00007800	64	-	-
	12	0x20055F00	0x00007400			
		0x20059F00	0x00007800			
	14	0x20065F00	0x00007400			
		0x20069F00	0x00007800			
	16	0x20075F00	0x00007400			
		0x20079F00	0x00007800			
	20	0x20099F00	0x00007800			
Non-Modulated[2]	10	0x20049F00	0x00007600	80	-	-
	12	0x20026300	0x00007800			
		0x20059F00	0x00007600			
	14	0x20067700	0x00007400			
		0x20069F00	0x00007600			
	16	0x20036300	0x00007800			
		0x20079F00	0x00007600			
	20	0x20099F00	0x00007600			

(1) The recommended PLLCTL1 and PLLCTL2 values make no assumption of the intended use of ROS, BPOS, and ROF fields within the PLL control registers. For these settings, the application should set these as appropriate for the specific application requirements.
(2) Non-Modulated settings provided show FM related bit fields as 0. When initializing the PLLCTL registers for non-modulated use, the FM related bit fields should be masked such that reset/default values are retained.

Table 5-6. Validated FMPLL Settings (continued)

Mode	OSCIN Frequency (MHz)	PLLCTL1[1]	PLLCTL2[1]	FMPLL Output Frequency (MHz)	Modulation Bandwidth (KHz)	Modulation Depth
Frequency Modulated	10	0x20048B00	0x8300B844	56	76.92	0.50%
		0x20048B00	0x8300B889			1.00%
		0x20048B00	0x82409859		100	0.50%
		0x20048B00	0x824098B2			1.00%
	12	0x20058B00	0x8300B844		76.92	0.50%
		0x20058B00	0x8300B889			1.00%
		0x20058B00	0x82409859		100	0.50%
		0x20058B00	0x824098B2			1.00%
	14	0x20068B00	0x8300B844		76.92	0.50%
		0x20068B00	0x8300B889			1.00%
		0x20068B00	0x82409859		100	0.50%
		0x20068B00	0x824098B2			1.00%
	16	0x20078B00	0x8300B844		76.92	0.50%
		0x20078B00	0x8300B889			1.00%
		0x20078B00	0x82409859		100	0.50%
		0x20078B00	0x824098B2			1.00%
	20	0x20098B00	0x8300B844		76.92	0.50%
		0x20098B00	0x8300B889			1.00%
		0x20098B00	0x82409859		100	0.50%
		0x20098B00	0x824098B2			1.00%
Frequency Modulated	10	0x20049F00	0x8300C83B	64	76.92	0.50%
		0x20049F00	0x8300C878			1.00%
		0x20049F00	0x8240A84D		100	0.50%
		0x20049F00	0x8240A89C			1.00%
	12	0x20059F00	0x8300C83B		76.92	0.50%
		0x20059F00	0x8300C878			1.00%
		0x20059F00	0x8240A84D		100	0.50%
		0x20059F00	0x8240A89C			1.00%
	14	0x20069F00	0x8300C83B		76.92	0.50%
		0x20069F00	0x8300C878			1.00%
		0x20069F00	0x8240A84D		100	0.50%
		0x20069F00	0x8240A89C			1.00%
	16	0x20079F00	0x8300C83B		76.92	0.50%
		0x20079F00	0x8300C878			1.00%
		0x20079F00	0x8240A84D		100	0.50%
		0x20079F00	0x8240A89C			1.00%
	20	0x20099F00	0x8300C83B		76.92	0.50%
		0x20099F00	0x8300C878			1.00%
		0x20099F00	0x8240A84D		100	0.50%
		0x20099F00	0x8240A89C			1.00%

Table 5-6. Validated FMPLL Settings (continued)

Mode	OSCIN Frequency (MHz)	PLLCTL1[1]	PLLCTL2[1]	FMPLL Output Frequency (MHz)	Modulation Bandwidth (KHz)	Modulation Depth
Frequency Modulated	10	0x20049F00	0x8300C63B	80	76.92	0.50%
		0x20049F00	0x8300C678			1.00%
		0x20049F00	0x8240A64D		100	0.50%
		0x20049F00	0x8240A69C			1.00%
	12	0x20059F00	0x8300C63B		76.92	0.50%
		0x20059F00	0x8300C678			1.00%
		0x20059F00	0x8240A64D		100	0.50%
		0x20059F00	0x8240A69C			1.00%
	14	0x20069F00	0x8300C63B		76.92	0.50%
		0x20069F00	0x8300C678			1.00%
		0x20069F00	0x8240A64D		100	0.50%
		0x20069F00	0x8240A69C			1.00%
	16	0x20079F00	0x8300C63B		76.92	0.50%
		0x20079F00	0x8300C678			1.00%
		0x20079F00	0x8240A64D		100	0.50%
		0x20079F00	0x8240A69C			1.00%
	20	0x20099F00	0x8300C63B		76.92	0.50%
		0x20099F00	0x8300C678			1.00%
		0x20099F00	0x8240A64D		100	0.50%
		0x20099F00	0x8240A69C			1.00%

5.2.4 LPO and Clock Detection

The LPOCLKDET module consists of a clock monitor (CLKDET) and 2 low-power oscillators (LPO): a low-frequency (LF) and a high-frequency (HF) oscillator. The CLKDET is a supervisor circuit for an externally supplied clock signal. In case the externally supplied clock frequency falls out of a frequency window, the clock detector flags this condition and switches to the HF LPO clock (limp mode). The OSCFAIL flag and clock switch-over remain, regardless of the behavior of the oscillator clock signal. The only way OSCFAIL can be cleared (and OSCIN be again the driving clock) is a power-on reset.

Table 5-7. LPO and Clock Detection

PARAMETER		MIN	TYP	MAX	UNIT
invalid frequency	Lower threshold	1.5		5.0	MHz
	Higher threshold	20.0		50.0	MHz
limp mode frequency (HFosc)		7.6	12	14.0	MHz
LFosc frequency		50	90	124	kHz
HFosc frequency		7.6	12	14.0	MHz

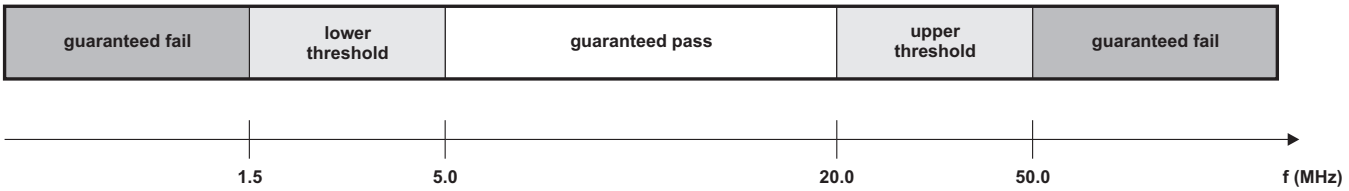
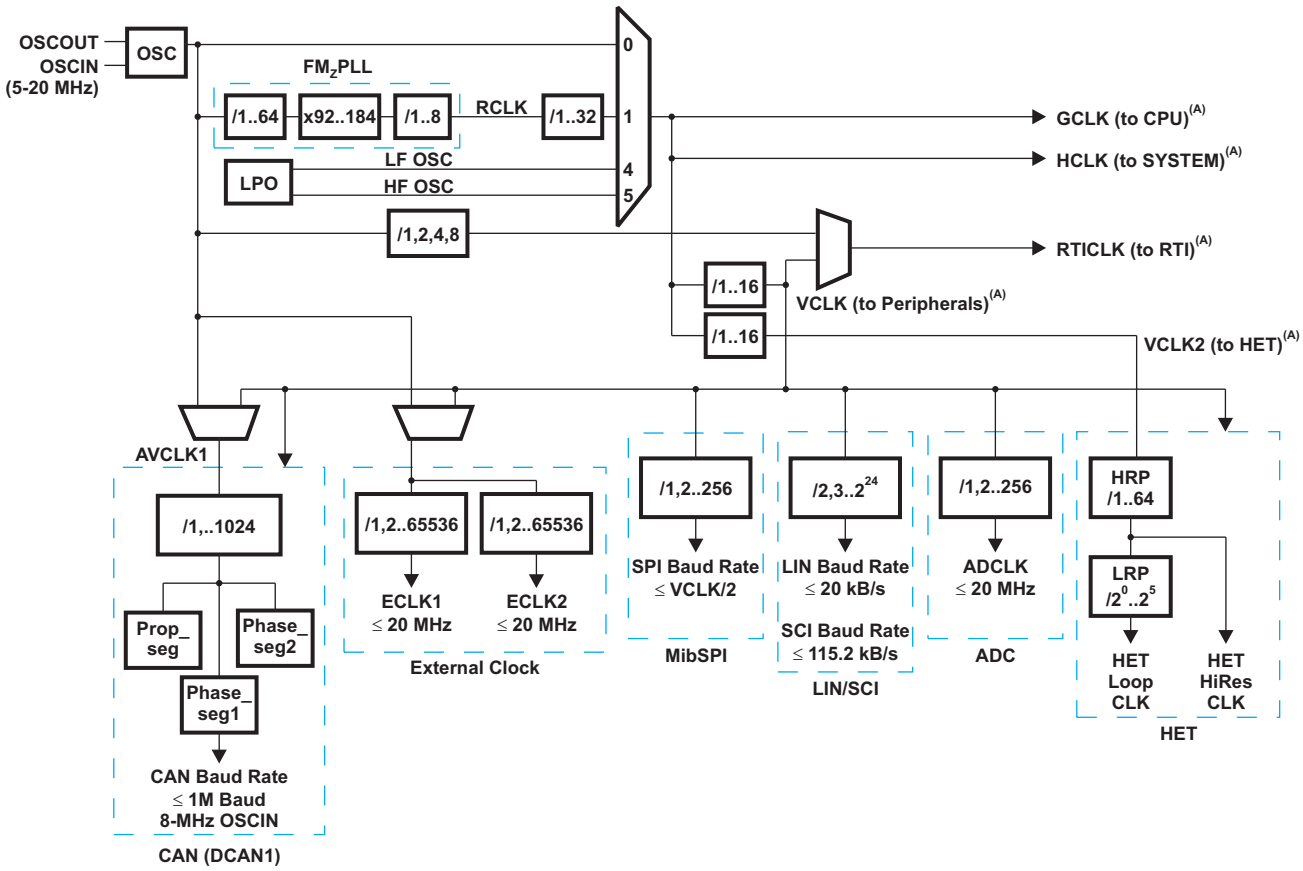


Figure 5-4. LPO and Clock Detection

5.2.5 Device Clock Domains Block Diagram

The clock domains block diagram and GCM clock source assignments are given in Figure 5-5 and Table 5-8.



A. See Table 5-9.

Figure 5-5. Device Clock Domains Block Diagram

Table 5-8. GCM Clock Source Assignments

GCM SOURCE NUMBER	CLOCK SOURCE
0	OSCIN
1	F035 FMzPLL
2	Reserved
3	Reserved
4	LF OSC
5	HF OSC
6	Reserved
7	Reserved

Table 5-9. Switching Characteristics Over Recommended Operating Conditions for Clocks(1)(2)(3)(4)(5)

PARAMETER		TEST CONDITIONS(6)	MIN	MAX	UNIT
$f_{(HCLK)}$	System clock frequency	Pipeline mode enabled		80	MHz
		Pipeline mode disabled, 0 flash wait states		28	
$f_{(PROG/ERASE)}$	System clock frequency Flash programming/erase			80	MHz
$f_{(VCLK/VCLK2)}$	Peripheral VBUS clock frequency			$f_{(HCLK)}$	MHz
$f_{(ECLK)}$	External clock output frequency for ECP Module			20	MHz
$f_{(RCLK)}$	RCLK - Frequency out of PLL macro into R-divider (Post ODPLL divider)			145	MHz
$t_{c(HCLK)}$	Cycle time, system clock	Pipeline mode enabled	12.50		ns
		Pipeline mode disabled, 0 flash wait states	35.71		
$t_{c(PROG/ERASE)}$	Cycle time, system clock - Flash programming/erase		12.50		ns
$t_{c(VCLK/VCLK2)}$	Cycle time, peripheral clock		$t_{c(HCLK)}$		ns
$t_{c(ECLK)}$	Cycle time, ECP module external clock output		50.0		ns
$t_{c(RCLK)}$	Cycle time, RCLK minimum input cycle time out of PLL macro into R-divider		6.90		ns

(1) $f_{(HCLK)} = f_{(OSC)}$ / NR *NF /ODPLL/PLLDIV; for details, see the PLL documentation. TI strongly recommends selection of NR and NF parameters such that NF ≤ 120 and ($f_{(OSC)}$ / NR *NF) ≤ 400.
$f_{(VCLK)} = f_{(HCLK)}$ / X, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the peripheral VBUS clock divider ratio determined by the VCLKR[3:0] bits in the SYS module.
(2) Enabling FM mode can reduce maximum rated operating frequencies. The degree of impact is application-specific and the specific settings, as well as the impact of the settings, should be discussed and agreed upon prior to using FM modes. Use of FM modes do not impact the maximum rated external clock output, $f_{(ECLK)}$, for the ECP module.
(3) Pipeline mode enabled or disabled is determined by FRDCNTL[2:0].
(4) $f_{(ECLK)} = f_{(VCLK)}$ / N, where N = {1 to 65536}. N is the ECP prescale value defined by the ECPCTRL.[15:0] register bits in the ECP module.
(5) ECLK output will increase radiated emissions within the system that is used. Rated emissions at the device level do not include emissions due to ECLK output.
(6) All test conditions assume FM Mode disabled and RAM ECC enabled with 0 waitstates for RAM.

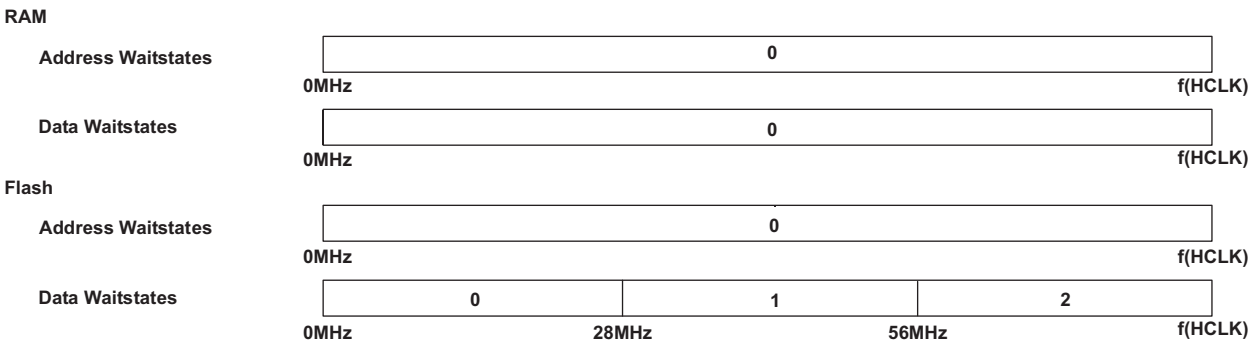


Figure 5-6. Timing - Wait States

NOTE

If FMzPLL frequency modulation is enabled, special care must be taken to ensure that the maximum system clock frequency f(HCLK) and peripheral clock frequency f(VCLK) are not exceeded. The speed of the device clocks may need be derated to accommodate the modulation depth when FMzPLL frequency modulation is enabled.

5.2.5.1 ECLK Specification

Table 5-10. Switching Characteristics Over Recommended Operating Conditions for External Clocks(1)(2)

(see Figure 5-7)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
1	$t_{w(EOL)}$	Pulse duration, ECLK low	Under all prescale factor combinations (X and N)	$0.5t_{c(ECLK)} - t_f$		ns
2	$t_{w(EOH)}$	Pulse duration, ECLK high	Under all prescale factor combinations (X and N)	$0.5t_{c(ECLK)} - t_r$		ns

(1) X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the VBUS interface clock divider ratio determined by the CLKCNTL.[19:16] bits in the SYS module.
(2) N = {1 to 65536}. N is the ECP prescale value defined by the ECPCNTL.[15:0] register bits in the SYS module.

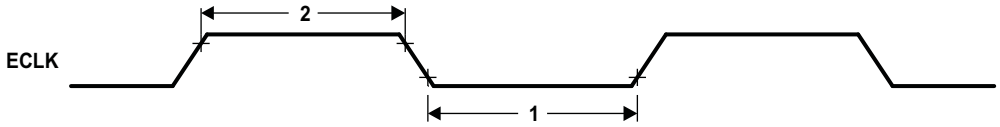


Figure 5-7. ECLK Timing Diagram

5.2.6 TEST Pin Glitch Filter Timing

Table 5-11. Test Pin Glitch Filter Timing

NO.	PARAMETER		MIN	MAX	UNIT
	$t_{f(TEST)}$	Filter time TEST, high pulses less than MIN will be filtered out.	40		ns

5.2.7 JTAG Timing

Table 5-12. JTAG Scan Interface Timing (JTAG Clock specification 10-MHz and 50-pF Load on TDO Output)

(see Figure 5-8

NO.			MIN	MAX	UNIT
1	$t_{c(JTAG)}$	Cycle time, JTAG low and high period	50		ns
2	$t_{su(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	5		ns
3	$t_{h(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	5		ns
4	$t_{h(TCKf -TDO)}$	Hold time, TDO after TCKf	5		ns
5	$t_{d(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)		45	ns

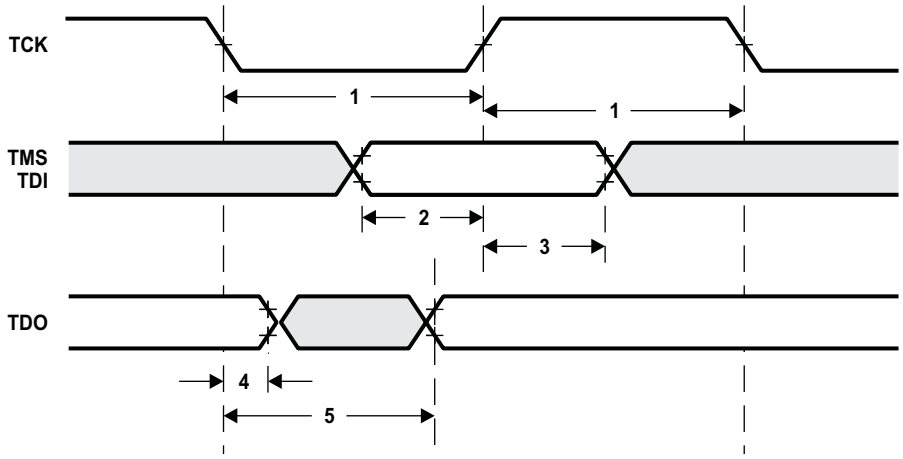


Figure 5-8. JTAG Scan Timings

5.2.8 Output Timings

Table 5-13. Switching Characteristics for Output Timings Versus Load Capacitance (C_L)(1)

(see Figure 5-9)

PARAMETER			MAX	UNIT
t_r	Adaptive impedance 4 mA pins	C_L = 15 pF	4	ns
		C_L = 50 pF	8	
		C_L = 100 pF	15	
		C_L = 150 pF	21	
t_f	Adaptive impedance 4 mA pins	C_L = 15 pF	5	ns
		C_L = 50 pF	8	
		C_L = 100 pF	12	
		C_L = 150 pF	17	

(1) Peripheral output timings given within this document are measured in either standard buffer or impedance control mode.

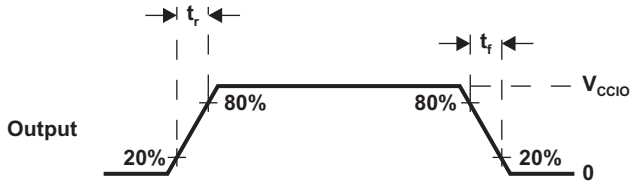


Figure 5-9. CMOS-Level Outputs

5.2.9 Input Timings

Table 5-14. Timing Requirements for Input Timings(1)

(see Figure 5-10)

		MIN	MAX	UNIT
t_{pw}	Input minimum pulse width	$t_{c(VCLK)}$ + 10		ns

(1) $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = 1 / $f_{(VCLK)}$.

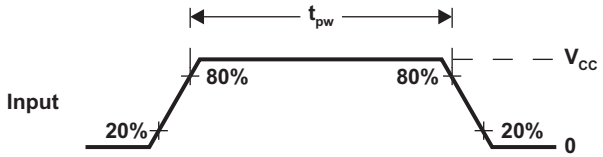


Figure 5-10. CMOS-Level Inputs

5.2.10 Flash Timings

Table 5-15. Timing Requirements for Program Flash

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{acc_delay}	Flash pump stabilization time	From Sleep Mode to Standby Mode	20			µs
		From Standby Mode to Active Mode	1			
	Flash bank stabilization time	From Sleep Mode to Standby Mode	1.9			
		From Standby Mode to Active Mode	0.1			
$t_{prog(32\text{-}bit)}$	Half-word (32-bit) programming time			37.5	300	µs
$t_{prog(Total)}$	384k-byte programming time(1)			3.7	29.5	s
	448k-byte programming time(1)			4.3	34.4	
$t_{erase(sector)}$	Sector erase time			1.5	15	s
N_{wec}	Write/erase cycles at TA = -40 to 125°C with 15-year Data Retention requirement				1000(2)	cycles
	Write/erase cycles at TA = -40 to 125°C EEPROM emulation requirement for 16k flash sectors in Bank 1				25000(2)(3)	cycles

(1) $t_{prog(Total)}$ programming time includes overhead of state machine, but does not include data transfer time.
(2) Flash write/erase cycles and data retention specifications are based on a validated implementation of the TI flash API. Non-TI flash API implementation is not supported. For detailed description see the *F035 Flash Validation Procedure (SPNA127)*.
(3) Flash write/erase cycle and data retention specifications are based on an assumed distribution of write/erase cycles over the life of the product including an even distribution over the rated temperature range and time between cycles. The EEPROM emulation bank has been qualified as outlined in the JEDEC specification JESD22-A117C.

5.3 SPIn Master Mode Timing Parameters

Table 5-16. SPIn Master Mode External Timing Parameters (CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3)

(see Figure 5-11 and Figure 5-12)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)	90	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$-8	$0.5t_{c(SPC)M}$ + 5	
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$-8	$0.5t_{c(SPC)M}$ + 5	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$-8	$0.5t_{c(SPC)M}$ + 5	
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$-8	$0.5t_{c(SPC)M}$ + 5	
4(5)	$t_{d(SIMO-SPCL)M}$	Delay time, SPISIMO data valid before SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}$ - 10		
	$t_{d(SIMO-SPCH)M}$	Delay time, SPISIMO data valid before SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M}$ - 10		
5(5)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid (clock polarity = 0)	$0.5t_{c(SPC)M} - t_{f(SPC)}$-5		
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid (clock polarity = 1)	$0.5t_{c(SPC)M} - t_{r(SPC)}$-5		
6(5)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	$t_{r(SPC)}$+4		
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	$t_{f(SPC)}$+4		
7(5)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	10		
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	10		
8(5)(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPICLK)}$-21	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPICLK)}$+6	
		Setup time CS active until SPICLK low (clock polarity = 1)	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPICLK)}$-21	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPICLK)}$+6	
9(5)(6)	$t_{T2CDELAY}$	Hold time SPICLK low until CS inactive (clock polarity = 0)	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPICLK)} + t_{r(SPICS)}$-4	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPICLK)} + t_{r(SPICS)}$+17	
		Hold time SPICLK high until CS inactive (clock polarity = 1)	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPICLK)} + t_{r(SPICS)}$-4	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPICLK)} + t_{r(SPICS)}$+17	
10	t_{SPIENA}	SPIENAn sample point	$C2TDELAY * t_{c(VCLK)} - t_{f(SPICS)}$-25	$C2TDELAY * t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is clear.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$.
(3) For rise and fall timings, see Table 5-13.
(4) When the SPI is in Master mode, the following must be true:
- For PS values from 1 to 255: t ≥ (PS +1)$t_{c(VCLK)}$ ≥ 90 ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
- For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)}$ ≥ 90 ns.

(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY are programmed in the SPIDELAY register.

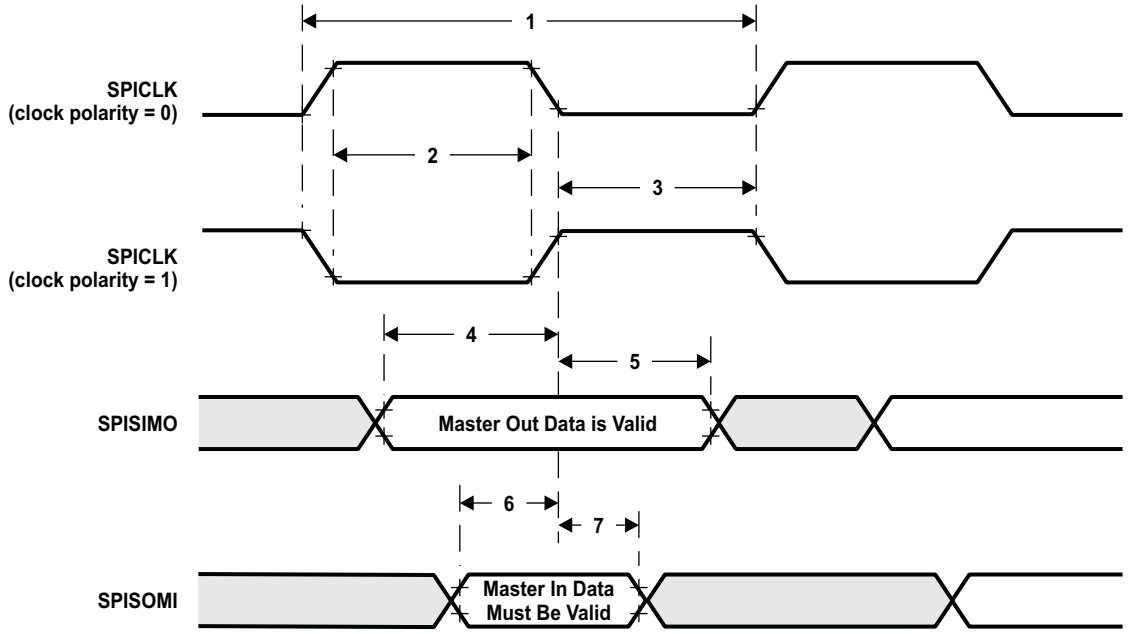


Figure 5-11. SPI Master Mode External Timing (CLOCK PHASE = 0)

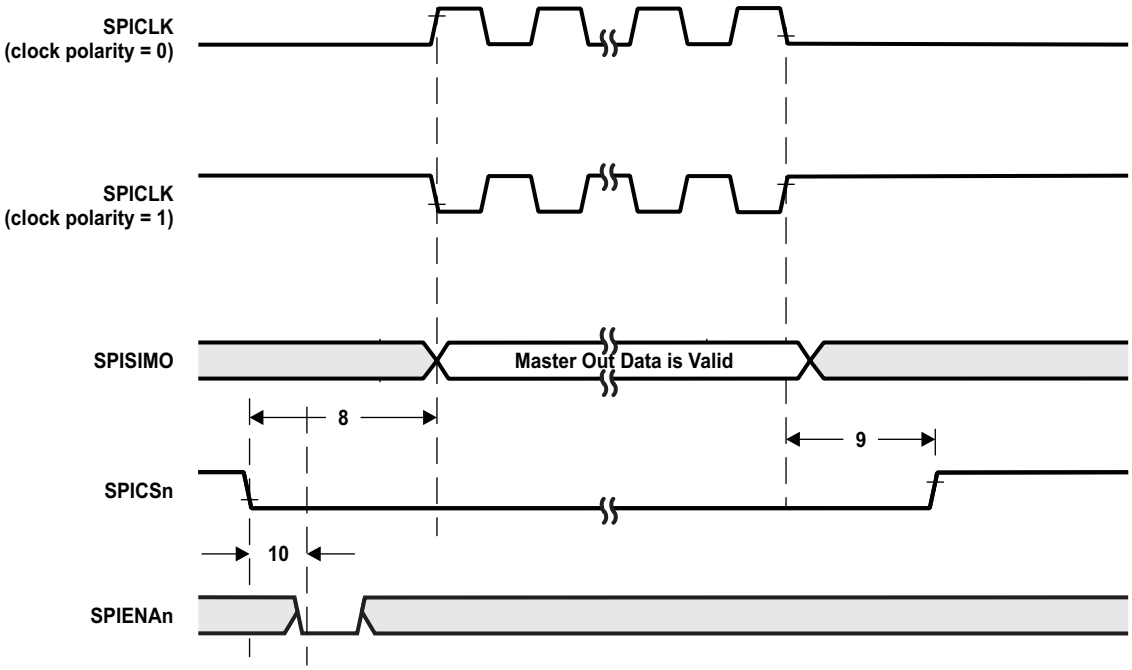


Figure 5-12. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

Table 5-17. SPIn Master Mode External Timing Parameters (CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3)

(see Figure 5-13 and Figure 5-14)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)	90	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$-8	$0.5t_{c(SPC)M}$ + 5	
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$-8	$0.5t_{c(SPC)M}$ + 5	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$-8	$0.5t_{c(SPC)M}$ + 5	
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$-8	$0.5t_{c(SPC)M}$ + 5	
4(5)	$t_{v(SIMO-SPCH)M}$	Valid time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$ - 10		
	$t_{v(SIMO-SPCL)M}$	Valid time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$ - 10		
5(5)	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_{r(SPC)}$-5		
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_{f(SPC)}$-5		
6(5)	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$t_{r(SPC)}$+4		
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$t_{f(SPC)}$+4		
7(5)	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	10		
	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	10		
8(5)(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$+(C2TDELAY +CSHOLD+2)*$t_{c(VCLK)}$- $t_{f(SPICS)}$ + $t_{r(SPICLK)}$-21	$0.5t_{c(SPC)M}$+(C2TDELAY +CSHOLD+2)*$t_{c(VCLK)}$ - $t_{f(SPICS)}$ + $t_{r(SPICLK)}$+6	
		Setup time CS active until SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$+(C2TDELAY +CSHOLD+2)*$t_{c(VCLK)}$ - $t_{f(SPICS)}$ + $t_{f(SPICLK)}$-21	$0.5t_{c(SPC)M}$+(C2TDELAY +CSHOLD+2)*$t_{c(VCLK)}$ - $t_{f(SPICS)}$ + $t_{f(SPICLK)}$+6	
9(5)(6)	$t_{T2CDELAY}$	Hold time SPICLK low CS until inactive (clock polarity = 0)	T2CDELAY*$t_{c(VCLK)}$ + $t_{c(VCLK)}$ - $t_{f(SPICLK)}$ + $t_{r(SPICS)}$-4	T2CDELAY*$t_{c(VCLK)}$ + $t_{c(VCLK)}$ - $t_{f(SPICLK)}$ + $t_{r(SPICS)}$+17	
		Hold time SPICLK high until CS inactive (clock polarity = 1)	T2CDELAY*$t_{c(VCLK)}$ + $t_{c(VCLK)}$ - $t_{r(SPICLK)}$ + $t_{r(SPICS)}$-4	T2CDELAY*$t_{c(VCLK)}$ + $t_{c(VCLK)}$ - $t_{r(SPICLK)}$ + $t_{r(SPICS)}$+17	
10(7)	t_{SPIENA}	SPIENAn Sample Point	C2TDELAY * $t_{c(VCLK)}$ - $t_{f(SPICS)}$-25	C2TDELAY * $t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is clear.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$.
(3) For rise and fall timings, see Table 5-13.
(4) When the SPI is in Master mode, the following must be true:
- For PS values from 1 to 255: t ≥ (PS +1)$t_{c(VCLK)}$ ≥ 90 ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
- For PS values of 0: $t_{c(SPC)M}$ = $2t_{c(VCLK)}$ ≥ 90 ns.

(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register.
(7) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register.

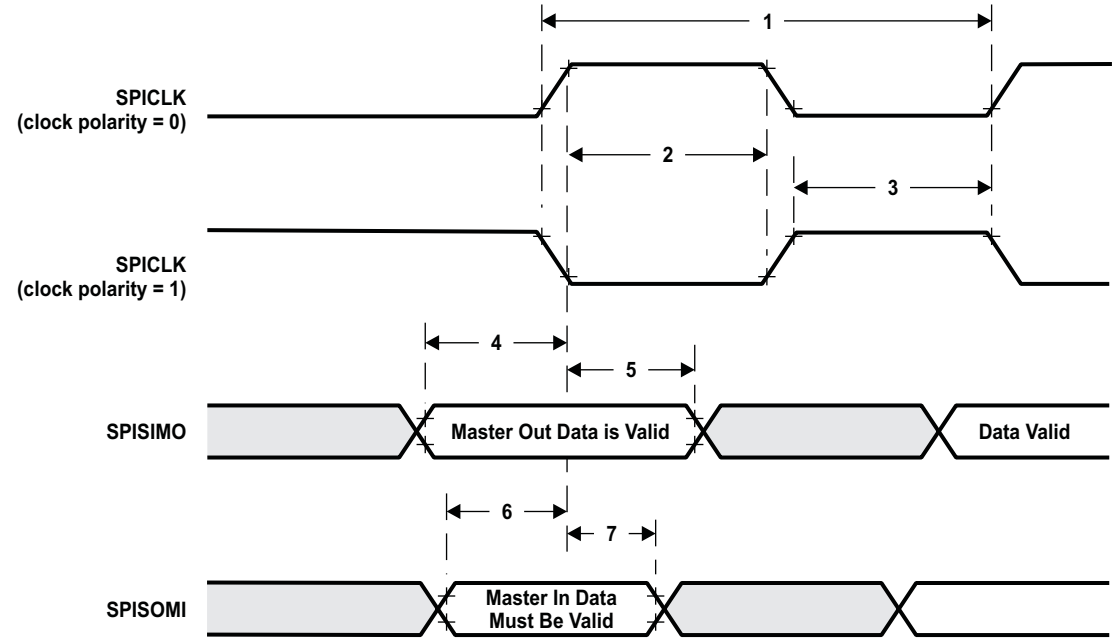


Figure 5-13. SPI Master Mode External Timing (CLOCK PHASE = 1)

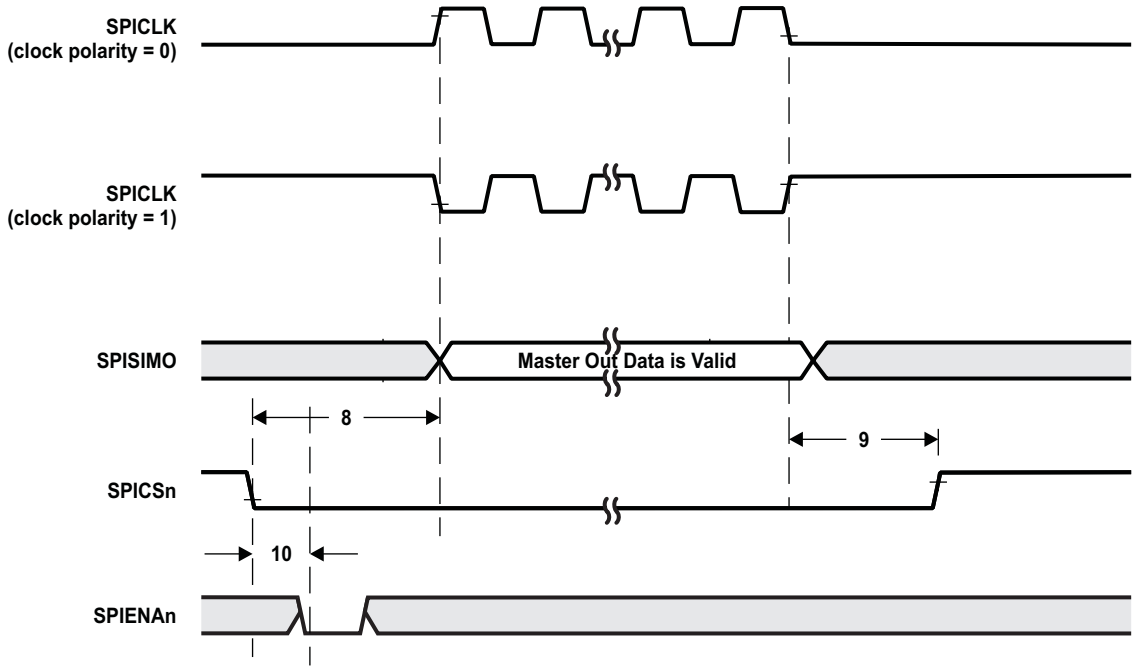


Figure 5-14. SPI Master Mode Chip Select timing (CLOCK PHASE = 1)

5.4 SPIn Slave Mode Timing Parameters

Table 5-18. SPIn Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4)

(see Figure 5-15 and Figure 5-16)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	90		ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	30		
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	30		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	30		
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	30		
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0)		$t_{rf(SOMI)}$+17	
	$t_{d(SPCL-SOMI)S}$	Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1)		$t_{rf(SOMI)}$+17	
5(6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	0		
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	0		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 0)	5		
	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 1)	5		
7(6)	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	6		
	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	6		
8	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}$+ $t_{r(ENAn)}$+20	ns
	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}$+ $t_{r(ENAn)}$+20	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}$+ $t_{f(ENAn)}$+18	ns

(1) The MASTER bit (SPIGCR1.0) is clear and the CLOCK PHASE bit (SPIFMTx.16) is clear.
(2) When the SPI is in Slave mode, the following must be true: $t_{c(SPC)S} > 2t_{c(VCLK)}$ and $t_{c(SPC)S} \geq 90$ ns.
(3) For rise and fall timings, see Table 5-13.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$.
(5) When the SPI is in Slave mode, the following must be true: $t_{w(SPCL)S} > t_{c(VCLK)}$, $t_{w(SPCL)S} \geq 30$, $t_{w(SPCH)S} > t_{c(VCLK)}$ ns and $t_{w(SPCH)S} \geq 30$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

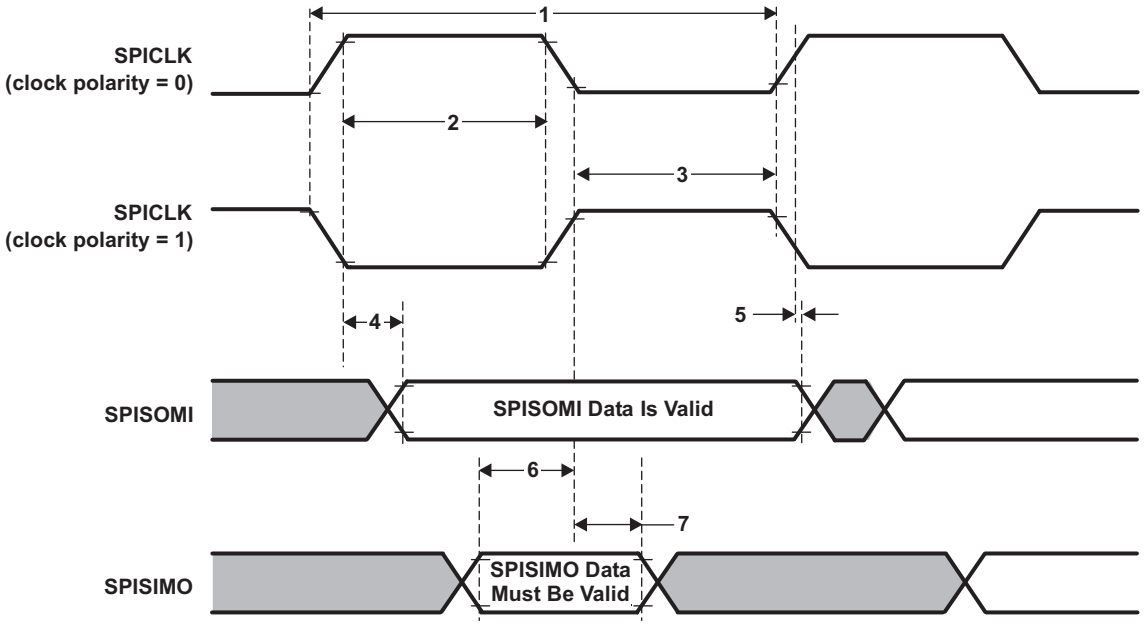


Figure 5-15. SPI Slave Mode External Timing (CLOCK PHASE = 0)

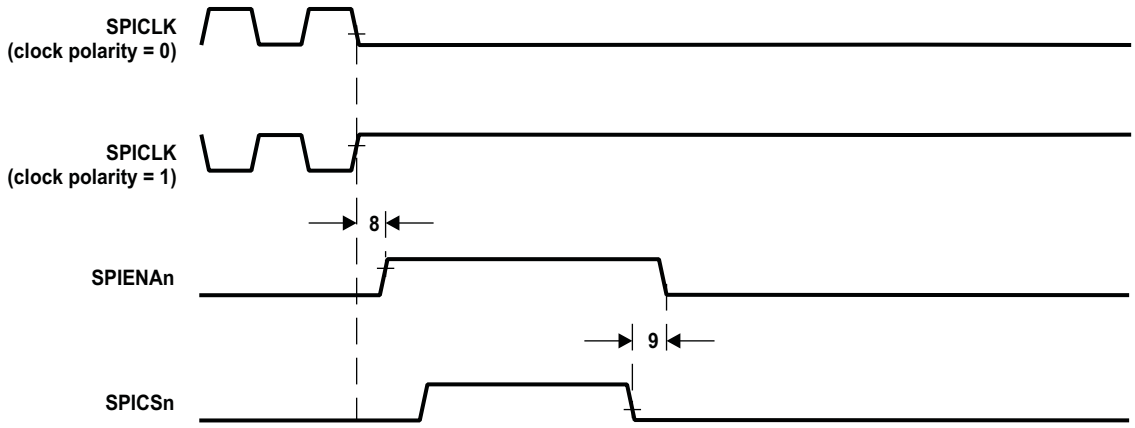


Figure 5-16. SPI Slave Mode Enable Timing (CLOCK PHASE = 0)

Table 5-19. SPIn Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4)

(see Figure 5-17 and Figure 5-18)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	90		ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	30		
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	30		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	30		
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	30		
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)		$t_{rf(SOMI)}$+17	
	$t_{d(SPCL-SOMI)S}$	Delay time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)		$t_{rf(SOMI)}$+17	
5(6)	$t_{v(SOMI-SPCH)S}$	Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0)	0		
	$t_{v(SOMI-SPCL)S}$	Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1)	0		
6(6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 0)	5		
	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 1)	5		
7(6)	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	6		
	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	6		
8	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}$+ tr(ENAn)+20	ns
	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}$+ $t_{f(ENAn)}$+20	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}$+ $t_{f(ENAn)}$+18	ns
10	$t_{d(SCSL-SOMI)S}$	Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer)	$t_{c(VCLK)}$	$2t_{c(VCLK)}$+ $t_{rf(SOMI)}$+17	ns

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is set.
(2) When the SPI is in Slave mode, the following must be true: $t_{c(SPC)S} > 2t_{c(VCLK)}$ and $t_{c(SPC)S} \geq 90$ ns.
(3) For rise and fall timings, see Table 5-13.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 /f(VCLK).
(5) When the SPI is in Slave mode, the following must be true: $t_{w(SPCL)S} > t_{c(VCLK)}$, $t_{w(SPCL)S} \geq 30$, $t_{w(SPCH)S} > t_{c(VCLK)}$ ns and $t_{w(SPCH)S} \geq 30$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

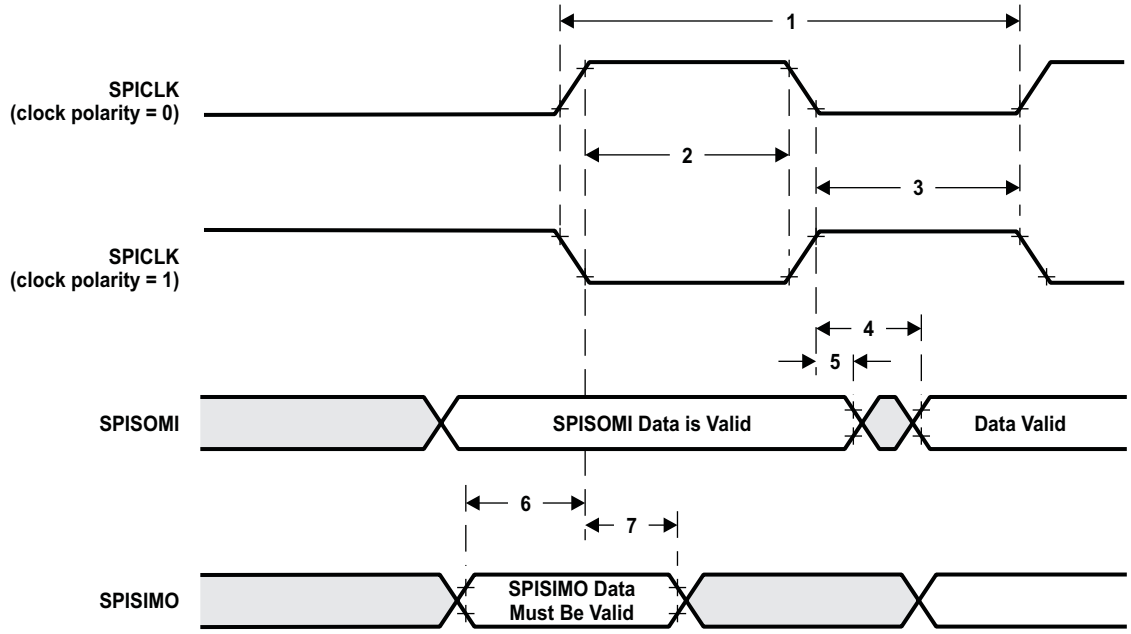


Figure 5-17. SPI Slave Mode External Timing (CLOCK PHASE = 1)

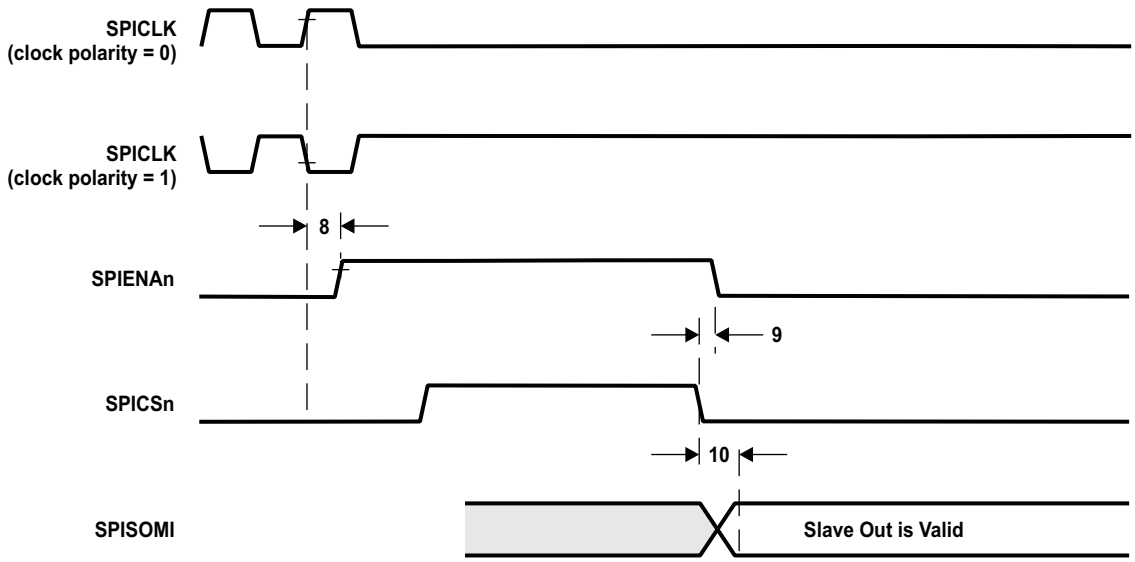


Figure 5-18. SPI Slave Mode Enable Timing (CLOCK PHASE = 1)

5.5 CAN Controller (DCANn) Mode Timings

Table 5-20. Dynamic Characteristics for the CANnSTX and CANnSRX Pins

PARAMETER		MIN	MAX	UNIT
$t_{d(CANnSTX)}$	Delay time, transmit shift register to CANnSTX pin(1)		15	ns
$t_{d(CANnSRX)}$	Delay time, CANnSRX pin to receive shift register		6	ns

(1) These values do not include rise/fall times of the output buffer.

5.6 High-End Timer (HET) Timings

Table 5-21. Dynamic Characteristics for the HET Pins

PARAMETER		MIN	MAX	UNIT
t_{opw}(HET)	Output pulse width, this is the minimum pulse width that can be generated(1)	$1/f_{(VCLK2)}$		ns
t_{ipw}(HET)	Input pulse width, this is the minimum pulse width that can be captured(2)	$1/f_{(VCLK2)}$		ns

(1) $t_{opw}(HET)_{min} = HRP_{(min)} = hr_{(min)}$ / VCLK2.
(2) $t_{ipw}(HET) = LRP_{(min)} = hr_{(min)} * lr_{(min)}$ / VCLK2.

5.7 Multi-Buffered A-to-D Converter (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on VSS and VCC from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to ADREFLO unless otherwise noted.

Resolution	10 bits (1024 values)
Monotonic	Assured
Output conversion code	00h to 3FFh [00 for $V_{AI} \leq AD_{REFLO}$; 3FF for $V_{AI} \geq A_{DREFHI}$]

Table 5-22. MibADC Recommended Operating Conditions(1)

		MIN	MAX	UNIT
AD_{REFHI}	A-to-D high -voltage reference source	3.0	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	0.3	V
V_{AI}	Analog input voltage	AD_{REFLO}	AD_{REFHI}	V
I_{AIC}	Analog input clamp current(2) ($V_{AI} < V_{SSAD}$ - 0.3 or $V_{AI} > V_{CCAD}$ + 0.3)	- 2	2	mA

(1) For V_{CCAD} and V_{SSAD} recommended operating conditions, see Section 4.2.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

Table 5-23. MibADC Operating Characteristics Over Full Range of Recommended Operating Conditions(1)

PARAMETER		DESCRIPTION/CONDITIONS	MIN	NOM	MAX	UNIT
R_{mux}	Analog input mux on-resistance	See Figure 5-19		125	1.5K	Ω
R_{samp}	ADC sample switch on-resistance	See Figure 5-19		150	1.5K	Ω
C_{mux}	Input mux capacitance	See Figure 5-19			16	pF
C_{samp}	ADC sample capacitance	See Figure 5-19			8	pF
I_{AIL}	Analog input leakage current	Input leakage per ADC input pin	-200		200	nA
$I_{ADREFHI}$	AD_{REFHI} input current	AD_{REFHI} = 3.6 V, $AD_{REFLO} = V_{SSAD}$			5	mA
CR	Conversion range over which specified accuracy is maintained	ADREFHI - ADREFLO	3		3.6	V
E_{DNL}	Differential non-linearity error	Difference between the actual step width and the ideal value (see Figure 5-20).			± 2	LSB
E_{INL}	Integral non-linearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error (see Figure 5-21).			± 2	LSB
E_{TOT}	Total error/Absolute accuracy	Maximum value of the difference between an analog value and the ideal midstep value (see Figure 5-22).			± 2	LSB

(1) 1 - LSB = $(AD_{REFHI} – AD_{REFLO})/ 2^{10}$ for the MibADC.

5.7.1 MibADC Input Model

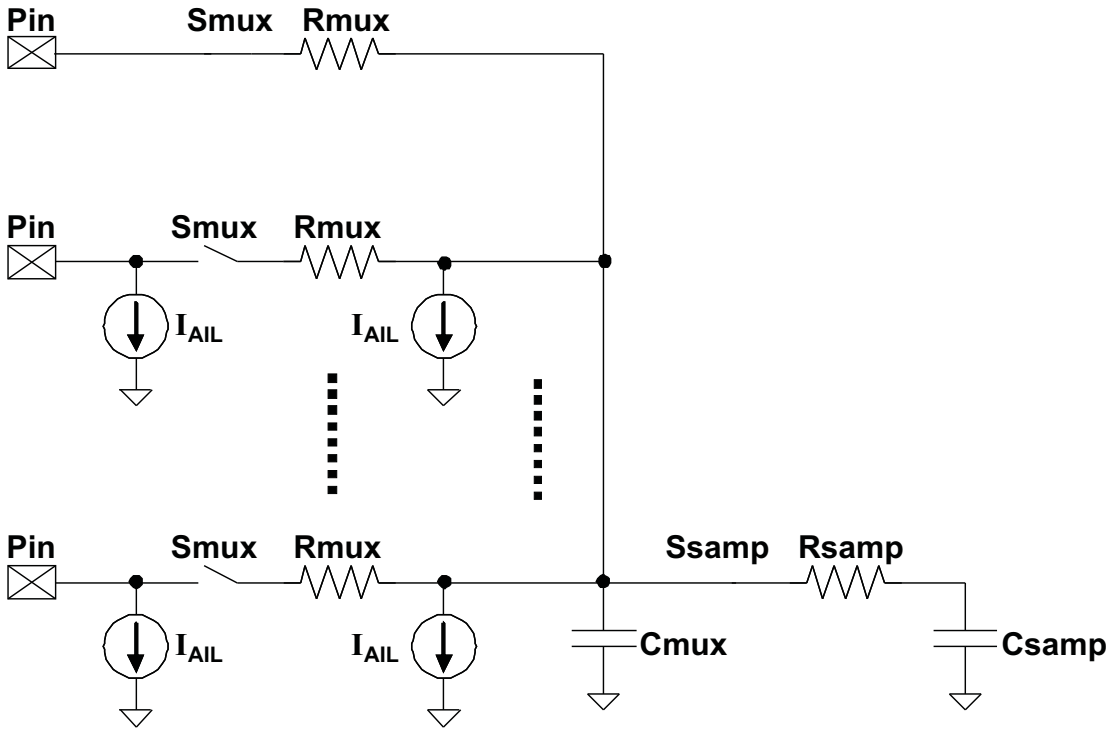


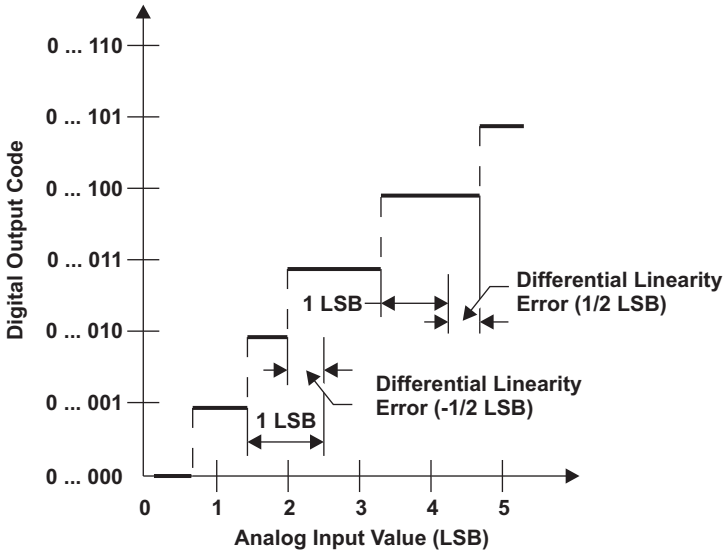
Figure 5-19. MibADC Input Equivalent Circuit

Table 5-24. Multi-Buffer ADC Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
$t_{c(ADCLK)}$	Cycle time, MibADC clock	0.05			µs
$t_{d(SH)}$	Delay time, sample and hold time	1			µs
$t_{d(C)}$	Delay time, conversion time	0.55			µs
$t_{d(SHC)}$ (1)	Delay time, total sample/hold and conversion time	1.55			µs

(1) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors.

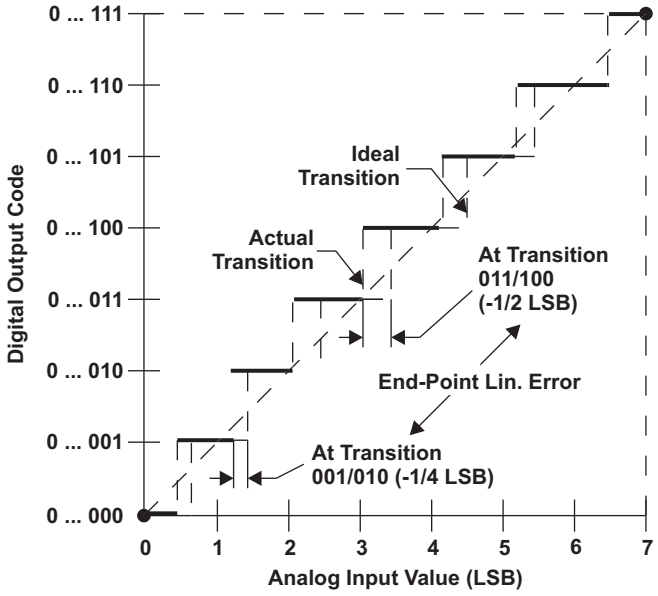
The differential non-linearity error shown in Figure 5-20 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



A. 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

Figure 5-20. Differential Non-linearity (DNL)

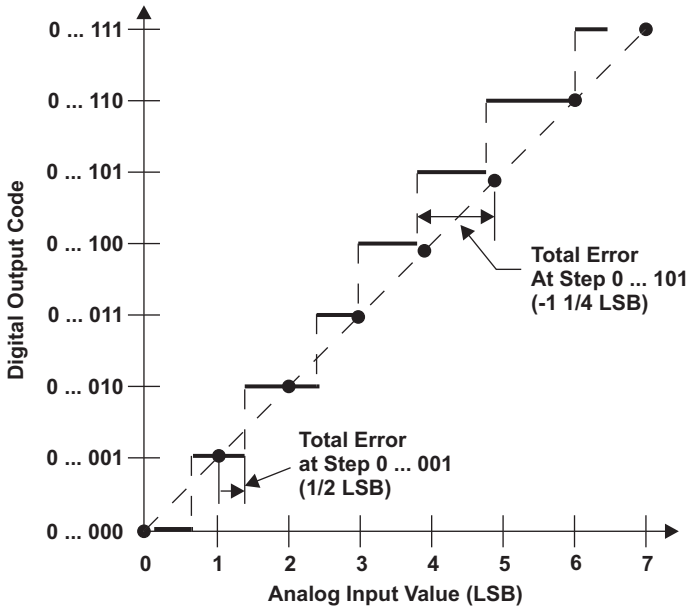
The integral non-linearity error shown in Figure 5-21 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.



A. 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

Figure 5-21. Integral Non-linearity (INL) Error

The absolute accuracy or total error of an MibADC as shown in Figure 5-22 is the maximum value of the difference between an analog value and the ideal midstep value.



A. 1 LSB = $(AD_{REFHI\mu} - AD_{REFLO})/2^{10}$

Figure 5-22. Absolute Accuracy (Total) Error

6 Revision History

This data sheet revision history highlights the technical changes made to the device or the datasheet.

Date	Additions, Deletions, And Modifications	Revision
August 2011	Added descriptions for the ENZ pin.	A
December 2011	Corrected number of GIO pins available from 8 to 4 in Device Characteristics table	B
	Updated LBIST section to include support for STCCLK = HCLK	
	Added additional detail about MBIST cycle counts	
	Operating Conditions and electrical specs upated with characterized values	
	Added upper limit to Vreg ramp specification	
	Removed support for low power modes	
	Added TEST Pin Glitch Filter Timing specification	
	Added note about back to back write/erase cycling in the EEPROM emulation bank.	
	Added FMPLL validated settings table	
January 2012	Updated programming times in the Flash Timings table.	C
	Corrected programming word size from 16-bit to 32-bit in the Flash Timings table to accurately reflect the default FSM configuration.	
	Added assumed use case and qualification standards for EEPROM emulation use in an application in the Flash Timings table.	

7 Mechanical Data

7.1 Thermal Data

Table 7-1 shows the thermal resistance characteristics for the PQFP - PZ mechanical packages.

Table 7-1. Thermal Resistance Characteristics (S-PQFP Package) [PZ]

PARAMETER	°C/W
$R_{\theta JA}$	48
$R_{\theta JC}$	5

7.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
S4MF03107SPZQQ1	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS470 MF03107SPZQQ1	Samples
S4MF03107SPZQQ1R	ACTIVE	LQFP	PZ	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS470 MF03107SPZQQ1	Samples
S4MF04207SPZQQ1	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS470 MF04207SPZQQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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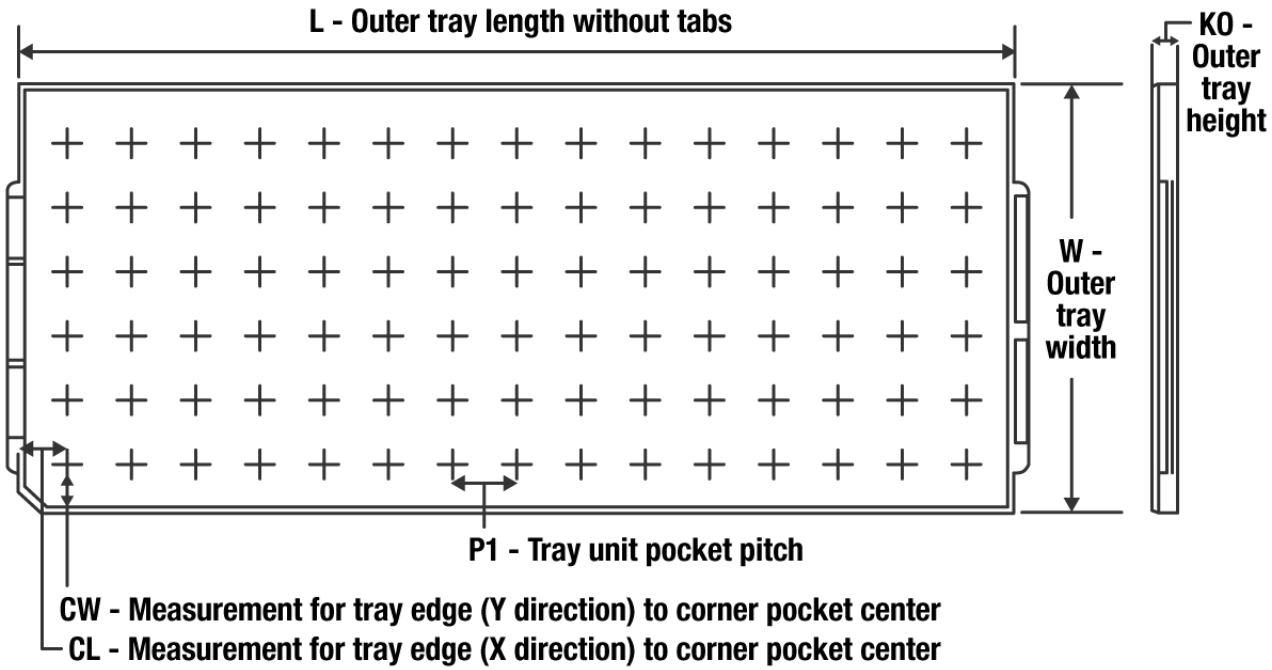
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
S4MF03107SPZQQ1	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
S4MF04207SPZQQ1	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4

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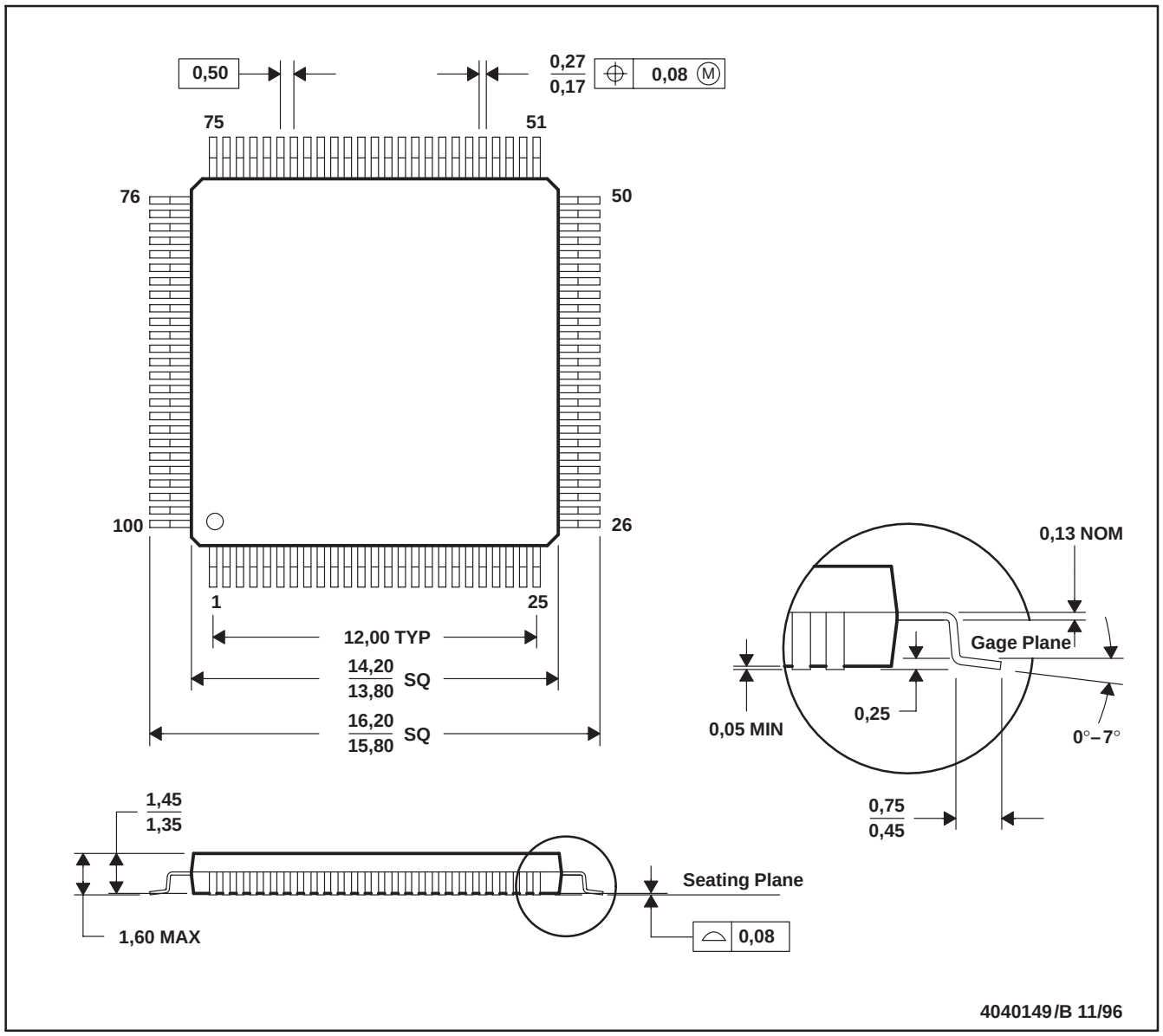
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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