

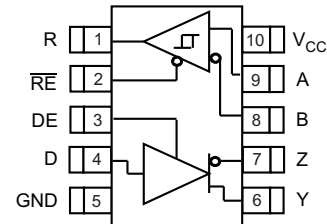
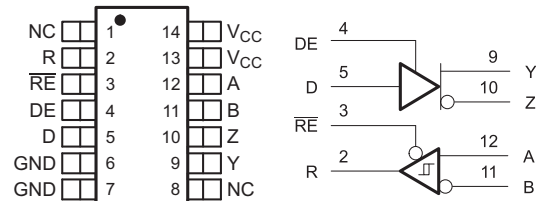


LOW-POWER RS-485 FULL-DUPLEX DRIVERS/RECEIVERS

 Check for Samples: [SN65HVD3080E](#), [SN65HVD3083E](#), [SN65HVD3086E](#)

FEATURES

- **Low Quiescent Power**
 - 375 μA (Typical) Enabled Mode
 - 2 nA (Typical) Shutdown Mode
- **Small MSOP Package**
- **1/8 Unit-Load—Up to 256 Nodes per Bus**
- **16 kV Bus-Pin ESD Protection, 6 kV All Pins**
- **Failsafe Receiver (Bus Open, Short, Idle)**
- **TIA/EIA-485A Standard Compliant**
- **RS-422 Compatible**
- **Power-Up, Power-Down Glitch-Free Operation**

**DGS PACKAGE
(TOP VIEW)**

**D PACKAGE
(TOP VIEW)**


NC - No internal connection
 Pins 6 and 7 are connected together internally
 Pins 13 and 14 are connected together internally

APPLICATIONS

- **Motion Controllers**
- **Point-of-Sale (POS) Terminals**
- **Rack-to-Rack Communications**
- **Industrial Networks**
- **Power Inverters**
- **Battery-Powered Applications**
- **Building Automation**

DESCRIPTION

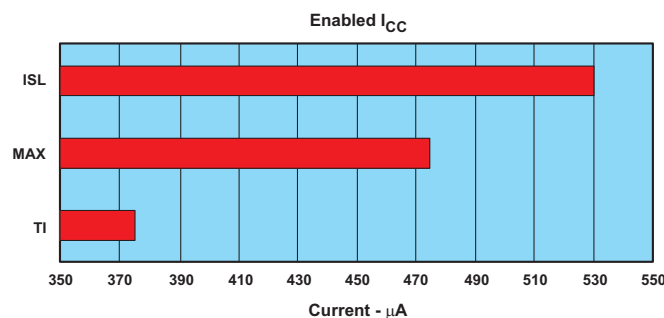
Each of these devices is a balanced driver and receiver designed for full-duplex RS-485 or RS-422 data bus networks. Powered by a 5-V supply, they are fully compliant with the TIA/EIA-485A standard.

With controlled bus output transition times, the devices are suitable for signaling rates from 200 kbps to 20 Mbps.

The devices are designed to operate with a low supply current, less than 1 mA (typical), exclusive of the load. When in the inactive shutdown mode, the supply current drops to a few nanoamps, making these devices ideal for power-sensitive applications.

The wide common-mode range and high ESD protection levels of these devices make them suitable for demanding applications such as motion controllers, electrical inverters, industrial networks, and cabled chassis interconnects where noise tolerance is essential.

These devices are characterized for operation over the temperature range -40°C to 85°C



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

| PART NUMBER | SIGNALING RATE | PACKAGE ⁽¹⁾ | MARKED AS |
|--------------|----------------|--------------------------------------|-----------|
| SN65HVD3080E | 200 kbps | DGS, DGSR 10-pin MSOP ⁽²⁾ | BTT |
| SN65HVD3083E | 1 Mbps | | BTU |
| SN65HVD3086E | 20 Mbps | | BTF |
| | | D 14-pin SOIC | HVD3086 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) The R suffix indicated tape and reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | | UNIT |
|---|---|----------------------------------|
| V _{CC} | Supply voltage range ⁽²⁾ | -0.3 V to 7 V |
| V _(A) , V _(B) , V _(Y) , V _(Z) | Voltage range at any bus terminal (A, B, Y, Z) | -9 V to 14 V |
| V _(TRANS) | Voltage input, transient pulse through 100 Ω. See Figure 10 (A, B, Y, Z) | -50 to 50 V |
| V _I | Input voltage range (D, DE, RE) | -0.3 V to V _{CC} +0.3 V |
| P _D | Continuous total power dissipation | See the dissipation rating table |
| T _J | Junction temperature | 170°C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

POWER DISSIPATION RATINGS

| PACKAGE | T _A < 25°C | DERATING FACTOR ⁽¹⁾ ABOVE T _A < 25°C | T _A = 85°C |
|-------------------|-----------------------|---|-----------------------|
| 10-pin MSOP (DGS) | 463 mW | 3.71 mW/°C | 241 mW |
| 14-pin SOIC (D) | 765 mW | 6.1 mW/°C | 400 mW |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

ELECTROSTATIC DISCHARGE PROTECTION

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|------------------|-----|-----|-----|------|
| Human Body Model ⁽¹⁾ | A,B,Y,Z, and GND | | 16 | | kV |
| | All pins | | 6 | | kV |
| Charged Device Mode ⁽²⁾ | All pins | | 1.5 | | kV |
| Machine Model ⁽³⁾ | All pins | | 400 | | V |

(1) Tested in accordance JEDEC Standard 22, Test Method A114-A. Bus pin stressed with respect to a common connection of GND and V_{CC}.

(2) Tested in accordance JEDEC Standard 22, Test Method C101.

(3) Tested in accordance JEDEC Standard 22, Test Method A115.

SUPPLY CURRENT

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|----------------|--|-----|-----|------|---------|
| I_{CC} | Supply current | \overline{RE} at 0 V, D and DE at V_{CC} , No load | | 375 | 750 | μA |
| | | \overline{RE} at 0 V, D and DE at 0 V, No load | | 300 | 680 | μA |
| | | \overline{RE} at V_{CC} , D and DE at V_{CC} , No load | | 240 | 600 | μA |
| | | \overline{RE} and D at V_{CC} , DE at 0 V, No load | | 2 | 1000 | nA |

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

| | | MIN | NOM | MAX | UNIT | |
|-------------------|---|--|-----|----------|-------------|----|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V | |
| V_I or V_{IC} | Voltage at any bus terminal (separately or common mode) | $-7^{(1)}$ | | 12 | V | |
| V_{IH} | High-level input voltage | D, DE, \overline{RE} | | V_{CC} | V | |
| V_{IL} | Low-level input voltage | D, DE, \overline{RE} | | 0.8 | V | |
| V_{ID} | Differential input voltage | | | -12 | 12 | V |
| | | Dynamic, See Figure 11 | | | | V |
| I_{OH} | High-level output current | Driver | | -60 | | mA |
| | | Receiver | | -10 | | |
| I_{OL} | Low-level output current | Driver | | | 60 | mA |
| | | Receiver | | | 10 | |
| T_J | Junction temperature | | | 150 | $^{\circ}C$ | |
| T_A | Ambient still-air temperature | -40 | | 85 | | |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|--|-----|-----------------|------|
| V _{OD} | Differential output voltage | No load, I _O = 0 | 3 | 4.3 | V _{CC} | V |
| | | R _L = 54 Ω, See Figure 1 | 1.5 | 2.3 | | |
| | | V _{test} = -7 V to 12 V, See Figure 2 | 1.5 | | | |
| | | R _L = 100 Ω, See Figure 1 | 2 | | | |
| Δ V _{OD} | Change in magnitude of differential output voltage | R _L = 54 Ω, See Figure 1 and Figure 2 | -0.2 | 0 | 0.2 | V |
| V _{OC(SS)} | Steady-state common-mode output voltage | See Figure 3 | 1 | 2.6 | 3 | V |
| ΔV _{OC(SS)} | Common-mode output voltage (Dominant) | | -0.1 | 0 | 0.1 | |
| V _{OC(PP)} | Peak-to-peak common-mode output voltage | | 0.5 | | | |
| I _{Z(Y)} or I _{Z(Z)} | High-impedance state output current | | V _{CC} = 0 V, V _(Z) or V _(Y) = 12 V Other input at 0 V | | | |
| | | V _{CC} = 0 V, V _(Z) or V _(Y) = -7 V Other input at 0 V | -1 | | | |
| | | V _{CC} = 5 V, V _(Z) or V _(Y) = 12 V Other input at 0 V | | | 1 | |
| | | V _{CC} = 5 V, V _(Z) or V _(Y) = -7 V Other input at 0 V | -1 | | | |
| I _I | Input current | D, DE | -100 | | 100 | μA |
| I _{OS} | Short-circuit output current | -7 V ≤ V _O ≤ 12 V | -250 | | 250 | mA |

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|---|---|---|-----|-----|------|----|
| t _{PLH} , t _{PHL} | Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output | HVD3080E | | 0.7 | 1.3 | μs | |
| | | HVD3083E | | 150 | 500 | ns | |
| | | HVD3086E | | 12 | 20 | ns | |
| t _r , t _f | Differential output signal rise time Differential output signal fall time | HVD3080E | R _L = 54 Ω, C _L = 50 pF, See Figure 4 | 0.5 | 0.9 | 1.5 | μs |
| | | HVD3083E | | 200 | 300 | ns | |
| | | HVD3086E | | 7 | 15 | ns | |
| t _{sk(p)} | Pulse skew (t _{PHL} - t _{PLH}) | HVD3080E | | 20 | 200 | ns | |
| | | HVD3083E | | 5 | 50 | ns | |
| | | HVD3086E | | 1.4 | 5 | ns | |
| t _{PZH} | Propagation delay time, high-impedance-to-high-level output | HVD3080E | R _L = 110 Ω, R _E at 0 V, See Figure 5 | 2.5 | 7 | μs | |
| | | HVD3083E | | 1 | 2.5 | μs | |
| | | HVD3086E | | 13 | 30 | ns | |
| t _{PHZ} | Propagation delay time, high-level-to-high-impedance output | HVD3080E | | 80 | 200 | ns | |
| | | HVD3083E | | 60 | 100 | ns | |
| | | HVD3086E | | 12 | 30 | ns | |
| t _{PZL} | Propagation delay time, high-impedance-to-low-level output | HVD3080E | | 2.5 | 7 | μs | |
| | | HVD3083E | | 1 | 2.5 | μs | |
| | | HVD3086E | | 13 | 30 | ns | |
| t _{PLZ} | Propagation delay time, low-level-to-high-impedance output | HVD3080E | | 80 | 200 | ns | |
| | | HVD3083E | | 60 | 100 | ns | |
| | | HVD3086E | | 12 | 30 | ns | |
| t _{PZH} , t _{PZL} | Propagation delay time, standby-to-high-level output (See Figure 5) Propagation delay time, standby-to-low-level output (See Figure 6) | R _L = 110 Ω, R _E at 3 V | | 3.5 | 7 | μs | |

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|------------------|---|---|--|--------------------|-------|-------|----|
| V _{IT+} | Positive-going differential input threshold voltage | I _O = -10 mA | -0.08 | | -0.01 | V | |
| V _{IT-} | Negative-going differential input threshold voltage | I _O = 10 mA | -0.2 | -0.1 | | | |
| V _{hys} | Hysteresis voltage (V _{IT+} - V _{IT-}) | | | 30 | | mV | |
| V _{OH} | High-level output voltage | V _{ID} = 200 mV, I _{OH} = -10 mA, See Figure 7 and Figure 8 | 4 | 4.6 | | V | |
| V _{OL} | Low-level output voltage | V _{ID} = -200 mV, I _{OH} = 10 mA, See Figure 7 and Figure 8 | | 0.15 | 0.4 | V | |
| I _{OZ} | High-impedance-state output current | V _O = 0 or V _{CC} | -1 | | 1 | μA | |
| I _I | Bus input current | Other input at 0V | V _A or V _B = 12 V | | 0.04 | 0.11 | mA |
| | | | V _A or V _B = 12 V, V _{CC} = 0 V | | 0.06 | 0.13 | |
| | | | V _A or V _B = -7 V | | -0.1 | -0.04 | |
| | | | V _A or V _B = -7 V, V _{CC} = 0 V | | -0.05 | -0.03 | |
| I _{IH} | High-level input current | V _{IH} = 2 V | -60 | -30 | | μA | |
| I _{IL} | Low-level input current | V _{IL} = 0.8 V | -60 | -30 | | μA | |
| C _{ID} | Differential input capacitance | V _I = 0.4 sin (4E6πt) + 0.5 V | | 7 | | pF | |

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|-----|-----|-----|------|
| t _{PLH} | Propagation delay time, low-to-high-level output | V _{ID} = -1.5 V to 1.5 V, C _L = 15 pF, See Figure 8 | | 75 | 100 | ns |
| t _{PHL} | Propagation delay time, high-to-low-level output | | | 79 | 100 | |
| t _{sk(p)} | Pulse skew ((t _{PHL} - t _{PLH})) | | | 4 | 10 | |
| t _r | Output signal rise time | | | 1.5 | 3 | |
| t _f | Output signal fall time | | | 1.8 | 3 | |
| t _{PZH} , t _{PZL} | Output enable time | DE at V _{CC} , See Figure 9 | | 10 | 50 | ns |
| | | From standby DE at GND, See Figure 9 | | 1.7 | 3.5 | μs |
| t _{PHZ} , t _{PLZ} | Output disable time | DE at GND or V _{CC} , See Figure 9 | | 7 | 50 | ns |

PARAMETER MEASUREMENT INFORMATION

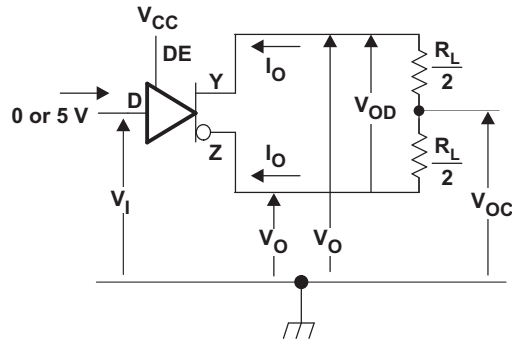


Figure 1. Driver V_{OD} Test Circuit and Current Definitions

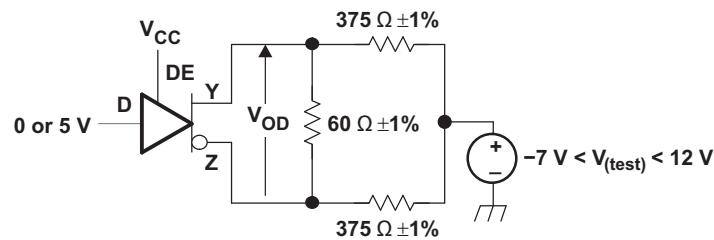


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

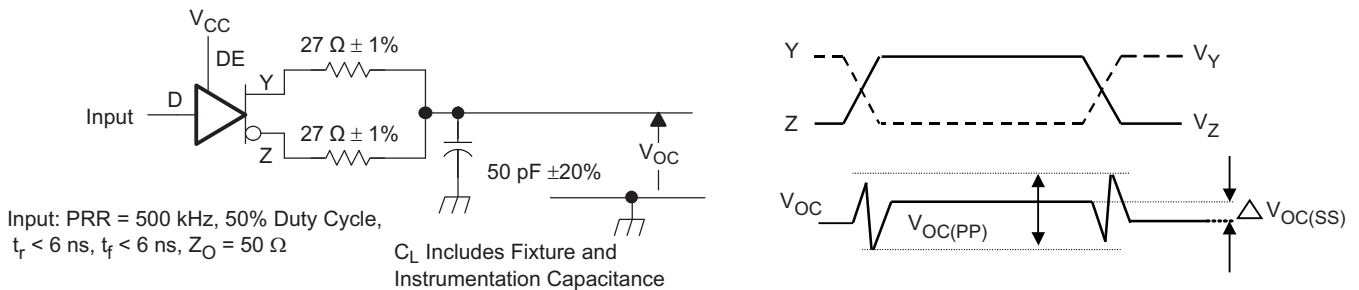


Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

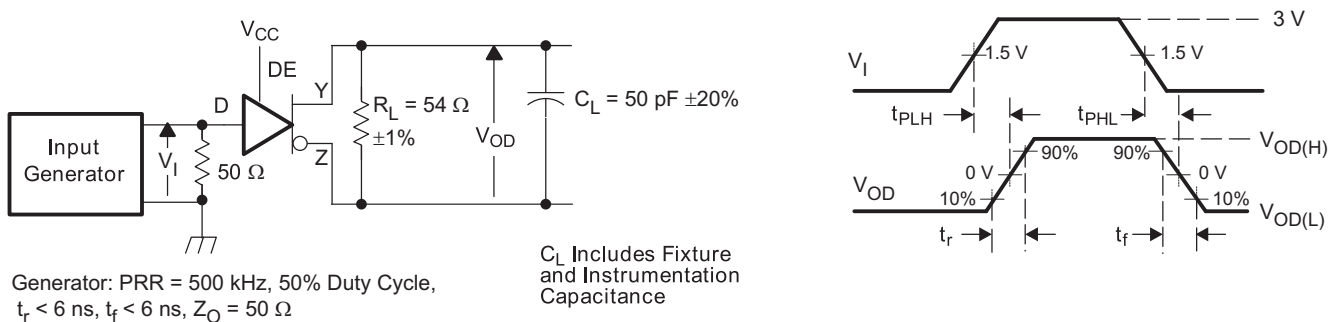


Figure 4. Driver Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

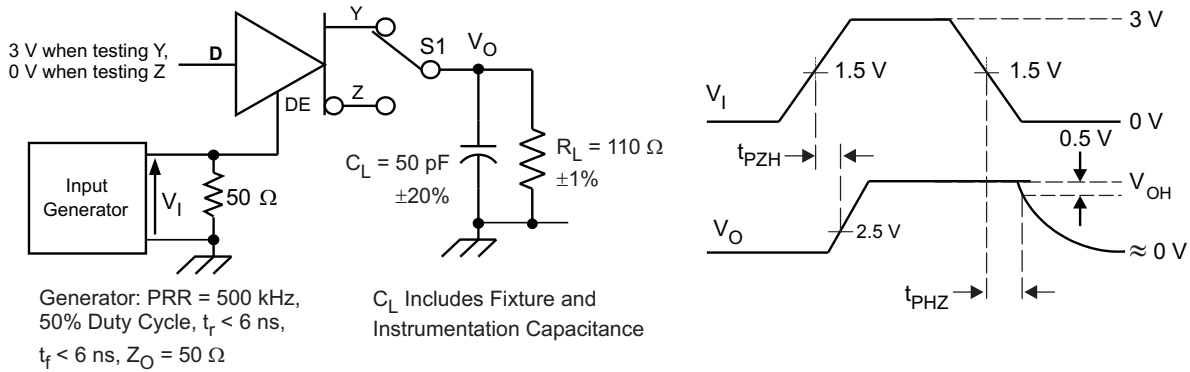


Figure 5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

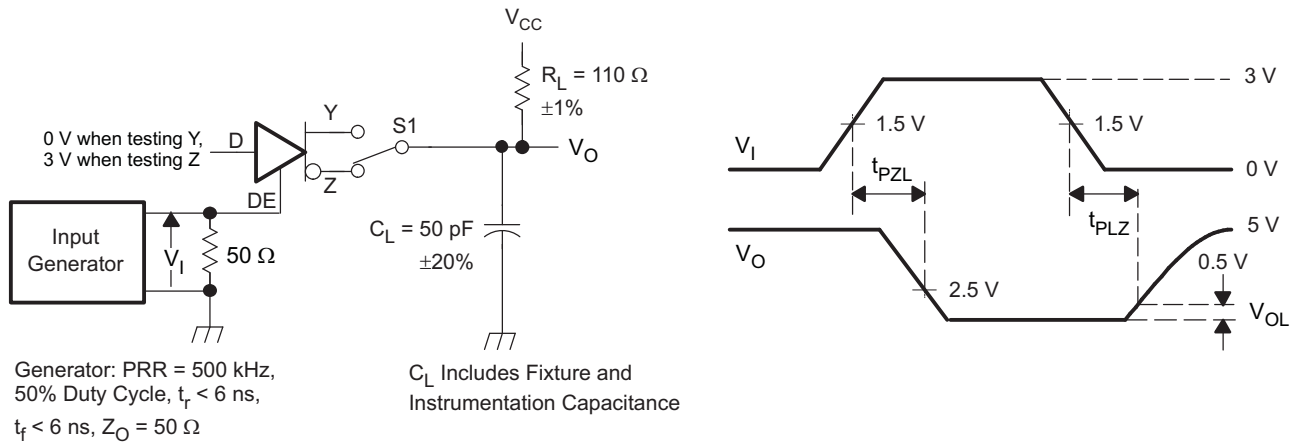


Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

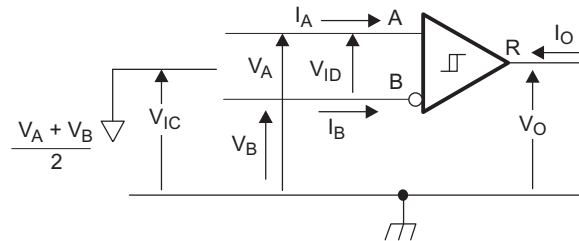


Figure 7. Receiver Voltage and Current Definitions

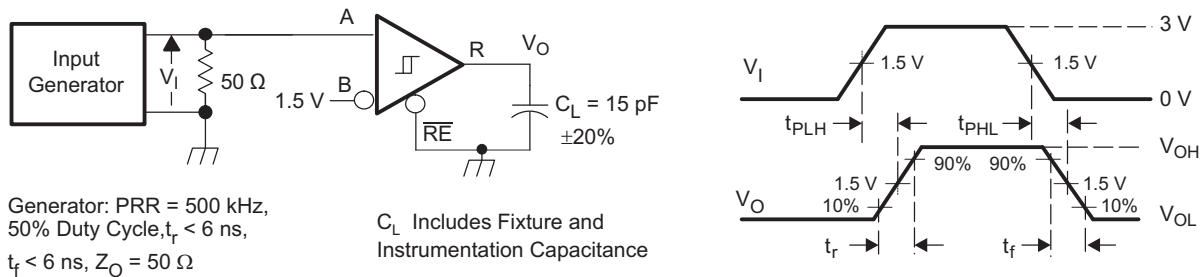


Figure 8. Receiver Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

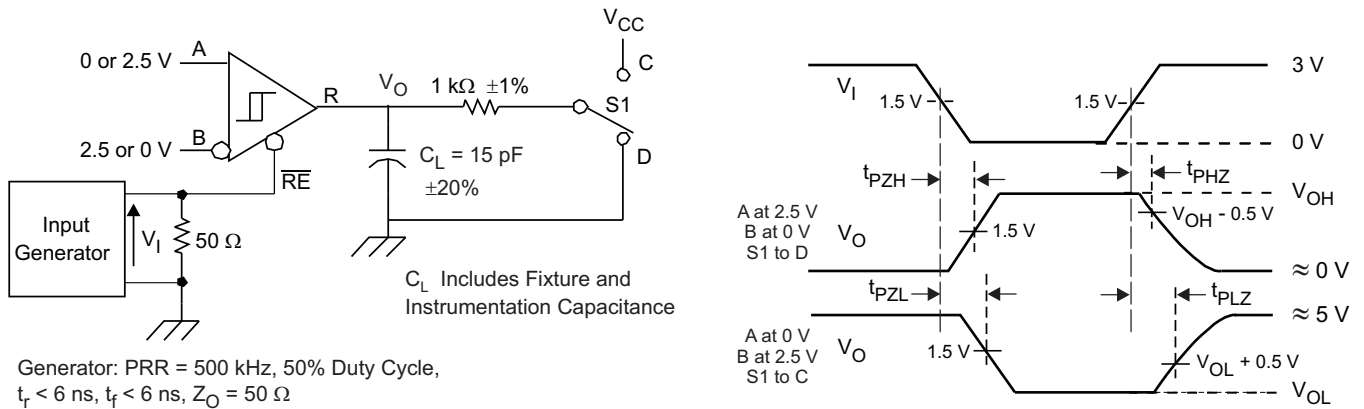
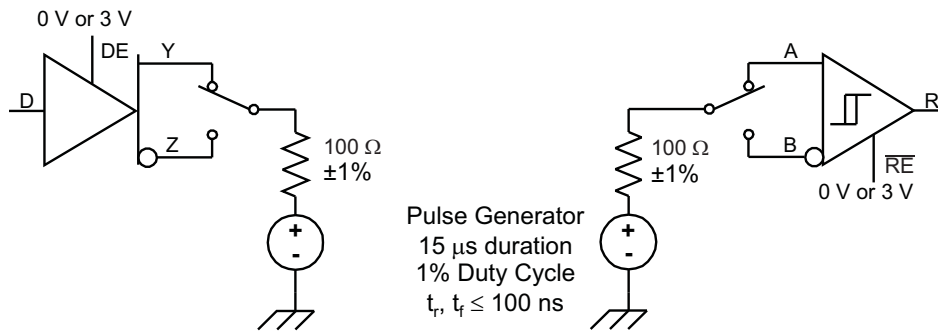


Figure 9. Receiver Enable and Disable Test Circuit and Voltage Waveforms



A. This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 10. Transient Overvoltage Test Circuit

DEVICE INFORMATION

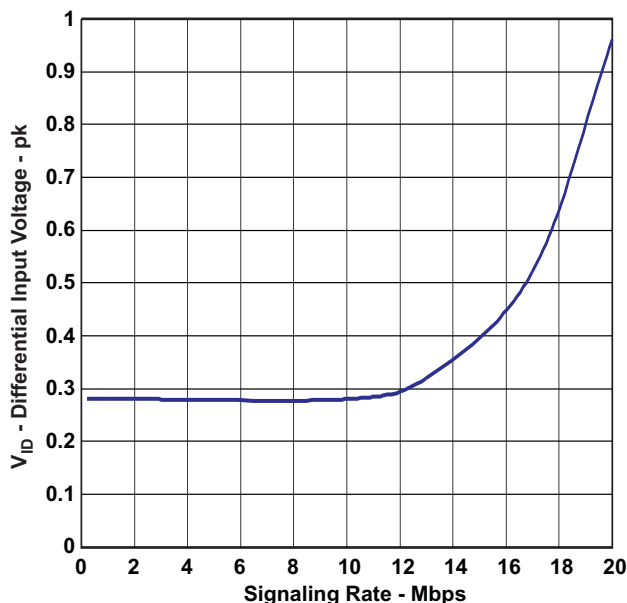


Figure 11. Recommended Minimum Differential Input Voltage vs Signaling Rate

FUNCTION TABLES

DRIVER⁽¹⁾

| INPUT | ENABLE | OUTPUTS | |
|-------|-----------|---------|---|
| D | DE | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L or OPEN | Z | Z |
| Open | H | H | L |

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

RECEIVER⁽¹⁾

| DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$ | ENABLE \overline{RE} | OUTPUT R |
|---|---------------------------|-------------|
| $V_{ID} \leq -0.2\text{ V}$ | L | L |
| $-0.2\text{ V} < V_{ID} < -0.01\text{ V}$ | L | ? |
| $-0.01\text{ V} \leq V_{ID}$ | L | H |
| X | H or OPEN | Z |
| Open Circuit | L | H |
| BUS Idle | L | H |
| Short Circuit | L | H |

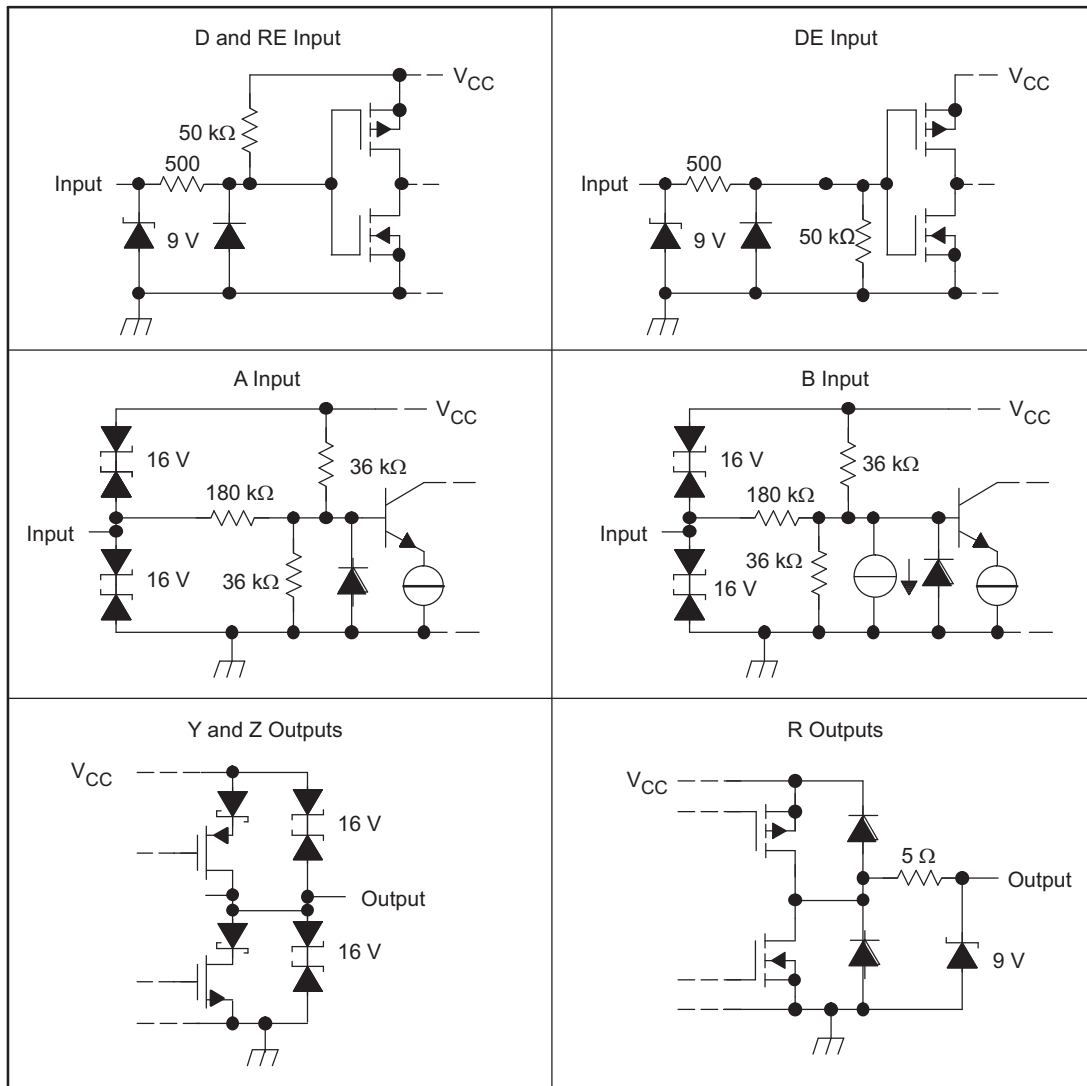
(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

DEVICE ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| | PARAMETERS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|---------------------------|---|-----|-----|-----|------|
| $P_{(AVG)}$ | Average power dissipation | $R_L = 60 \Omega$, Input to D a 500-kHz 50% duty cycle square-wave | 85 | 109 | 136 | mW |

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

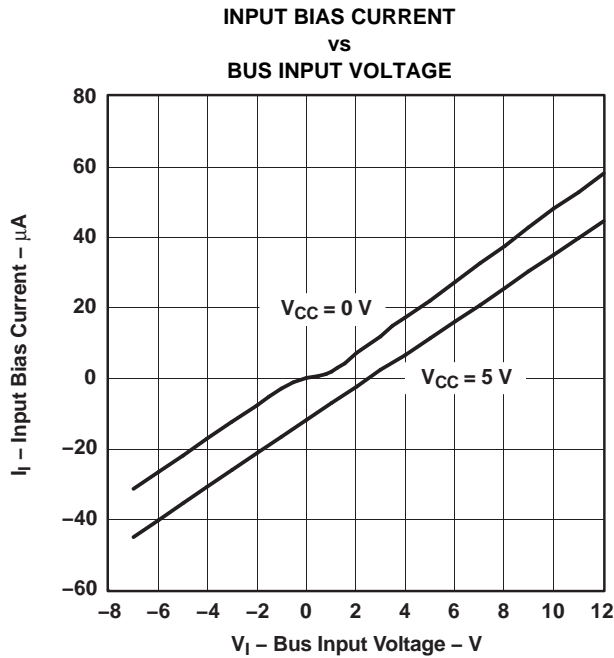


Figure 12.

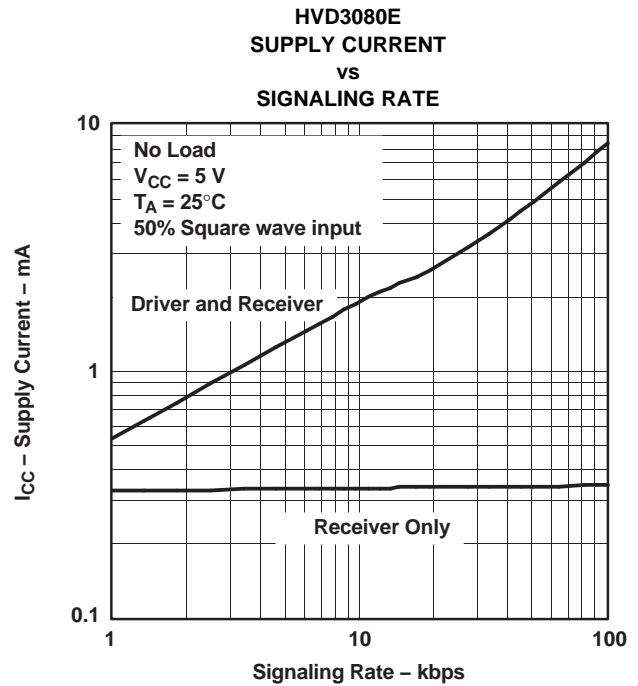


Figure 13.

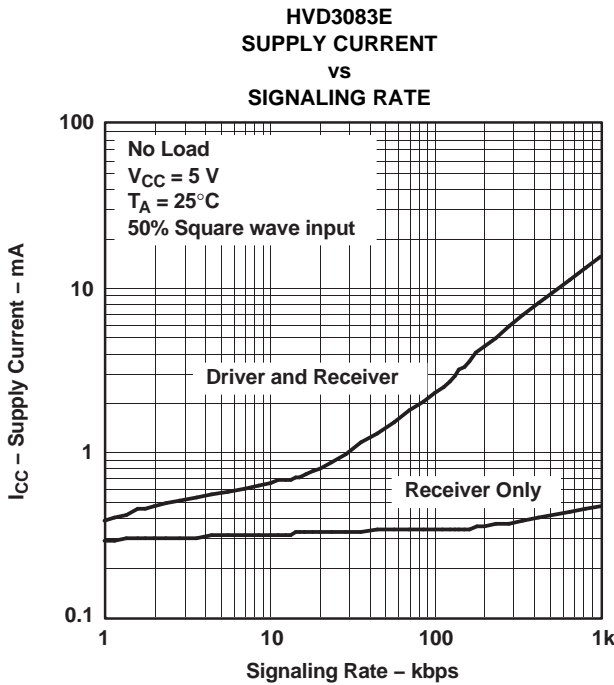


Figure 14.

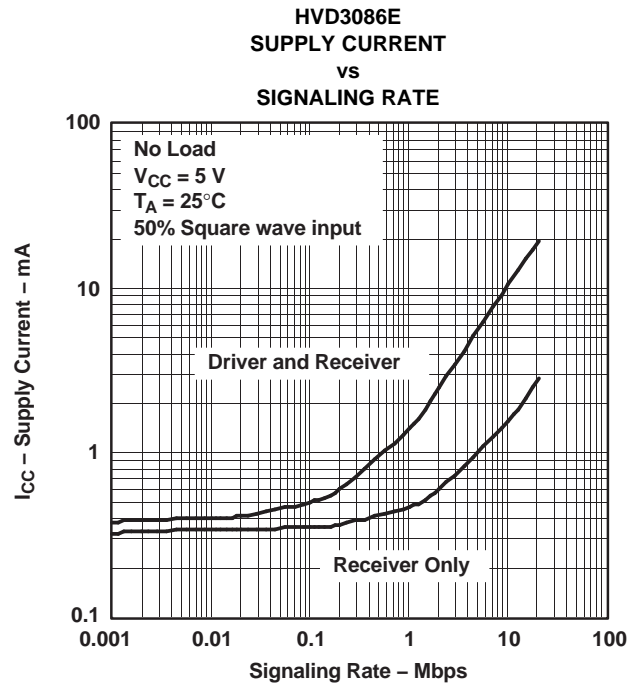
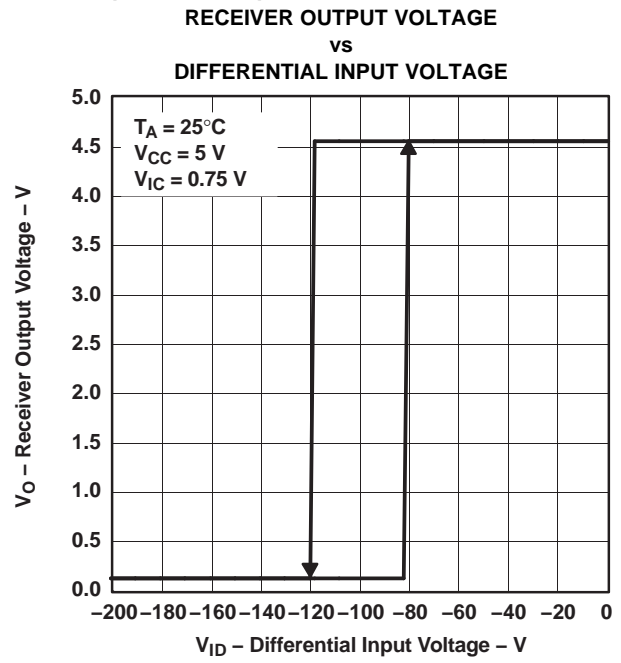
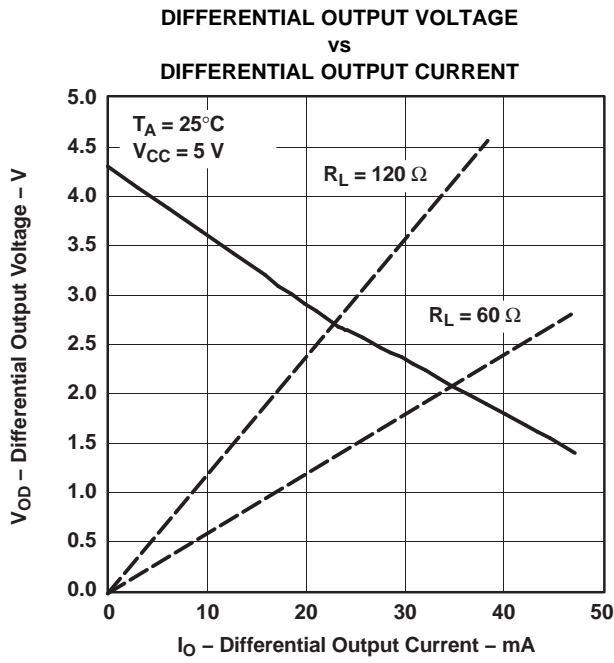


Figure 15.

TYPICAL CHARACTERISTICS (continued)



APPLICATION INFORMATION

Hot-Plugging

These devices are designed to operate in “hot swap” or “hot pluggable” applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. An internal Power-On Reset circuit keeps the outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device FUNCTION TABLES, the ENABLE inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

REVISION HISTORY

Changes from Revision B (March 2007) to Revision C Page

| | |
|--|---|
| • Added D package | 1 |
| • Added D package and information to Ordering Information | 2 |
| • Added D package information to Power Dissipation Ratings | 2 |
| • Changed Electrostatic Discharge Protection | 2 |
| • Changed Supply Current information | 3 |
| • Changed Receiver Switching Characteristics | 5 |
| • Changed Figure 5 | 7 |
| • Changed Figure 6 | 7 |

Changes from Revision C (December 2009) to Revision D Page

| | |
|--|---|
| • Added Differential input voltage dynamic to RECOMMENDED OPERATING CONDITIONS | 3 |
| • Added Figure 11 | 9 |

Changes from Revision D (January 2011) to Revision E Page

| | |
|---|----|
| • Added Power-Up, Power-Down Glitch-Free Operation to FEATURES | 1 |
| • Changed ENABLE in DRIVER FUNCTION TABLE from L to L or OPEN | 9 |
| • Changed ENABLE in RECEIVER FUNCTION TABLE from H to H or OPEN | 9 |
| • Added APPLICATION INFORMATION section | 13 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65HVD3080EDGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | Call TI NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BTT | Samples |
| SN65HVD3080EDGSG4 | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BTT | Samples |
| SN65HVD3080EDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BTT | Samples |
| SN65HVD3083EDGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BTU | Samples |
| SN65HVD3083EDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | Call TI NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BTU | Samples |
| SN65HVD3086ED | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HVD3086E | Samples |
| SN65HVD3086EDGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | Call TI NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BTF | Samples |
| SN65HVD3086EDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BTF | Samples |
| SN65HVD3086EDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HVD3086E | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65HVD3080EDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD3086EDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65HVD3086EDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65HVD3080EDGSR | VSSOP | DGS | 10 | 2500 | 356.0 | 356.0 | 35.0 |
| SN65HVD3086EDGSR | VSSOP | DGS | 10 | 2500 | 356.0 | 356.0 | 35.0 |
| SN65HVD3086EDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65HVD3080EDGS | DGS | VSSOP | 10 | 80 | 330.2 | 6.6 | 3005 | 1.88 |
| SN65HVD3080EDGSG4 | DGS | VSSOP | 10 | 80 | 330.2 | 6.6 | 3005 | 1.88 |
| SN65HVD3083EDGS | DGS | VSSOP | 10 | 80 | 330.2 | 6.6 | 3005 | 1.88 |
| SN65HVD3086ED | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN65HVD3086EDGS | DGS | VSSOP | 10 | 80 | 330.2 | 6.6 | 3005 | 1.88 |

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

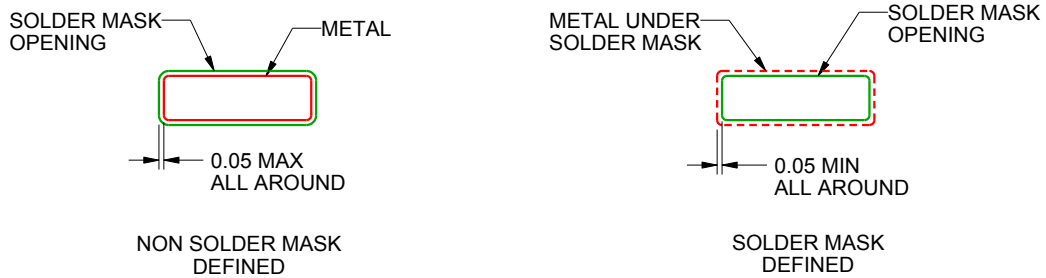
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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