低功耗差动线路驱动器和接收器对

1 特性

- 专为通过长电缆进行高速多点数据传输而设计
- 以低至 30ns 的脉冲宽度运行
- 低电源电流：5 mA（最大值）
- 符合或超出 ANSI RS-485 和 ISO 8482:1987(E) 的标准要求
- -7V 至 12V 的共模电压范围
- 正负输出电流限制
- 驱动器热关断保护
- 引脚与 SN75179B 兼容

2 说明

SN65LBC179、SN65LBC179Q 和 SN75LBC179 差分驱动器和接收器对是单片集成电路，设计用于通过具有传输线特性的长电缆进行双向数据通信。这些器件是平衡或差分电压模式器件，符合或超过行业标准 ANSIRS-485 和 ISO 8482:1987(E) 的要求。这两款器件采用 TI 专有 LinBiCMOS™ 进行设计，具有 CMOS 的低功耗以及同一电路中双极晶体管的精度和稳健性。

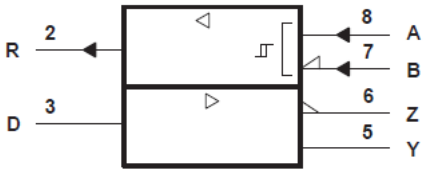
SN65LBC179、SN65LBC179Q 和 SN75LBC179 整合了差分线路驱动器和差分线路接收器，并采用 5V 单电源供电。驱动器差分输出和接收器差分输入连接到单独的端子以实现全双工工作，并且用于在断电 (V_{CC} = 0) 时为总线提供最小负载。这些器件具有宽共模电压范围，使其适用于点对点或多点数据总线应用。这些器件还提供正负电流限制和热关断功能，避免出现线路故障状况。线路驱动器在结温约为 172°C 时关闭。

SN65LBC179、SN65LBC179Q 和 SN75LBC179 采用 8 引脚双列直插式和小外形封装。SN75LBC179 可在 0°C 至 70°C 的商业温度范围内运行。SN65LBC179 的额定工业温度范围为 −40°C 至 85°C。SN65LBC179Q 可在 −40°C 至 125°C 的扩展工业或汽车温度范围内运行。

封装信息

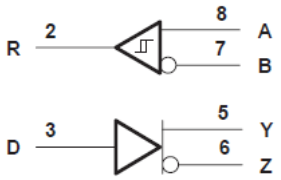
器件型号	封装(1)	封装尺寸（标称值）
SN75179B	D (SOIC)	4.9 mm x 3.91 mm
	P (PDIP)	9.81mm x 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



A. 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

逻辑符号



逻辑图（正逻辑）

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3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (April 2006) to Revision G (October 2022)	Page
• 将数据表格式更改为最新的数据表格式	1
• Added the *Thermal Information* table	5

4 Pin Configuration and Functions

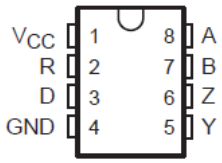


图 4-1. D or P Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1	V_{CC}	P	5 V Voltage Supply
2	R	O	RS485 Logic Output
3	D	I	RS485 Logic Input
4	GND	G	Ground
5	Y	O	Non-Inverting RS485 Bus Output
6	Z	O	Inverted RS485 Bus Output
7	B	I	Inverted RS485 Bus Input
8	A	I	Non-Inverting RS485 Bus Input

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

See note (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.3	7	V
	Voltage range at A, B, Y, or Z(2)	-10	15	V
	Voltage range at D or R(2)	-0.3	V_{CC} + 0.5	V
I_O	Receiver output current		±10	mA
	Continuous total power dissipation(3)	Internally limited		
$P_{(AVG)}$	Average power dissipation R_L = 54 Ω, input to D is 10 Mbps 50% duty cycle square wave, V_{CC} = 5.25 V, T_J = 130°C		330	mW
T_{SD}	Thermal shutdown junction temperature		165	°C
	Total power dissipation	See 节 5.4		

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) The maximum operating junction temperature is internally limited. Uses the dissipation rating table to operate below this temperature.

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	D	2			V
V_{IL}	Low-level input voltage	D			0.8	V
V_{ID}	Differential input voltage		−6(1)		6	V
V_O, V_I, or V_{IC}	Voltage at any bus terminal (separately or common-mode)	A, B, Y, or Z	−7		12	V
I_{OH}	High-level output current	Y or Z			−60	mA
		R			−8	
I_{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T_J	Junction temperature				140	°C
T_A	Operating free-air temperature	SN65LBC179	−40		85	°C
		SN65LBC179Q	−40		125	
		SN75LBC179	0		70	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for differential input voltage, voltage at any bus terminal (separately or common mode), operating temperature, input threshold voltage, and common-mode output voltage.

5.3 Thermal Information

THERMAL METRIC(1)		D (SOIC)	P (PDIP)	UNIT
		8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	65.6.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.4	54.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.3	42.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	22.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	41.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) See TI application note literature number SZZA003, Package Thermal Characterization Methodologies, for an explanation of this parameter.

5.4 Dissipation Rating Table

PACKAGE	THERMAL MODEL	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	Low K(1)	526 mW	5.0 mW/°C	301 mW	226 mW
		882 mW	8.4 mW/°C	504 mW	378 mW
P	High K(2)	840 mW	8.0 mW/°C	480 mW	360 mW

(1) In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51−3.
(2) In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51−7.

5.5 Electrical Characteristics - Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I= − 18 mA				−1.5	V
$\|V_{OD}\|$	Differential output voltage(2)	R_L = 54 Ω See 图 6-1	SN65LBC179, SN65LBC179Q	1.1	2.2	5	V
			SN75LBC179	1.5	2.2	5	
		R_L = 60 Ω See 图 6-2	SN65LBC179, SN65LBC179Q	1.1	2.2	5	
			SN75LBC179	1.5	2.2	5	
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(3)	See 图 6-1 and 图 6-2				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω	See 图 6-1	1	2.5	3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = − 7 V to 12 V			±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				−100	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	μA
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V				±250	mA
I_{CC}	Supply current	No load	SN65LBC179, SN75LBC179		4.2	5	mA
			SN65LBC179Q		4.2	7	mA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The minimum V_{OD} specification of the SN65179 may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal transmission distance.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

5.6 Switching Characteristics - Driver

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω	See 图 6-3	7	18	ns
$t_{t(OD)}$	Differential transition time			5	20	ns

5.7 Electrical Characteristics - Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = − 8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		−0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} − V_{IT-})				45		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = − 8 mA	3.5	4.5		V
V_{OL}	Low-level output voltage	V_{ID} = − 200 mV,	I_{OL} = 8 mA		0.3	0.5	V
I_I	Bus input current	V_I = 12 V, Other inputs at 0 V,	SN65LBC179, SN75LBC179		0.7	1	mA
		V_{CC} = 5 V	SN65LBC179Q		0.7	1.2	mA
		V_I = 12 V, Other inputs at 0 V,	SN65LBC179, SN75LBC179		0.8	1	mA
		V_{CC} = 0 V	SN65LBC179Q		0.8	1.2	mA
		V_I = − 7 V, Other inputs at 0 V,	SN65LBC179, SN75LBC179		−0.5	−0.8	mA
		V_{CC} = 5 V	SN65LBC179Q		−0.5	−1.0	mA
		V_I = − 7 V, Other inputs at 0 V,	SN65LBC179, SN75LBC179		−0.5	−0.8	mA
		V_{CC} = 0 V	SN65LBC179Q		−0.5	−1.0	mA

5.8 Switching Characteristics - Receiver

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V,	See 图 6-4	15		30	ns
t_{PLH}	Propagation delay time, low- to high-level output			15		30	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See 图 6-4			3	6	ns
t_t	Transition time				3	5	ns

5.9 Typical Characteristics

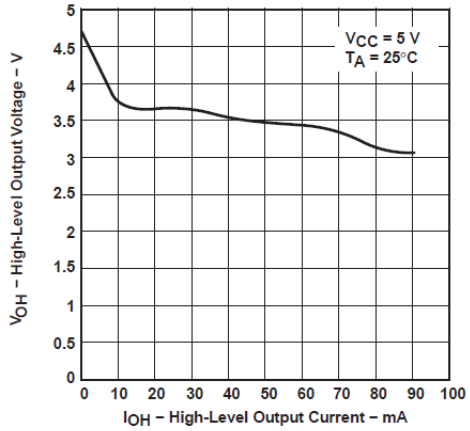


图 5-1. Driver High-Level Output Voltage vs High-Level Output Current

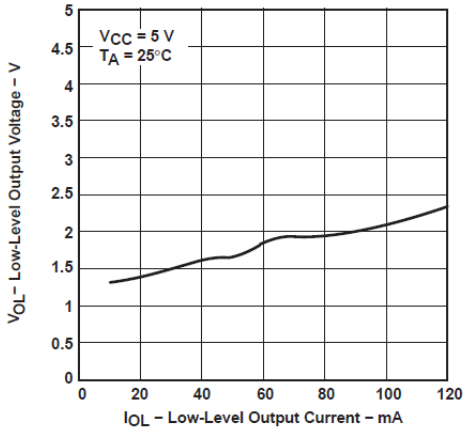


图 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current

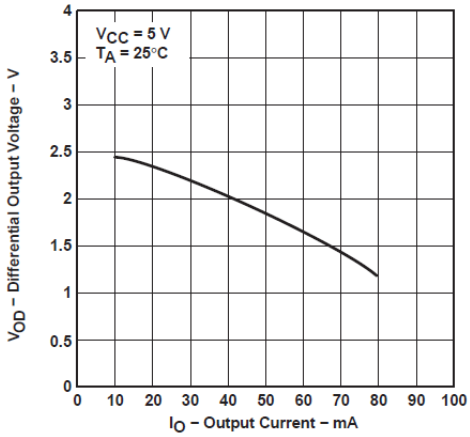


图 5-3. Driver Differential Output Voltage vs Output Current

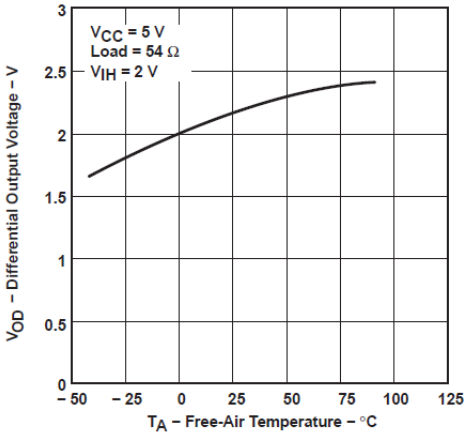


图 5-4. Driver Differential Output Voltage vs Free-Air Temperature

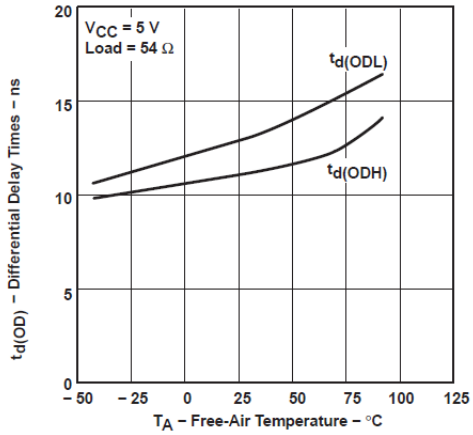


图 5-5. Driver Differential Delay Time vs Free-Air Temperature

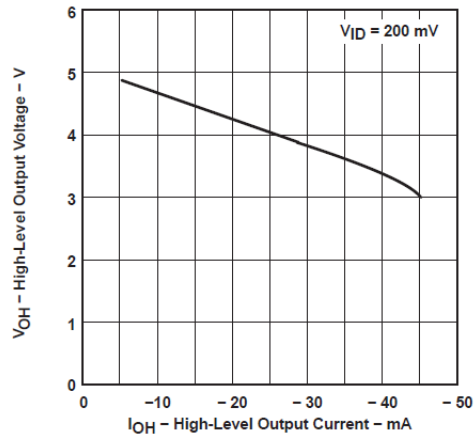


图 5-6. Receiver High-Level Output Voltage vs High-Level Output Current

5.9 Typical Characteristics (continued)

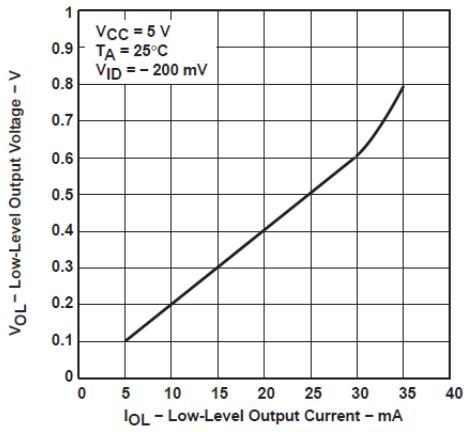


图 5-7. Receiver Low-Level Output Voltage vs Low-Level Output Current

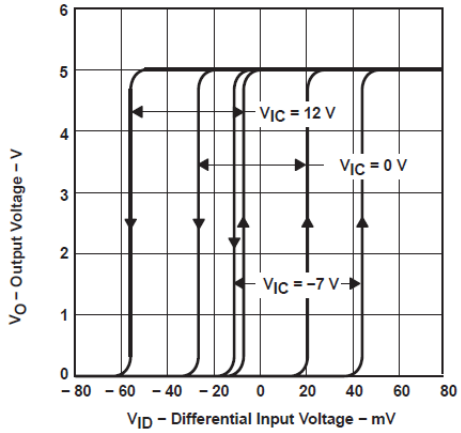


图 5-8. Receiver Output Voltage vs Differential Input Voltage

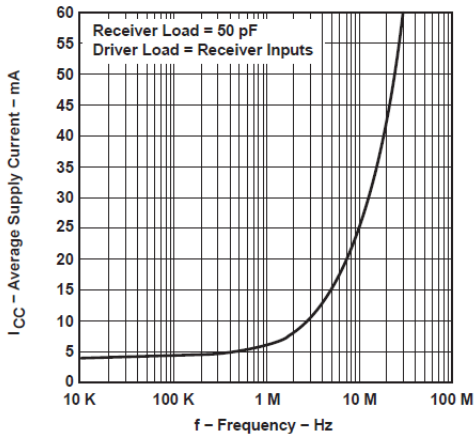


图 5-9. Average Supply Current vs Frequency

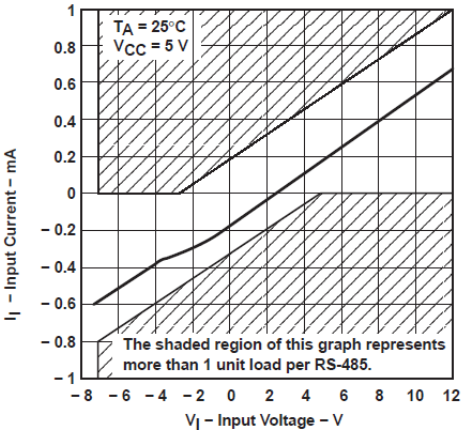


图 5-10. Receiver Input Current vs Input Voltage (Complementary Input at 0 V)

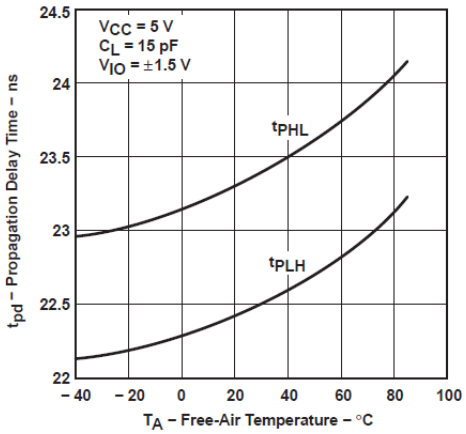


图 5-11. Receiver Propagation Delay Time vs Free-Air Temperature

6 Parameter Measurement Information

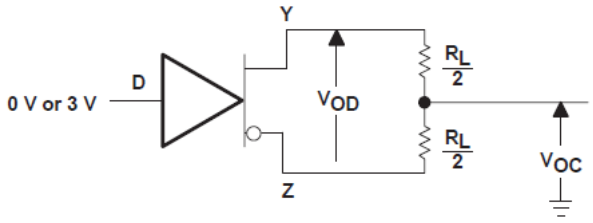


图 6-1. Differential and Common-Mode Output Voltage Test Circuit

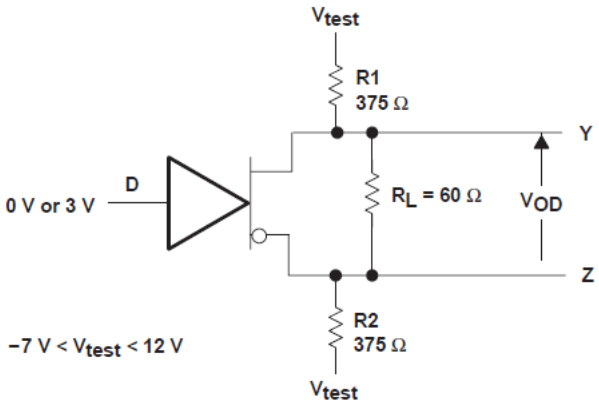
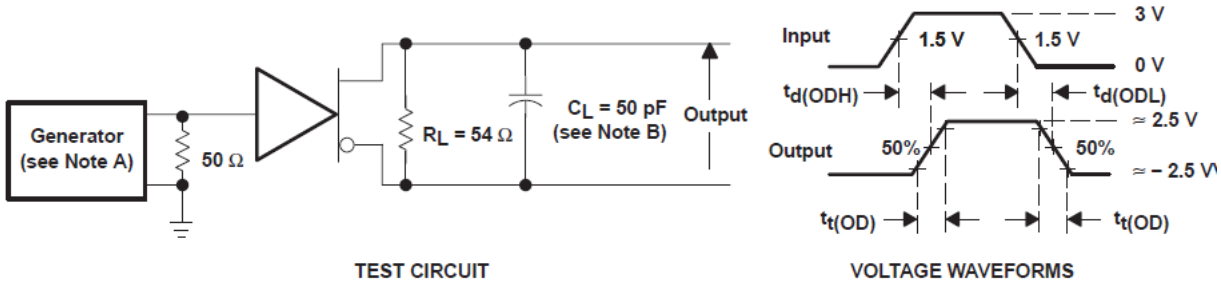


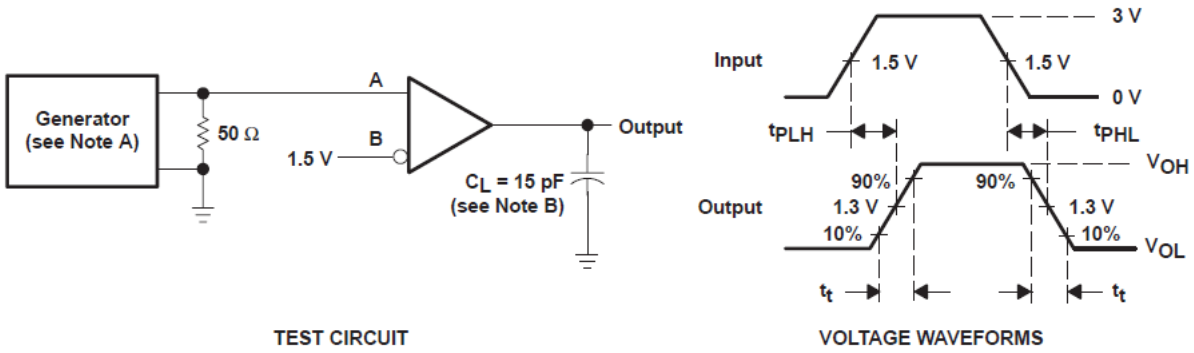
图 6-2. Differential Output Voltage Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

图 6-3. Driver Test Circuits and Differential Output Delay and Transition Time Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f⩽ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

图 6-4. Receiver Test Circuit and Propagation Delay and Transition Time Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

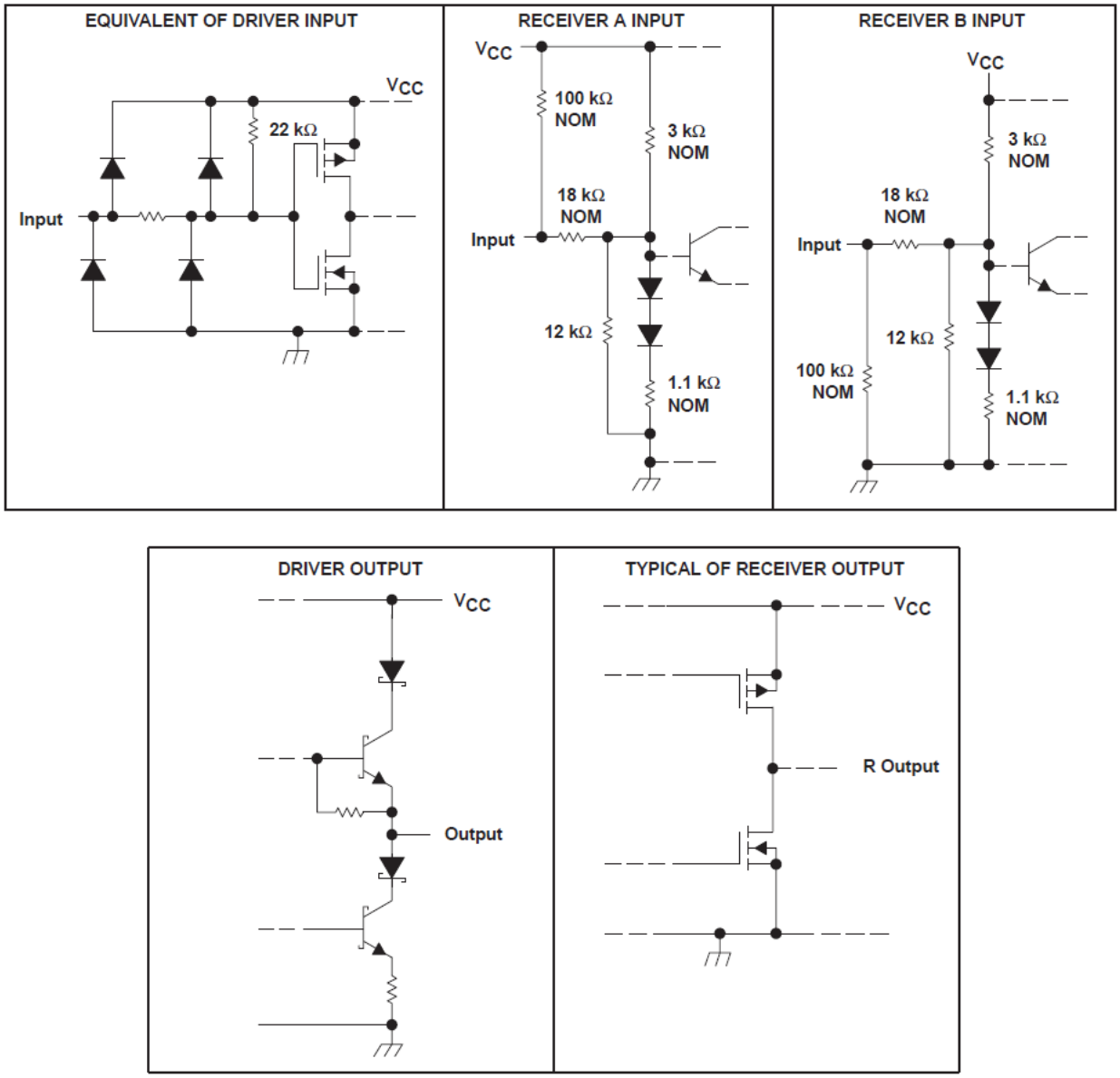


图 7-1. Schematics of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

表 7-1. Driver(1)

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H

(1) H = high level, L = low level, ? = indeterminate

表 7-2. Receiver(1)

DIFFERENTIAL INPUTS A−B	OUTPUT R
$V_{ID} \geqslant 0.2$ V	H
−0.2 V < V_{ID} < 0.2 V	?
$V_{ID} \leqslant -0.2$ V	L
Open circuit	H

(1) H = high level, L = low level, ? = indeterminate

7.3 Thermal Characteristics of IC Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is not a constant and is a strong function of:

- the PCB design (50% variation
- altitude (20% variation)
- device power (5% variation

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in−use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is not a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{jb} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. θ_{jb} is only defined for the high-k test card.

θ_{JB} provide an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGAs with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see 图 7-2).

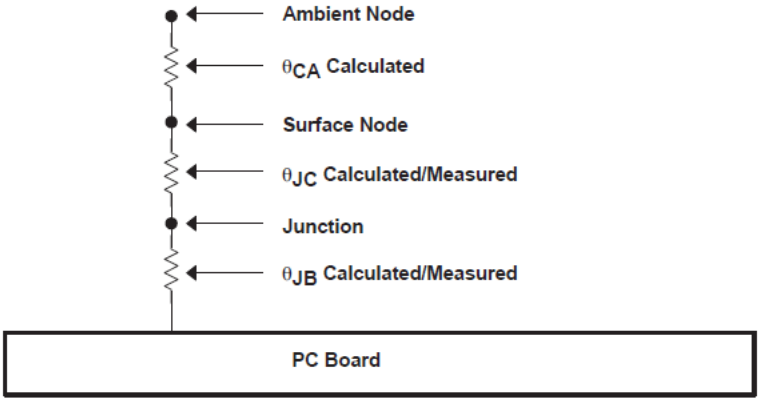


图 7-2. Thermal Resistance

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.2 Documentation Support

8.2.1 Related Documentation

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.5 Trademarks

LinBiCMOS™ is a trademark of LinBiCMOS.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC179D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB179	
SN65LBC179DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB179	Samples
SN65LBC179DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB179	Samples
SN65LBC179P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC179	Samples
SN65LBC179QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q	Samples
SN65LBC179QDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q	Samples
SN65LBC179QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q	Samples
SN65LBC179QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q	Samples
SN75LBC179D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB179	
SN75LBC179DR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB179	
SN75LBC179DRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB179	
SN75LBC179P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC179	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

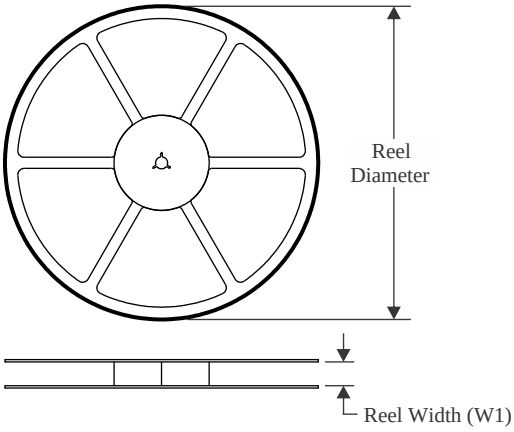
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

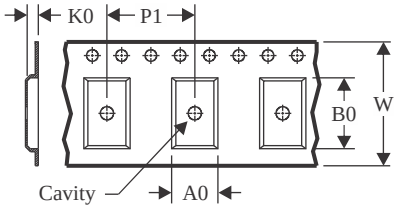
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

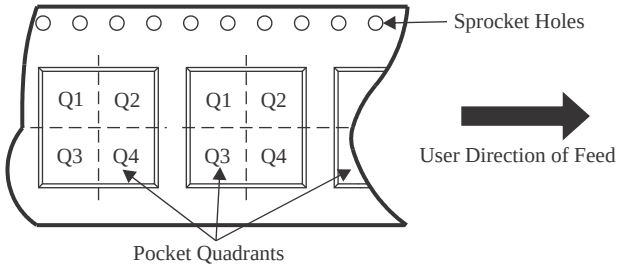


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

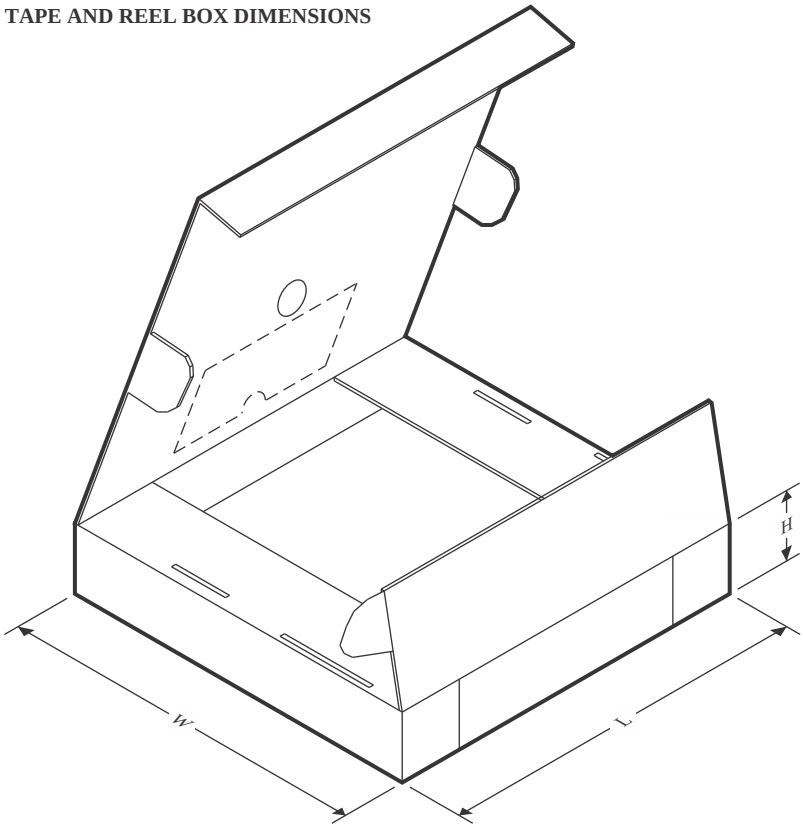
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC179QDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

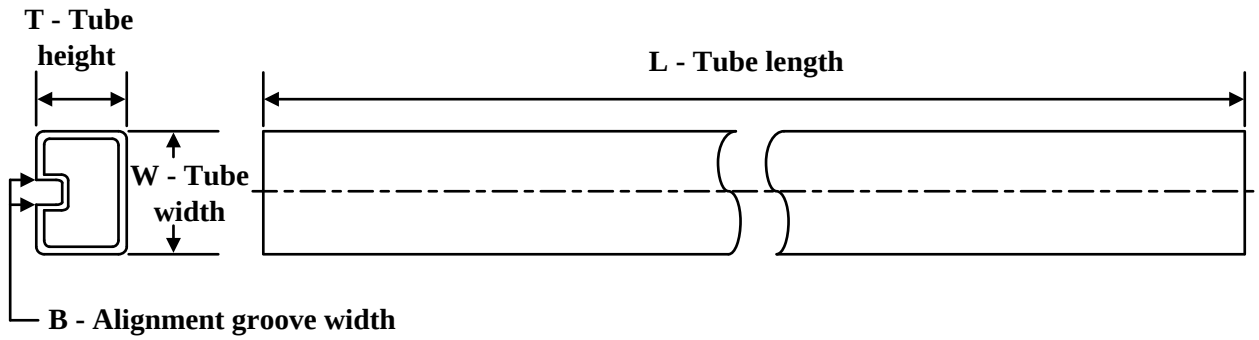
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

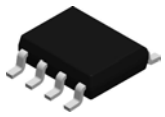
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC179DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65LBC179QDR	SOIC	D	8	2500	340.5	336.1	25.0
SN75LBC179DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC179D	D	SOIC	8	75	507	8	3940	4.32
SN65LBC179P	P	PDIP	8	50	506	13.97	11230	4.32
SN65LBC179QD	D	SOIC	8	75	507	8	3940	4.32
SN65LBC179QDG4	D	SOIC	8	75	507	8	3940	4.32
SN75LBC179D	D	SOIC	8	75	507	8	3940	4.32
SN75LBC179P	P	PDIP	8	50	506	13.97	11230	4.32

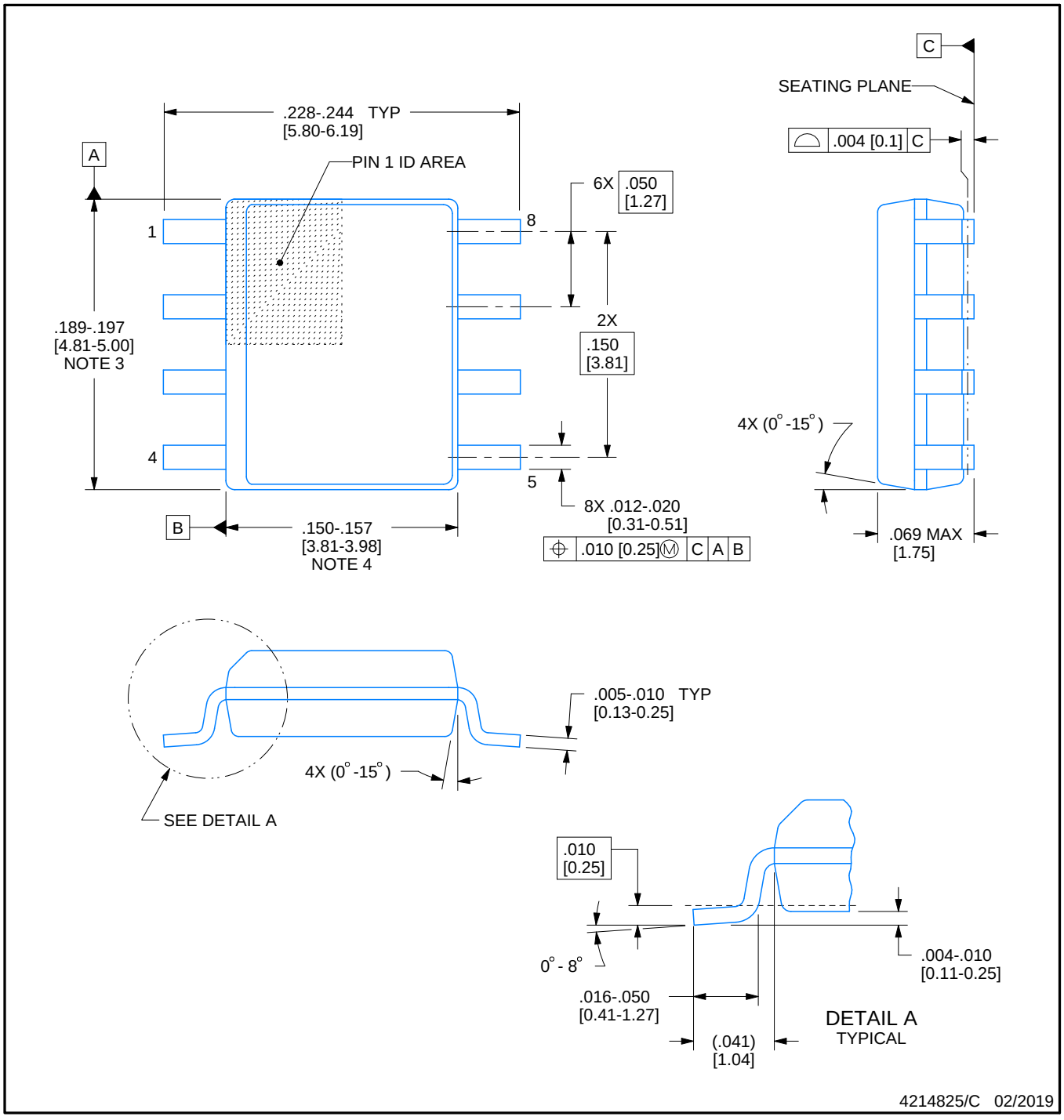


PACKAGE OUTLINE

D0008A

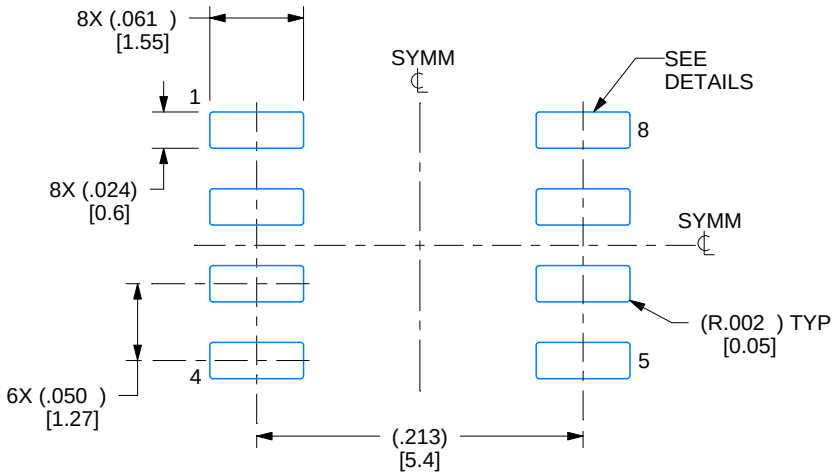
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

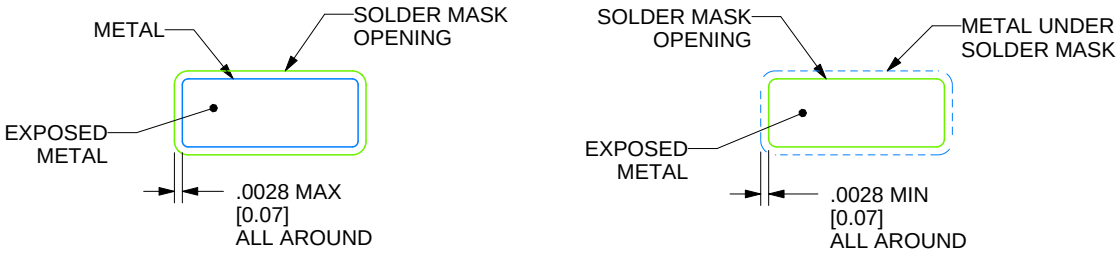


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

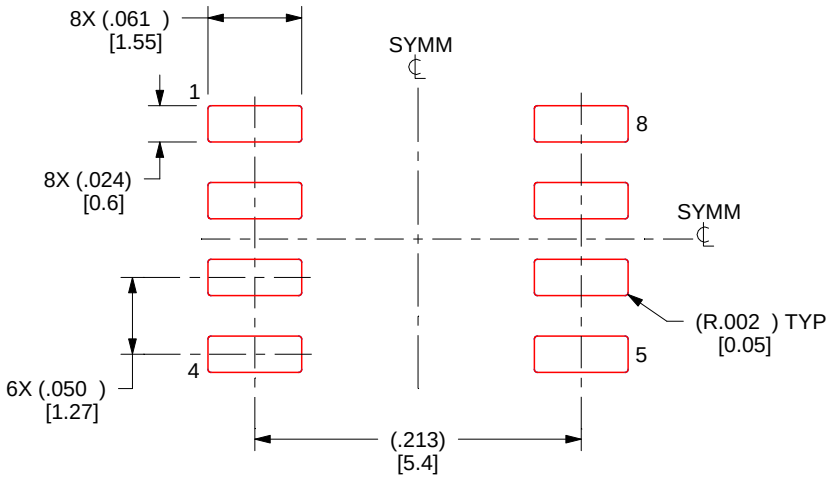
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



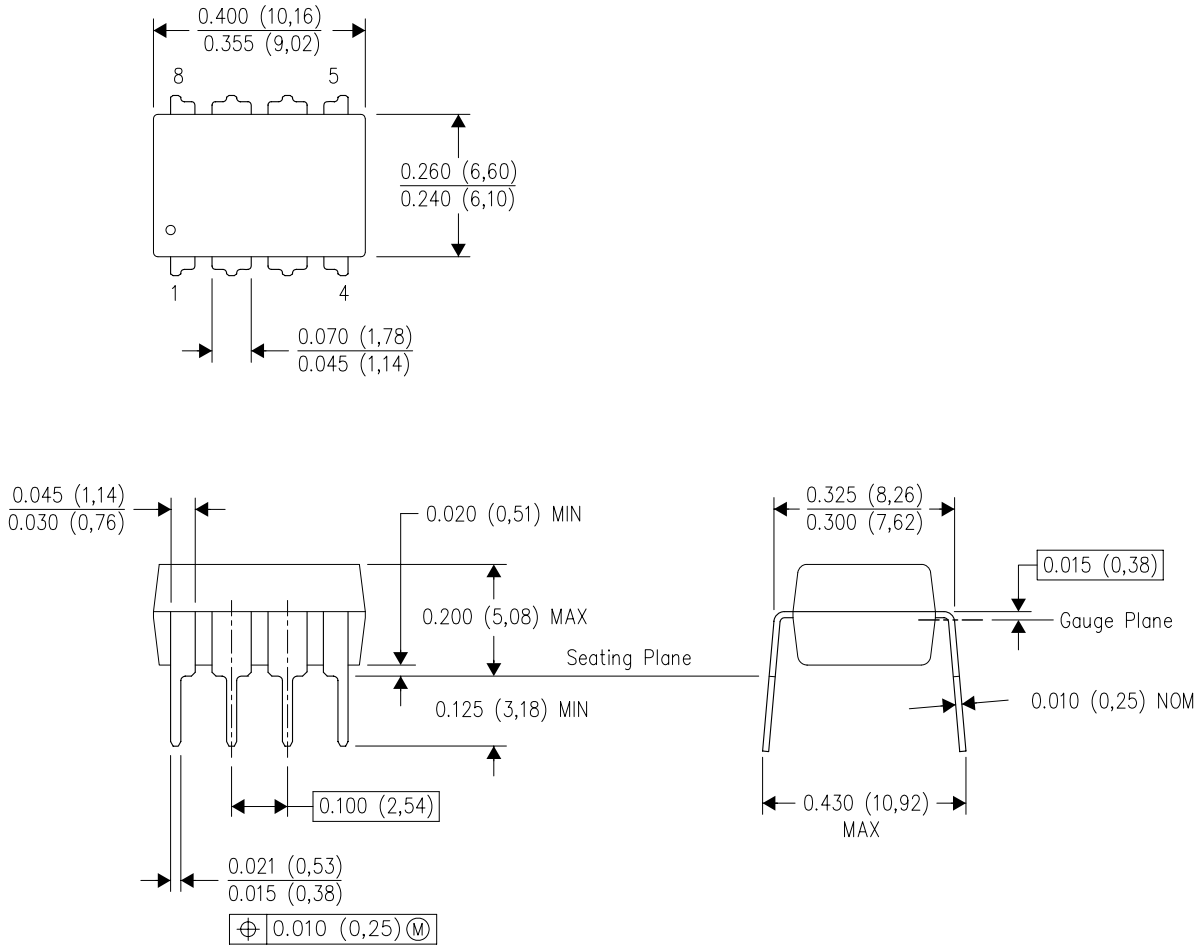
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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