

# SN74CBTD3306 DUAL FET BUS SWITCH WITH LEVEL SHIFTING

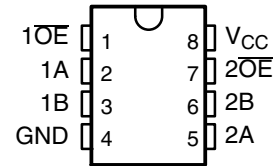
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- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications

## description/ordering information

The SN74CBTD3306 features two independent line switches. Each switch is disabled when the associated output-enable ( $\overline{OE}$ ) input is high. A diode to  $V_{CC}$  is integrated on the chip to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

D OR PW PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

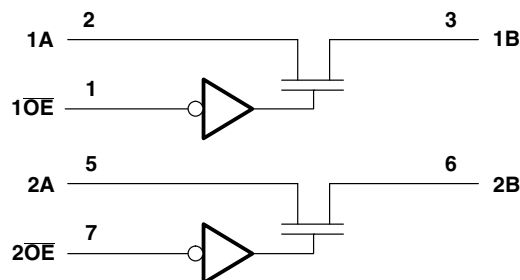
$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Tube	SN74CBTD3306D	CC306
		Tape and reel	SN74CBTD3306DR	
	TSSOP – PW	Tube	SN74CBTD3306PW	CC306
		Tape and reel	SN74CBTD3306PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

## logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN74CBTD3306 DUAL FET BUS SWITCH WITH LEVEL SHIFTING

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_{I/O} < 0$ )	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	97°C/W
PW package	149°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	-40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA				-1.2	V
$V_{OH}$	See Figure 2					
$I_I$	$V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND				$\pm 1$	$\mu$ A
$I_{CC}$	$V_{CC} = 5.5$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND				1.5	mA
$\Delta I_{CC}^{\S}$	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2.5	mA
$C_i$	Control inputs	$V_I = 3$ V or 0		3		pF
$C_{io(OFF)}$		$V_O = 3$ V or 0, $\overline{OE} = V_{CC}$		4		pF
$r_{on}^{\parallel}$	$V_{CC} = 4.5$ V	$V_I = 0$		5	7	$\Omega$
			$I_I = 64$ mA			
			$I_I = 30$ mA			
		$V_I = 2.4$ V, $I_I = 15$ mA		35	50	

<sup>‡</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ$ C.

<sup>\S</sup> This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

<sup>\parallel</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

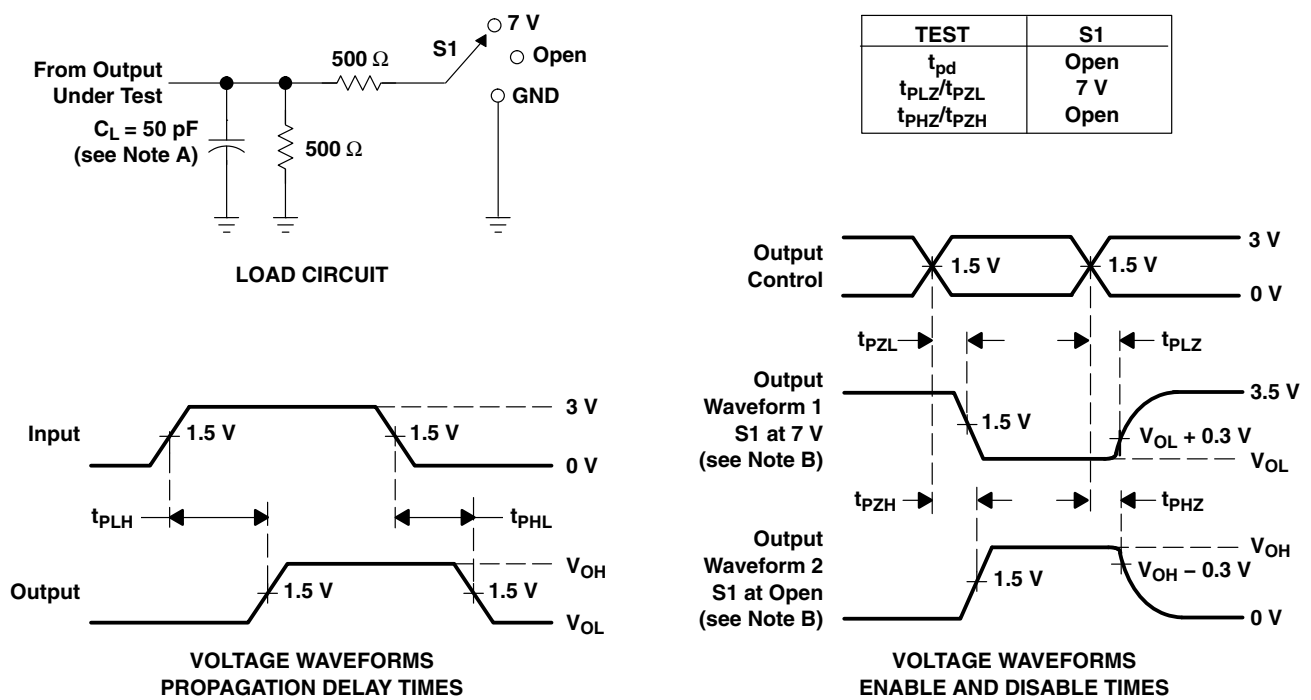


switching characteristics over recommended ranges of supply voltage and operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^\dagger$	A or B	B or A		0.25	ns
$t_{en}$	$\overline{OE}$	A or B	2.1	5.4	ns
$t_{dis}$	$\overline{OE}$	A or B	1	4.7	ns

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

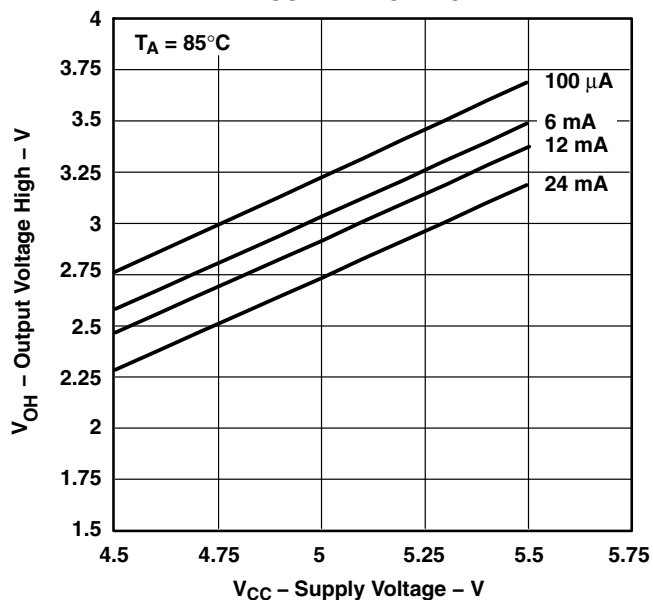
**Figure 1. Load Circuit and Voltage Waveforms**

**SN74CBTD3306**  
**DUAL FET BUS SWITCH**  
**WITH LEVEL SHIFTING**

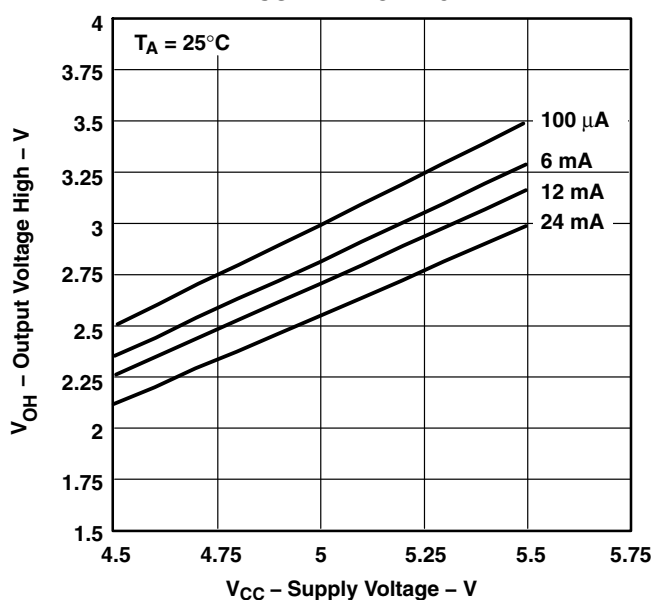
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**TYPICAL CHARACTERISTICS**

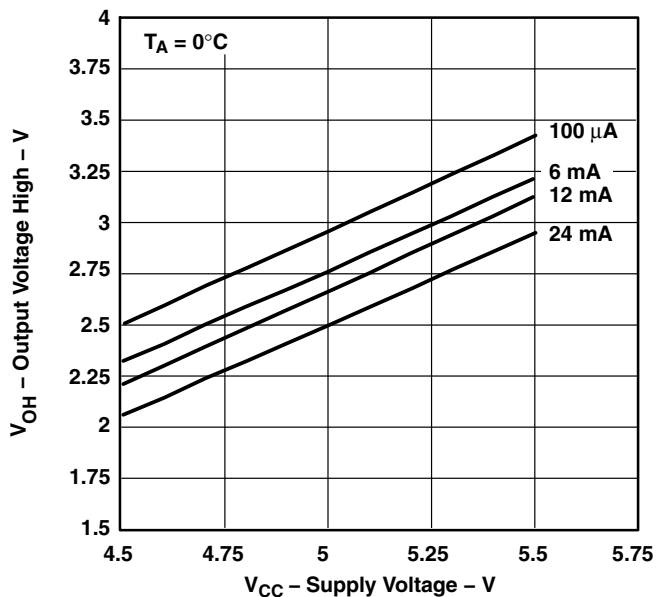
**OUTPUT VOLTAGE HIGH**  
**vs**  
**SUPPLY VOLTAGE**



**OUTPUT VOLTAGE HIGH**  
**vs**  
**SUPPLY VOLTAGE**



**OUTPUT VOLTAGE HIGH**  
**vs**  
**SUPPLY VOLTAGE**



**Figure 2.  $V_{OH}$  Values**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTD3306D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC306	<a href="#">Samples</a>
SN74CBTD3306DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC306	<a href="#">Samples</a>
SN74CBTD3306DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC306	<a href="#">Samples</a>
SN74CBTD3306DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC306	<a href="#">Samples</a>
SN74CBTD3306PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC306	<a href="#">Samples</a>
SN74CBTD3306PWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC306	<a href="#">Samples</a>
SN74CBTD3306PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC306	<a href="#">Samples</a>
SN74CBTD3306PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		
SN74CBTD3306PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	CC306	<a href="#">Samples</a>
SN74CBTD3306PWRG3	PREVIEW	TSSOP	PW	8	2000	TBD	Call TI	Call TI	-40 to 85		
SN74CBTD3306PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC306	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTD3306DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTD3306DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTD3306PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SN74CBTD3306PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTD3306DR	SOIC	D	8	2500	340.5	338.1	20.6
SN74CBTD3306DR	SOIC	D	8	2500	367.0	367.0	35.0
SN74CBTD3306PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
SN74CBTD3306PWR	TSSOP	PW	8	2000	367.0	367.0	35.0



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

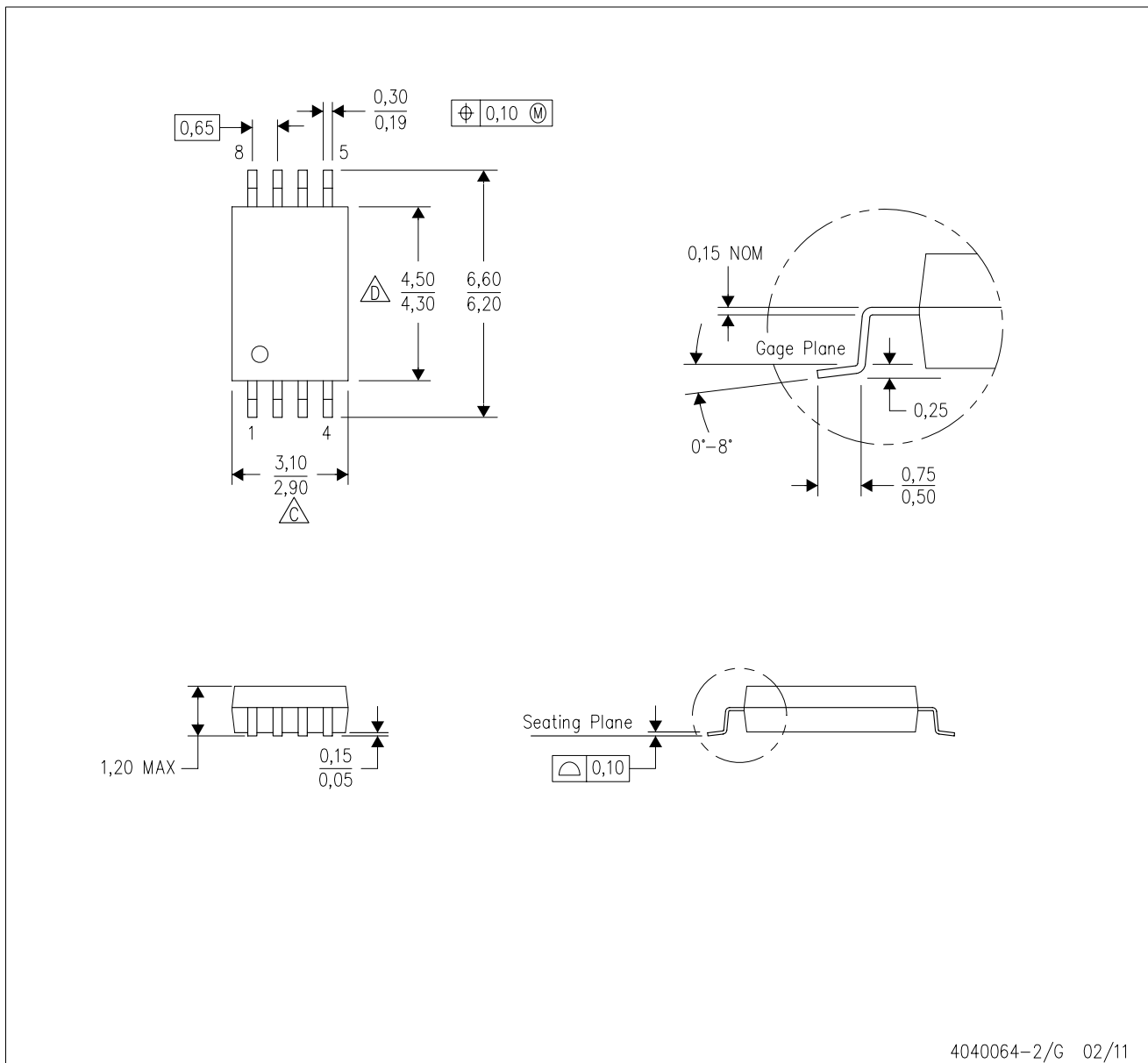


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- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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