TEXAS INSTRUMENTS

具有清零和预设功能的 SNx4HC109 双路 J-$\overline{K}$ 正边沿触发式触发器

1 特性

- 2V 至 6V 的宽工作电压范围
- 低输出电流，最大值 1µA
- 高电流输出可驱动多达 10 个 LSTTL 负载
- 低功耗，I_{CC} 最大值为 40µA
- t_{pd} 典型值 = 12ns
- ±4mA 输出驱动（在 5 V 时）

2 说明

这些器件包含两个独立的 J-$\overline{K}$ 正边沿触发式触发器。预设 (PRE) 或清零 ($\overline{CLR}$) 输入端的低电平会设置或复位输出，不受其他输入端电平的影响。当 $\overline{PRE}$ 和 $\overline{CLR}$ 处于非有效状态（高电平）时，满足设置时间要求的 J 和 $\overline{K}$ 输入端数据将在时钟 (CLK) 脉冲的正向边沿传输到输出端。时钟触发在一个特定电压电平下发生，与时钟脉冲的上升时间没有直接关系。经过保持时间间隔后，可以更改 J 和 $\overline{K}$ 输入端的数据而不影响输出端的电平。这些多功能触发器通过将 $\overline{K}$ 接地并将 J 连接到高电平来作为切换触发器运行。如果将 J 和 $\overline{K}$ 连接到一起，也能作为 D 型触发器运行。

器件信息

器件型号	封装[(1)]	封装尺寸（标称值）
SN54HC109J	CDIP (16)	24.38mm × 6.92mm
SN74HC109D	SOIC (16)	9.90mm × 3.90mm
SN74HC109N	PDIP (16)	19.31mm × 6.35mm
SN74HC109NS	SO (16)	6.20mm x 5.30mm
SNJ54HC109FK	LCCC (20)	8.89mm × 8.45mm
SNJ54HC109W	CFP (16)	10.16mm × 6.73mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能方框图

English Data Sheet: SCLS470

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3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Product Folder Links: *SN54HC109 SN74HC109*

4 Pin Configuration and Functions

J, W, D, N, or NS Package
16-Pin CDIP, CFP, SOIC, PDIP, or SO
Top View
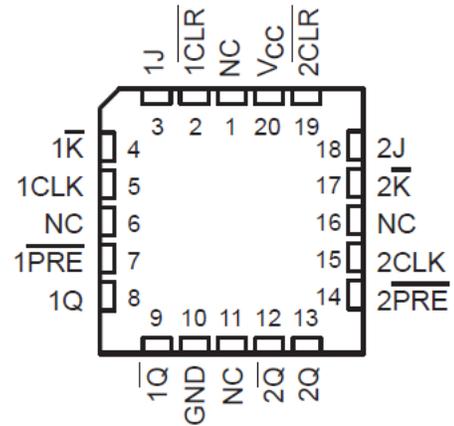
NC - No internal connection

FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FK package		300	°C
		J package			
		W package			
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D package		260	°C
		N package			
		NS package			
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions[1]

			SN54HC109			SN74HC109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 6$ V	4.2			4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.3			0.5	V
		$V_{CC} = 4.5$ V			0.9			1.35	
		$V_{CC} = 6$ V			1.2			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2$ V			1000			1000	ns
		$V_{CC} = 4.5$ V			500			500	
		$V_{CC} = 6$ V			400			400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	NS (SO)	UNIT
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	117.2	60.5	88.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.2	47.9	45.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.6	40.4	50.9	°C/W

5.3 Thermal Information (continued)

THERMAL METRIC		D (SOIC)	N (PDIP)	NS (SO)	UNIT
		16 PINS	16 PINS	16 PINS	
ψ_{JT}	Junction-to-top characterization parameter	38.1	27.3	12.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.3	40.2	50.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC109		SN74HC109		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = −20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = −4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = −5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			4		80		40	µA
C_i			2 V to 6 V		3	10		10		10	pF

5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC109		SN74HC109		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2		5	MHz
			4.5 V		31		21		25	
			6 V		36		25		29	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		

over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC109		SN74HC109		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time before CLK ↑	Data (J, $\overline{K}$)	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	25		40		30		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time	Data after CLK↑	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

5.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see 图 6-1)

| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC109		SN74HC109		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		ns
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		60	230		345		290	ns
			4.5 V		15	46		69		58	
			6 V		12	39		59		49	
	CLK	Q or $\overline{Q}$	2 V		50	175		250		220	
			4.5 V		15	35		50		44	
			6 V		12	30		42		37	
t_t		Q or $\overline{Q}$	2 V		28	75		110		95	ns
			4.5V		8	15		22		19	
			6 V		6	13		19		16	

5.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

Product Folder Links: *SN54HC109 SN74HC109*

6 Parameter Measurement Information
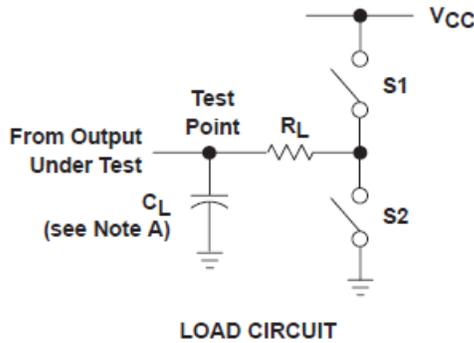
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS
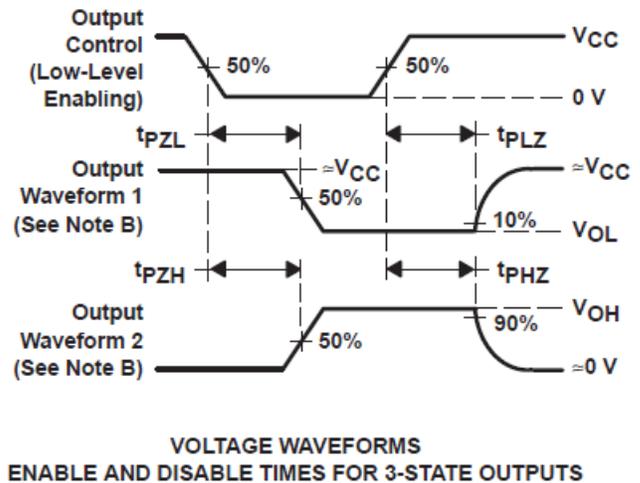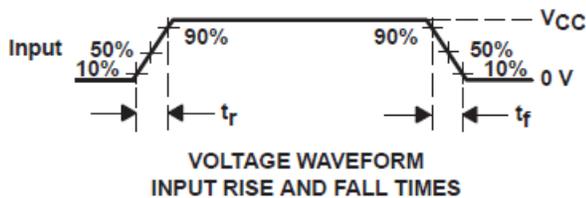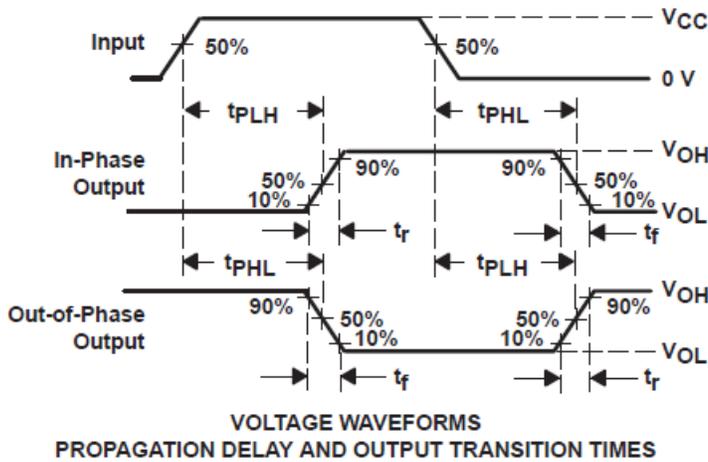
A. C_L includes probe and test-fixture capacitance.

B.   Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C.   Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

D.   The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the J and $\overline{K}$ inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

7.2 Functional Block Diagram
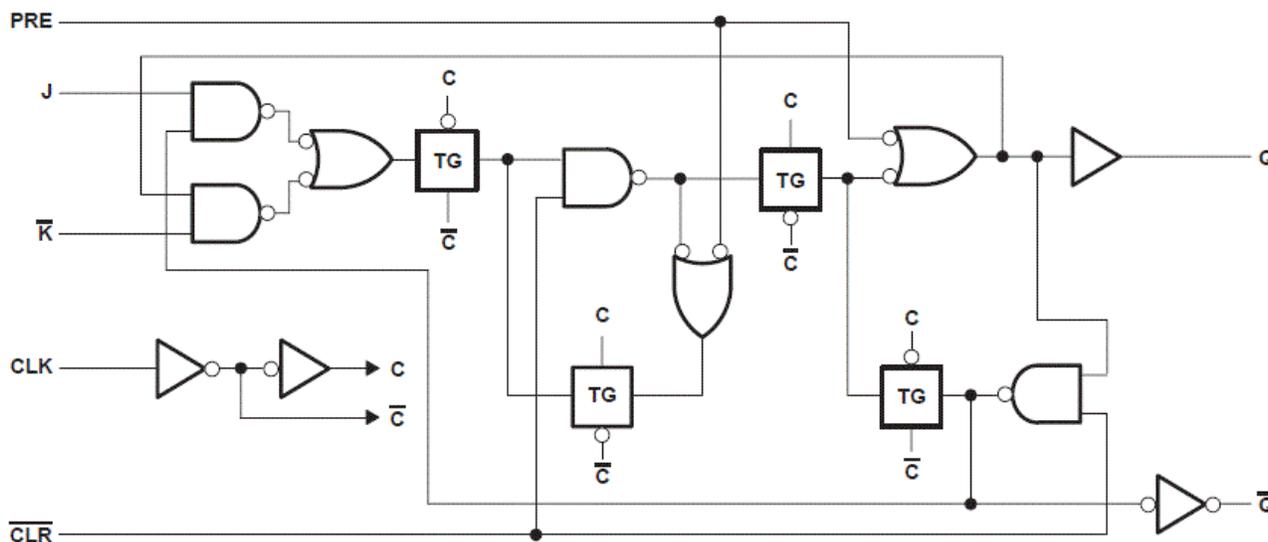
7.3 Device Functional Modes

表 7-1. Function Table

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H[1]	H[1]
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q0	$\overline{Q0}$
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q0}$

(1)   This configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表　　　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8415001VFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8415001VF A SNV54HC109W	Samples
84150012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84150012A SNJ54HC 109FK	Samples
8415001EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8415001EA SNJ54HC109J	Samples
8415001FA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8415001FA SNJ54HC109W	Samples
JM38510/65304BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65304BEA	Samples
M38510/65304BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65304BEA	Samples
SN54HC109J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC109J	Samples
SN74HC109D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC109	Samples
SN74HC109DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	SN	Level-1-260C-UNLIM	-40 to 85	HC109	Samples
SN74HC109DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC109	Samples
SN74HC109N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC109N	Samples
SN74HC109NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC109N	Samples
SN74HC109NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC109	Samples
SNJ54HC109FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84150012A SNJ54HC 109FK	Samples
SNJ54HC109J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8415001EA SNJ54HC109J	Samples
SNJ54HC109W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8415001FA SNJ54HC109W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC109, SN54HC109-SP, SN74HC109 :

- Catalog : SN74HC109, SN54HC109

- Military : SN54HC109

- Space : SN54HC109-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
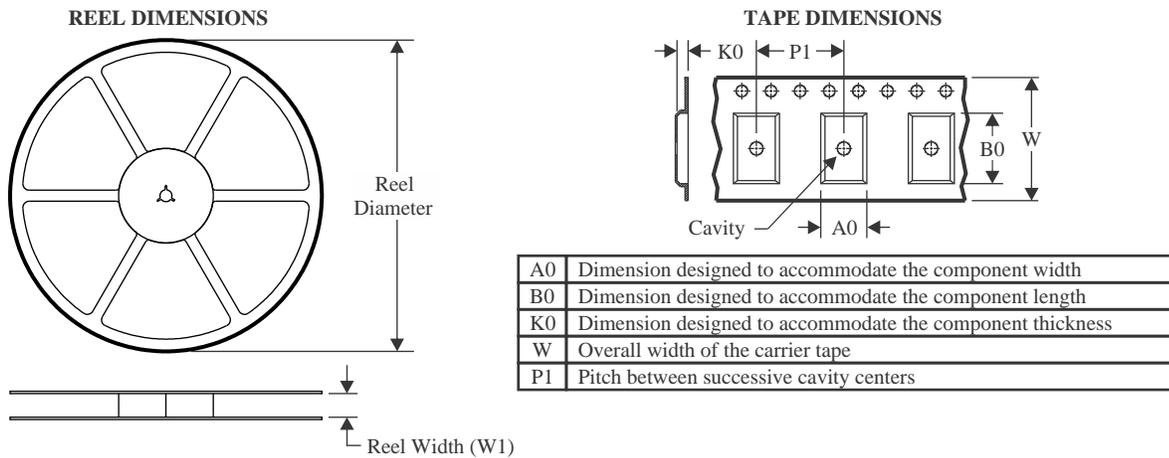
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
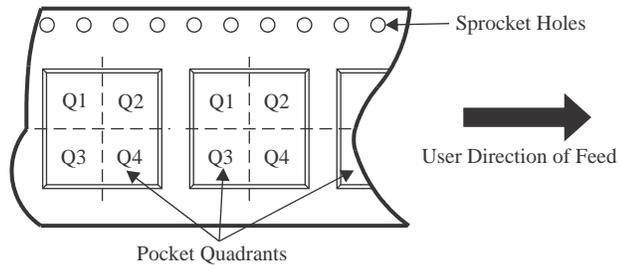
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC109DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC109DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC109DR	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HC109NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS
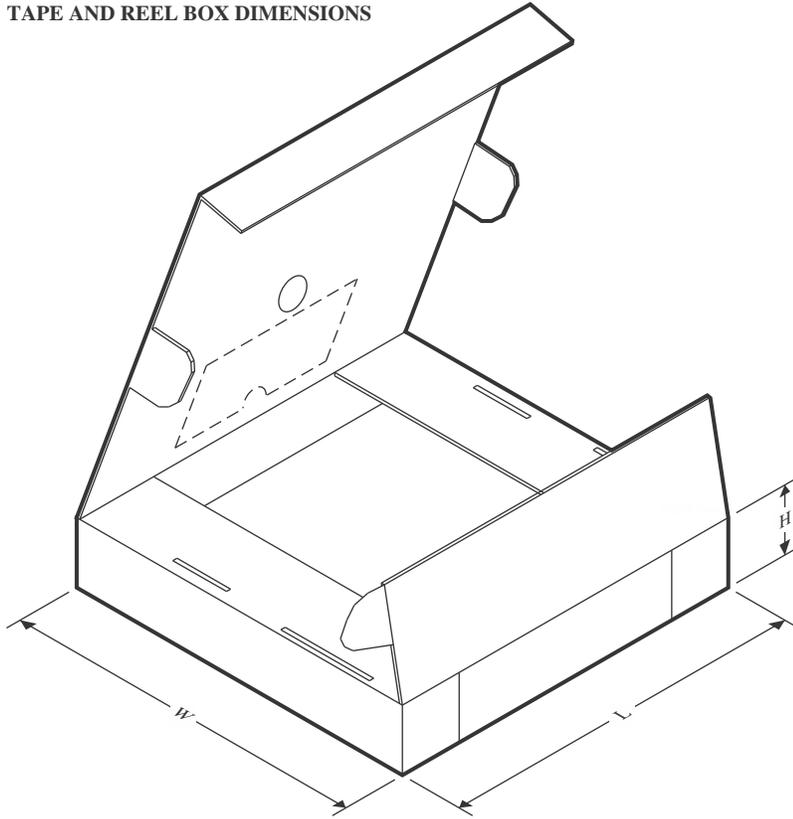
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC109DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC109DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC109DR	SOIC	D	16	2500	366.0	364.0	50.0
SN74HC109NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
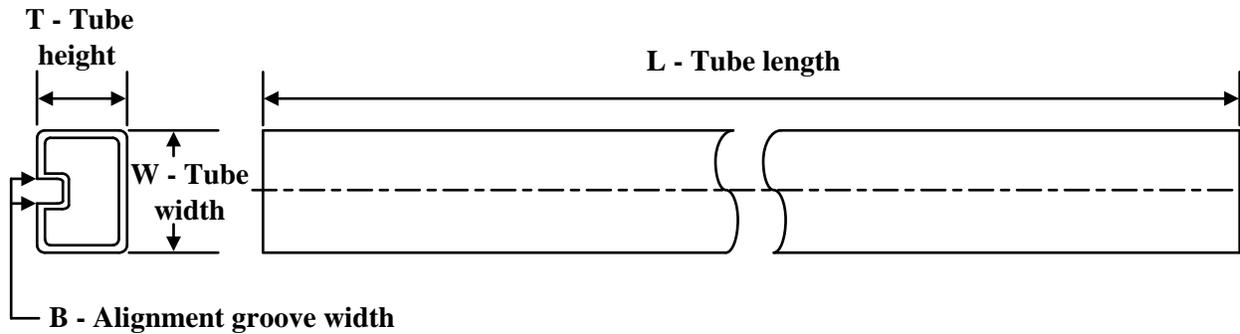
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8415001VFA	W	CFP	16	1	506.98	26.16	6220	NA
84150012A	FK	LCCC	20	1	506.98	12.06	2030	NA
8415001FA	W	CFP	16	1	506.98	26.16	6220	NA
SN74HC109D	D	SOIC	16	40	507	8	3940	4.32
SN74HC109N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC109N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC109NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC109NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC109FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54HC109W	W	CFP	16	1	506.98	26.16	6220	NA

8.2
7.4 TYP

A

PIN 1 ID
AREA

1

16

14X 1.27

10.4
10.0
NOTE 3

2X
8.89

8

9

5.4
5.2
NOTE 4

B

16X 0.51
0.35

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.00 MAX

SEE DETAIL A

0.15 TYP

0.25

GAGE PLANE

0° - 10°

1.05
0.55

(1.25)

0.3
0.1

DETAIL A
TYPICAL
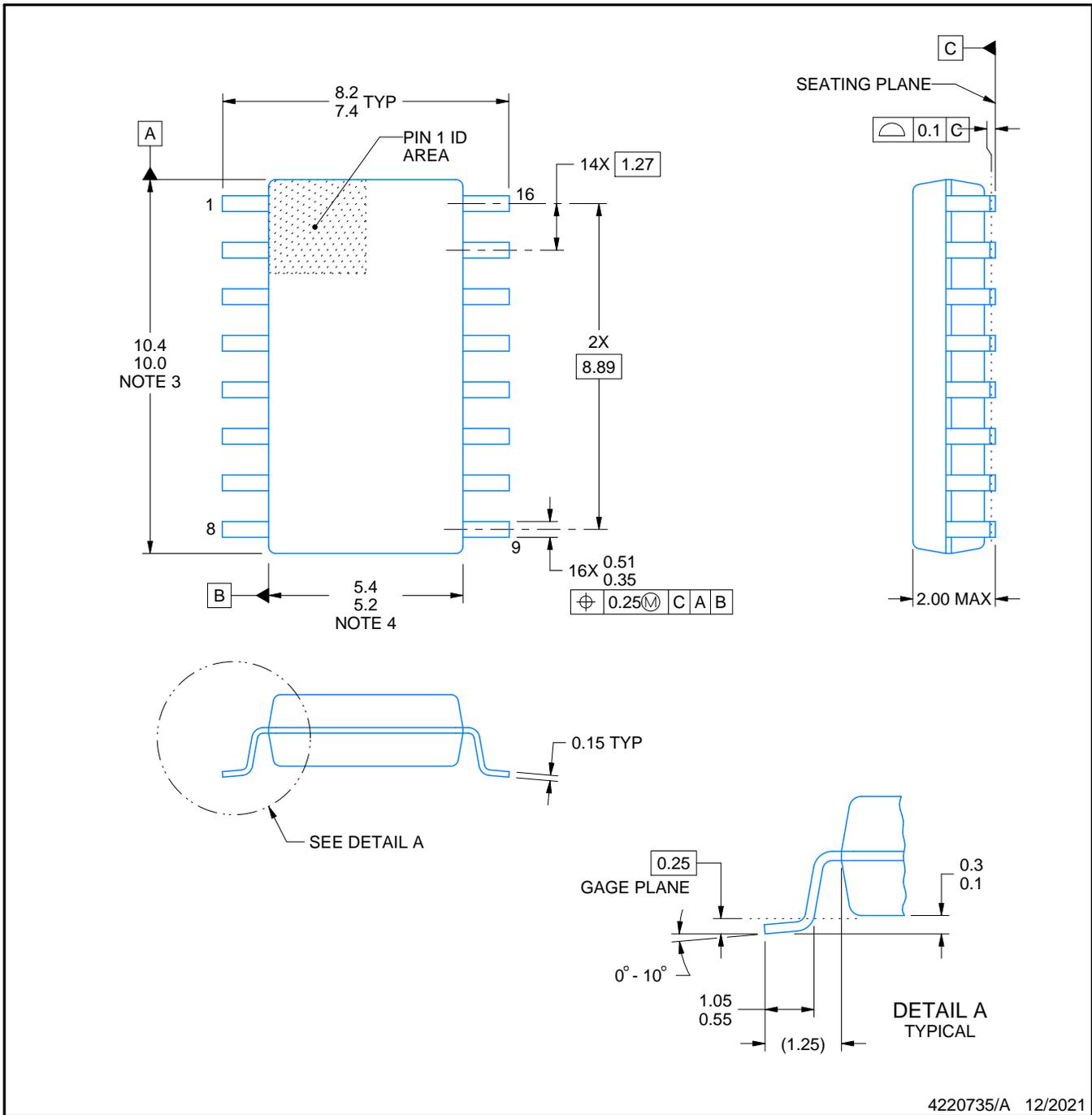
4220735/A   12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

16X (1.85)

SYMM

SEE DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK OPENING

SOLDER MASK OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
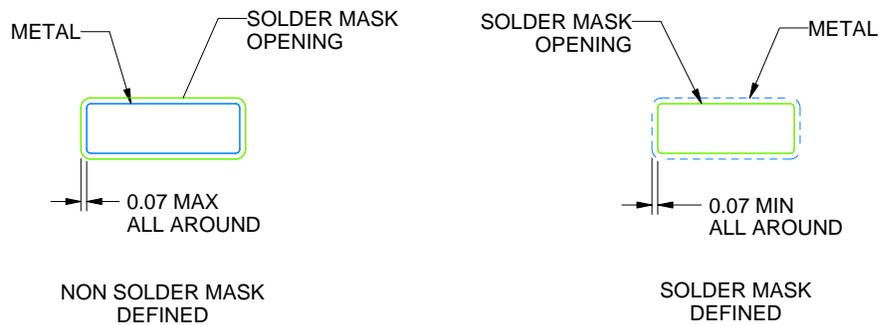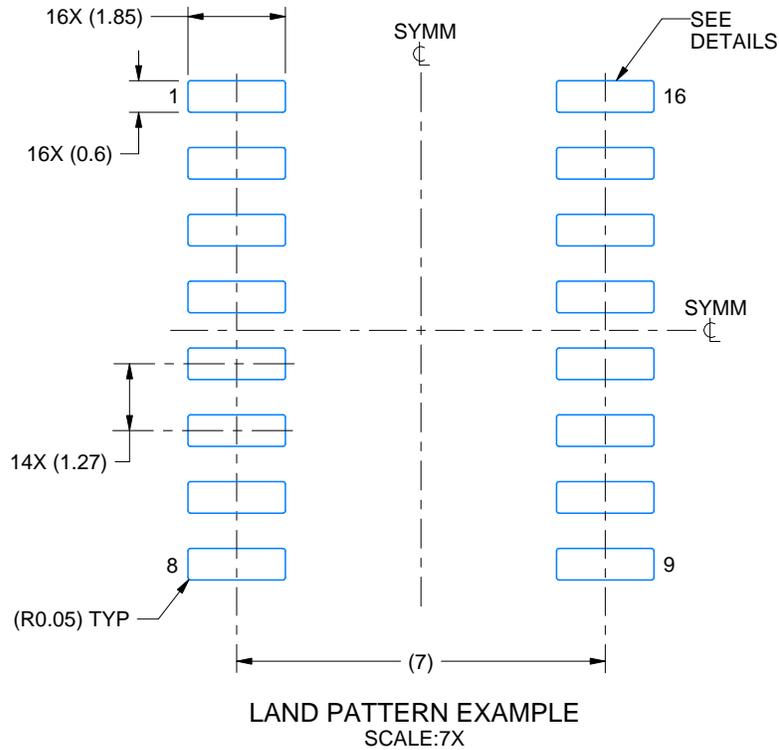
4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
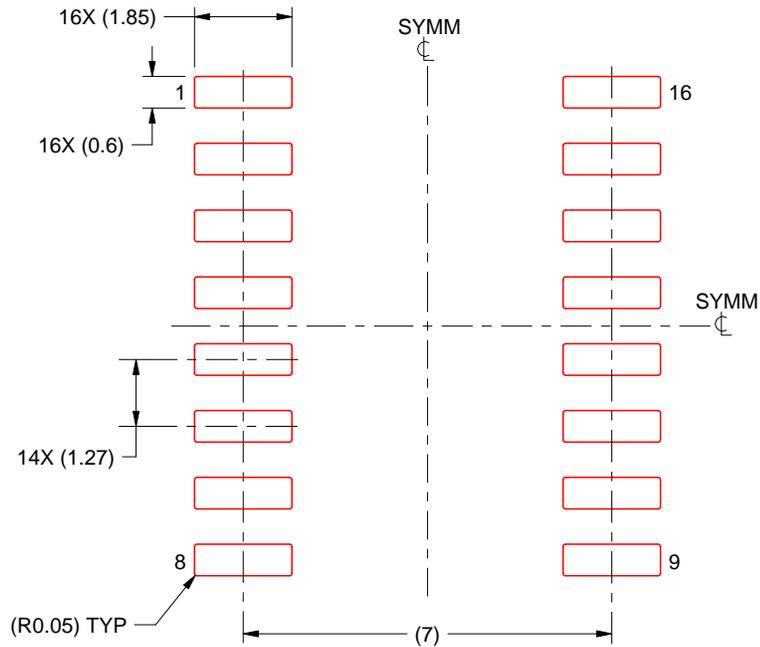
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE
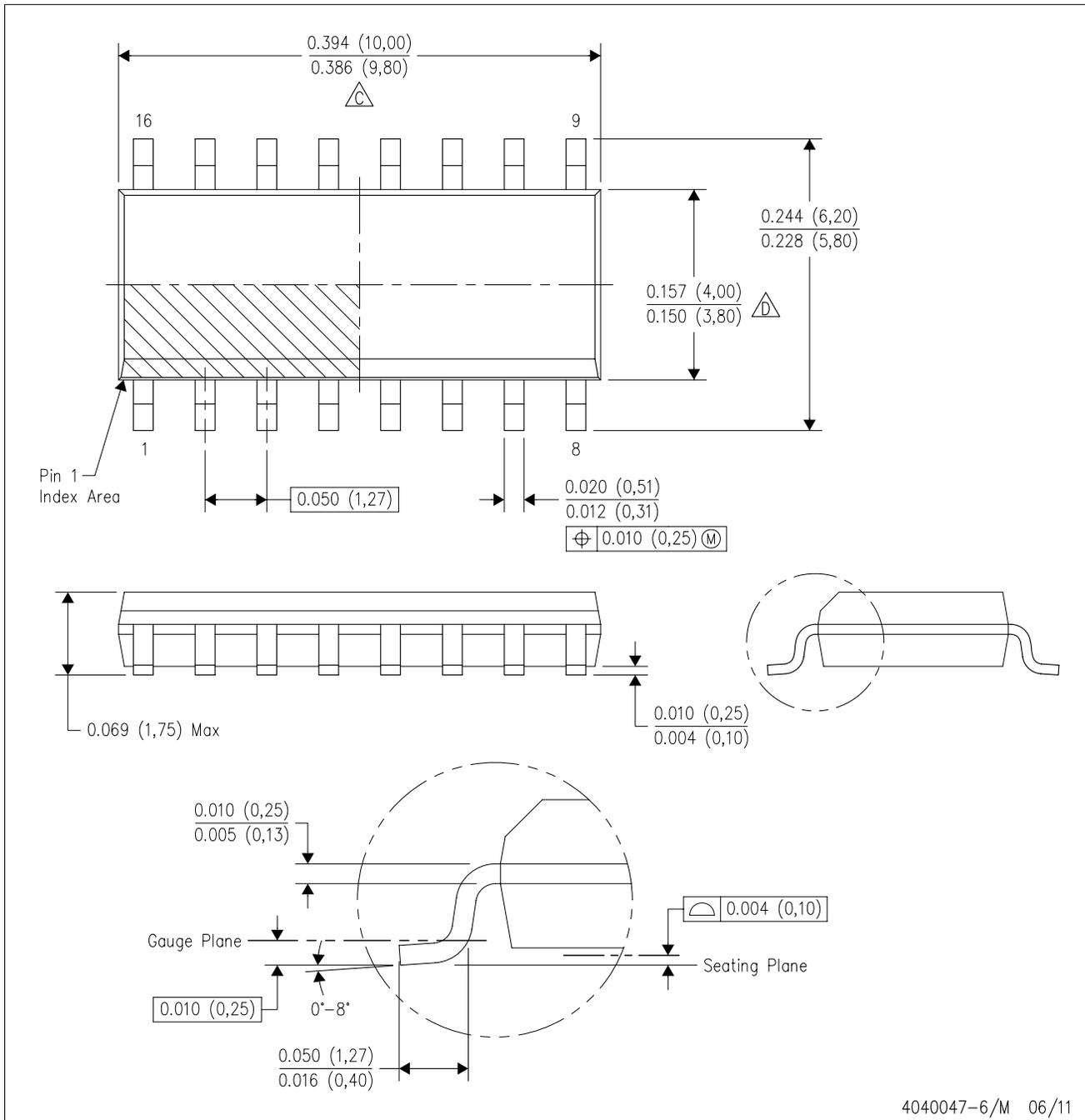
0.394 (10,00)
0.386 (9,80)
△C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      △C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
      △D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.
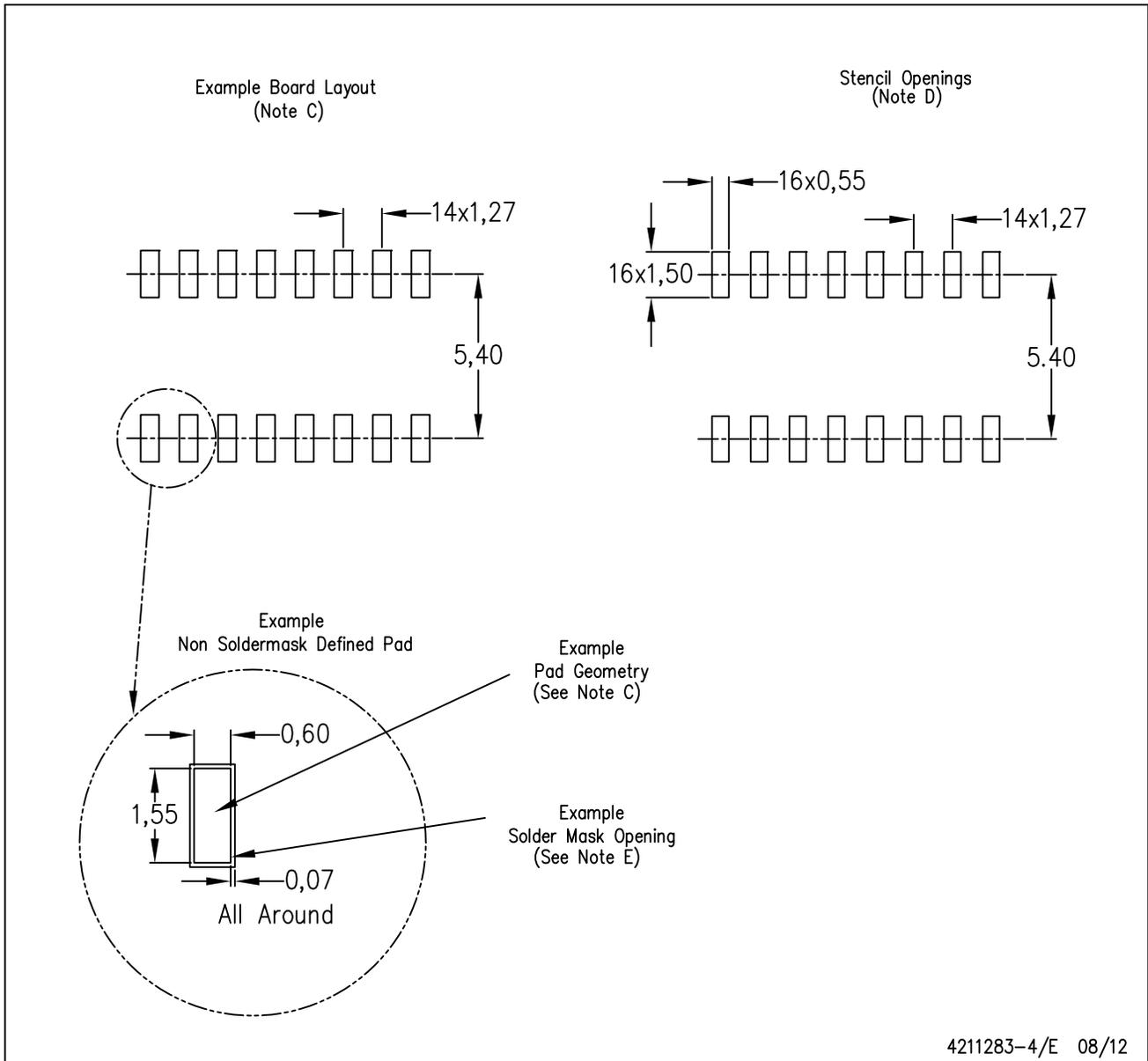
TEXAS
INSTRUMENTS
www.ti.com

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

—14x1,27

—16x0,55

—14x1,27

5,40

16x1,50

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

—0,60

1,55

Example
Solder Mask Opening
(See Note E)

—0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA
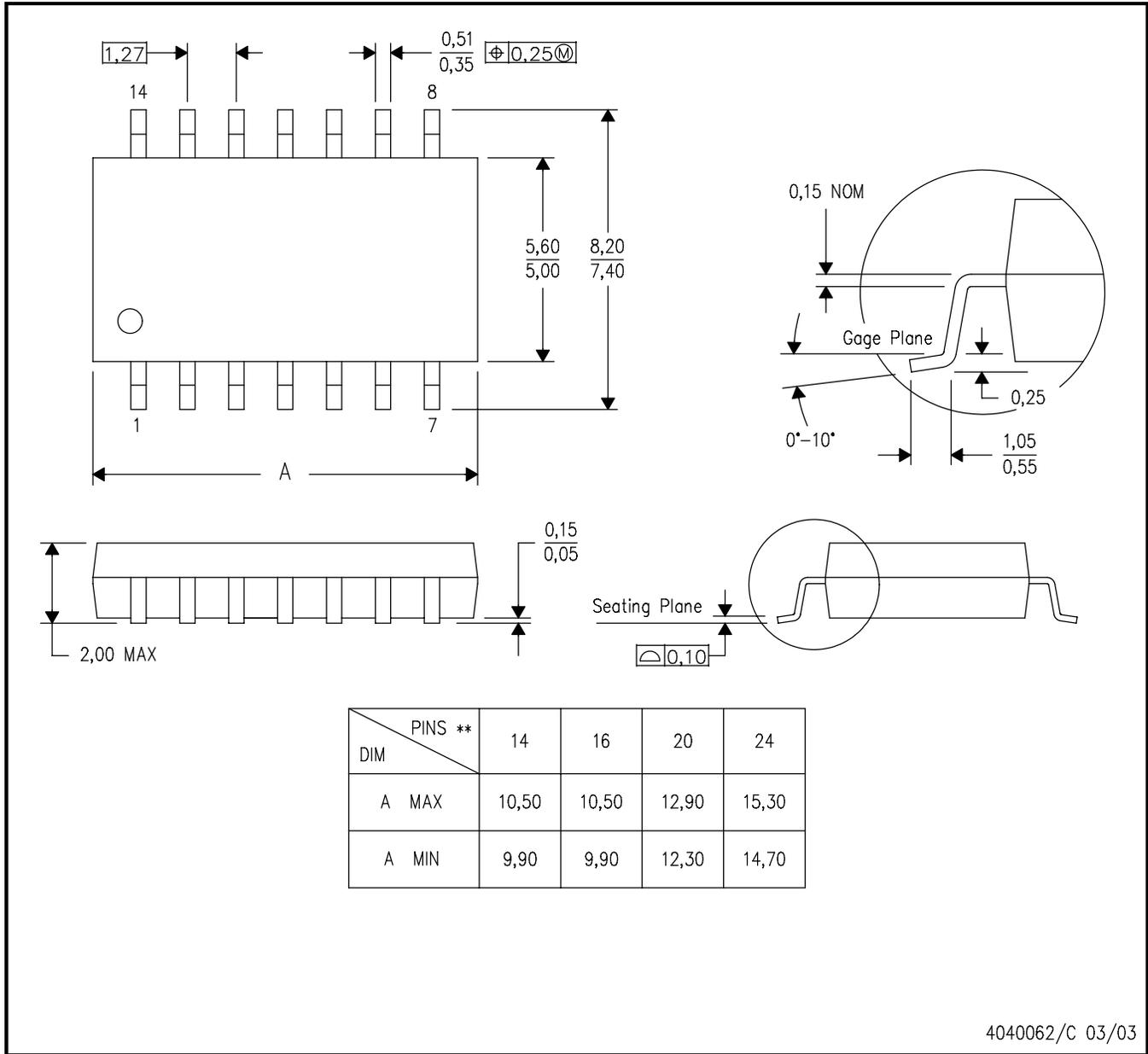
PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

TEXAS
INSTRUMENTS
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W (R—GDFP—F16)   CERAMIC DUAL FLATPACK
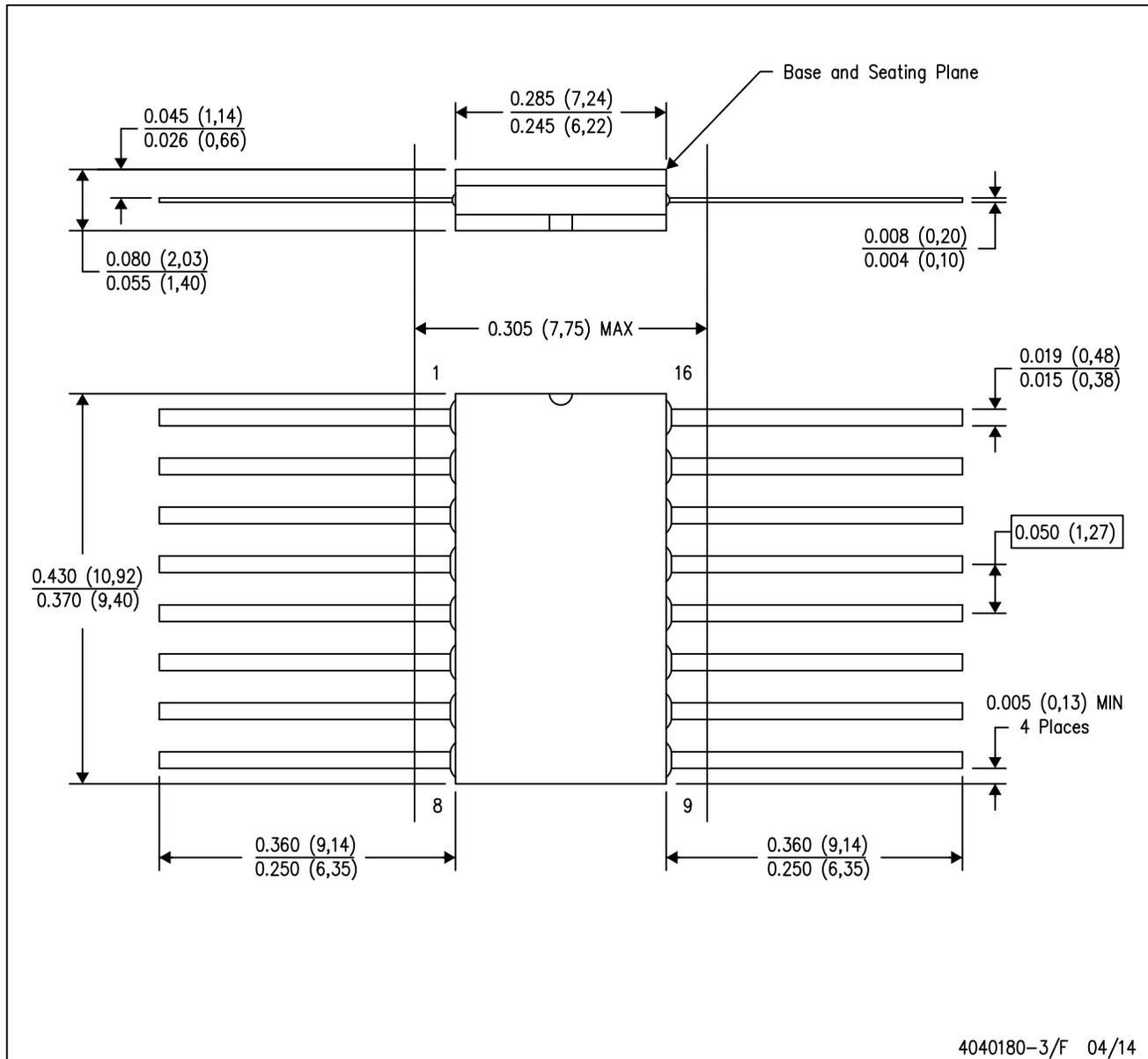
0.045 (1,14)
0.026 (0,66)

0.285 (7,24)
0.245 (6,22)

Base and Seating Plane

0.080 (2,03)
0.055 (1,40)

0.008 (0,20)
0.004 (0,10)

0.305 (7,75) MAX

1   16

0.019 (0,48)
0.015 (0,38)

0.430 (10,92)
0.370 (9,40)

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8   9

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180–3/F 04/14

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package can be hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only.
         E. Falls within MIL STD 1835 GDFP2–F16

TEXAS
INSTRUMENTS
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DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE
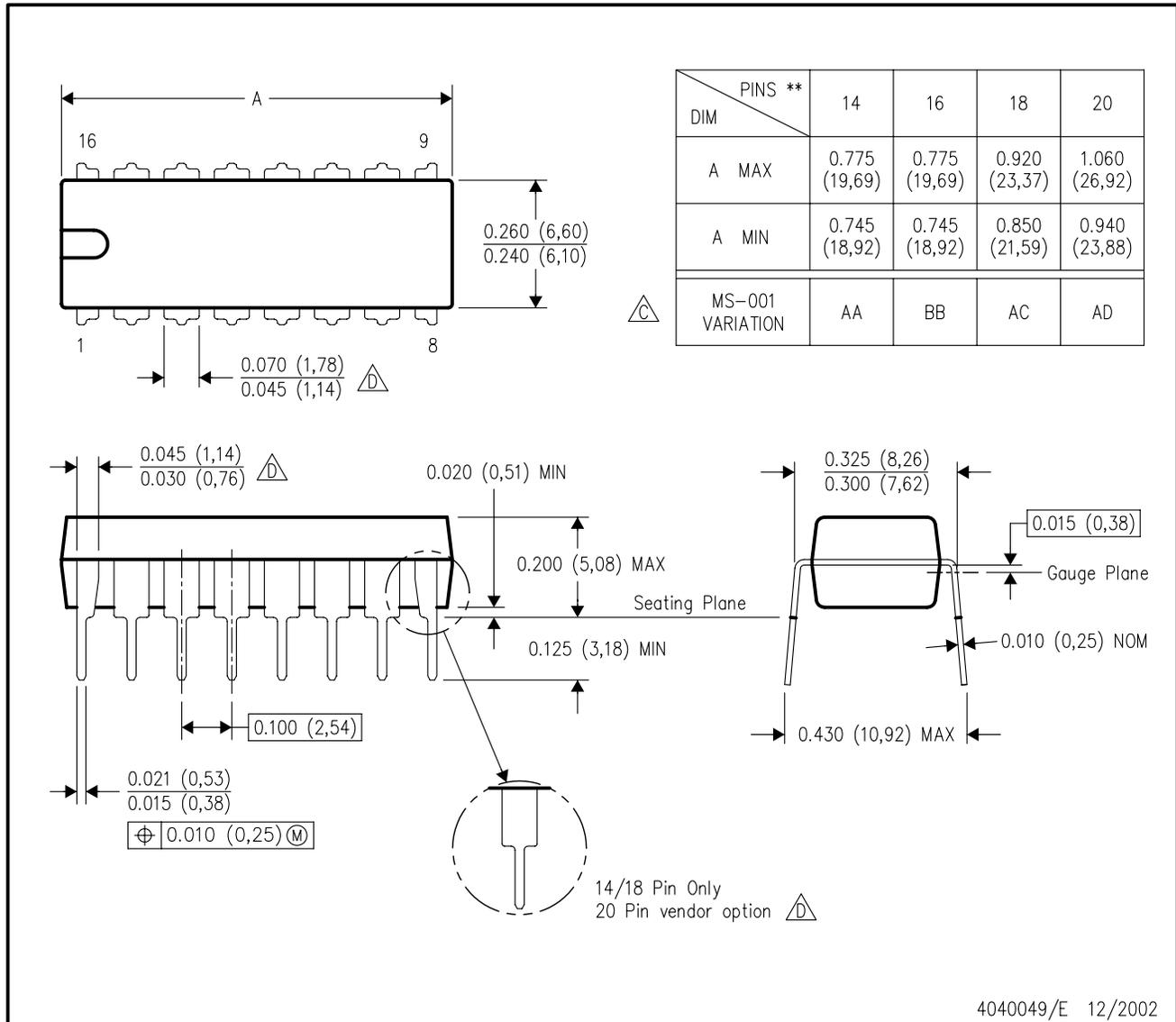
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) /D\

0.045 (1,14) / 0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
  B.   This drawing is subject to change without notice.
  /C\   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
  /D\   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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