# SNx4HCT04 六路反相器

## 1 特性

- 4.5V 至 5.5V 的工作电压范围
- 输出可驱动多达 10 个 LSTTL 负载
- 低功耗，$I_{CC}$ 最大值为 20 µA
- $t_{pd}$ 典型值 = 13ns
- ±4mA 输出驱动（在 5V 时）
- 低输入电流，最大值 1 µA
- 输入兼容 TTL 电压

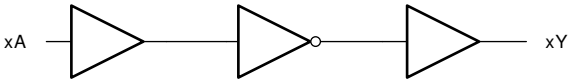
## 2 说明

这些器件包含六个独立的反相器。它们以正逻辑执行布尔函数 $Y = \overline{A}$。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| SN74HCT04PW | TSSOP (14) | 5.00mm × 4.40mm |
| SN74HCT04D | SOIC (14) | 8.65mm × 3.90mm |
| SN74HCT04N | PDIP (14) | 19.31mm × 6.35mm |
| SN74HCT04NSR | SO (14) | 10.20mm × 5.30mm |
| SNJ54HCT04FK | LCCC (20) | 8.89mm × 8.89mm |
| SNJ54HCT04J | CDIP (14) | 19.55mm × 6.71mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




功能方框图

# Table of Contents



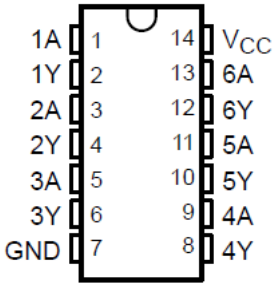
## 3 Revision History

注：以前版本的页码可能与当前版本的页码不同

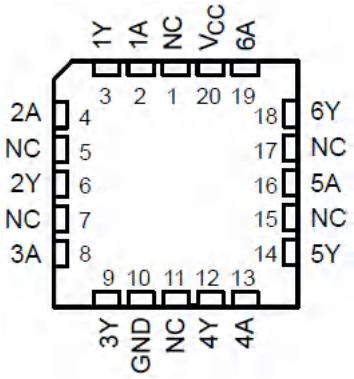
| Changes from Revision E (February 2022) to Revision F (October 2022) | Page |
|---|---|
| • Increased R θ JA for packages: D (86 to 138.7); N (80 to 62.7); NS (76 to 90.9); PW (113 to 117.6) | 4 |

| Changes from Revision D (July 2003) to Revision E (February 2022) | Page |
|---|---|
| • 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准 | 1 |

## 4 Pin Configuration and Functions




**J, D, N, NS, or PW Package**
**14-Pin CDIP, SOIC, PDIP, SO, or TSSOP**
**Top View**




**FK Package**
**20-Pin LCCC**
**Top View**

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | ($V_I$ < 0 or $V_I$ > $V_{CC}$) | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | ($V_O$ < 0 or $V_O$ > $V_{CC}$) | | ±20 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| $V_{CC}$ or GND | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 Recommended Operating Conditions(1)

| | | | SN54HCT04 | | | SN74HCT04 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $\Delta t/\Delta v$ | Input transition rise/fall time | | | | 500 | | | 500 | ns |
| $T_A$ | Operating free-air temperature | | -55 | | 125 | -40 | | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating SMOS Inputs*, literature number SCBA004.

## 5.3 Thermal Information

| THERMAL METRIC | | D (SOIC) 14 PINS | N (PDIP) 14 PINS | NS (SO) 14 PINS | PW (TSSOP) 14 PINS | UNIT |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance(1) | 138.7 | 62.7 | 90.9 | 117.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 93.8 | 50.5 | 48.5 | 46.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 94.7 | 42.5 | 51.5 | 60.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 49.1 | 30.1 | 15.9 | 5.6 | °C/W |
| $\psi_{JB}$ | Junction-to-case (bottom) thermal resistance | 94.3 | 42.2 | 51 | 60 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 5.4 Electrical Characteristics

| PARAMETER | | TEST CONDITIONS(1) | $V_{CC}$ (V) | $T_A$ = 25°C | | | SN54HCT00 | | SN74HCT00 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = – 20 μA | 4.5 | 4.4 | 4.499 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = – 4 mA | | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 20 μA | 5.5 | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 4 mA | | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | Input hold current | $V_I$ = $V_{CC}$ or 0 | 5.5 | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or 0. $I_O$ = 0 | 5.5 | | | 2 | | 40 | | 20 | μA |
| Δ ICC (2) | Supply-current change | One input at 0.5V or 2.4 V, Other inputs at 0 or $V_{CC}$ | 5.5 | | 1.4 | 2.4 | | 3 | | 2.9 | mA |
| $C_i$ | Input capacitance | | 4.5 to 5.5 | | 3 | 10 | | 10 | | 10 | pF |

(1) $V_I$ = $V_{IH}$ or $V_{IL}$, unless otherwise noted.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

## 5.5 Switching Characteristics

$C_L$ = 50 pF. See Parameter Measurement Information

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ (V) | $T_A$ = 25°C | | | SN54HCT04 | | SN74HCT04 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay | A or B | Y | 4.5 | | 14 | 20 | | 30 | | 25 | ns |
| | | | | 5.5 | | 13 | 18 | | 27 | | 23 | |
| $t_t$ | Transition time | | Y | 4.5 | | 9 | 15 | | 22 | | 19 | ns |
| | | | | 5.5 | | 8 | 14 | | 20 | | 17 | |

## 5.6 Operating Characteristics

$T_A$ = 25°C

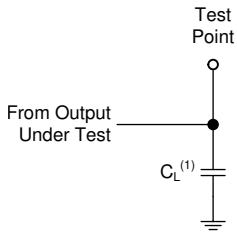
| | | Test Conditions | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load | 20 | pF |

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 6 ns.

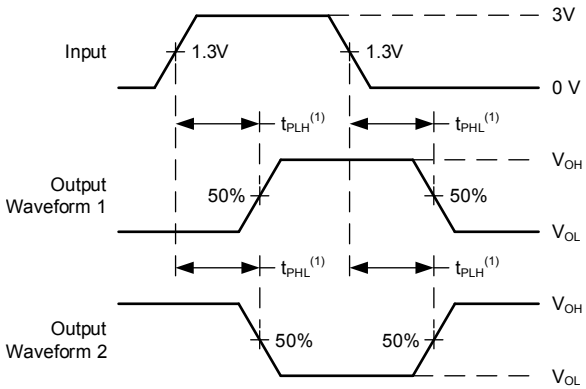
For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.




(1) $C_L$ includes probe and test-fixture capacitance.

**图 6-1. Load Circuit for Push-Pull Outputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

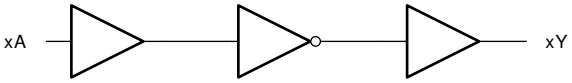
**图 6-2. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**

# 7 Detailed Description

## 7.1 Overview

These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

## 7.2 Functional Block Diagram




## 7.3 Device Functional Modes

**表 7-1. Function Table (each inverter)**

| Input A | Output Y |
|---|---|
| H | L |
| L | H |

# 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

# 9 Layout

## 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

# 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 10.1 Documentation Support

### 10.1.1 Related Documentation

## 10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-89747012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-89747012A SNJ54HCT 04FK | Samples |
| 5962-8974701CA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8974701CA SNJ54HCT04J | Samples |
| 5962-8974701VCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8974701VCA SNV54HCT04J | Samples |
| 5962-8974701VDA | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8974701VDA SNV54HCT04W | Samples |
| JM38510/65751BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65751BCA | Samples |
| M38510/65751BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65751BCA | Samples |
| SN54HCT04J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54HCT04J | Samples |
| SN74HCT04D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT04 | Samples |
| SN74HCT04DE4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT04 | Samples |
| SN74HCT04DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HCT04 | Samples |
| SN74HCT04DRE4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT04 | Samples |
| SN74HCT04DRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT04 | Samples |
| SN74HCT04DT | ACTIVE | SOIC | D | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT04 | Samples |
| SN74HCT04N | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HCT04N | Samples |
| SN74HCT04NE4 | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HCT04N | Samples |
| SN74HCT04NSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT04 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCT04PW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT04 | Samples |
| SN74HCT04PWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HT04 | Samples |
| SN74HCT04PWT | ACTIVE | TSSOP | PW | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT04 | Samples |
| SNJ54HCT04FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-89747012A SNJ54HCT 04FK | Samples |
| SNJ54HCT04J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8974701CA SNJ54HCT04J | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN54HCT04, SN54HCT04-SP, SN74HCT04 :**

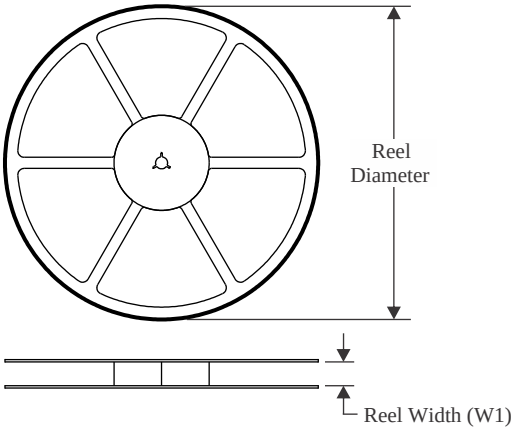
- Catalog : SN74HCT04, SN54HCT04
- Enhanced Product : SN74HCT04-EP, SN74HCT04-EP
- Military : SN54HCT04
- Space : SN54HCT04-SP

NOTE: Qualified Version Definitions:

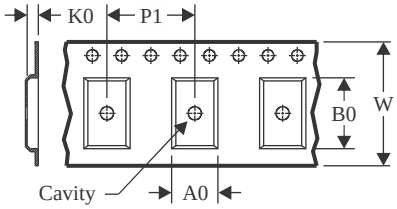
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

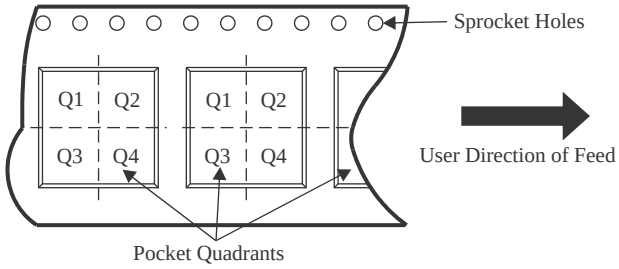



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

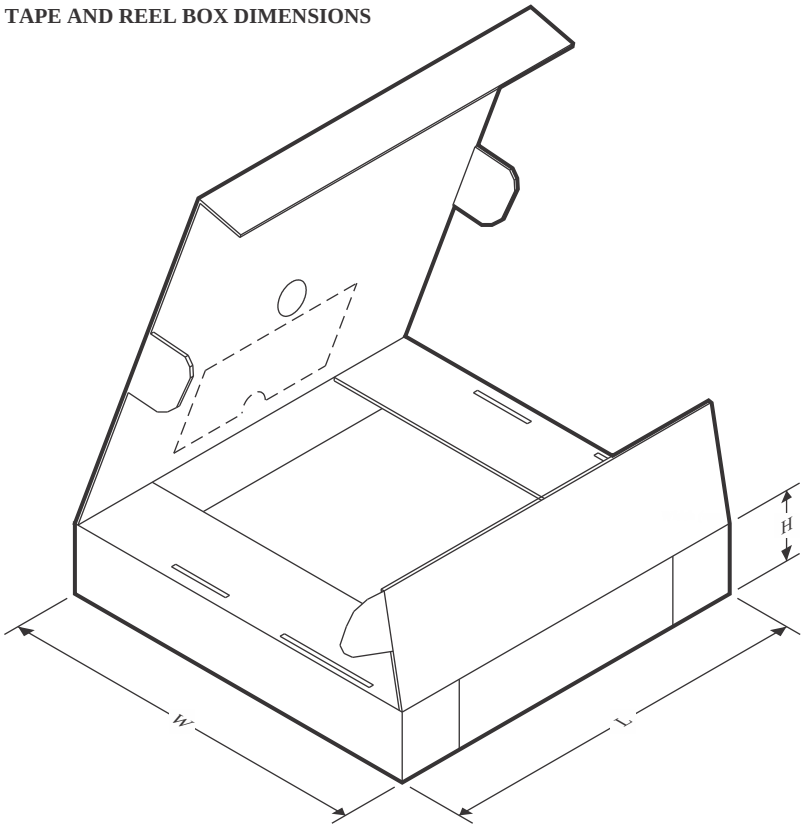
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCT04DR | SOIC | D | 14 | 2500 | 330.0 | 16.8 | 6.5 | 9.5 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT04DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.6 | 9.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT04DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT04DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT04DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT04DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT04DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT04DT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCT04NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HCT04NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.45 | 10.55 | 2.5 | 12.0 | 16.2 | Q1 |
| SN74HCT04PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT04PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT04PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT04PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.85 | 5.45 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCT04PWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

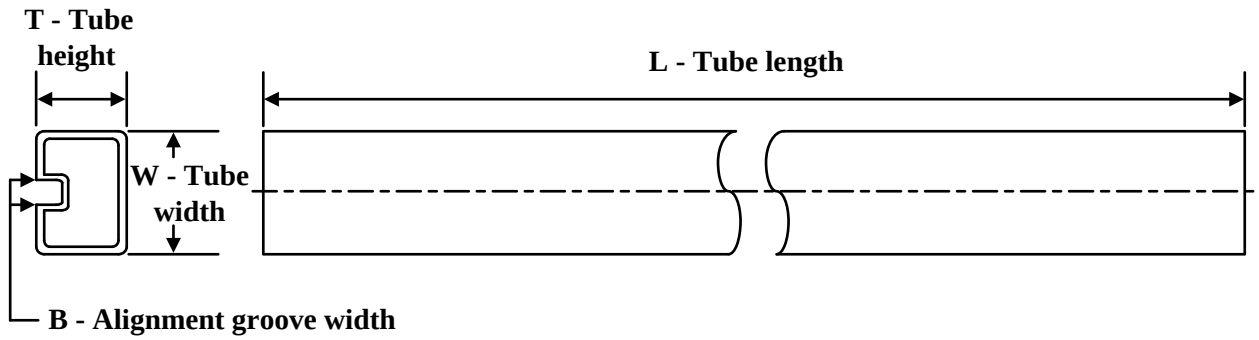
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HCT04DR | SOIC | D | 14 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74HCT04DR | SOIC | D | 14 | 2500 | 366.0 | 364.0 | 50.0 |
| SN74HCT04DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74HCT04DR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HCT04DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74HCT04DRG4 | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HCT04DRG4 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74HCT04DT | SOIC | D | 14 | 250 | 210.0 | 185.0 | 35.0 |
| SN74HCT04NSR | SO | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCT04NSR | SO | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCT04PWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74HCT04PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCT04PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCT04PWR | TSSOP | PW | 14 | 2000 | 366.0 | 364.0 | 50.0 |
| SN74HCT04PWT | TSSOP | PW | 14 | 250 | 356.0 | 356.0 | 35.0 |

## TUBE



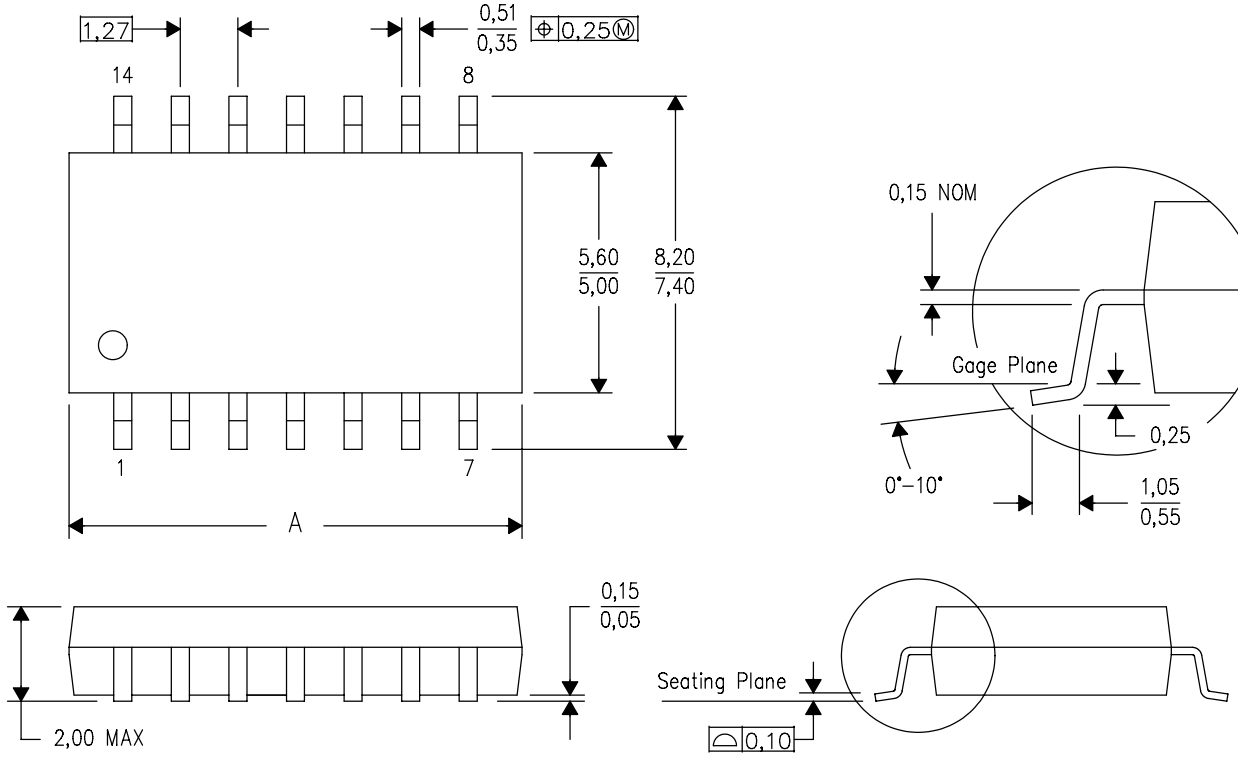

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-89747012A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 5962-8974701VDA | W | CFP | 14 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74HCT04D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74HCT04DE4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74HCT04N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT04N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT04NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT04NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT04PW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54HCT04FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

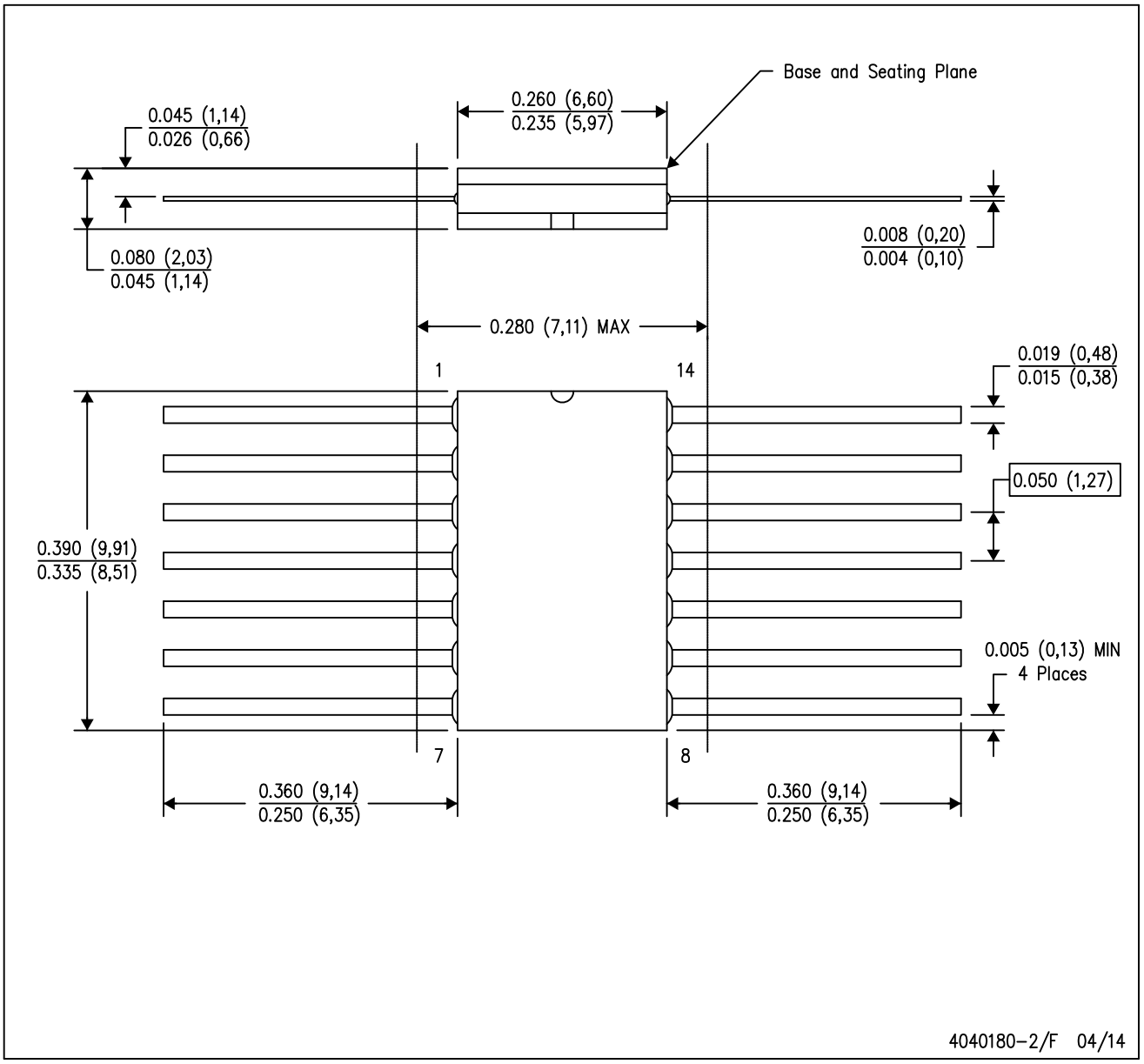



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

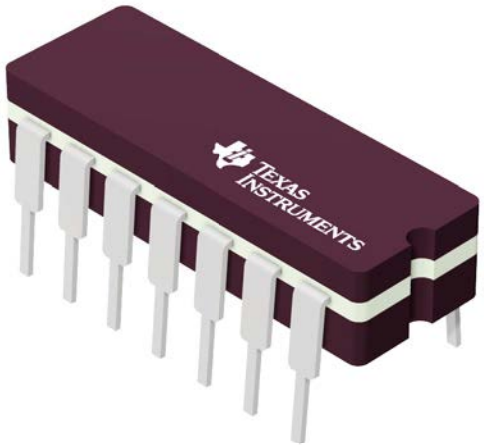



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

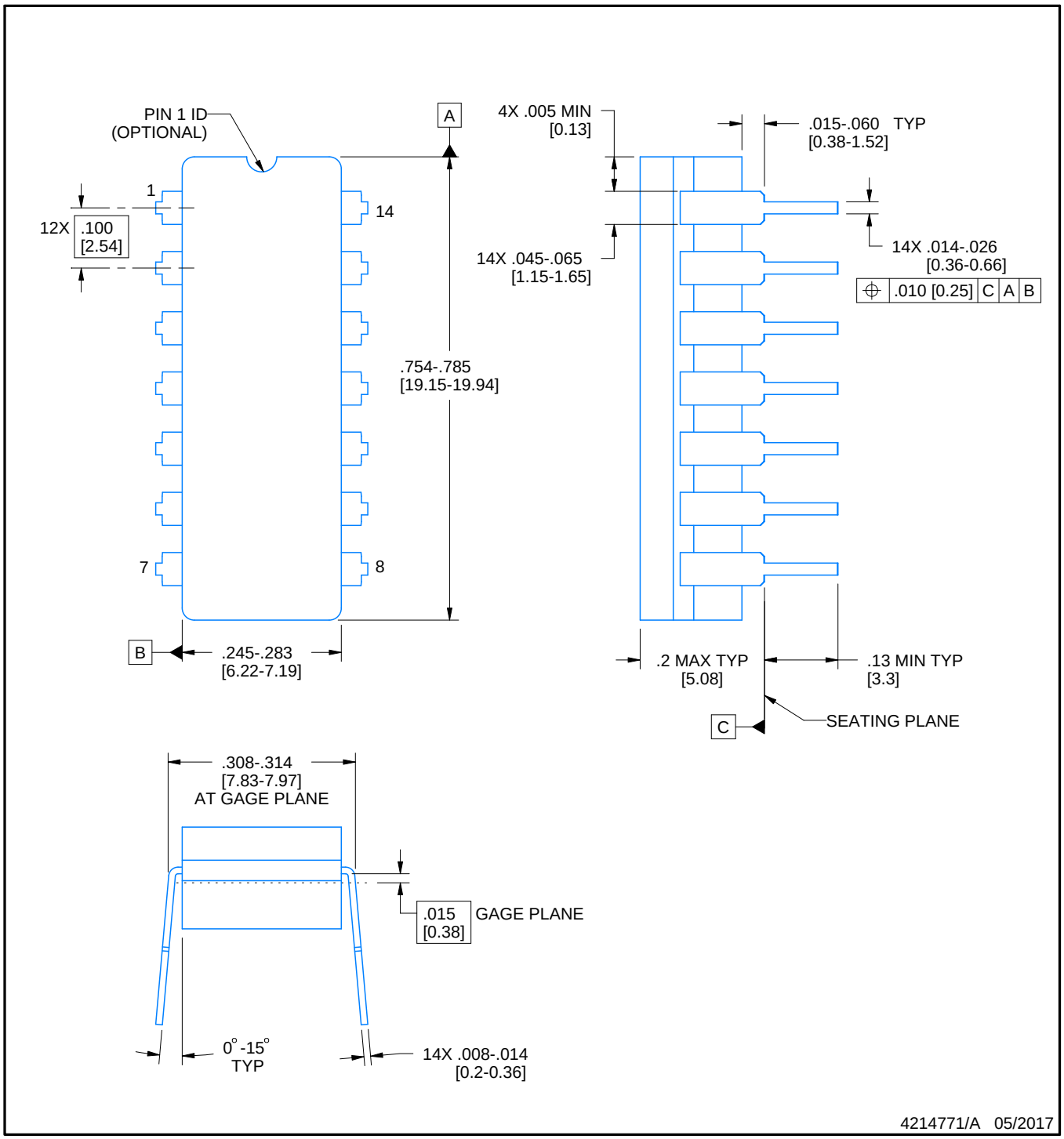
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

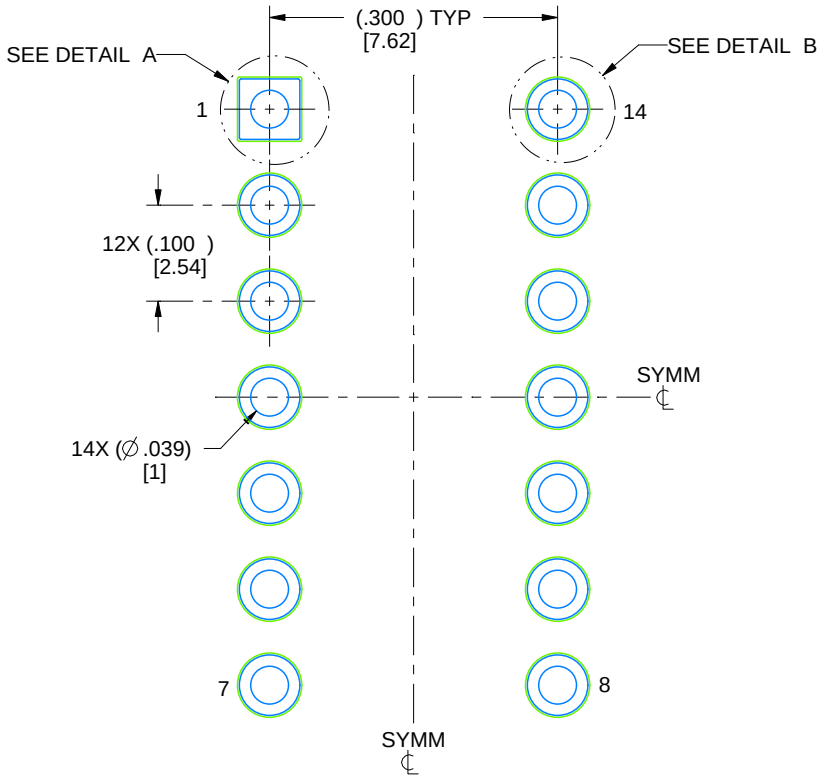
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

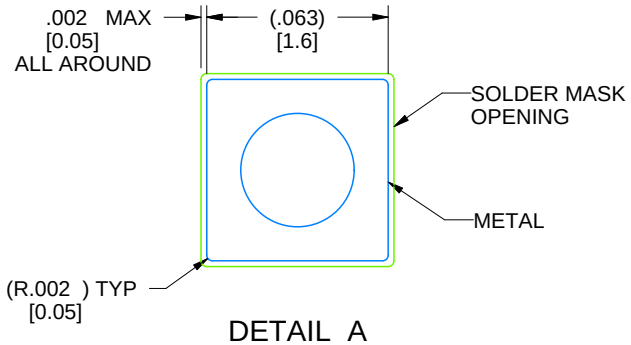
## J0014A

## CDIP - 5.08 mm max height

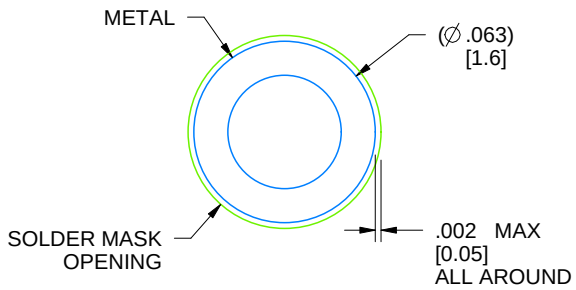
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



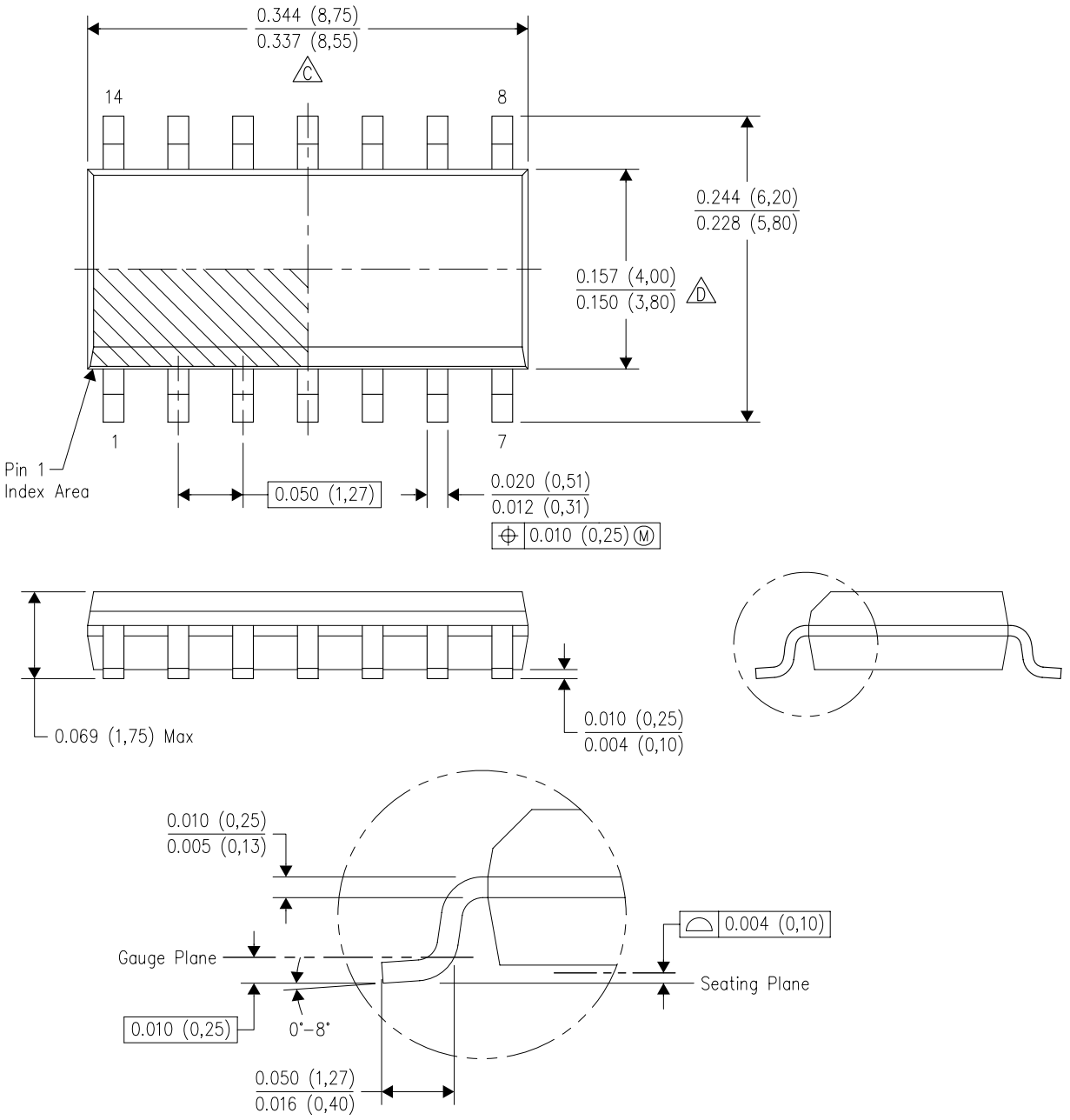

DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

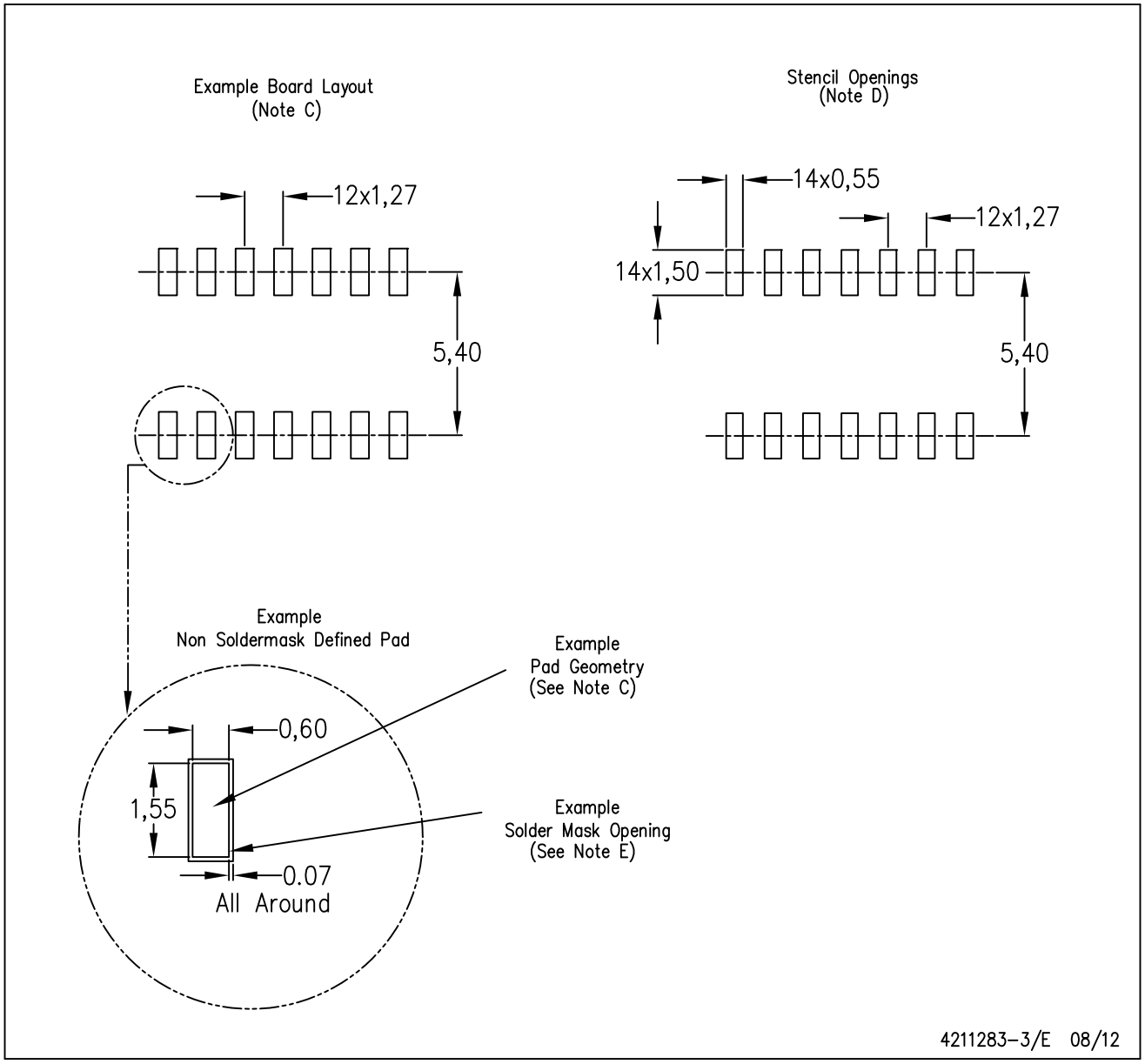
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

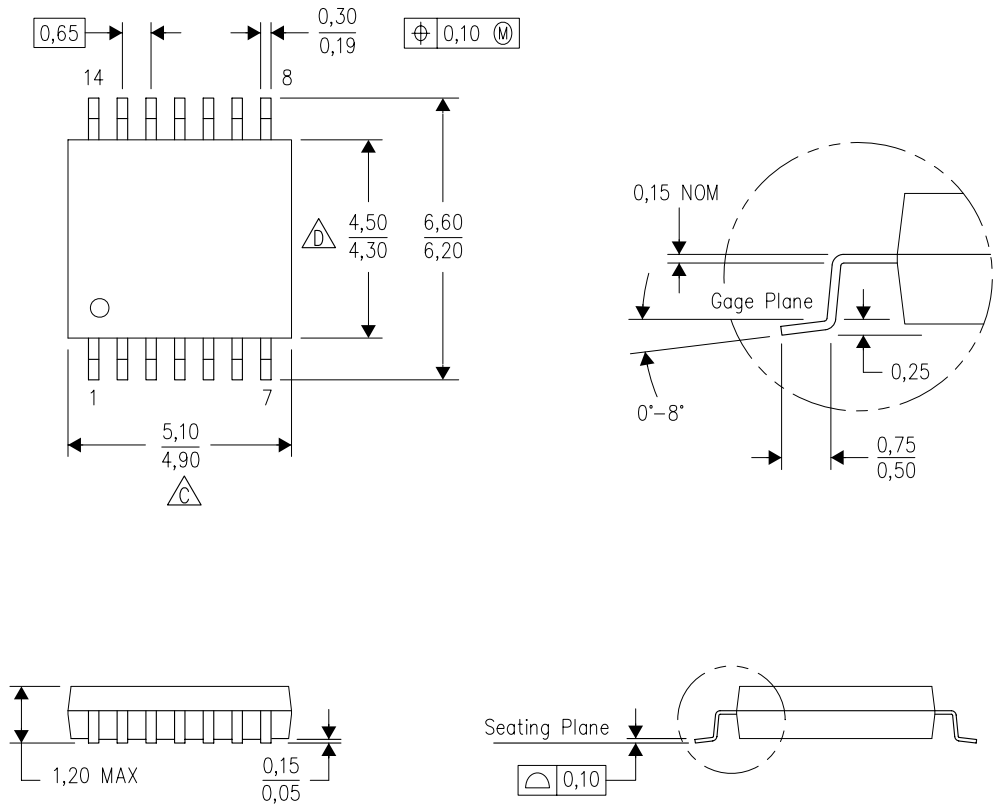
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

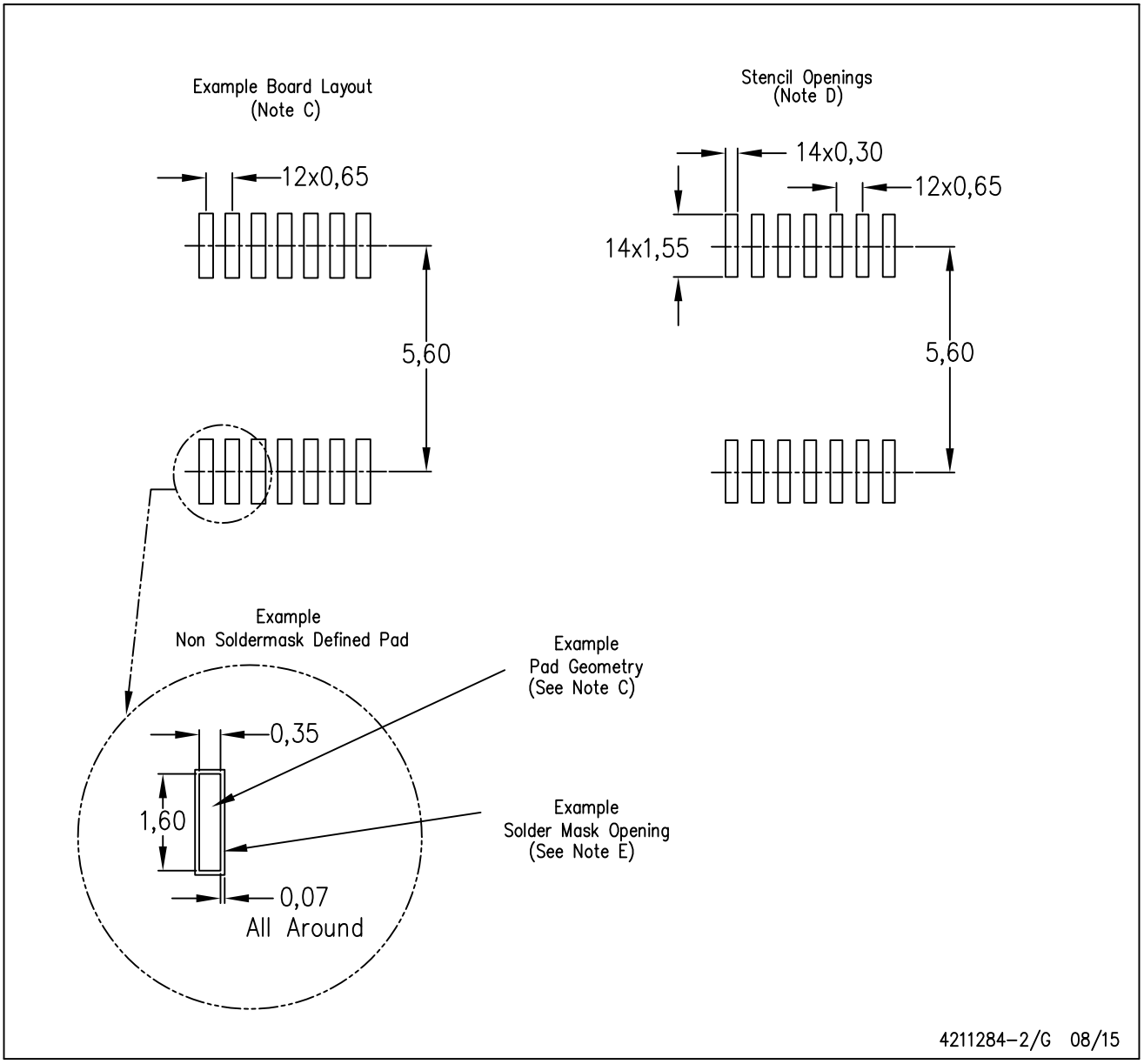
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

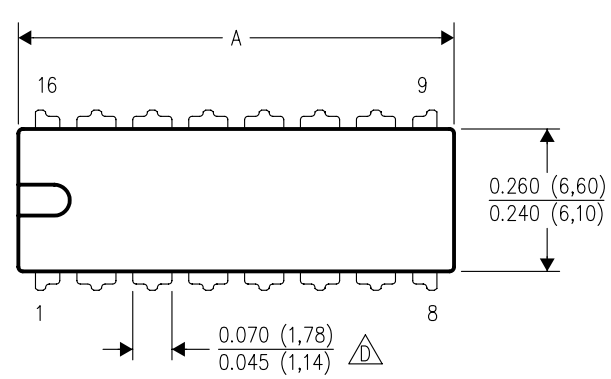



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

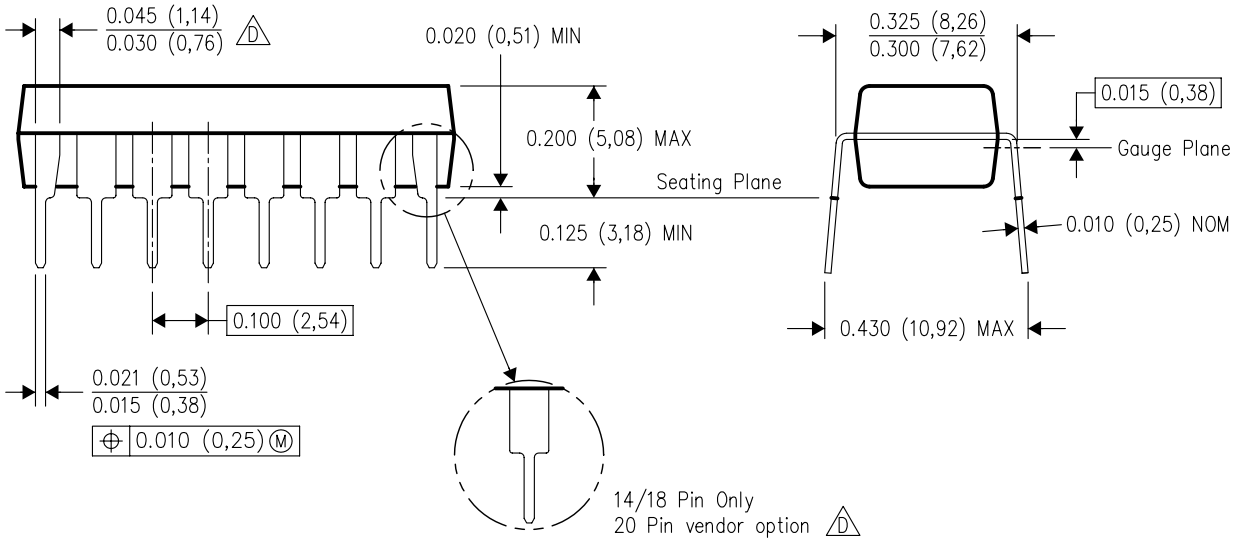
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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