

# SN74LV273A 具有清零功能的八路 D 类触发器

## 1 特性

- $V_{CC}$  工作范围为 2V 至 5.5V
- 5V 时  $t_{pd}$  最大值为 10.5 ns
- $V_{OLP}$  (输出接地反弹) 典型值小于 0.8V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ )
- $V_{OHV}$  (输出  $V_{OH}$  下冲) 典型值大于 2.3V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ )
- $I_{off}$  支持局部断电模式运行
- 所有端口上均支持以混合模式电压运行
- 闩锁性能超过 250mA, 符合 JESD 17 规范
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求:
  - 3000V 人体放电模型
  - 2000V 充电器件模型

## 2 应用

- 变电站控制
- I/O 模块; 模拟 PLC/DCS 输入
- 人机界面 (HMI)
- 流量计
- 患者监护
- 测试和测量解决方案

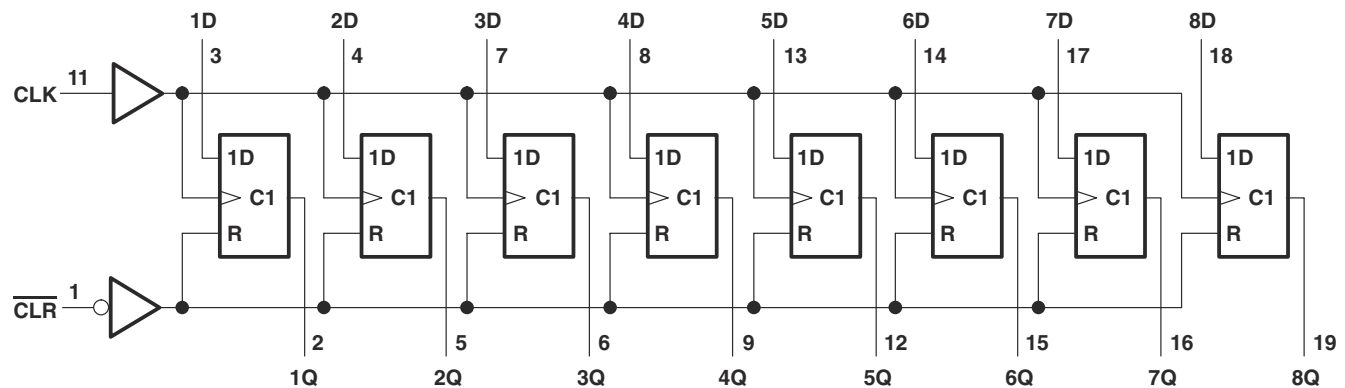
## 3 说明

SN74LV273A 器件是一款八路 D 类触发器, 旨在 2V 至 5.5V  $V_{CC}$  下运行。

封装信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (NOM)
SN74LV273A	DB (SSOP, 20)	7.20mm × 5.30mm
	DGV (TVSOP, 20)	5.00mm × 4.40mm
	DW (SOIC, 20)	12.80mm × 7.50mm
	NS (SOP, 20)	12.60mm × 5.30mm
	PW (TSSOP, 20)	6.50mm × 4.40mm
	RGY (VQFN 20)	4.50mm × 3.50mm
	RKS (VQFN, 20)	4.50mm × 2.50mm
	GQN (BGA, 20)	4.00mm × 3.00mm
	ZQN (BGA, 20)	4.00mm × 3.00mm
DGS (VSSOP, 20)	5.10mm × 3.00mm	

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



逻辑图 (正逻辑)

## Table of Contents

<b>1 特性</b> .....	<b>1</b>	<b>7 Parameter Measurement Information</b> .....	<b>12</b>
<b>2 应用</b> .....	<b>1</b>	<b>8 Detailed Description</b> .....	<b>13</b>
<b>3 说明</b> .....	<b>1</b>	8.1 Overview.....	13
<b>4 Revision History</b> .....	<b>2</b>	8.2 Functional Block Diagram.....	13
<b>5 Pin Configurations and Functions</b> .....	<b>3</b>	8.3 Feature Description.....	13
<b>6 Specifications</b> .....	<b>5</b>	8.4 Device Functional Modes.....	14
6.1 Absolute Maximum Ratings .....	5	<b>9 Application and Implementation</b> .....	<b>15</b>
6.2 ESD Ratings.....	5	9.1 Application Information.....	15
6.3 Recommended Operating Conditions .....	6	9.2 Typical Application .....	15
6.4 Thermal Information.....	6	9.3 Power Supply Recommendations.....	18
6.5 Electrical Characteristics.....	7	9.4 Layout.....	18
6.6 Timing Requirements, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ .....	7	<b>10 Device and Documentation Support</b> .....	<b>19</b>
6.7 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	7	10.1 接收文档更新通知.....	19
6.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	8	10.2 支持资源.....	19
6.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ .....	8	10.3 Trademarks.....	19
6.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	8	10.4 静电放电警告.....	19
6.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	9	10.5 术语表.....	19
6.12 Noise Characteristics .....	9	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>19</b>
6.13 Operating Characteristics.....	9		
6.14 Typical Characteristics.....	10		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision L (November 2022) to Revision M (January 2023)</b>	<b>Page</b>
• 向数据表添加了 <i>DGS</i> 封装信息.....	1

---

<b>Changes from Revision K (April 2014) to Revision L (November 2022)</b>	<b>Page</b>
• 删除了 <i>特性</i> 部分中的 200V 机器放电模型.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 向数据表中添加了 <i>RKS</i> 封装.....	1
• Added the <i>Balanced CMOS Push-Pull Output, Latching Logic, Partial Power Down (<math>I_{off}</math>)</i> sections.....	13
• Removed the <i>Design Requirements</i> section.....	15
• Added the <i>Power Considerations, Input Considerations, Output Considerations</i> sections.....	15
• Updated the <i>Layout Example</i> section.....	18

---

<b>Changes from Revision J (April 2005) to Revision K (December 2014)</b>	<b>Page</b>
• 添加了 <i>应用、器件信息表、引脚功能表、ESD 等级表、热性能信息表、典型特性、特性说明</i> 部分、 <i>器件功能模式、应用和实施</i> 部分、 <i>电源相关建议</i> 部分、 <i>布局</i> 部分、 <i>器件和文档支持</i> 部分以及 <i>机械、封装和可订购信息</i> 部分.....	1
• 删除了“订购信息”表.....	1
• Changed MAX operating temperature to 125°C in Recommended Operating Conditions table. ....	6

## 5 Pin Configurations and Functions

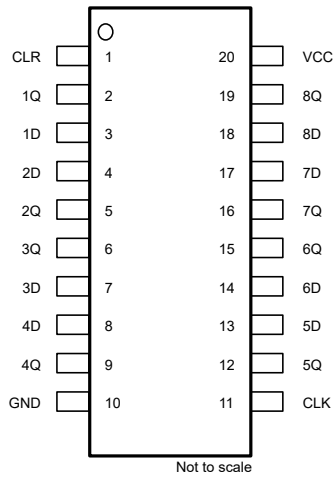


图 5-1. SN74LV273A DB, DGV, DW, NS, PW, or DGS Package, 20-Pin SSOP, TVSOP, SOP, TSSOP, or VSSOP (Top View)

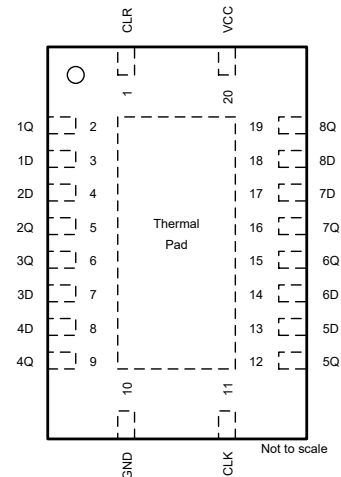


图 5-2. SN74LV273A RGY or RKS Package, 20-Pin VQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
CLR	1	I	Clear Pin
1Q	2	O	1Q Output
1D	3	I	1D Input
2D	4	I	2D Input
2Q	5	O	2Q Output
3Q	6	O	3Q Output
3D	7	I	3D Input
4D	8	I	4D Input
4Q	9	O	4Q Output
GND	10	—	Ground Pin
CLK	11	I	Clock Pin
5Q	12	O	5Q Output
5D	13	I	5D Input
6D	14	I	6D Input
6Q	15	O	6Q Output
7Q	16	O	7Q Output
7D	17	I	7D Input
8D	18	I	8D Input
8Q	19	O	8Q Output
V <sub>CC</sub>	20	—	Power Pin
Thermal Pad		—	Thermal Pad <sup>(2)</sup>

(1) I = input, O = output

(2) RKS package only

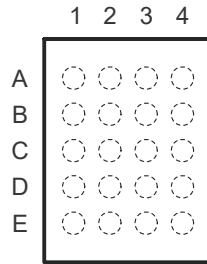


图 5-3. GQN or ZQN Package, 20-Pin BGA (Top View)

表 5-2. GQN or ZQN Pin Assignments

	1	2	3	4
<b>A</b>	1Q	$\overline{\text{CLR}}$	$V_{\text{CC}}$	8Q
<b>B</b>	2D	7D	1D	8D
<b>C</b>	3Q	2Q	6Q	7Q
<b>D</b>	4D	5D	3D	6D
<b>E</b>	GND	4Q	CLK	5Q

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		- 0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		- 0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>		- 0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2) (3)</sup>		- 0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		- 20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		- 50	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>stg</sub>	Storage temperature range		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	2000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

(1)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	-50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	-2	
		V <sub>CC</sub> = 3 V to 3.6 V	-6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	-12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	2	
		V <sub>CC</sub> = 3 V to 3.6 V	6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	20	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs ([SCBA004](#)).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LV273A									UNIT
	DB	DGV	DW	NS	PW	RGY	RKS	DGS		
	20 PINS									
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	98.7	118.1	81.8	79.4	104.7	37.1	75.2	125.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	60.4	33.4	47.8	45.9	38.8	46.1	79.4	80.0	
R <sub>θJB</sub>	Junction-to-board thermal resistance	56.9	59.6	49.4	46.9	55.7	14.9	47.8	63.8	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	21.6	1.1	20.1	19.1	2.9	1.3	14.6	8.4	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	53.5	58.9	49.0	46.5	55.1	15.0	47.8	79.9	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	9.8	31.5	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			- 40°C to 85°C		- 40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = - 50 μA	2 V to 5.5 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1		V <sub>CC</sub> - 0.1		V
	I <sub>OH</sub> = - 2 mA	2.3 V	2			2		2		
	I <sub>OH</sub> = - 6 mA	3 V	2.48			2.48		2.48		
	I <sub>OH</sub> = - 12 mA	4.5 V	3.8			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = - 50 μA	2 V to 5.5 V				0.1		0.1		V
	I <sub>OL</sub> = - 2 mA	2.3 V				0.4		0.4		
	I <sub>OL</sub> = - 6 mA	3 V				0.44		0.44		
	I <sub>OL</sub> = - 12 mA	4.5 V				0.55		0.55		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V				±1		±1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V				20		20		μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V				5		5		μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	2							pF

## 6.6 Timing Requirements, V<sub>CC</sub> = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [图 7-1](#))

			T <sub>A</sub> = 25°C		- 40°C to 85°C		- 40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLR low	6.5		7		7.5		ns
		CLK high or low	7		8.5		9		
t <sub>su</sub>	Setup time, data before CLK ↑	Data	8.5		10.5		12		ns
		CLR inactive	4		4		4.5		
t <sub>h</sub>	Hold time, data after CLK ↑		0.5		1		2.5		ns

## 6.7 Timing Requirements, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [图 7-1](#))

			T <sub>A</sub> = 25°C		- 40°C to 85°C		- 40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLR low	5		6		6.5		ns
		CLK high or low	5		6.5		7		
t <sub>su</sub>	Setup time, data before CLK ↑	Data	5.5		6.5		8		ns
		CLR inactive	2.5		2.5		3		
t <sub>h</sub>	Hold time, data after CLK ↑		1		1		2.5		ns

## 6.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

			$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to }85^\circ\text{C}$		$-40^\circ\text{C to }125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLR low	5		5		5.5		ns
		CLK high or low	5		5		5.5		
$t_{su}$	Setup time, data before CLK $\uparrow$	Data	4.5		4.5		6		ns
		CLR inactive	2		2		2.5		
$t_h$	Hold time, data after CLK $\uparrow$		1		1		2		ns

## 6.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to }85^\circ\text{C}$		$-40^\circ\text{C to }125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}$	55	95		45		45		MHz
			$C_L = 50\text{ pF}$	45	75		40		40		
$t_{pd}$	CLK	Q	$C_L = 15\text{ pF}$	10.4	18.3		1	20.5	1	22.5	ns
$t_{PHL}$	$\overline{\text{CLR}}$	Q		10.3	19		1	21	1	23	ns
$t_{pd}$	CLK	Q	$C_L = 50\text{ pF}$	12.9	22.1		1	25	1	27	ns
$t_{PHL}$	$\overline{\text{CLR}}$	Q		13.1	22.8		1	25.5	1	27.5	ns
$t_{sk(o)}$						2				2	ns

## 6.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to }85^\circ\text{C}$		$-40^\circ\text{C to }125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}$	75	140		65		65		MHz
			$C_L = 50\text{ pF}$	50	110		45		45		
$t_{pd}$	CLK	Q	$C_L = 15\text{ pF}$	7.1	13.6		1	16	1	17.5	ns
$t_{PHL}$	$\overline{\text{CLR}}$	Q		6.9	13.6		1	16	1	17.5	ns
$t_{pd}$	CLK	Q	$C_L = 50\text{ pF}$	9.1	17.1		1	19.5	1	21	ns
$t_{PHL}$	$\overline{\text{CLR}}$	Q		8.7	17.1		1	19.5	1	21	ns
$t_{sk(o)}$						1.5				1.5	ns



## 6.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	120	205		100		100		MHz
			$C_L = 50\text{ pF}$	80	160		70		70		
$t_{\text{pd}}$	CLK	Q	$C_L = 15\text{ pF}$		4.8	9	1	10.5	1	11.5	ns
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q			4.7	8.5	1	10	1	11	ns
$t_{\text{pd}}$	CLK	Q	$C_L = 50\text{ pF}$		6.2	11	1	12.5	1	14	ns
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q			6	10.5	1	12	1	13.5	ns
$t_{\text{sk(o)}}$							1			1	ns

## 6.12 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		SN74LV273A			UNIT
		MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic $V_{\text{OL}}$		0.4	0.8	V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic $V_{\text{OL}}$		-0.4	-0.8	V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic $V_{\text{OH}}$		2.9		V
$V_{\text{IH(D)}}$	High-level dynamic input voltage		2.31		V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage			0.99	V

## 6.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		$V_{CC}$	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 10\text{ MHz}$	3.3 V	15.9	pF
				5 V	17.1	

## 6.14 Typical Characteristics

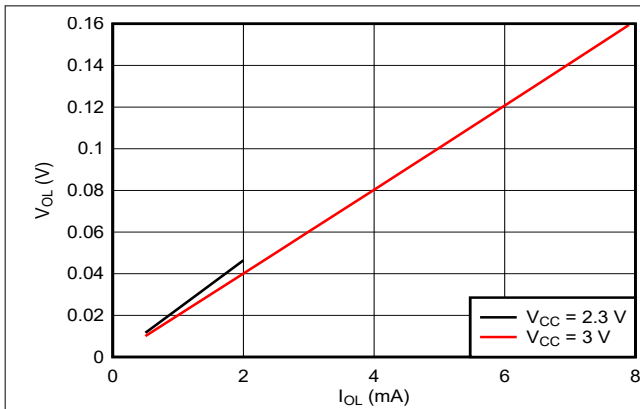


图 6-1. Output Voltage in LOW state, 2.3- and 3-V Supply

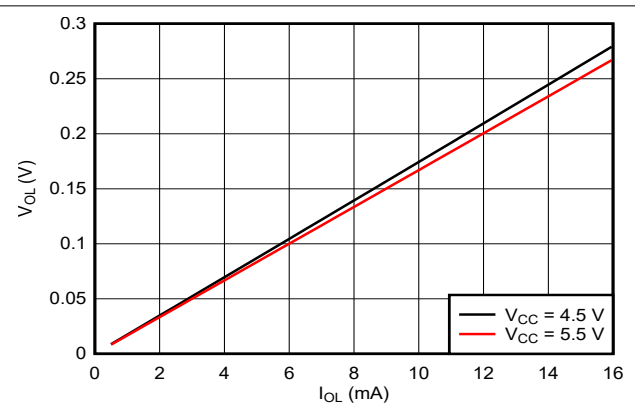


图 6-2. Output Voltage in LOW state, 4.5- and 5.5-V Supply

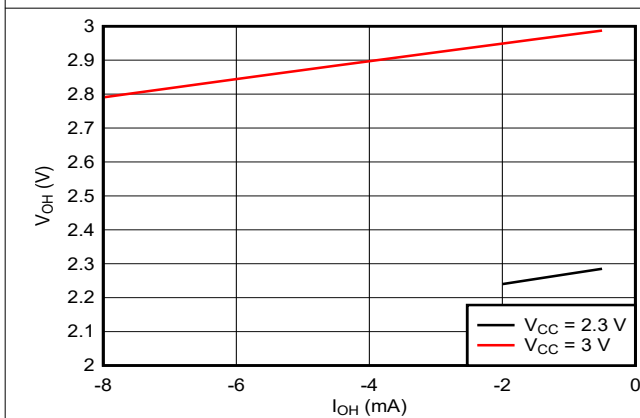


图 6-3. Output Voltage in HIGH state, 2.3- and 3-V Supply

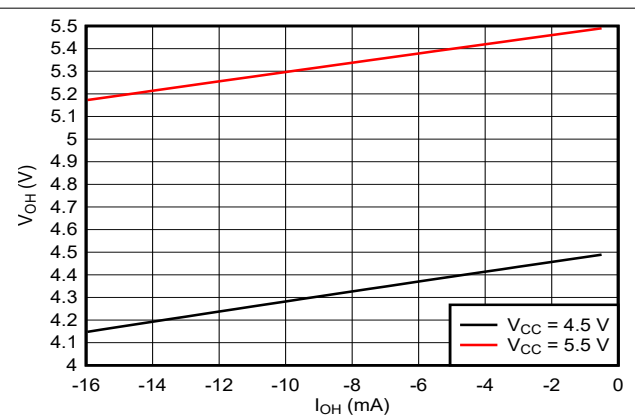


图 6-4. Output Voltage in HIGH state, 4.5- and 5.5-V Supply

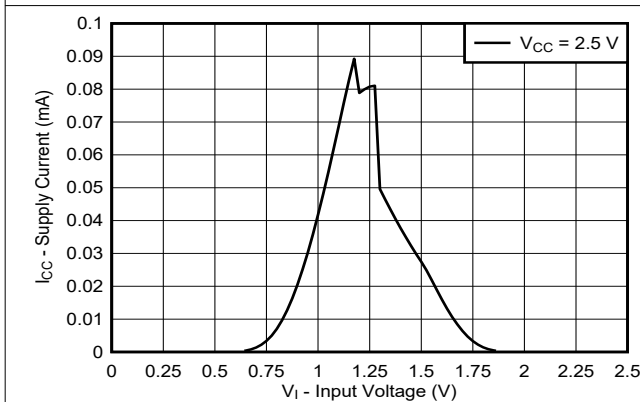


图 6-5. Supply Current across Input Voltage, 2.5-V Supply

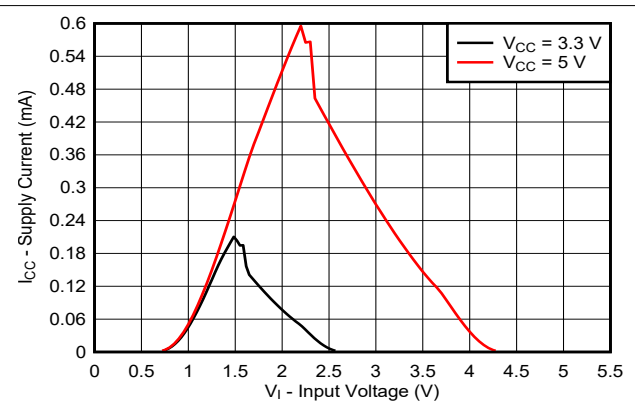
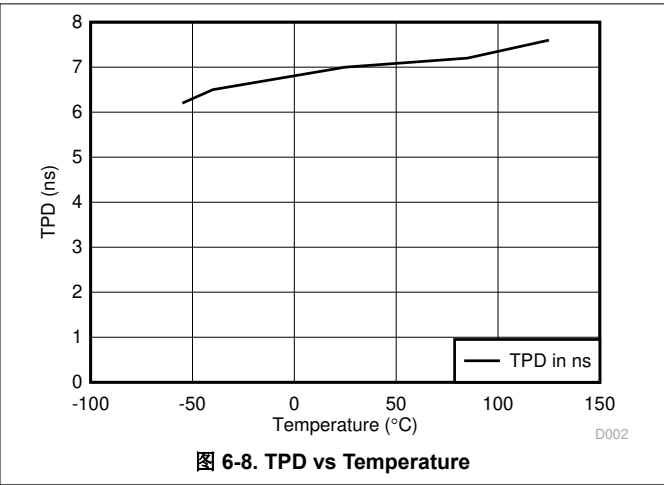
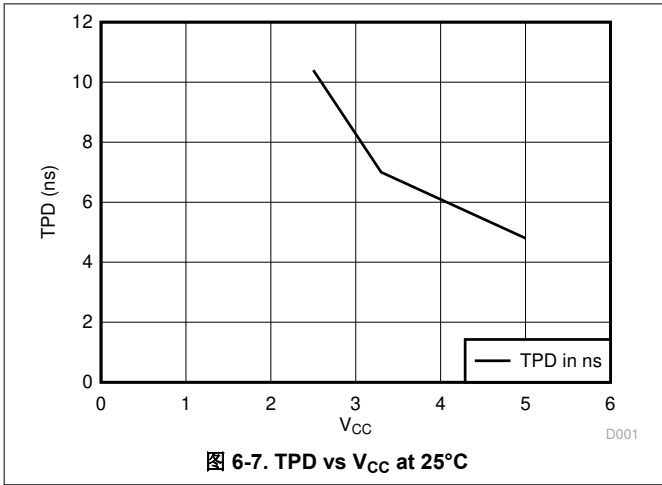
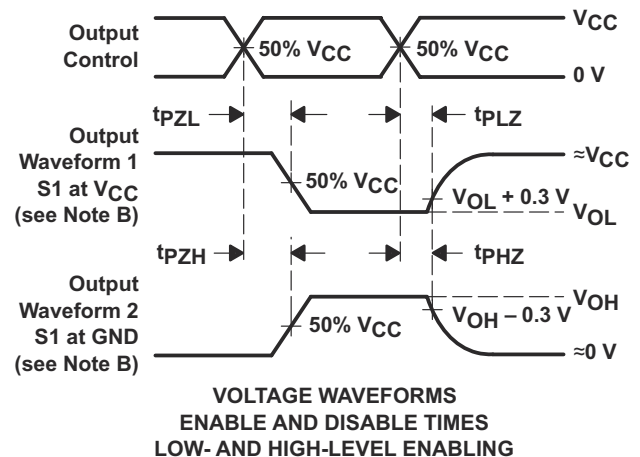
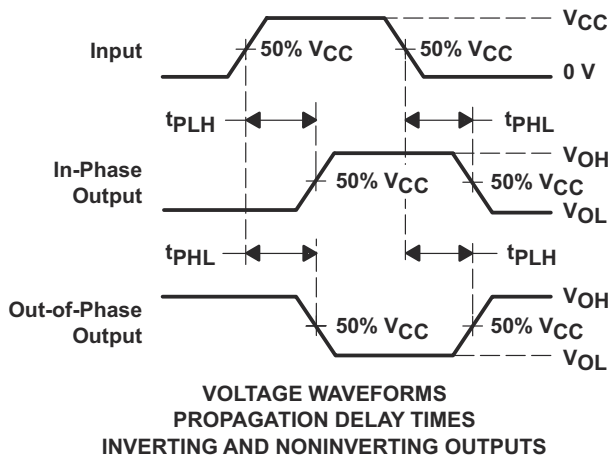
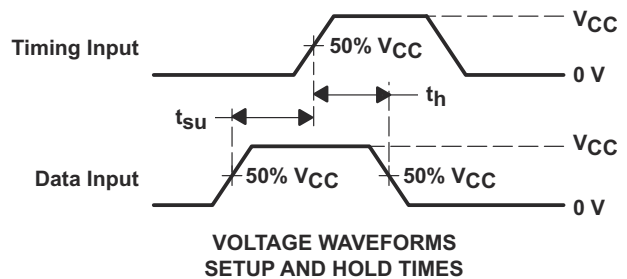
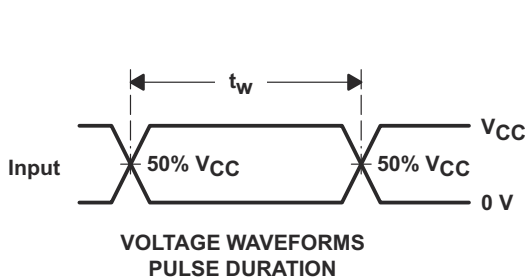
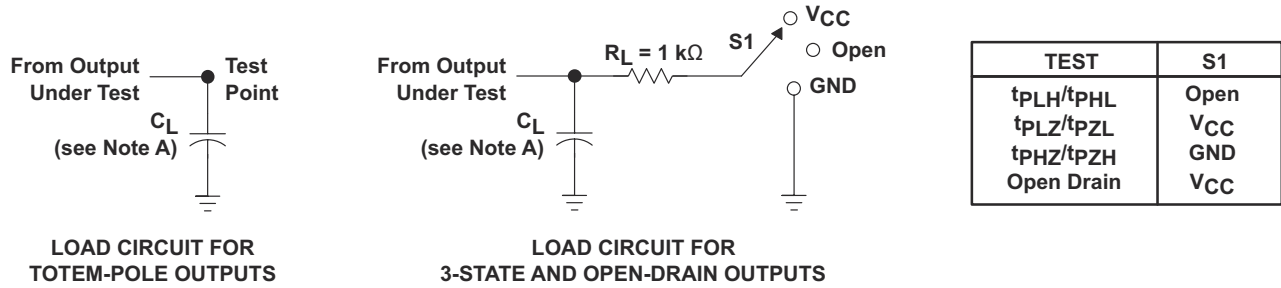


图 6-6. Supply Current across Input Voltage, 3.3- and 5-V Supply

### 6.14 Typical Characteristics (continued)



## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

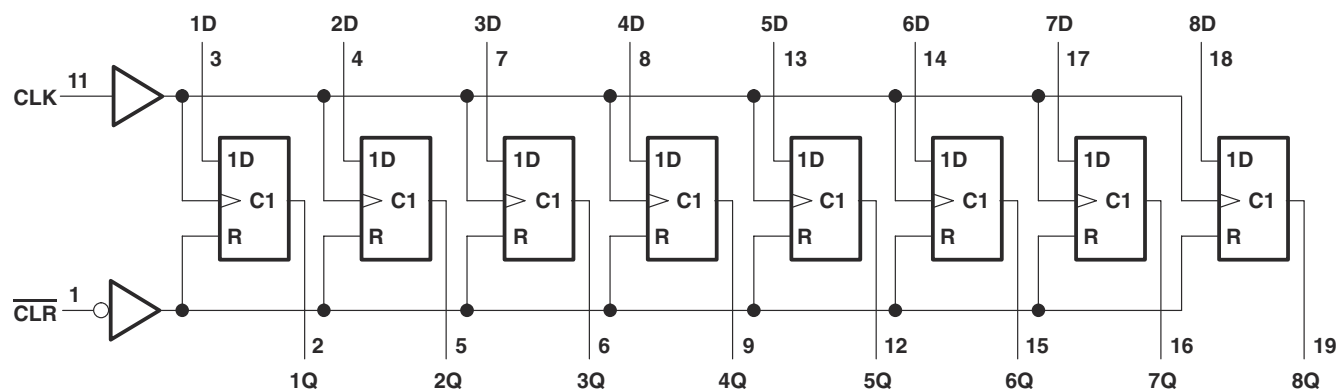
### 8.1 Overview

The SN74LV273A device is an octal D-type flip-flop designed for 2-V to 5.5-V  $V_{CC}$  operation.

This device is a positive-edge-triggered flip-flop with direct clear ( $\overline{CLR}$ ) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV273A device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

#### 8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

#### 8.3.3 Partial Power Down ( $I_{off}$ )

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the  $I_{off}$  specification in the *Electrical Characteristics* table.

### 8.3.4 Clamp Diode Structure

图 8-1 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

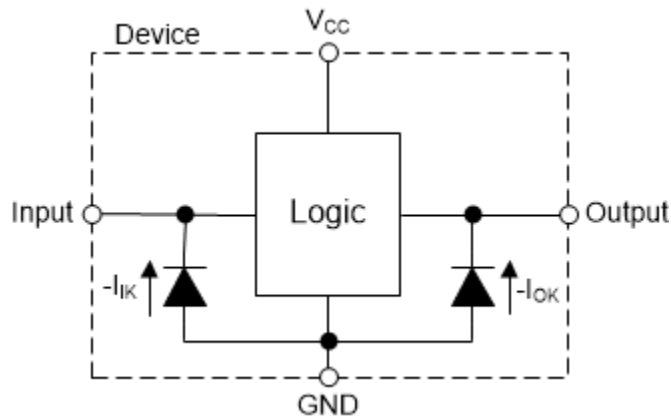


图 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

### 8.4 Device Functional Modes

表 8-1. Function Table  
(Each Flip-Flop)

INPUTS			OUTPUT Q
CLR	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The SN74LV273A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid  $V_{CC}$ . This feature makes it Ideal for translating down to the  $V_{CC}$  level. 图 9-2 shows the reduction in ringing compared to higher drive parts such as AC.

### 9.2 Typical Application

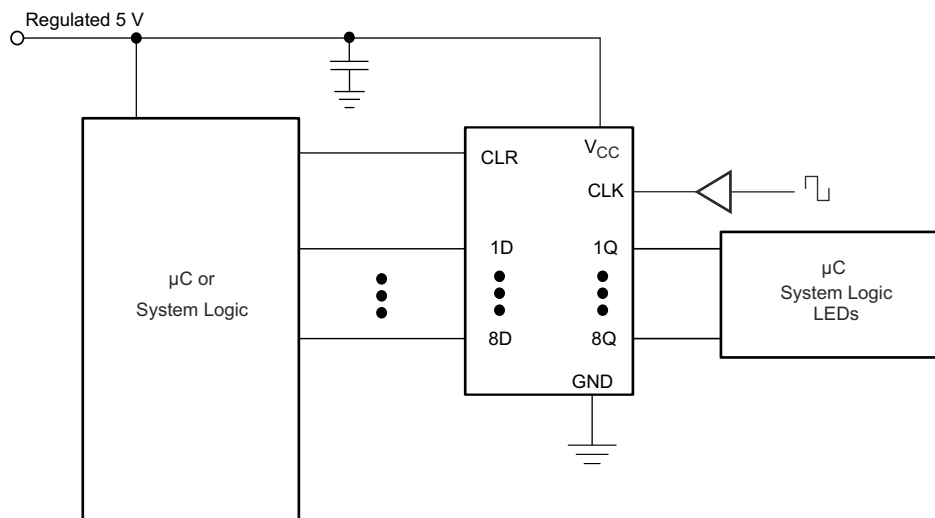


图 9-1. Typical Application Schematic

### 9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV273A plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV273A plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV273A can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV273A can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV273A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74LV273A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.



### 9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV273A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 9.2.5 Application Curves

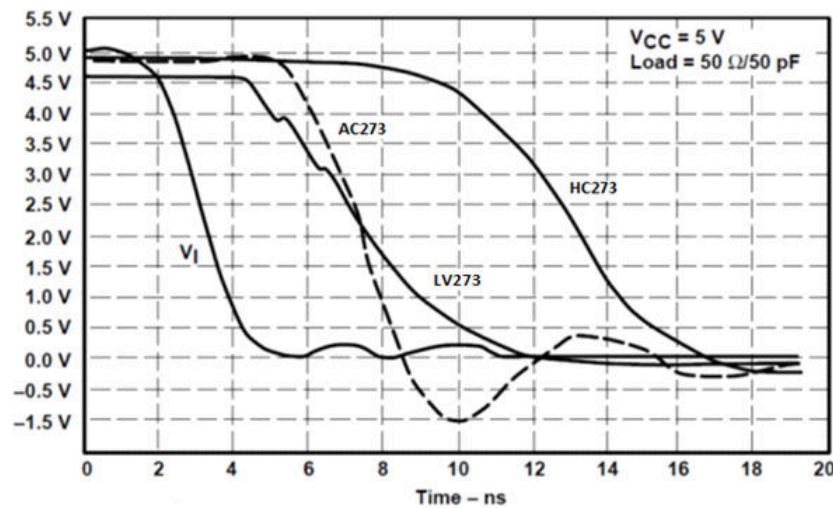


图 9-2. Switching Characteristics Comparison

### 9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

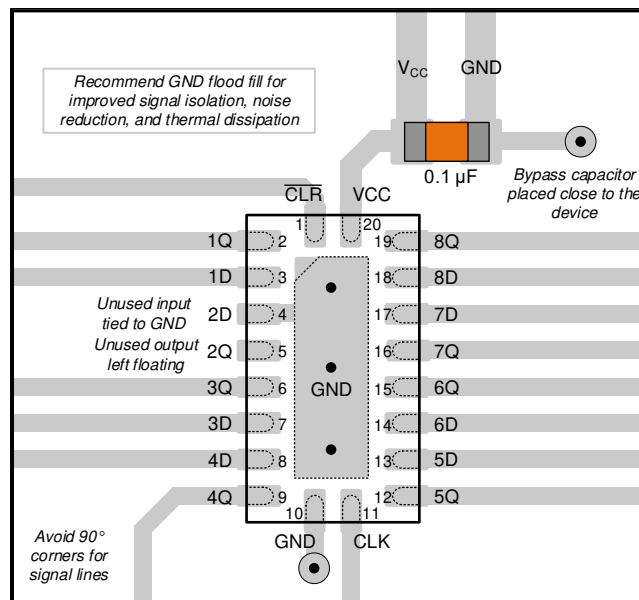
### 9.4 Layout

#### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 9-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

#### 9.4.2 Layout Example



**Figure 9-3. Layout Example for SN74LV273A in the RKS Package**

## 10 Device and Documentation Support

### 10.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 10.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
所有商标均为其各自所有者的财产。

### 10.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 10.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV273ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273ADBRE4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273ADBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273ADGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L273A	<a href="#">Samples</a>
SN74LV273ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273ADWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV273A	<a href="#">Samples</a>
SN74LV273APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273APWE4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273APWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273APWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273APWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV273A	<a href="#">Samples</a>
SN74LV273ARKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

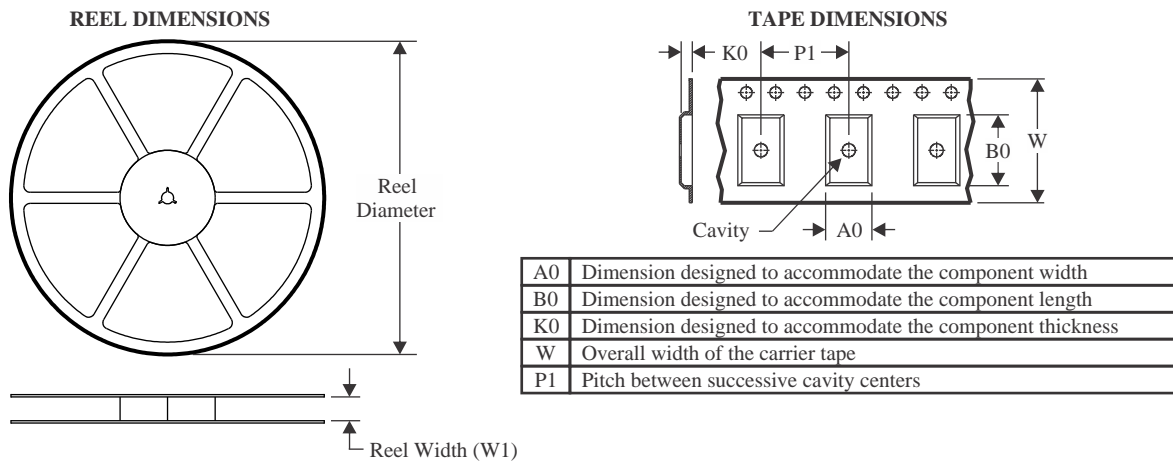
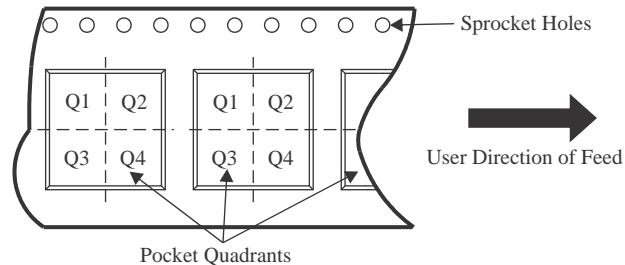
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV273A :**

- Automotive : [SN74LV273A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


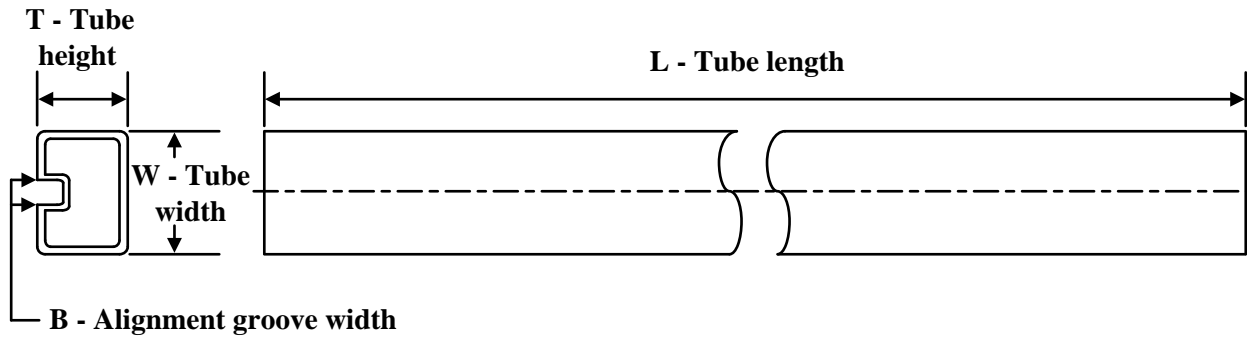
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV273ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV273ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LV273ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV273ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV273ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV273APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV273APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV273APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV273APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV273ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LV273ARKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV273ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LV273ADGSR	VSSOP	DGS	20	5000	356.0	356.0	35.0
SN74LV273ADGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74LV273ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV273ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV273APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV273APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LV273APWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV273APWT	TSSOP	PW	20	250	356.0	356.0	35.0
SN74LV273ARGYR	VQFN	RGY	20	3000	356.0	356.0	35.0
SN74LV273ARKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV273ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LV273ADWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LV273APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LV273APWE4	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LV273APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5



## GENERIC PACKAGE VIEW

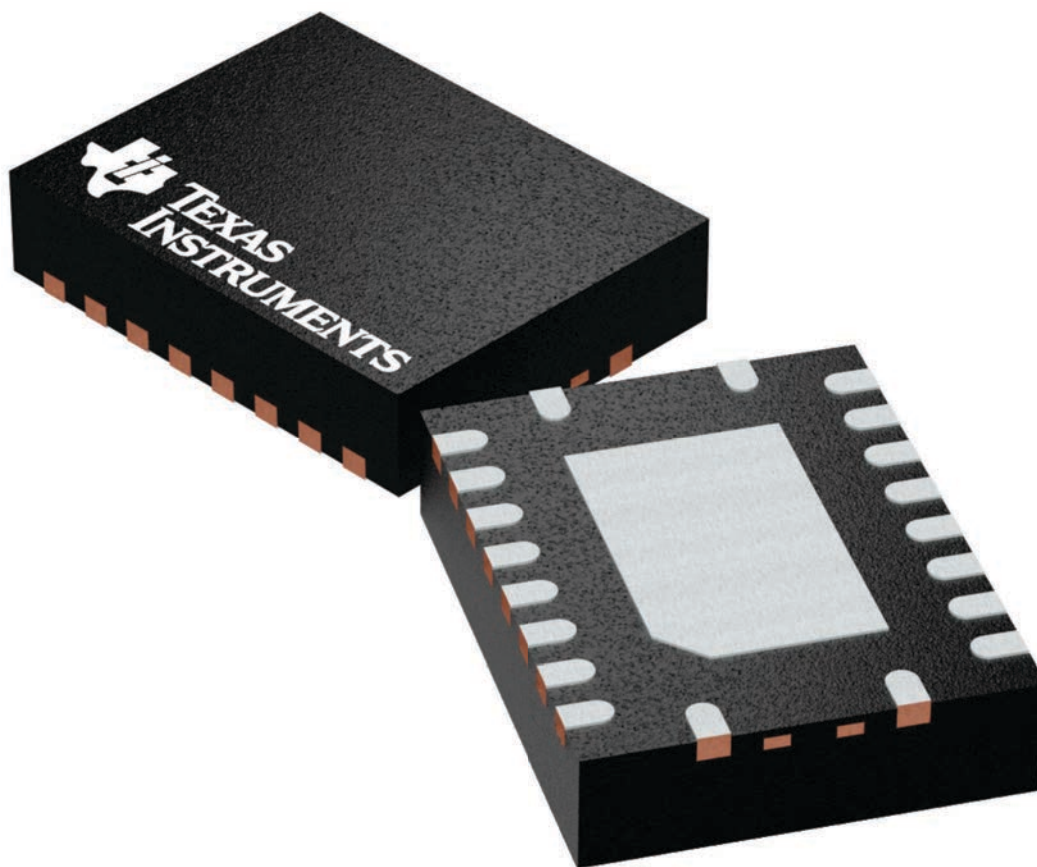
**RGY 20**

**VQFN - 1 mm max height**

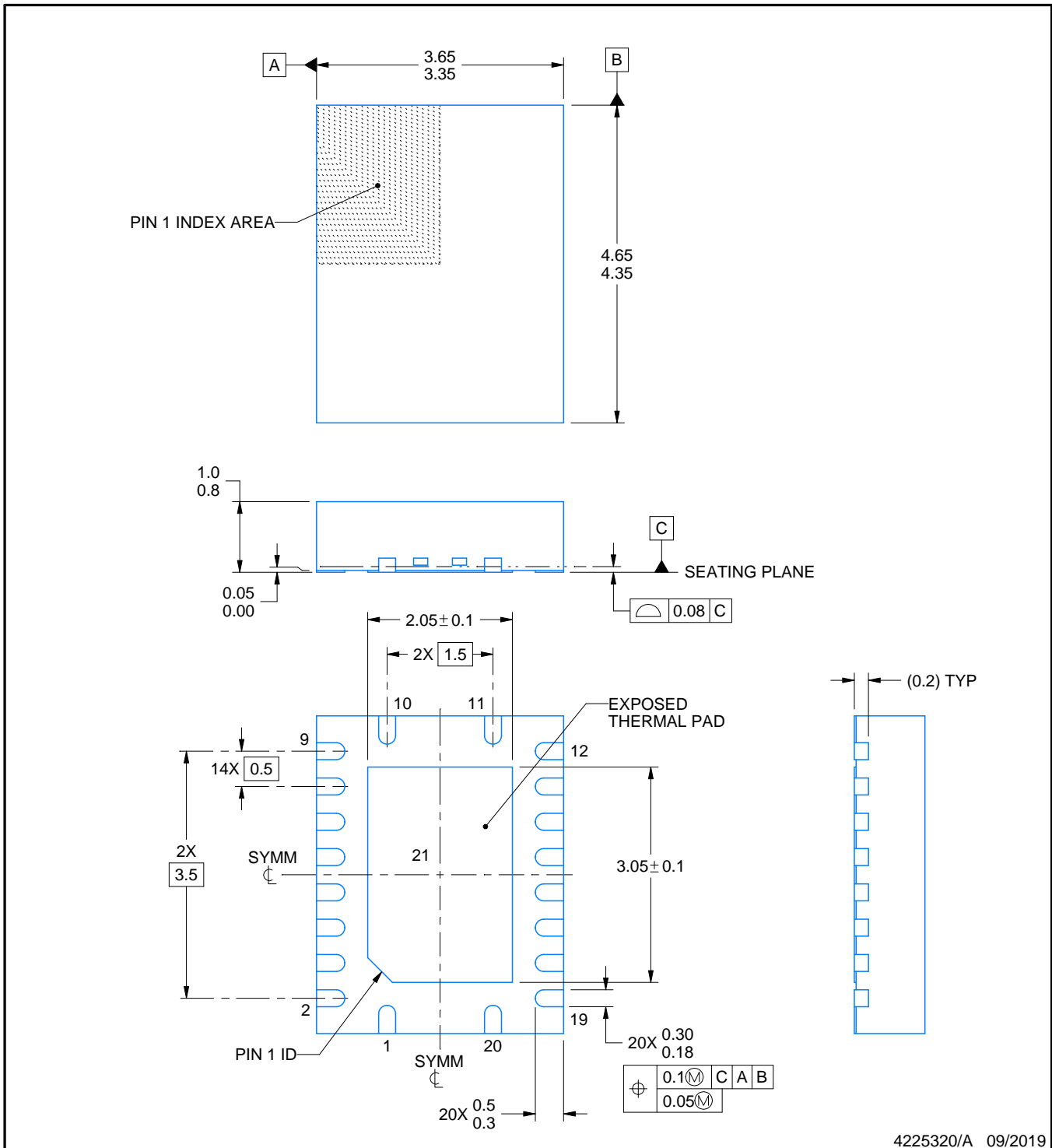
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

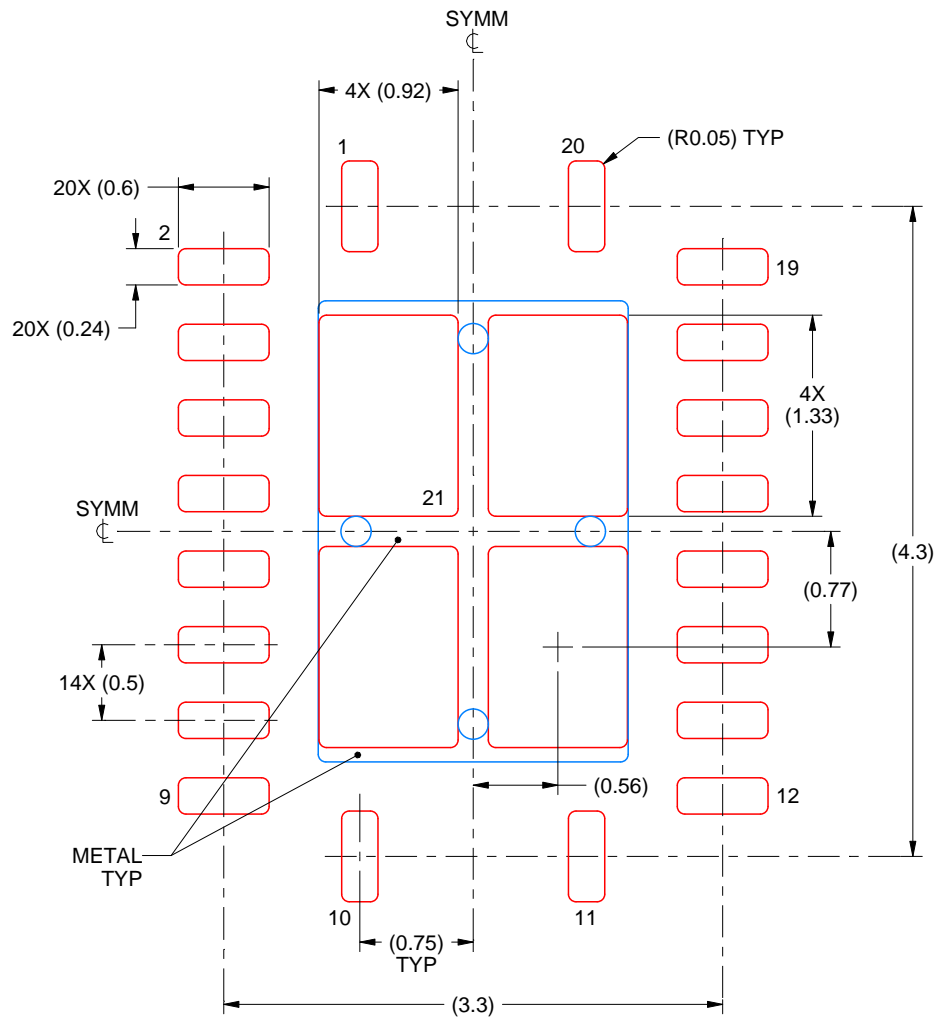
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

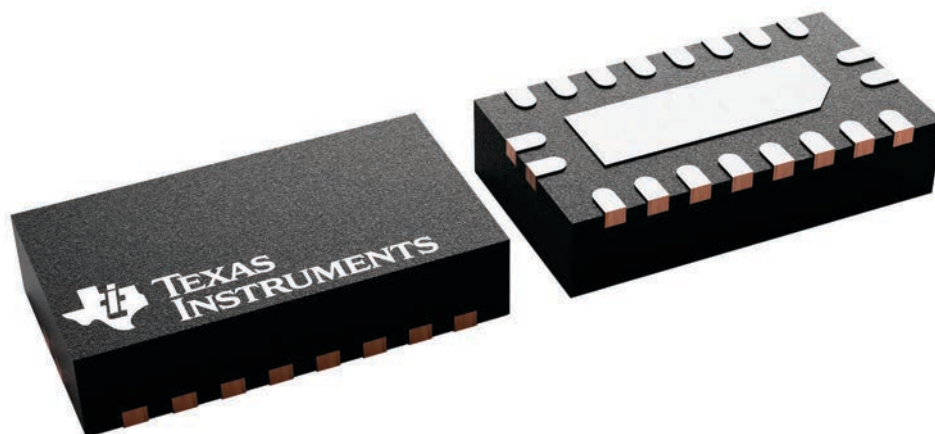
**RKS 20**

**VQFN - 1 mm max height**

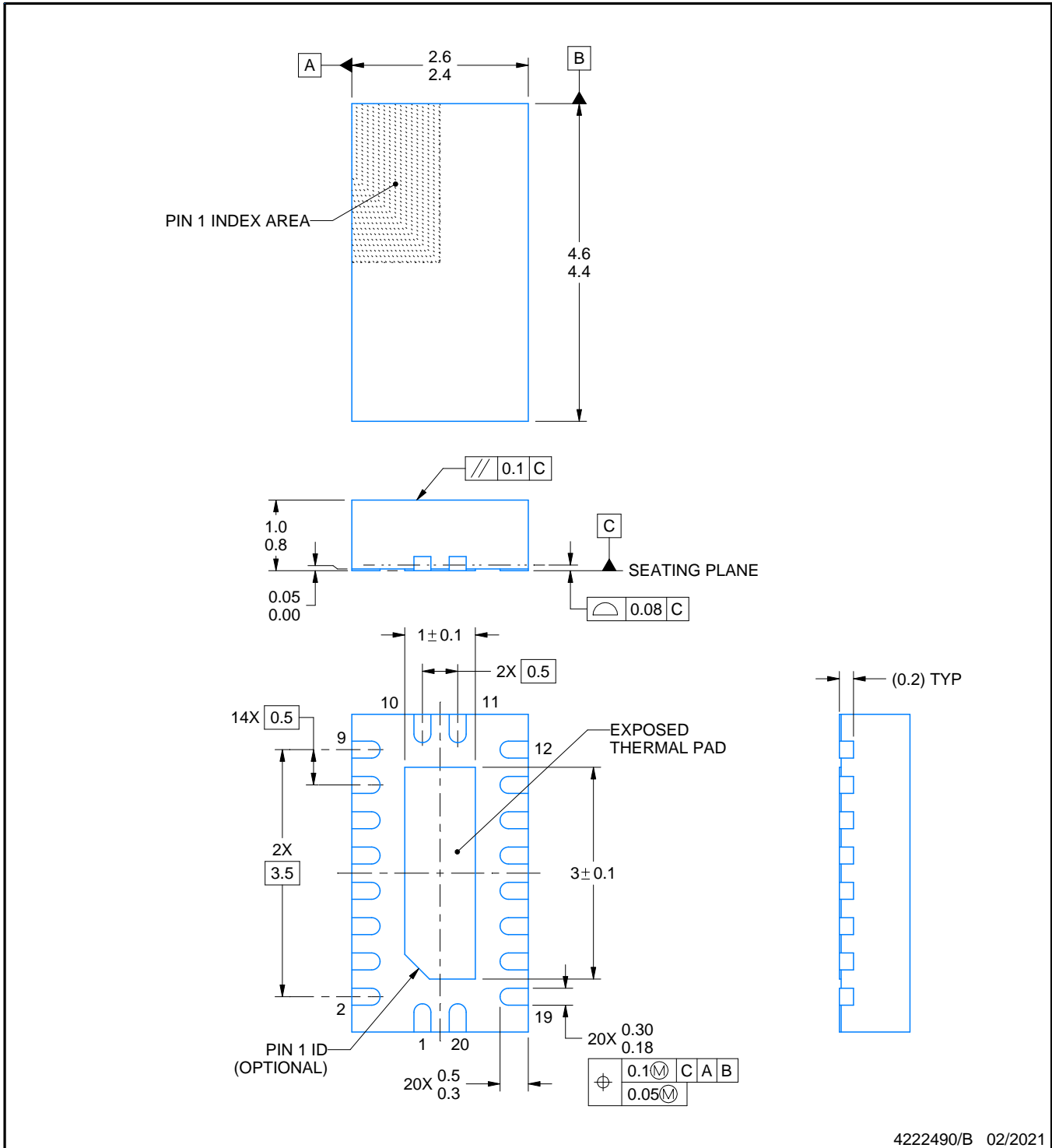
2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226872/A



NOTES:

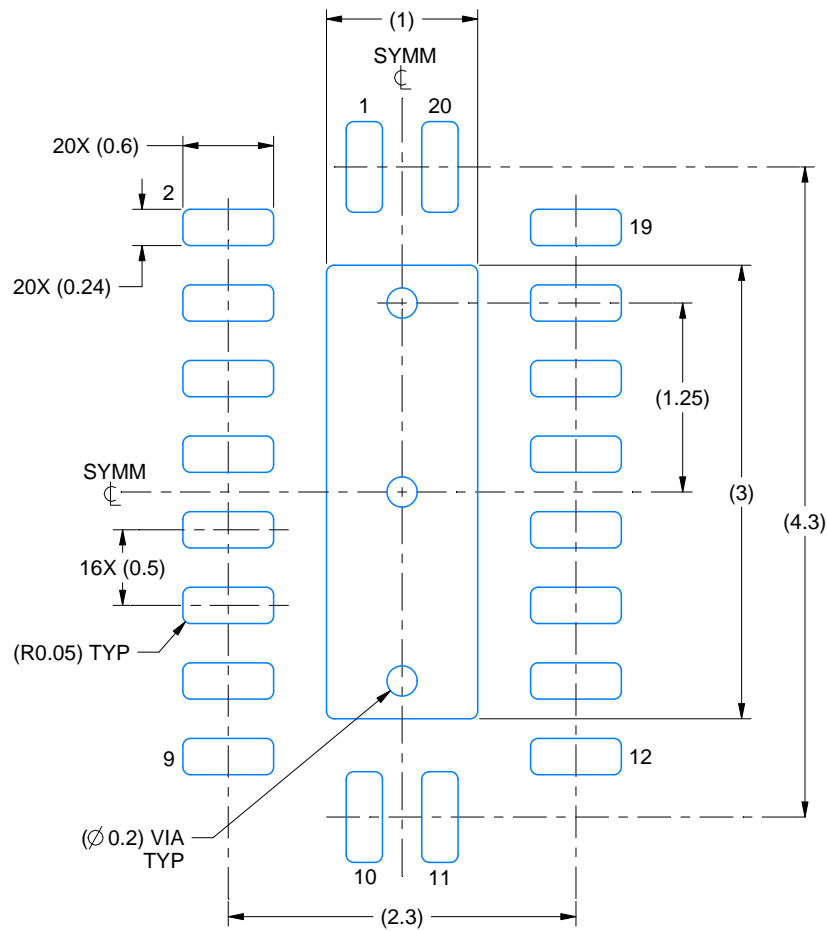
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

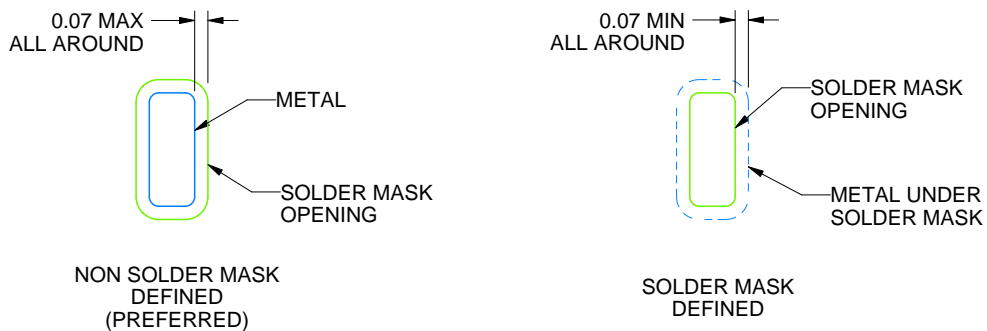
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

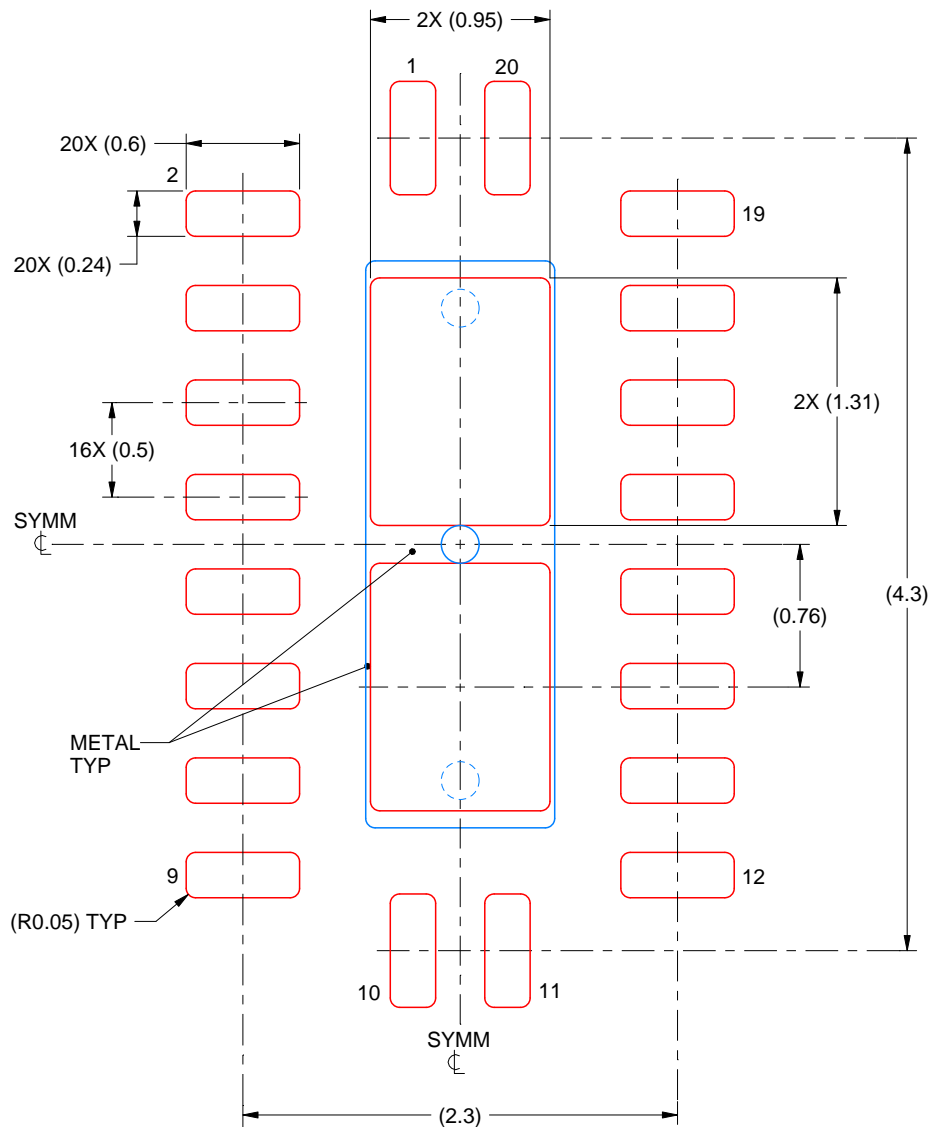
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 83% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:25X

4222490/B 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Flip-Flops](#) category:*

*Click to view products by [Texas Instruments](#) manufacturer:*

Other Similar products are found below :

[NLV74HC74ADTR2G](#) [74F574SC](#) [TC7W74FUTE12LF](#) [NLV14013BDR2G](#) [NLV74HC74ADR2G](#) [MC10EP131MNG](#) [MC74AC74DTR2](#)  
[74VHC574FT\(BJ\)](#) [HT4093ARZ](#) [SN74HC374ANSR](#) [CD4528BE](#) [CD4027BE](#) [RS74HC74XQ](#) [RS74HC74XP](#) [RS574XTSS20](#) [CD40106BM-](#)  
[JSM](#) [74HCT273PW-Q100J](#) [SN74ABT273PWRE4](#) [CLVC2G74QDCURG4Q1](#) [CD4067TA24.TB](#) [CD4013SA.TR](#) [AIP74HCT14TA14.TB](#)  
[HSN74LVC1G14DBVR](#) [CD4013BPWRG](#) [AiP74LVC74TA14.TB](#) [CD4013BDRG](#) [CD4528SA16.TR](#) [AIP74HC273SA.TB](#)  
[SN74HCS74QDYRQ1](#) [CD4013TA14.TB](#) [SN74LS107N](#) [SN74LS374DWR](#) [SN74LVC2G14DC\(LX\)](#) [MC74HC73ADG](#) [MC74HC73ADR2G](#)  
[74LCX16374MTDX](#) [74LVT74D,118](#) [74VHCT9273FT\(BJ\)](#) [MM74HC374WM](#) [MM74HC74AMX](#) [74ALVCH162374PAG](#)  
[74LVC1G175GS,132](#) [74LVX74MTCX](#) [TC7WZ74FK,LJ\(CT](#) [MM74HCT273WM](#) [SN74LVC74AD](#) [SN74HC273DWR](#) [M74HC374RM13TR](#)  
[M74HC175B1R](#) [M74HC174RM13TR](#)