TEXAS INSTRUMENTS

SN74LV574A 具有三态输出的八路边沿触发 D 类触发器

1 特性

- 2V 至 5.5V V_{CC} 运行
- 5V 时 t_{pd} 最大值为 7.1ns
- V_{OLP}（输出接地反弹）
  典型值小于 0.8V（V_{CC} = 3.3V、T_A = 25°C）
- V_{OHV}（输出 V_{OH} 下冲）典型值
  大于 2.3 V（V_{CC} = 3.3V、T_A = 25°C）
- 支持所有端口上的混合模式电压运行
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 服务器
- 发光二极管 (LED) 显示屏
- 网络交换机
- 电信基础设施
- 电机驱动器
- I/O 扩展器
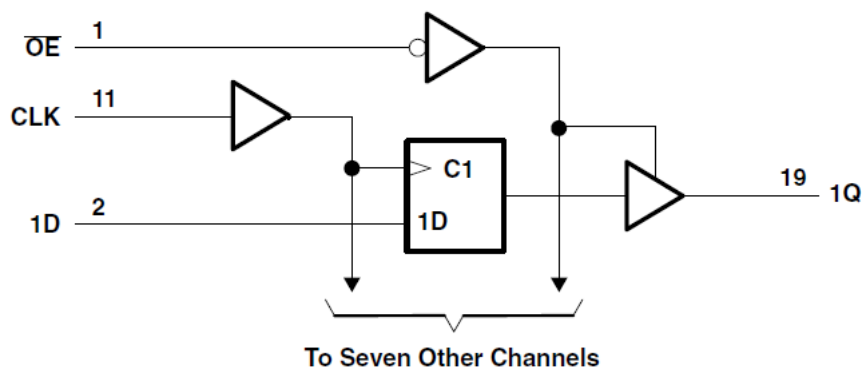
3 说明

'LV574A 器件是八路边沿触发 D 类触发器，旨在于 2V 至 5.5V V_{CC} 下运行。

这些器件具有专门设计用于驱动高容性或较低阻抗负载的三态输出。这些器件特别适用于实现缓冲寄存器、I/O 端口、双向总线驱动器和工作寄存器。

在时钟 (CLK) 输入发生正转换时，Q 输出被设置为在数据 (D) 输入端设置的逻辑电平。

封装信息[1]

器件型号	封装	封装尺寸（标称值）
SN74LV574A	DB (SSOP, 16)	6.2mm × 5.3mm
	DGV (TVSOP, 16)	3.6mm × 4.4mm
	DW（SOIC，16）	10.3mm × 7.5mm
	NS（SOP，16）	10.3mm × 5.3mm
	PW (TSSOP, 16)	5mm × 4.4mm
	RGY（VQFN，16）	4mm × 3.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

逻辑图（正逻辑）

English Data Sheet: SCLS412

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (April 2005) to Revision J (December 2022)	Page
• 通篇更新了表格、图和交叉参考的格式...1	

5 Pin Configuration and Functions
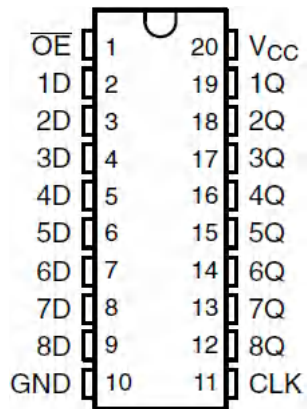
图 5-1. DB, DGV, DW, NS, or PW Package (Top View)
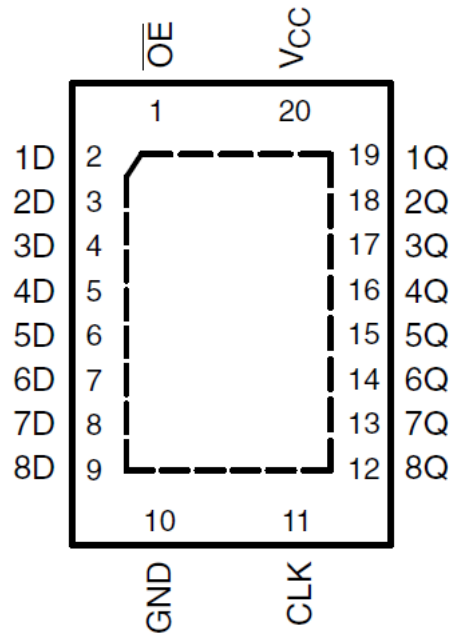
图 5-2. RGY Package (Top View)

表 5-1. Pin Functions

PIN		TYPE	Description
NO.	NAME		
1	$\overline{OE}$	I	Clear all channels, active low
2	1D	I	Channel 1, D input
3	2D	I	Channel 2, D input
4	3D	I	Channel 3, D input
5	4D	I	Channel 4, D input
6	5D	I	Channel 5, D input
7	6D	I	Channel 6, D input
8	7D	I	Channel 7, D input
9	8D	I	Channel 8, D input
10	GND	—	Ground
11	CLK	I	Clock Pin
12	8Q	O	Channel 8, Q output
13	7Q	O	Channel 7, Q output
14	6Q	O	Channel 6, Q output
15	5Q	O	Channel 5, Q output
16	4Q	O	Channel 4, Q output
17	3Q	O	Channel 3, Q output
18	2Q	O	Channel 2, Q output
19	1Q	O	Channel 1, Q output
20	V_{CC}	—	Power Pin

Product Folder Links: SN74LV574A

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	7	V
V_O	Output voltage range applied in the high or low state[2] [3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (A114-A)	±2000	V
		Machine Model (A115-A)	±200	
		Charged-Device Model (C101)	±1000	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	µA
		V_{CC} = 2.3 V to 2.7 V		– 2	mA
		V_{CC} = 3 V to 3.6 V		– 8	
		V_{CC} = 4.5 V to 5.5 V		– 16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		8	
		V_{CC} = 4.5 V to 5.5 V		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		– 40	125	°C

(1)   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

	THERMAL METRIC[1]	SN74LV574A							UNIT
		DB	DGV	DW	GQN	NS	PW	RGY	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	92	58	78	60	83	37	°C/W

(1)   For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$I_{OH} = -50\ \mu A$	2 V to 5.5 V	$V_{CC} - 0.1$			V
	$I_{OH} = -2\ mA$	2.3 V	2			
	$I_{OH} = -8\ mA$	3 V	2.48			
	$I_{OH} = -16\ mA$	4.5 V	3.8			
V_{OL}	$I_{OL} = 50\ \mu A$	2 V to 5.5 V			0.1	V
	$I_{OH} = 2\ mA$	2.3 V			0.4	
	$I_{OL} = 8\ mA$	3 V			0.44	
	$I_{OL} = 16\ mA$	4.5 V			0.55	
I_I	$V_I = 5.5\ V$ or GND	0 to 5.5 V			±1	μA
I_{OZ}	$V_O = VCC$ or GND	5.5 V			± 5	μA
I_{CC}	$V_I = VCC$ or GND, $I_O = 0$	5.5 V			20	μA
I_{off}	V_I or $V_O = 0$ to 5.5 V	0			5	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		1.8		pF

6.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted)

			T_A = 25°C		SN74LV574A		UNIT
			MIN	**MAX**	**MIN**	**MAX**	
t_w	Pulse duration	CLK high or low	7		7		ns
t_{su}	Setup time	High or low before CLK ↑	5.5		5.5		
t_h	Hold time	Data after CLK ↑	2		2		

Product Folder Links: *SN74LV574A*

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

			T_A = 25°C		SN74LV574A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		ns
t_{su}	Setup time	High or low before CLK ↑	3.5		3.5		
t_h	Hold time	Data after CLK ↑	1.5		1.5		

6.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted)

			T_A = 25°C		SN74LV574A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		ns
t_{su}	Setup time	High or low before CLK ↑	3.5		3.5		
t_h	Hold time	Data after CLK ↑	1.5		1.5		

Product Folder Links: *SN74LV574A*

6.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN74LV574A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	60	100		50		MHz
			C_L = 50 pF	50	85		40		
t_{pd}	CLK	Q	C_L = 15 pF		9.6	16.6	1	20	ns
t_{en}	$\overline{OE}$	Q			9.2	16.1	1	19	
t_{dis}	$\overline{OE}$	Q			6.5	12.8	1	15	
t_{pd}	CLK	Q	C_L = 50 pF		11.6	19.6	1	23	
t_{en}	$\overline{OE}$	Q			10.9	19	1	22	
t_{dis}	$\overline{OE}$	Q			8.4	17.5	1	20	
$t_{sk(o)}$						2		2	

6.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN74LV574A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80	145		65		MHz
			C_L = 50 pF	50	120		45		
t_{pd}	CLK	Q	C_L = 15 pF		6.8	13.2	1	15.5	ns
t_{en}	$\overline{OE}$	Q			6.4	12.8	1	15	
t_{dis}	$\overline{OE}$	Q			4.8	13	1	15	
t_{pd}	CLK	Q	C_L = 50 pF		8.1	16.7	1	19	
t_{en}	$\overline{OE}$	Q			7.7	16.3	1	18.5	
t_{dis}	$\overline{OE}$	Q			6.1	15	1	17	
$t_{sk(o)}$						1.5		1.5	

6.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN74LV574A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	130	205		110		MHz
			C_L = 50 pF	85	175		75		
t_{pd}	CLK	Q	C_L = 15 pF		4.8	8.6	1	10	ns
t_{en}	$\overline{OE}$	Q			4.6	9	1	10.5	
t_{dis}	$\overline{OE}$	Q			3.5	9	1	10.5	
t_{pd}	CLK	Q	C_L = 50 pF		5.7	10.6	1	12	
t_{en}	$\overline{OE}$	Q			5.5	11	1	12.5	
t_{dis}	$\overline{OE}$	Q			4.1	10.1	1	11.5	
$t_{sk(o)}$						1		1	

6.12 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C[1]

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		– 0.6	– 0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C[1]

PARAMETER		MIN	TYP	MAX	UNIT
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1)   Characteristics are for surface-mount packages only.

6.13 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF f = 10 MHz	3.3 V	20.4	pF
				5 V	23.8	

6.14 Typical Characteristics

图 6-1. TPD vs V_{CC}

Product Folder Links: *SN74LV574A*
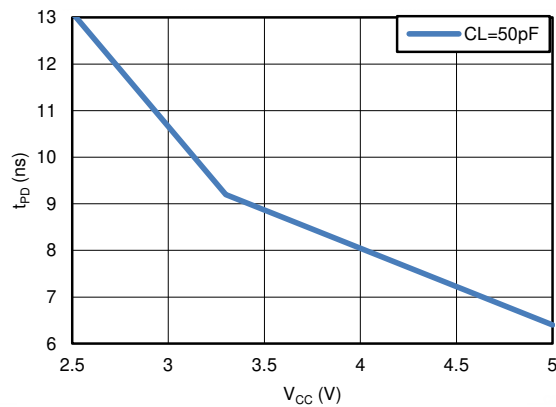
7 Parameter Measurement Information

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω , t_r ⩽ 3 ns,
   t_f ⩽ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

Product Folder Links: *SN74LV574A*

8 Detailed Description

8.1 Overview

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.
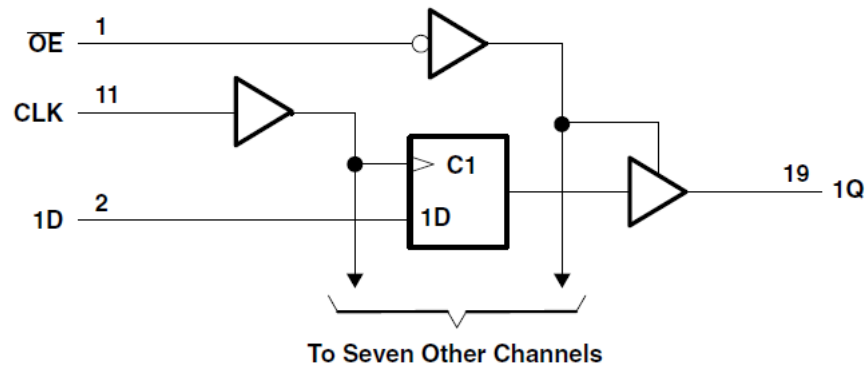
8.2 Functional Block Diagram

图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

8.3.3 Partial Power Down (I$_{off}$)

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I$_{off}$ specification in the *Electrical Characteristics* table.

8.3.4 Clamp Diode Structure

图 8-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION
Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
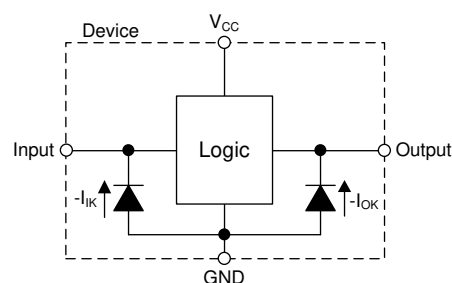
图 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 8-1. Function Table

INPUTS[1]			OUTPUT Q
$\overline{\text{OE}}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L, H, ↓	X	Q_0
H	X	X	Z

(1)   H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

Product Folder Links: *SN74LV574A*

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN74LV574A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are 5 V tolerant allowing for down translation to V_{CC}.

9.2 Typical Application

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV574A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

9.2.3 Application Curves
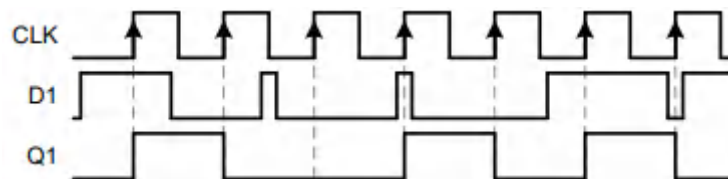
图 9-1. **Simplified Functional Diagram Showing Clock Operation**

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Recommended Operating Conditions table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1.0 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or VCC, whichever makes more sense for the logic function or is more convenient.
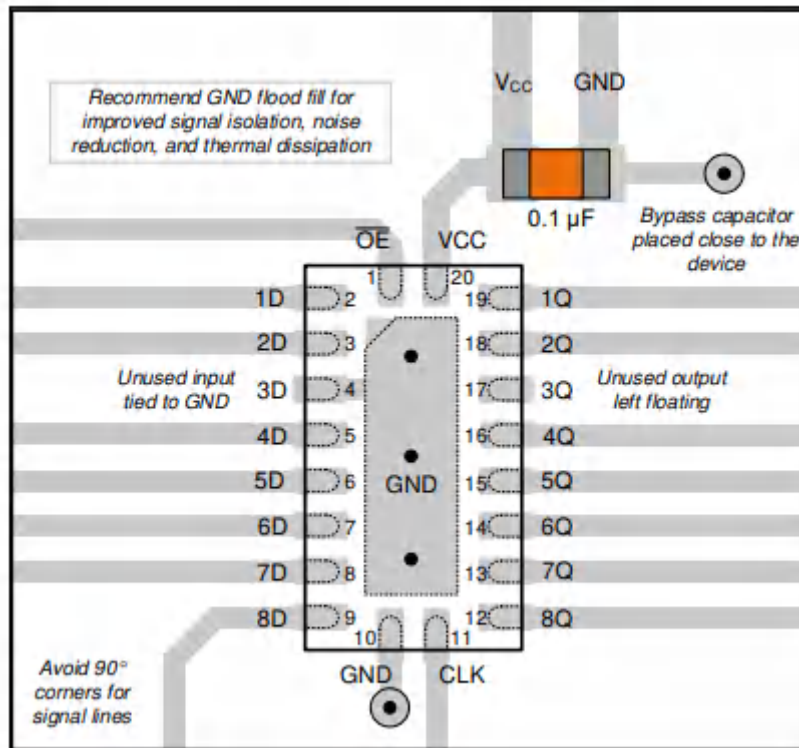
11.2 Layout Example

图 11-1. Layout Example for the SN74LV574A in TSSOP

Product Folder Links: *SN74LV574A*

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV574ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV574A	Samples
SN74LV574APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574APWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574APWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV574A	Samples
SN74LV574ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV574A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV574ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV574ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV574ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV574ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV574APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV574APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV574ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV574ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LV574ADGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74LV574ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV574ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV574APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV574APWT	TSSOP	PW	20	250	356.0	356.0	35.0
SN74LV574ARGYR	VQFN	RGY	20	3000	356.0	356.0	35.0

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
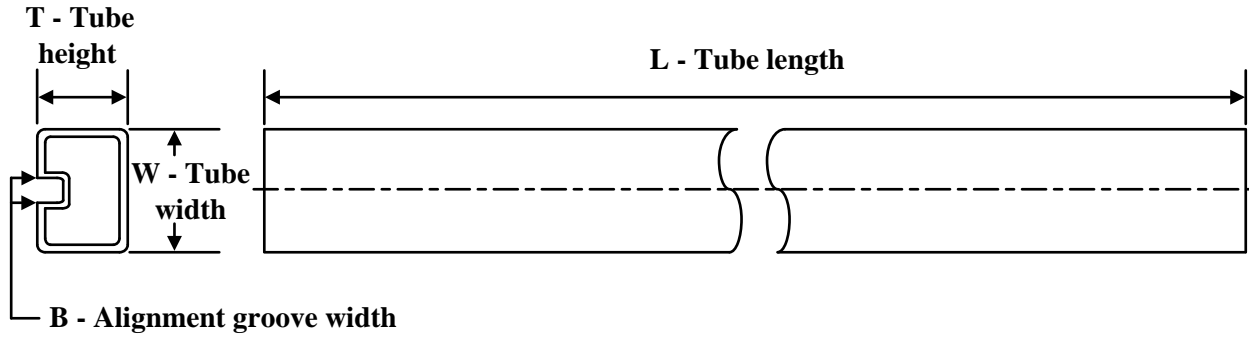
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV574ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LV574APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LV574APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

8.2 TYP
7.4

A

PIN 1 INDEX AREA

1

20

18X 0.65

7.5
6.9
NOTE 3

2X
5.85

10

11

20X 0.38
0.22

B

5.6
5.0
NOTE 4

⊕ 0.1 Ⓜ C A B

C

◠ 0.1 C

SEATING
PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0°-8°

0.95
0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

4214851/B   08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

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DB0020A

20X (1.85)

1

20X (0.45)

(R0.05) TYP

20

18X (0.65)

SYMM

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SYMM

20X (1.85)

1

20X (0.45)

(R0.05) TYP

20

SYMM

18X (0.65)

10

11

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN

0,40

$\frac{0,23}{0,13}$ ⊕ 0,07 Ⓜ

24   13

$\frac{4,50}{4,30}$ $\frac{6,60}{6,20}$

1   12

A

0,16 NOM

Gage Plane

0°−8°

0,25

$\frac{0,75}{0,50}$

1,20 MAX

$\frac{0,15}{0,05}$

Seating Plane

⌒ 0,08

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

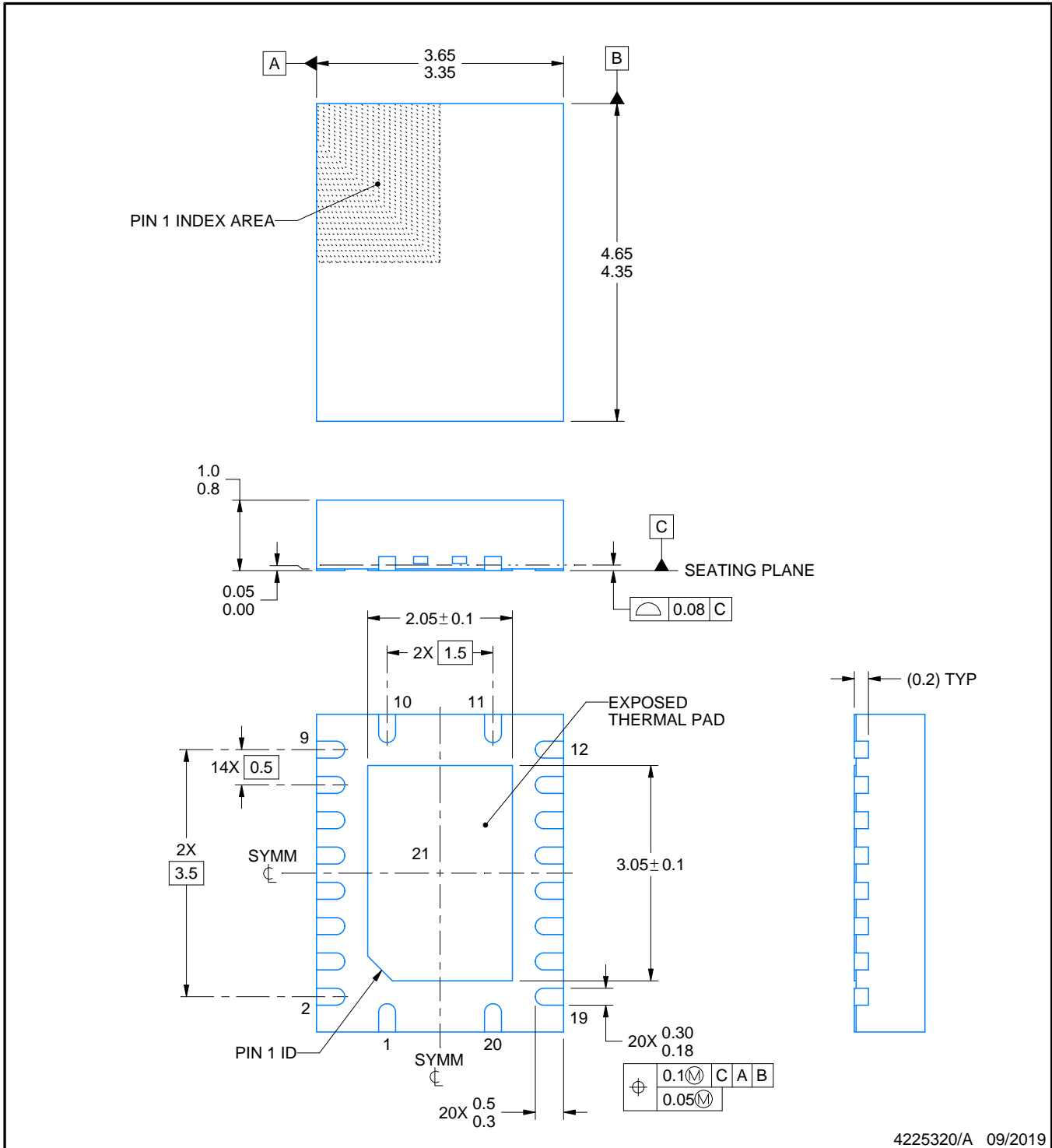**RGY 20**

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4225264/A

A

3.65
3.35

B

PIN 1 INDEX AREA

4.65
4.35

1.0
0.8

0.05
0.00

C

SEATING PLANE

⌒ | 0.08 | C

2.05 ± 0.1

2X 1.5

10   11

EXPOSED
THERMAL PAD

9

14X 0.5

12

2X
3.5

SYMM
₵

21

3.05 ± 0.1

2

PIN 1 ID   1   SYMM
₵   20

19

20X 0.30
0.18

⊕ | 0.1 Ⓜ | C | A | B
| 0.05 Ⓜ

20X 0.5
0.3

(0.2) TYP

4225320/A   09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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RGY0020A

(2.05)

SYMM

1   20

20X (0.6)

2

19

20X (0.24)

(1.275)

(4.3)

SYMM

21   (3.05)

14X (0.5)

9

(R0.05) TYP

(0.775)

12

(∅ 0.2) TYP
VIA

10   11

(0.75) TYP

(3.3)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

0.07 MAX
ALL AROUND

METAL

EXPOSED
METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

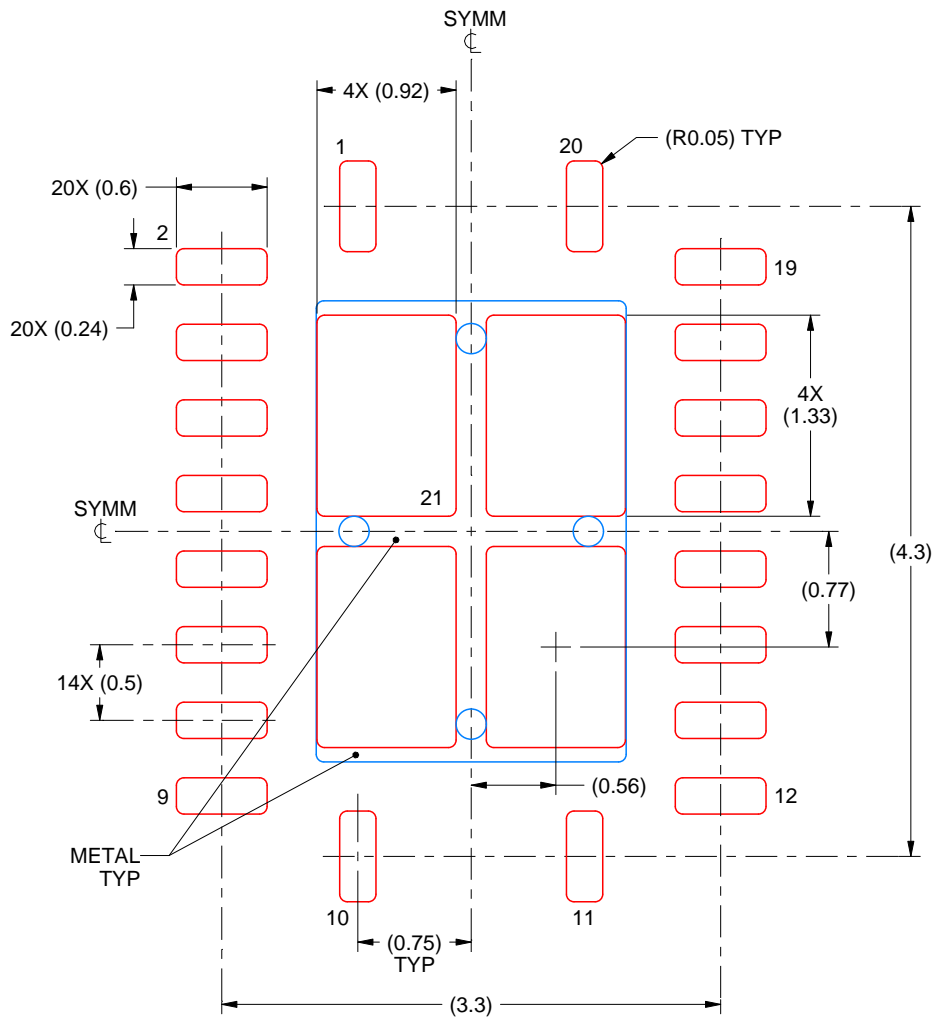**SOLDER MASK DETAILS**

4225320/A   09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RGY0020A

SYMM

4X (0.92)

1

20

(R0.05) TYP

20X (0.6)

2

19

20X (0.24)

4X
(1.33)

SYMM

21

(4.3)

(0.77)

14X (0.5)

9

12

(0.56)

METAL
TYP

10

11

(0.75)
TYP

(3.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A   09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

18X 0.65

20

6.6
6.4
NOTE 3

2X

5.85

10

11

20X 0.30
0.19

B

4.5
4.3
NOTE 4

⊕ 0.1Ⓜ C A B

C

SEATING
PLANE

⌒ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL

4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

SOLDER MASK
DEFINED

4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

(R0.05) TYP

1

20

20X (0.45)

18X (0.65)

SYMM

10

11

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R−PDSO−G20) PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

5,6

L1,55

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−5/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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