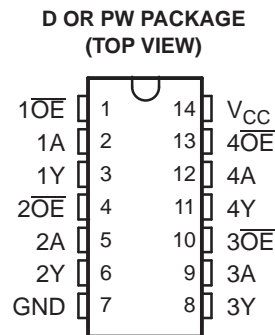


## QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

### FEATURES

- Qualified for Automotive Applications
- Operates From 1.65 V to 3.6 V
- Specified From  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.8 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



### DESCRIPTION/ORDERING INFORMATION

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

#### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	SN74LVC125AQDRQ1	LC125AQ
	TSSOP – PW	Reel of 2000	SN74LVC125AQPWRQ1	LC125AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

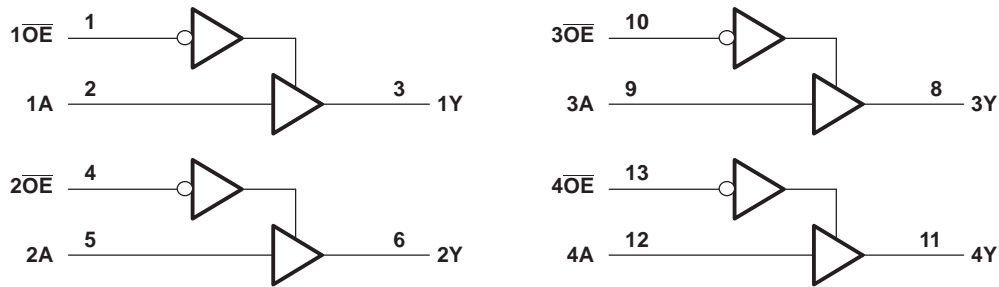
(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

#### FUNCTION TABLE (EACH BUFFER)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**LOGIC DIAGRAM (POSITIVE LOGIC)****Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage range	-0.5	6.5	V	
$V_I$	Input voltage range	-0.5	6.5	V	
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V	
$I_{IK}$	Input clamp current		-50	mA	
$I_{OK}$	Output clamp current		-50	mA	
$I_O$	Continuous output current		±50	mA	
	Continuous current through $V_{CC}$ or GND		±100	mA	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	D package	86	°C/W	
		PW package	113		
$T_{stg}$	Storage temperature range	-65	150	°C	
$P_{tot}$	Power dissipation <sup>(5)(6)</sup>	$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		500	mW

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) For the D package: above 70°C, the value of  $P_{tot}$  derates linearly with 8 mW/K.
- (6) For the PW package: above 60°C, the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

**Recommended Operating Conditions<sup>(1)</sup>**

		$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT	
		MIN	MAX	MIN	MAX		
$V_{CC}$	Supply voltage	Operating	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.7		1.7		
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	2		2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	0.7		0.7		
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	0.8		0.8		
$V_I$	Input voltage	0	5.5	0	5.5	V	
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V	
$I_{OH}$	High-level output current	$V_{CC} = 1.65\text{ V}$	-4		-4		mA
		$V_{CC} = 2.3\text{ V}$	-8		-8		
		$V_{CC} = 2.7\text{ V}$	-12		-12		
		$V_{CC} = 3\text{ V}$	-24		-24		
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$	4		4		mA
		$V_{CC} = 2.3\text{ V}$	8		8		
		$V_{CC} = 2.7\text{ V}$	12		12		
		$V_{CC} = 3\text{ V}$	24		24		
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V	

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$	1.65 V to 3.6 V	$V_{CC} - 0.2$		$V_{CC} - 0.2$		V	
	$I_{OH} = -4\text{ mA}$	1.65 V	1.29		1.1			
	$I_{OH} = -8\text{ mA}$	2.3 V	1.9		1.75			
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2		2.1			
	$I_{OH} = -24\text{ mA}$	3 V	2.4		2.35			
	$I_{OH} = -24\text{ mA}$	3 V	2.3		2.1			
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$	1.65 V to 3.6 V	0.1		0.2		V	
	$I_{OL} = 4\text{ mA}$	1.65 V	0.24		0.45			
	$I_{OL} = 8\text{ mA}$	2.3 V	0.3		0.7			
	$I_{OL} = 12\text{ mA}$	2.7 V	0.4		0.5			
	$I_{OL} = 24\text{ mA}$	3 V	0.55		0.7			
$I_I$	$V_I = 5.5\text{ V or GND}$	3.6 V	$\pm 1$		$\pm 10$		$\mu\text{A}$	
$I_{OZ}$	$V_O = V_{CC}\text{ or GND}$	3.6 V	$\pm 1$		$\pm 10$		$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}\text{ or GND, } I_O = 0$	3.6 V	1		20		$\mu\text{A}$	
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$	2.7 V to 3.6 V	500		500		$\mu\text{A}$	
$C_i$	$V_I = V_{CC}\text{ or GND}$	3.3 V	5				pF	

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

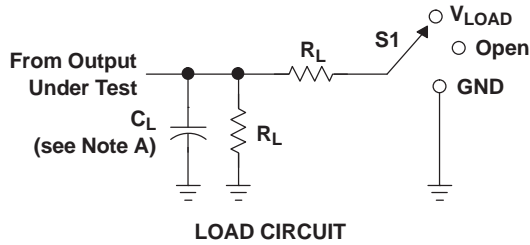
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2.7 V	1	3	5.3	1	7	ns
			3.3 V ± 0.3 V	1	2.5	4.6	1	6	
t <sub>en</sub>	$\overline{OE}$	Y	2.7 V	1	3.3	6.4	1	8.5	ns
			3.3 V ± 0.3 V	1	2.4	5.2	1	7	
t <sub>dis</sub>	$\overline{OE}$	Y	2.7 V	1	2.5	4.8	1	6.5	ns
			3.3 V ± 0.3 V	1	2.4	4.4	1	6	
t <sub>sk(o)</sub>			3.3 V ± 0.3 V					1.5	ns

## Operating Characteristics

T<sub>A</sub> = 25°C

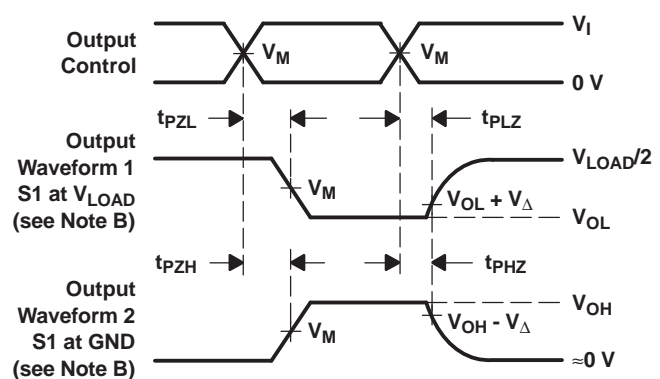
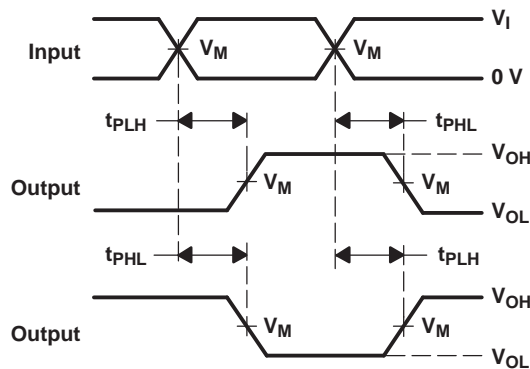
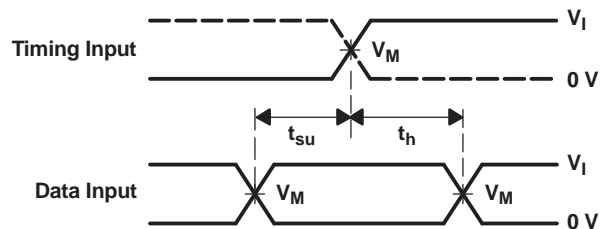
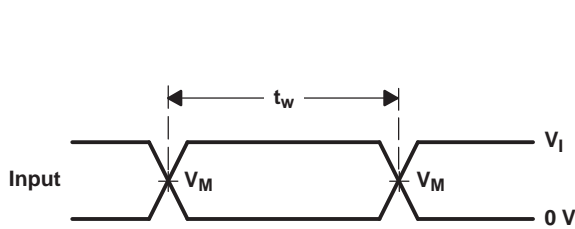
PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per gate	f = 10 MHz	3.3 V	15	pF

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
2.7 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVC125AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ	<a href="#">Samples</a>
SN74LVC125AQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ	<a href="#">Samples</a>
SN74LVC125AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC125A-Q1 :**

- Catalog: [SN74LVC125A](#)
- Enhanced Product: [SN74LVC125A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

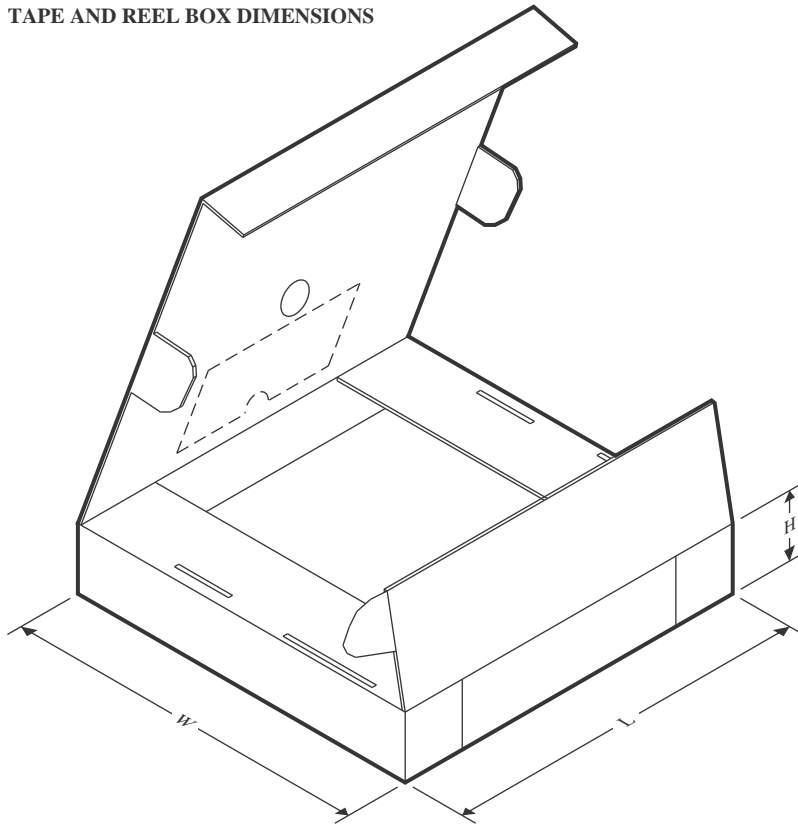
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC125AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



## TAPE AND REEL BOX DIMENSIONS





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC125AQPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC125AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

D (R-PDSO-G14)

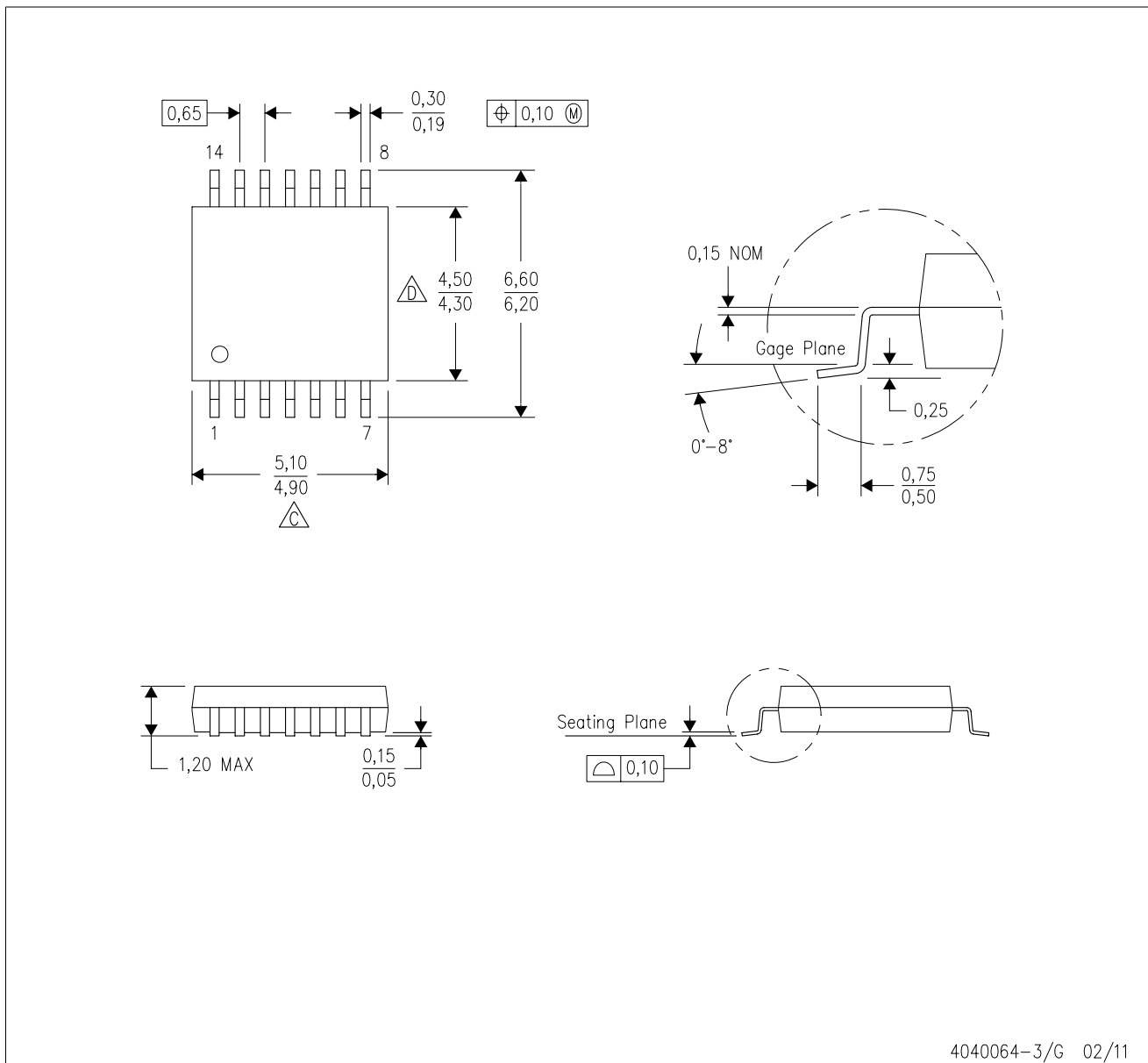
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Buffers & Line Drivers](#) category:*

*Click to view products by [Texas Instruments](#) manufacturer:*

Other Similar products are found below :

[LXV200-024SW](#) [74AUP2G34FW3-7](#) [HEF4043BP](#) [NL17SG125DFT2G](#) [NLU1GT126CMUTCG](#) [CD4041UBE](#) [54FCT240CTDB](#)  
[74HCT540N](#) [DS14C88N](#) [070519XB](#) [NL17SZ07P5T5G](#) [74LVC2G17FW4-7](#) [CD4502BE](#) [5962-8982101PA](#) [61446R00](#) [NL17SH17P5T5G](#)  
[NLV37WZ17USG](#) [74HCT126T14-13](#) [74VHC9126FT\(BJ\)](#) [RHRXH162244K1](#) [74AUP1G34FW5-7](#) [74AUP1G07FW5-7](#) [74LVC1G126FW4-7](#)  
[74LVC2G126RA3-7](#) [74LVCE1G125FZ4-7](#) [54FCT240TLB](#) [NLX3G16DMUTCG](#) [NLX2G06AMUTCG](#) [LE87100NQCT](#) [LE87285NQC](#)  
[LE87290YQC](#) [LE87290YQCT](#) [74AUP1G125FW5-7](#) [NLU2G16CMUTCG](#) [MC74LCX244MN2TWG](#) [NL17SG17P5T5G](#)  
[NLV74HC125ADR2G](#) [NLVHCT245ADTR2G](#) [NLVVHC1G126DFT2G](#) [EL5623IRZ](#) [ISL15102AIRZ-T13](#) [ISL1539IRZ-T13](#)  
[MC100EP17MNG](#) [MC74HCT365ADR2G](#) [MC74LCX244ADTR2G](#) [NL27WZ126US](#) [NL37WZ16US](#) [NLU1G07MUTCG](#) [NLU2G07MUTCG](#)  
[NLX3G17BMX1TCG](#)