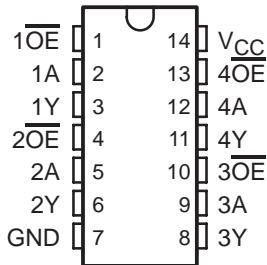


# SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

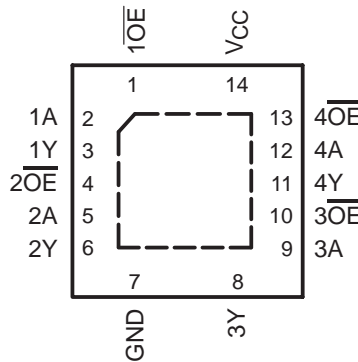
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

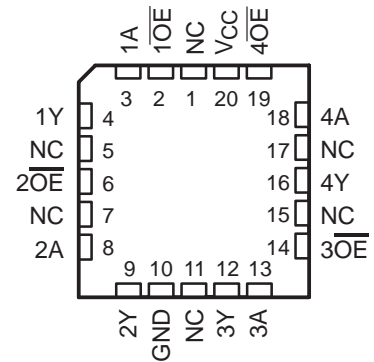
SN54LVTH125 . . . J OR W PACKAGE  
SN74LVTH125 . . . D, DB, DGV, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LVTH125 . . . RGY PACKAGE  
(TOP VIEW)



SN54LVTH125 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These bus buffers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH125 devices feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable ( $\overline{OE}$ ) input is high.

## ORDERING INFORMATION

| $T_A$          | PACKAGE†      |                 | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|-----------------|-----------------------|------------------|
| –40°C to 85°C  | QFN – RGY     | Tape and reel   | SN74LVTH125RGYR       | LXH125           |
|                | SOIC – D      | Tube            | SN74LVTH125D          | LVTH125          |
|                |               | Tape and reel   | SN74LVTH125DR         |                  |
|                | SOP – NS      | Tape and reel   | SN74LVTH125NSR        | LVTH125          |
|                | SSOP – DB     | Tape and reel   | SN74LVTH125DBR        | LXH125           |
|                | TSSOP – PW    | Tube            | SN74LVTH125PW         | LXH125           |
|                |               | Tape and reel   | SN74LVTH125PWR        |                  |
| TVSOP – DGV    | Tape and reel | SN74LVTH125DGVR | LXH125                |                  |
| –55°C to 125°C | CDIP – J      | Tube            | SNJ54LVTH125J         | SNJ54LVTH125J    |
|                | CFP – W       | Tube            | SNJ54LVTH125W         | SNJ54LVTH125W    |
|                | LCCC – FK     | Tube            | SNJ54LVTH125FK        | SNJ54LVTH125FK   |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
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# SN54LVTH125, SN74LVTH125

## 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS703I – AUGUST 1997 – REVISED OCTOBER 2003

### description/ordering information (continued)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

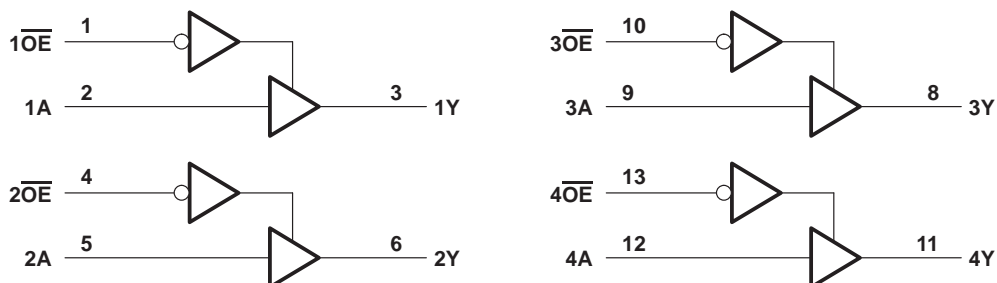
When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE  
(each buffer)

| INPUTS          |   | OUTPUT |
|-----------------|---|--------|
| $\overline{OE}$ | A | Y      |
| L               | H | H      |
| L               | L | L      |
| H               | X | Z      |

### logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

# SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS703I – AUGUST 1997 – REVISED OCTOBER 2003

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |                            |
|---|----------------------------|
| Supply voltage range, $V_{CC}$ .....  | –0.5 V to 4.6 V            |
| Input voltage range, $V_I$ (see Note 1) .....   | –0.5 V to 7 V              |
| Voltage range applied to any output in the high-impedance<br>or power-off state, $V_O$ (see Note 1) ..... | –0.5 V to 7 V              |
| Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....                           | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, $I_O$ : SN54LVTH125 .....                                       | 96 mA                      |
| SN74LVTH125 .....   | 128 mA                     |
| Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH125 .....                          | 48 mA                      |
| SN74LVTH125 .....   | 64 mA                      |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....   | –50 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....  | –50 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): D package .....                                    | 86°C/W                     |
| (see Note 3): DB package .....  | 96°C/W                     |
| (see Note 3): DGV package .....   | 127°C/W                    |
| (see Note 3): NS package .....  | 76°C/W                     |
| (see Note 3): PW package .....  | 113°C/W                    |
| (see Note 4): RGY package .....   | 47°C/W                     |
| Storage temperature range, $T_{stg}$ .....  | –65°C to 150°C             |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.  
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

## recommended operating conditions (see Note 5)

|                          |                                    | SN54LVTH125     |     | SN74LVTH125 |     | UNIT |
|--------------------------|------------------------------------|-----------------|-----|-------------|-----|------|
|                          |                                    | MIN             | MAX | MIN         | MAX |      |
| $V_{CC}$                 | Supply voltage                     | 2.7             | 3.6 | 2.7         | 3.6 | V    |
| $V_{IH}$                 | High-level input voltage           | 2               |     | 2           |     | V    |
| $V_{IL}$                 | Low-level input voltage            |                 | 0.8 |             | 0.8 | V    |
| $V_I$                    | Input voltage                      |                 | 5.5 |             | 5.5 | V    |
| $I_{OH}$                 | High-level output current          |                 | –24 |             | –32 | mA   |
| $I_{OL}$                 | Low-level output current           |                 | 48  |             | 64  | mA   |
| $\Delta t/\Delta v$      | Input transition rise or fall rate | Outputs enabled |     | 10          | 10  | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate                 | 200             |     | 200         |     | μs/V |
| $T_A$                    | Operating free-air temperature     | –55             | 125 | –40         | 85  | °C   |

NOTE 5: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVTH125, SN74LVTH125

## 3.3-V ABT QUADRUPLE BUS BUFFERS

### WITH 3-STATE OUTPUTS

SCBS7031 – AUGUST 1997 – REVISED OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS  |  | SN54LVTH125             |                |      | SN74LVTH125  |      |      | UNIT          |               |
|--------------------------|--|--|-------------------------|----------------|------|--------------|------|------|---------------|---------------|
|                          |  |  | MIN                     | TYP†           | MAX  | MIN          | TYP† | MAX  |               |               |
| $V_{IK}$                 | $V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$  |  | -1.2                    |                |      | -1.2         |      |      | V             |               |
| $V_{OH}$                 | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$   |  | $V_{CC}-0.2$            |                |      | $V_{CC}-0.2$ |      |      | V             |               |
|                          | $V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$  |  | 2.4                     |                |      | 2.4          |      |      |               |               |
|                          | $V_{CC} = 3\text{ V}$  | $I_{OH} = -24\text{ mA}$   | 2                       |                |      |              |      |      |               |               |
| $I_{OH} = -32\text{ mA}$ |  |  |                         |                | 2    |              |      |      |               |               |
| $V_{OL}$                 | $V_{CC} = 2.7\text{ V}$  | $I_{OL} = 100\text{ }\mu\text{A}$                                  | 0.2                     |                |      | 0.2          |      |      | V             |               |
|                          |  | $I_{OL} = 24\text{ mA}$  | 0.5                     |                |      | 0.5          |      |      |               |               |
|                          | $V_{CC} = 3\text{ V}$  | $I_{OL} = 16\text{ mA}$  | 0.4                     |                |      | 0.4          |      |      |               |               |
|                          |  | $I_{OL} = 32\text{ mA}$  | 0.5                     |                |      | 0.5          |      |      |               |               |
|                          |  | $I_{OL} = 48\text{ mA}$  | 0.55                    |                |      |              |      |      |               |               |
|                          |  | $I_{OL} = 64\text{ mA}$  |                         |                |      | 0.55         |      |      |               |               |
| $I_I$                    | $V_{CC} = 0\text{ or }3.6\text{ V}$ , $V_I = 5.5\text{ V}$   |  | 10                      |                |      | 10           |      |      | $\mu\text{A}$ |               |
|                          | Control inputs   | $V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$             | $\pm 1$                 |                |      | $\pm 1$      |      |      |               |               |
|                          |  | Data inputs  | $V_{CC} = 3.6\text{ V}$ | $V_I = V_{CC}$ | 1    |              |      | 1    |               |               |
| $V_I = 0$                | -5   |  |                         | -5             |      |              |      |      |               |               |
| $I_{off}$                | $V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$  |  |                         |                |      | $\pm 100$    |      |      | $\mu\text{A}$ |               |
| $I_I(\text{hold})$       | Data inputs  | $V_{CC} = 3\text{ V}$  | $V_I = 0.8\text{ V}$    | 75             |      |              | 75   |      |               | $\mu\text{A}$ |
|                          |  |  | $V_I = 2\text{ V}$      | -75            |      |              | -75  |      |               |               |
|                          |  | $V_{CC} = 3.6\text{ V}\ddagger$ , $V_I = 0\text{ to }3.6\text{ V}$ |                         |                |      | $\pm 500$    |      |      |               |               |
| $I_{OZH}$                | $V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$   |  | 5                       |                |      | 5            |      |      | $\mu\text{A}$ |               |
| $I_{OZL}$                | $V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$   |  | -5                      |                |      | -5           |      |      | $\mu\text{A}$ |               |
| $I_{OZPU}$               | $V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ ,<br>$OE = \text{don't care}$                   |  | $\pm 50^*$              |                |      | $\pm 50$     |      |      | $\mu\text{A}$ |               |
| $I_{OZPD}$               | $V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ ,<br>$OE = \text{don't care}$                          |  | $\pm 50^*$              |                |      | $\pm 50$     |      |      | $\mu\text{A}$ |               |
| $I_{CC}$                 | $V_{CC} = 3.6\text{ V}$ ,<br>$I_O = 0$ ,<br>$V_I = V_{CC}\text{ or GND}$   | Outputs high   | 0.12                    | 0.19           | 0.12 |              |      | 0.19 | mA            |               |
|                          |  | Outputs low  | 4.5                     | 7              | 4.5  |              |      | 7    |               |               |
|                          |  | Outputs disabled   | 0.12                    | 0.19           | 0.12 |              |      | 0.19 |               |               |
| $\Delta I_{CC}\S$        | $V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ ,<br>Other inputs at $V_{CC}\text{ or GND}$ |  | 0.3                     |                |      | 0.2          |      |      | mA            |               |
| $C_i$                    | $V_I = 3\text{ V or }0$  |  | 4                       |                |      | 4            |      |      | pF            |               |
| $C_o$                    | $V_O = 3\text{ V or }0$  |  | 6.5                     |                |      | 6.5          |      |      | pF            |               |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

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# SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | SN54LVTH125                                |     |                          |     | SN74LVTH125                                |      |     |                          | UNIT |     |
|-----------|-----------------|-------------|--|-----|--------------------------|-----|--|------|-----|--------------------------|------|-----|
|           |                 |             | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ |     | $V_{CC} = 2.7 \text{ V}$ |     | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ |      |     | $V_{CC} = 2.7 \text{ V}$ |      |     |
|           |                 |             | MIN  | MAX | MIN                      | MAX | MIN  | TYP† | MAX | MIN                      |      | MAX |
| $t_{PLH}$ | A               | Y           | 1  | 4.2 |                          | 4.7 | 1  | 2    | 3.5 |                          | 4.5  | ns  |
| $t_{PHL}$ |                 |             | 1  | 4.1 |                          | 5.1 | 1  | 2.1  | 3.9 |                          | 4.9  |     |
| $t_{PZH}$ | $\overline{OE}$ | Y           | 1  | 4.9 |                          | 5.6 | 1  | 2    | 4   |                          | 5.5  | ns  |
| $t_{PZL}$ |                 |             | 1.1  | 4.9 |                          | 5.6 | 1.1  | 2.1  | 4   |                          | 5.4  |     |
| $t_{PHZ}$ | $\overline{OE}$ | Y           | 1.5  | 5.3 |                          | 5.9 | 1.5  | 2.3  | 4.5 |                          | 5.7  | ns  |
| $t_{PLZ}$ |                 |             | 1.3  | 4.7 |                          | 4.2 | 1.3  | 2.8  | 4.5 |                          | 4    |     |

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

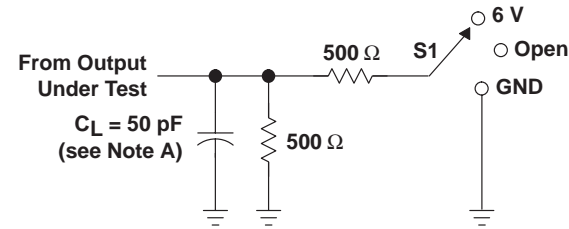
# SN54LVTH125, SN74LVTH125

## 3.3-V ABT QUADRUPLE BUS BUFFERS

### WITH 3-STATE OUTPUTS

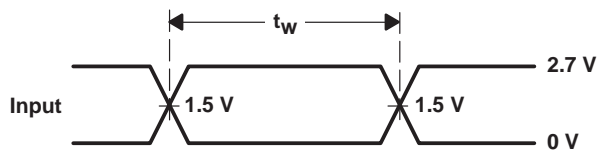
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#### PARAMETER MEASUREMENT INFORMATION

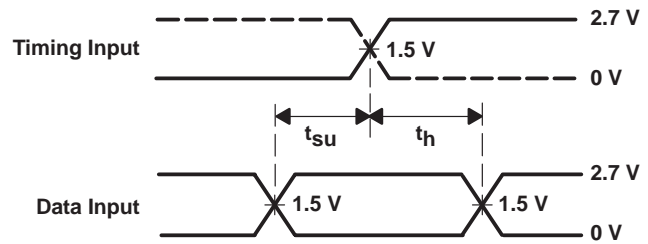


LOAD CIRCUIT

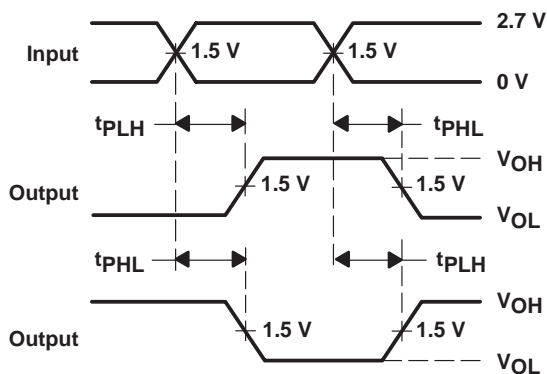
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |



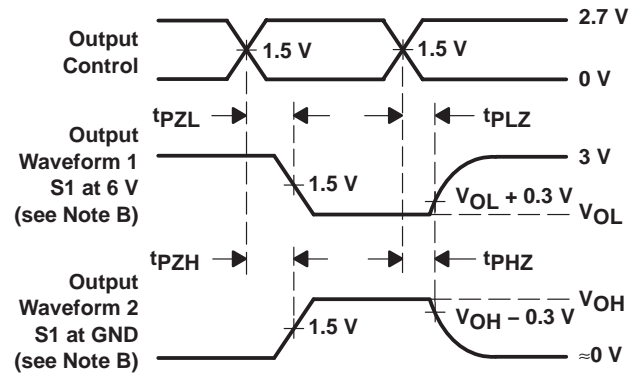
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVTH125D     | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH125                 | <a href="#">Samples</a> |
| SN74LVTH125DBR   | ACTIVE        | SSOP         | DB              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH125                  | <a href="#">Samples</a> |
| SN74LVTH125DBRE4 | ACTIVE        | SSOP         | DB              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH125                  | <a href="#">Samples</a> |
| SN74LVTH125DGVR  | ACTIVE        | TVSOP        | DGV             | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH125                  | <a href="#">Samples</a> |
| SN74LVTH125DR    | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH125                 | <a href="#">Samples</a> |
| SN74LVTH125DRG4  | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH125                 | <a href="#">Samples</a> |
| SN74LVTH125NSR   | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH125                 | <a href="#">Samples</a> |
| SN74LVTH125NSRE4 | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LVTH125                 | <a href="#">Samples</a> |
| SN74LVTH125PW    | ACTIVE        | TSSOP        | PW              | 14   | 90          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH125                  | <a href="#">Samples</a> |
| SN74LVTH125PWE4  | ACTIVE        | TSSOP        | PW              | 14   | 90          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH125                  | <a href="#">Samples</a> |
| SN74LVTH125PWG4  | ACTIVE        | TSSOP        | PW              | 14   | 90          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH125                  | <a href="#">Samples</a> |
| SN74LVTH125PWR   | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH125                  | <a href="#">Samples</a> |
| SN74LVTH125PWRG4 | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LXH125                  | <a href="#">Samples</a> |
| SN74LVTH125RGYR  | ACTIVE        | VQFN         | RGY             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | LXH125                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVTH125 :**

- Enhanced Product : [SN74LVTH125-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH125DBR  | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74LVTH125DGVR | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVTH125DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVTH125DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVTH125NSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVTH125PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVTH125RGYR | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH125DBR  | SSOP         | DB              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVTH125DGVR | TVSOP        | DGV             | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVTH125DR   | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| SN74LVTH125DR   | SOIC         | D               | 14   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74LVTH125NSR  | SO           | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVTH125PWR  | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVTH125RGYR | VQFN         | RGY             | 14   | 3000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVTH125D    | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LVTH125PW   | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVTH125PWE4 | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVTH125PWG4 | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

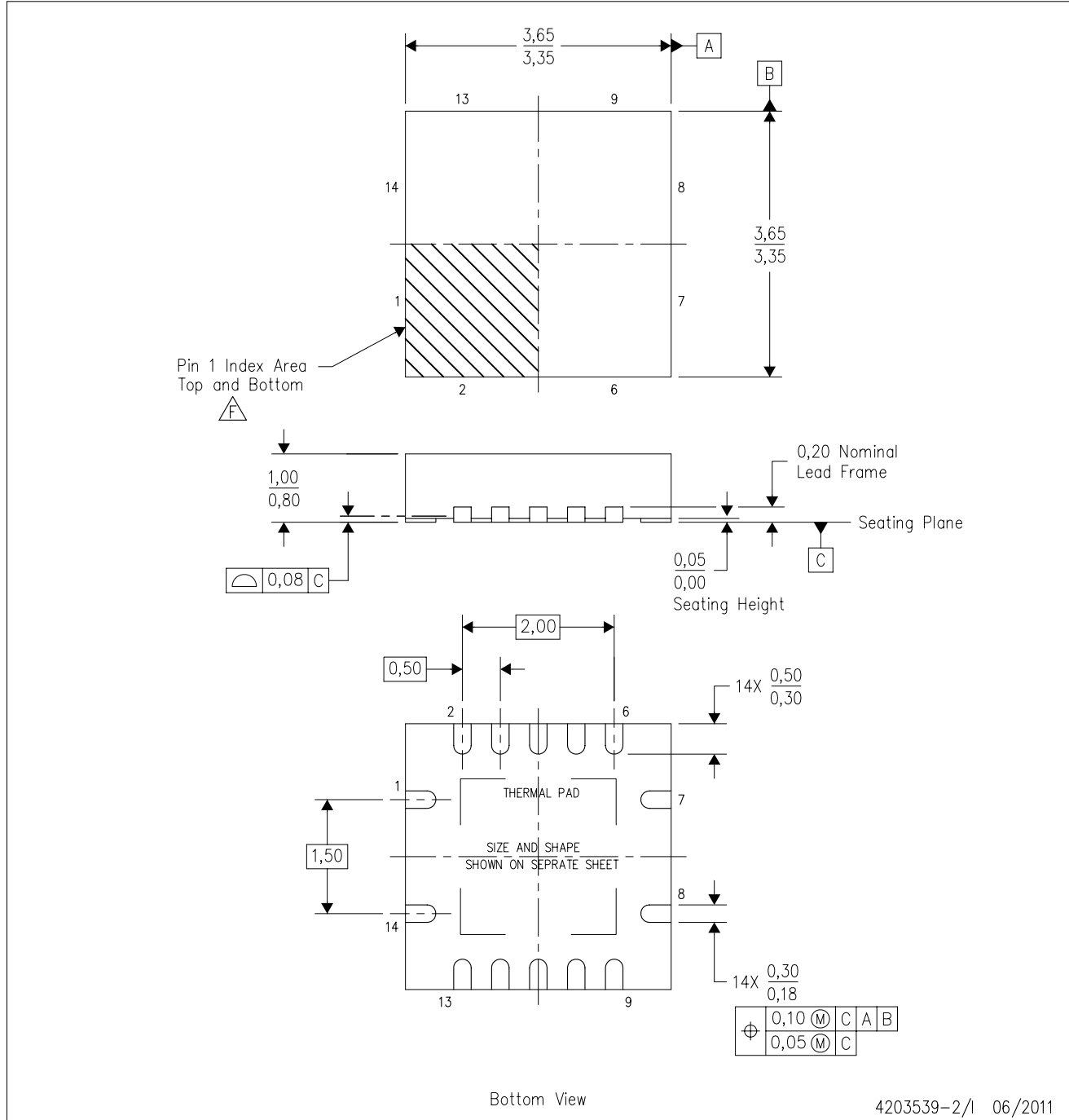
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - △ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

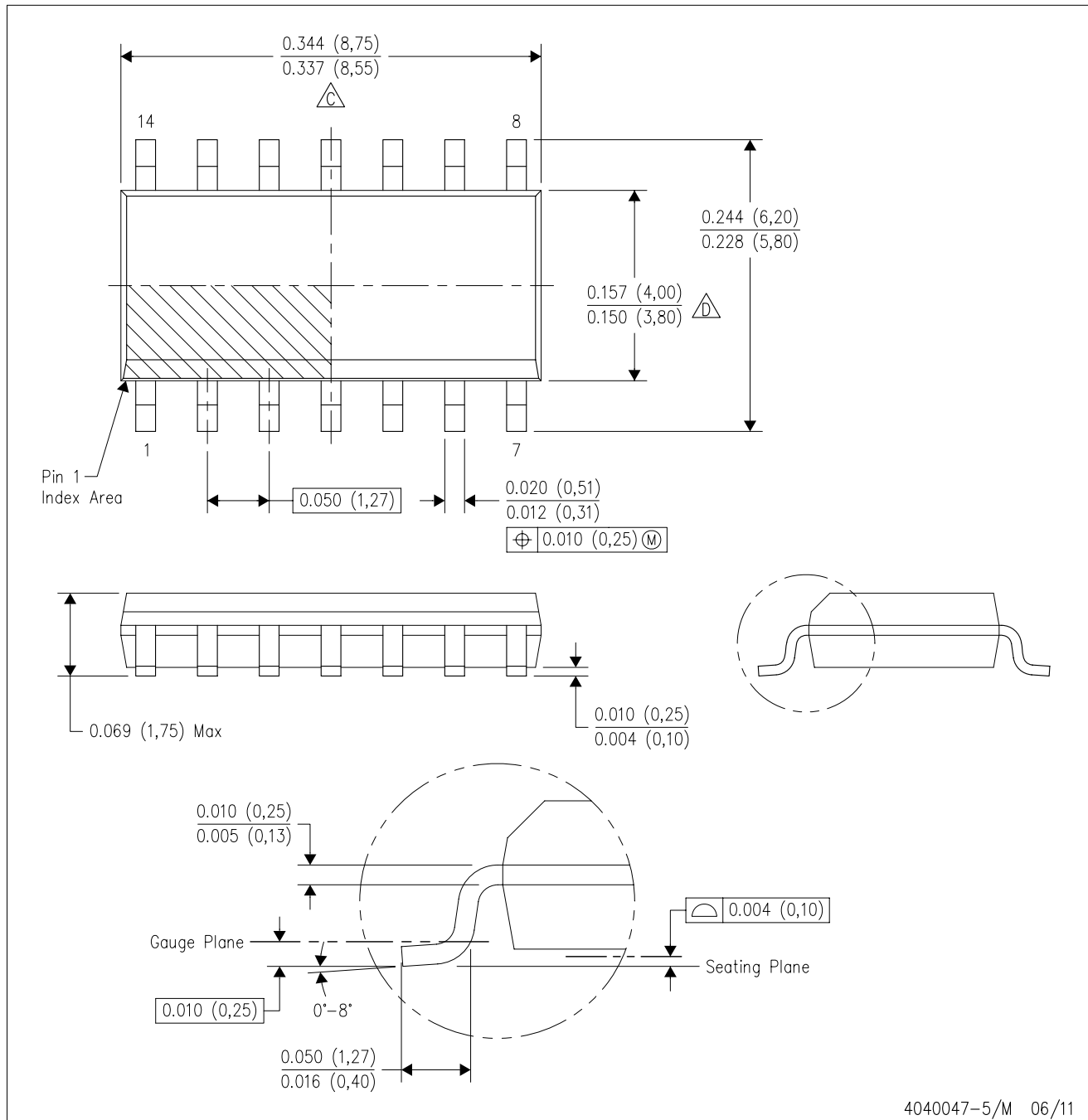
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

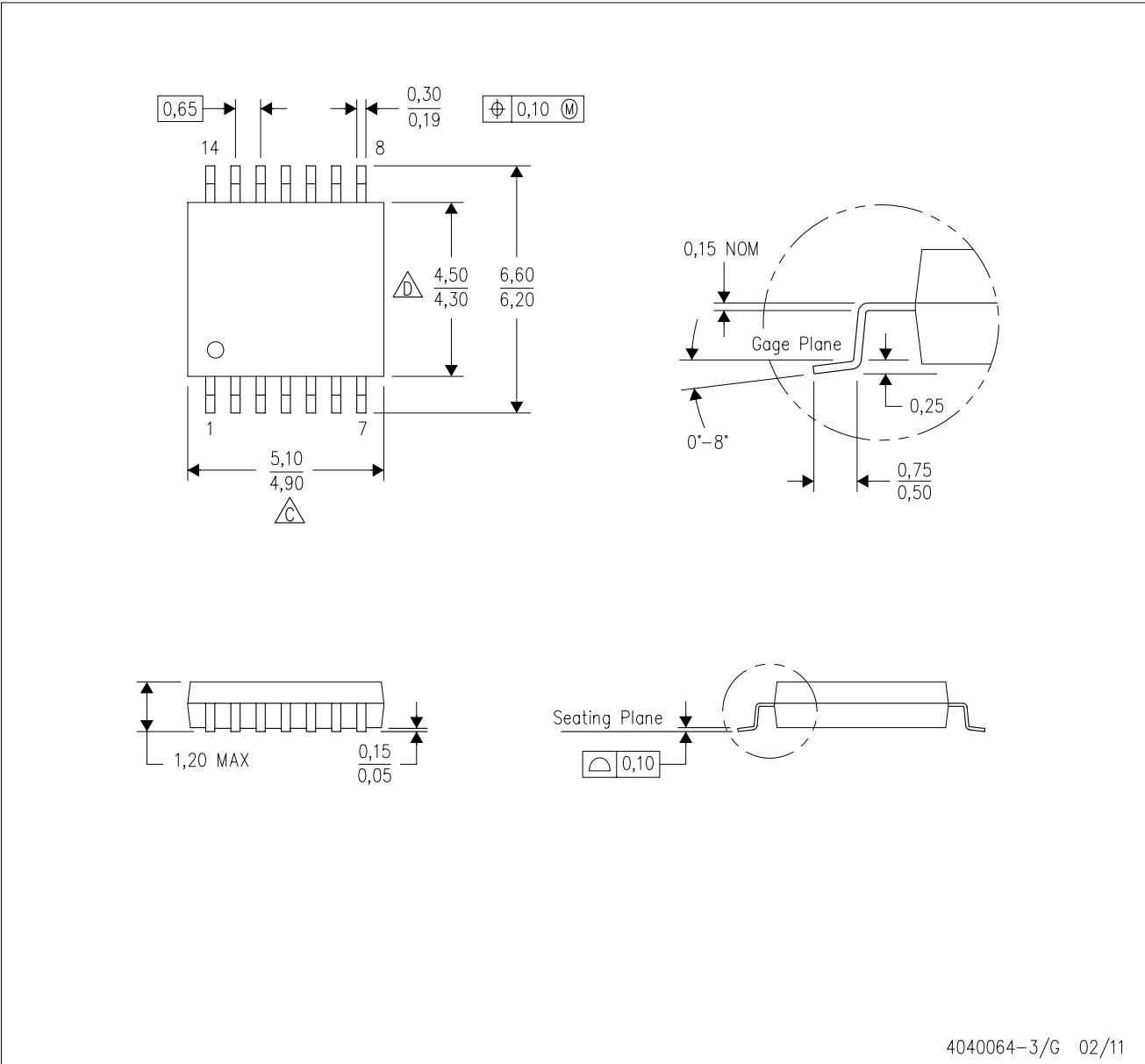
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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