

SN54LVTH2245, SN74LVTH2245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS707E – SEPTEMBER 1997 – REVISED OCTOBER 2003

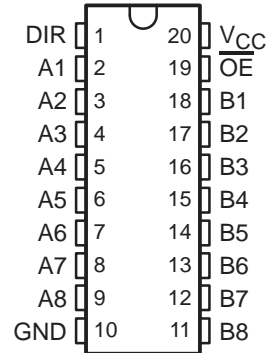
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- B-Port Outputs Have Equivalent 22- Ω Series Resistors, So No External Resistors Are Required
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

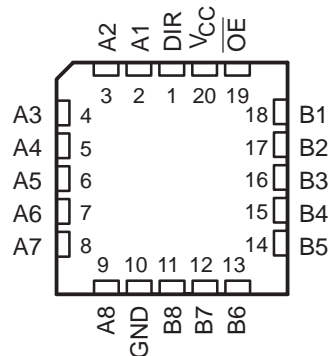
These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so the buses are effectively isolated.

SN54LVTH2245 . . . J OR W PACKAGE
SN74LVTH2245 . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVTH2245 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------|---------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – DW | Tube | SN74LVTH2245DW | LVTH2245 |
| | | Tape and reel | SN74LVTH2245DWR | |
| | SOP – NS | Tape and reel | SN74LVTH2245NSR | LVTH2245 |
| | SSOP – DB | Tape and reel | SN74LVTH2245DBR | LK245 |
| | TSSOP – PW | Tube | SN74LVTH2245PW | LK245 |
| | | Tape and reel | SN74LVTH2245PWR | |
| | TVSOP – DGV | Tape and reel | SN74LVTH2245DGVR | LK245 |
| –55°C to 125°C | CDIP – J | Tube | SNJ54LVTH2245J | SNJ54LVTH2245J |
| | CFP – W | Tube | SNJ54LVTH2245W | SNJ54LVTH2245W |
| | LCCC – FK | Tube | SNJ54LVTH2245FK | SNJ54LVTH2245FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54LVTH2245, SN74LVTH2245

3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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description/ordering information (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

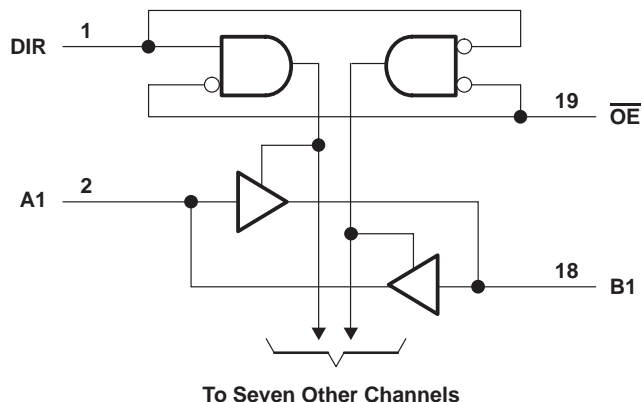
When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

logic diagram (positive logic)



SN54LVTH2245, SN74LVTH2245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O : SN54LVTH2245 (A port) | 96 mA |
| SN74LVTH2245 (A port) | 128 mA |
| B port | 30 mA |
| Current into any output in the high state, I_O (see Note 2): SN54LVTH2245 (A port) | 48 mA |
| SN74LVTH2245 (A port) | 64 mA |
| B port | 30 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DB package | 70°C/W |
| DGV package | 92°C/W |
| DW package | 58°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

| | | SN54LVTH2245 | | SN74LVTH2245 | | UNIT |
|--------------------------|------------------------------------|--------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | | 5.5 | | 5.5 | V |
| I_{OH} | High-level output current | A port | –24 | | –32 | mA |
| | | B port | | –12 | | |
| I_{OL} | Low-level output current | A port | | 48 | | mA |
| | | B port | | 12 | | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | 200 | | μs/V |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH2245, SN74LVTH2245

3.3-V ABT OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH2245 | | SN74LVTH2245 | | UNIT | |
|--|--|--|--------------------------|----------------------------------|----------------------|----------------------|----------|------|------|
| | | | | MIN | TYP† | MAX | MIN | | TYP† |
| V _{IK} | | V _{CC} = 2.7 V, I _I = -18 mA | | -1.2 | | -1.2 | | V | |
| V _{OH} | A port | V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA | | V _{CC} -0.2 | | V _{CC} -0.2 | | V | |
| | | V _{CC} = 2.7 V, I _{OH} = -8 mA | | 2.4 | | 2.4 | | | |
| | | V _{CC} = 3 V | | 2 | | 2 | | | |
| | | | I _{OH} = -24 mA | | | | | | |
| | | I _{OH} = -32 mA | | | | | | | |
| B port | V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA | | V _{CC} -0.2 | | V _{CC} -0.2 | | | | |
| | V _{CC} = 3 V, I _{OH} = -12 mA | | 2 | | 2 | | | | |
| V _{OL} | A port | V _{CC} = 2.7 V | | I _{OL} = 100 μA | | 0.2 | | 0.2 | |
| | | | | I _{OL} = 24 mA | | 0.5 | | 0.5 | |
| | | V _{CC} = 3 V | | I _{OL} = 16 mA | | 0.4 | | 0.4 | |
| | | | | I _{OL} = 32 mA | | 0.5 | | 0.5 | |
| | | | | I _{OL} = 48 mA | | 0.55 | | | |
| | | | I _{OL} = 64 mA | | | | 0.55 | | |
| | B port | V _{CC} = 2.7 V to 3.6 V, I _{OL} = 100 μA | | | | 0.2 | | 0.2 | |
| V _{CC} = 3 V, I _{OL} = 12 mA | | | | 0.8 | | 0.8 | | | |
| I _I | Control inputs | V _{CC} = 3.6 V, V _I = V _{CC} or GND | | ±1 | | ±1 | | μA | |
| | | V _{CC} = 0 or 3.6 V, V _I = 5.5 V | | 10 | | 10 | | | |
| | A or B ports‡ | V _{CC} = 3.6 V | | V _I = 5.5 V | | 20 | | | 20 |
| | | | | V _I = V _{CC} | | 1 | | | 1 |
| | | | | V _I = 0 | | -5 | | -5 | |
| I _{off} | | V _{CC} = 0, V _I or V _O = 0 to 4.5 V | | | | ±100 | | μA | |
| I _I (hold) | A or B ports | V _{CC} = 3 V | | V _I = 0.8 V | | 75 | | μA | |
| | | | | V _I = 2 V | | -75 | | | |
| | | V _{CC} = 3.6 V§, V _I = 0 to 3.6 V | | | | 500 | | | -750 |
| I _{OZPU} | | V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care | | ±100* | | ±100 | | μA | |
| I _{OZPD} | | V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care | | ±100* | | ±100 | | μA | |
| I _{CC} | V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND | | Outputs high | | 0.19 | | 0.1 0.19 | | mA |
| | | | Outputs low | | 5 | | 3 5 | | |
| | | | Outputs disabled | | 0.19 | | 0.1 0.19 | | |
| ΔI _{CC} ¶ | | V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | | 0.2 | | 0.2 | | mA | |
| C _i | | V _I = 3 V or 0 | | 4 | | 4 | | pF | |
| C _{io} | | V _O = 3 V or 0 | | 9 | | 9 | | pF | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Unused terminals are at V_{CC} or GND.

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

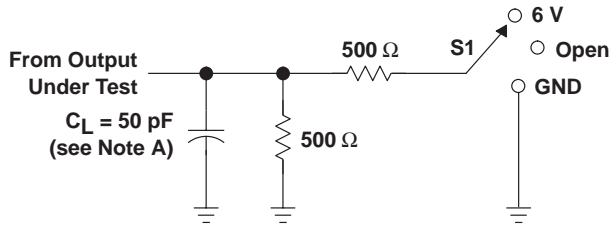
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH2245 | | | | SN74LVTH2245 | | | | UNIT | |
|-----------|-----------------|-------------|--|-----|-------------------------|-----|--|------|-----|-------------------------|------|-----|
| | | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | | MAX |
| t_{PLH} | A | B | 1 | 4.6 | 5.3 | | 1.1 | 2.9 | 4.4 | 5.1 | | ns |
| t_{PHL} | | | 1 | 4.6 | 5.3 | | 1.1 | 2.6 | 4.4 | 5.1 | | |
| t_{PLH} | B | A | 1 | 3.7 | 4.2 | | 1.1 | 2.2 | 3.5 | 4 | | ns |
| t_{PHL} | | | 1 | 3.7 | 4.2 | | 1.1 | 2 | 3.5 | 4 | | |
| t_{PZH} | \overline{OE} | A | 1.2 | 5.7 | 7.4 | | 1.3 | 3.1 | 5.5 | 7.1 | | ns |
| t_{PZL} | | | 1.6 | 5.7 | 6.8 | | 1.7 | 3.2 | 5.5 | 6.5 | | |
| t_{PHZ} | \overline{OE} | A | 2 | 6.2 | 6.8 | | 2.2 | 3.6 | 5.9 | 6.5 | | ns |
| t_{PLZ} | | | 2 | 5.3 | 5.5 | | 2.2 | 3.4 | 5 | 5.1 | | |
| t_{PZH} | \overline{OE} | B | 1.2 | 6.4 | 7.6 | | 1.3 | 3.5 | 6.2 | 7.3 | | ns |
| t_{PZL} | | | 1.6 | 6.4 | 7.5 | | 1.7 | 3.7 | 6.2 | 7.3 | | |
| t_{PHZ} | \overline{OE} | B | 2 | 6.1 | 6.8 | | 2.2 | 3.9 | 5.9 | 6.5 | | ns |
| t_{PLZ} | | | 2 | 5.7 | 5.9 | | 2.2 | 3.7 | 5.4 | 5.7 | | |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN54LVTH2245, SN74LVTH2245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

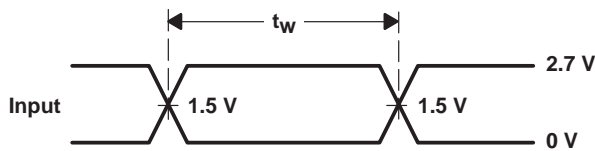
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PARAMETER MEASUREMENT INFORMATION

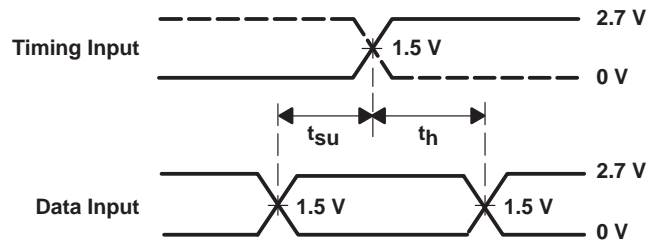


LOAD CIRCUIT

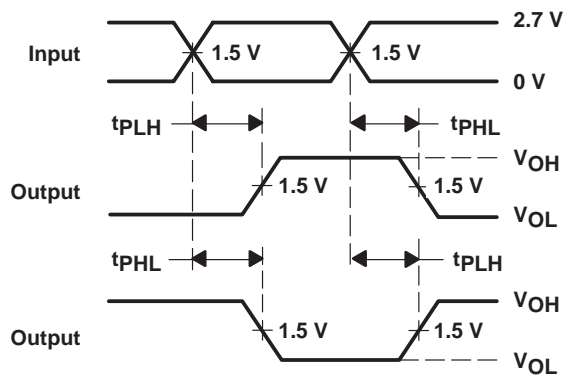
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



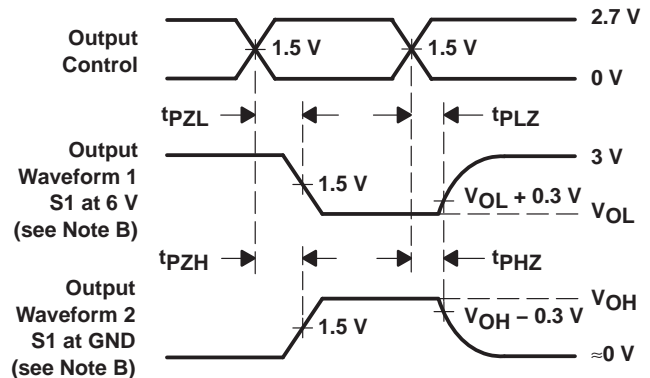
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVTH2245DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LK245 | Samples |
| SN74LVTH2245DGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LK245 | Samples |
| SN74LVTH2245DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH2245 | Samples |
| SN74LVTH2245DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH2245 | Samples |
| SN74LVTH2245PW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LK245 | Samples |
| SN74LVTH2245PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LK245 | Samples |
| SN74LVTH2245PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LK245 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH2245DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVTH2245DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVTH2245DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVTH2245PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH2245DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVTH2245DGVR | TVSOP | DGV | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVTH2245DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVTH2245PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVTH2245DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LVTH2245PW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

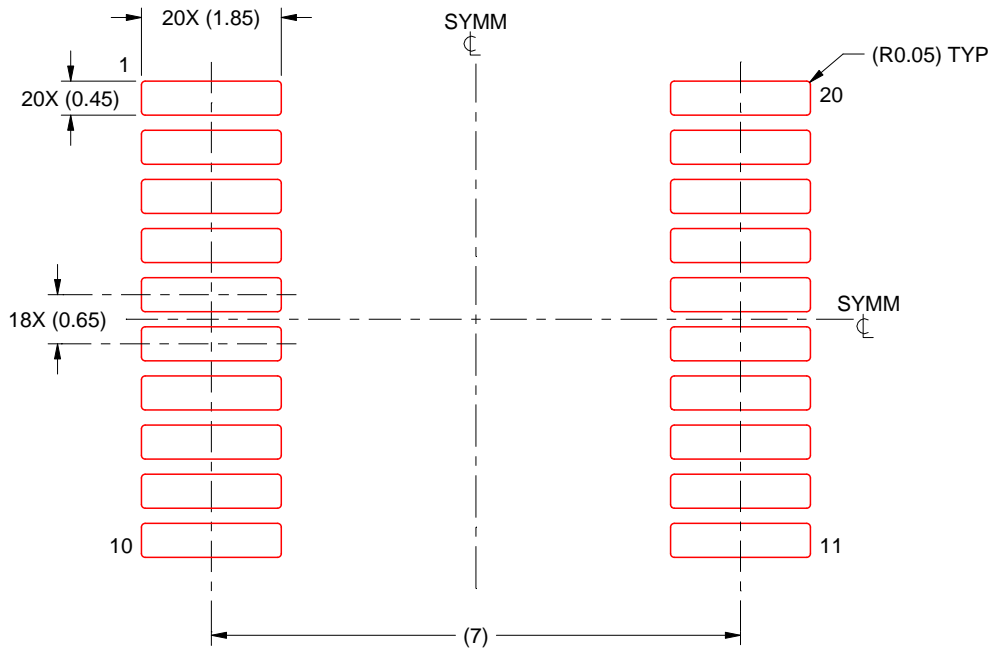
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

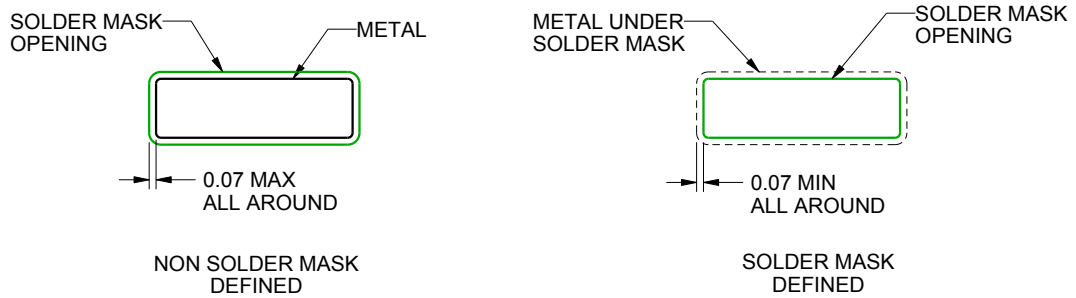
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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