具有均衡器 (EQ)，动态范围控制 (DRC)，2.1 支持，和头戴式耳机/线路驱动器的数字音频功率放大器

查询样品: TAS5721

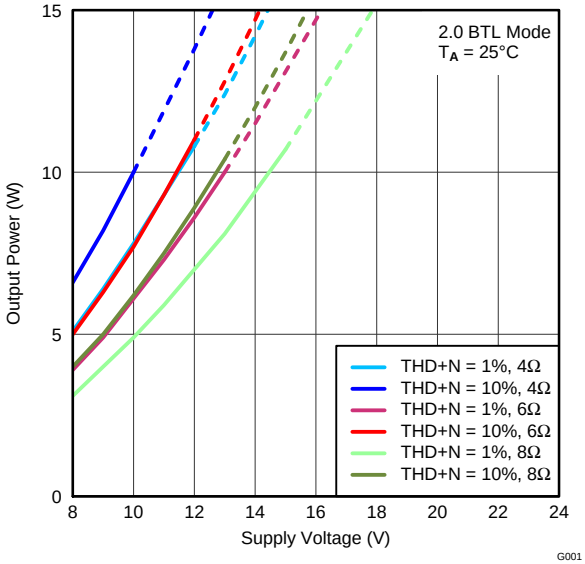
特性

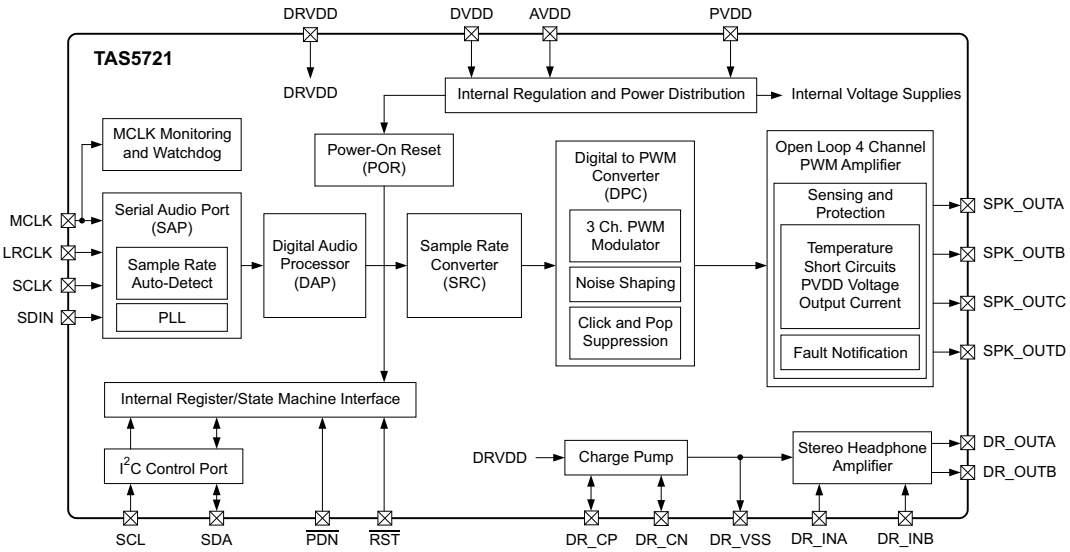
- 音频输入/输出
  - **PVDD=24V** 时，到 **8Ω** 的输入功率为 **10W x 2**
  - **PVDD=24V** 时，到 **8Ω** 的输入功率为 **8W x 2 + 12W x 1**
  - 支持 **2.0**，单器件 **2.1**，和单声道模式
  - 支持 **8kHz** 至 **48kHz** 采样率 **(LJ/RJ/I²S)**
  - 集成的 **DirectPath™** 头戴式耳机放大器和 **2V_{RMS}**线路驱动器
- 音频/脉宽调制 **(PWM)** 处理
  - 独立通道音量控制（从 **24dB** 至静音，步长 **0.5dB**）
  - 针对卫星和子通道的独立动态范围控制
  - 针对扬声器 **EQ** 的 **21** 个可编程双二次滤波器
  - 可编程双波段动态范围控制
  - 支持 **3D** 效果
- 一般特性
  - **I²C™** 无主时钟 **(MCLK)** 的串行控制接口运行
  - 可配置的 **I²C** 地址（**0x34** 或 **0x36**）
  - 自动采样率检测
  - 过热和短路保护
  - 宽 **PVDD** 电源范围（**4.5V** 至 **24V**）

应用范围

- **LED/LCD TV**，**Soundbar** 音箱，扩展坞，**PC** 扬声器

输出功率与 **PVDD** 间的关系（**2.0** 模式下）





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

说明

TAS5721是一款高效、数字输入音频放大器，此放大器用于驱动被配置为一个桥接负载 (BTL) 的 2.0 扬声器系统、具有两个卫星扬声器和一个低音炮的 2.1 系统、或者在 PBTL 系统中驱动一个被配置为平行桥接负载 (PBTL) 的单扬声器。 一个串行数据输入可处理最多两个独立的音频通道并能与大多数数字音频处理器和 MPEG 解码器无缝整合。 此器件可接受宽范围的输入数据格式和采样率。 一个完全可编程数据路径将这些通道路由至内部扬声器驱动器。

TAS5721是一个用于从外部源接收所有时钟的从属器件。 根据输出采样率的不同，TAS5721运行时带有 384kHz 开关速率至 288KHz 开关速率间的 PWM 载波。 与一个四阶噪声整形器结合的过采样可提供一个真实白噪音基准以及从 20Hz 至 20kHz 的出色动态范围。

一个集成的中心接地 DirectPath™ 组合头戴式耳机放大器和 $2V_{RMS}$线路驱动器被集成在TAS5721中。

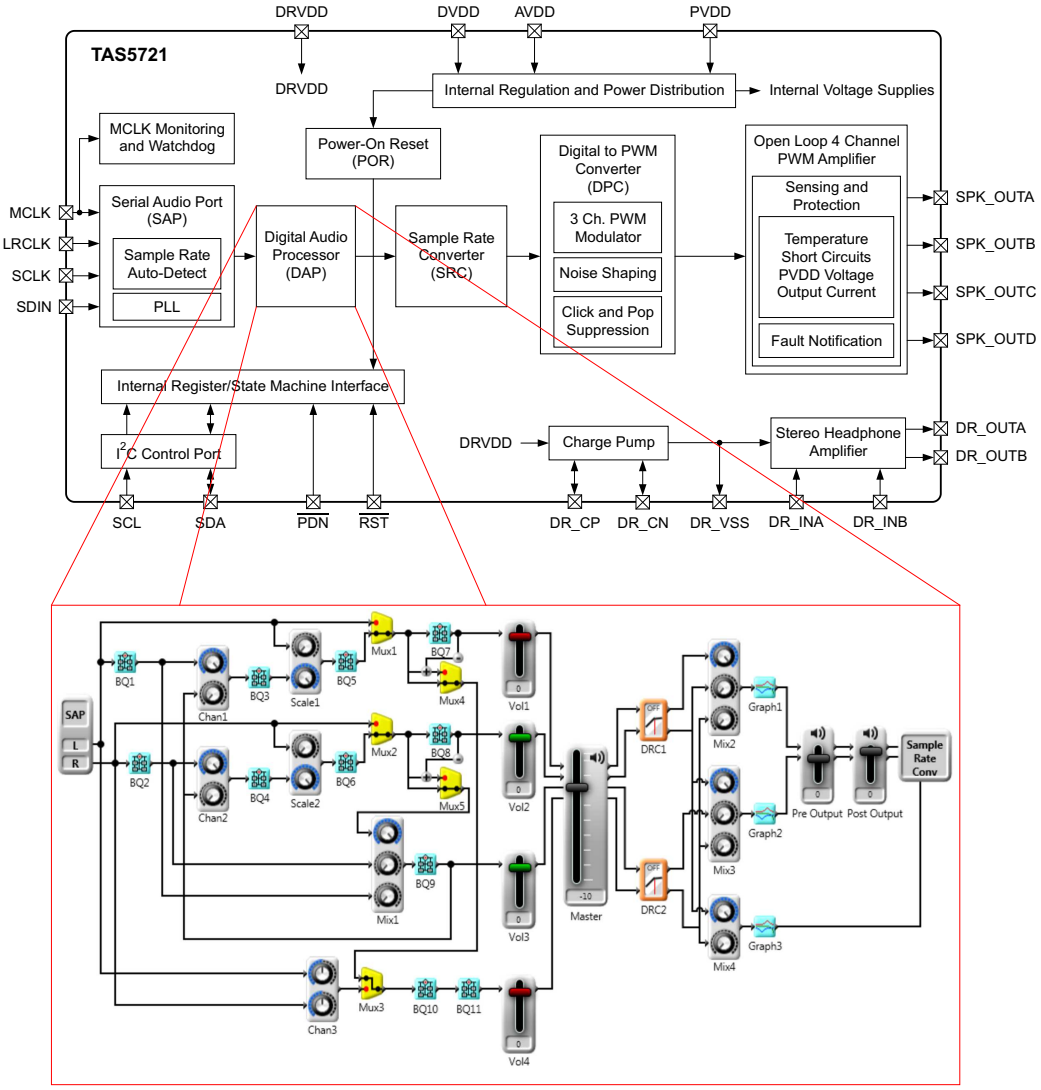
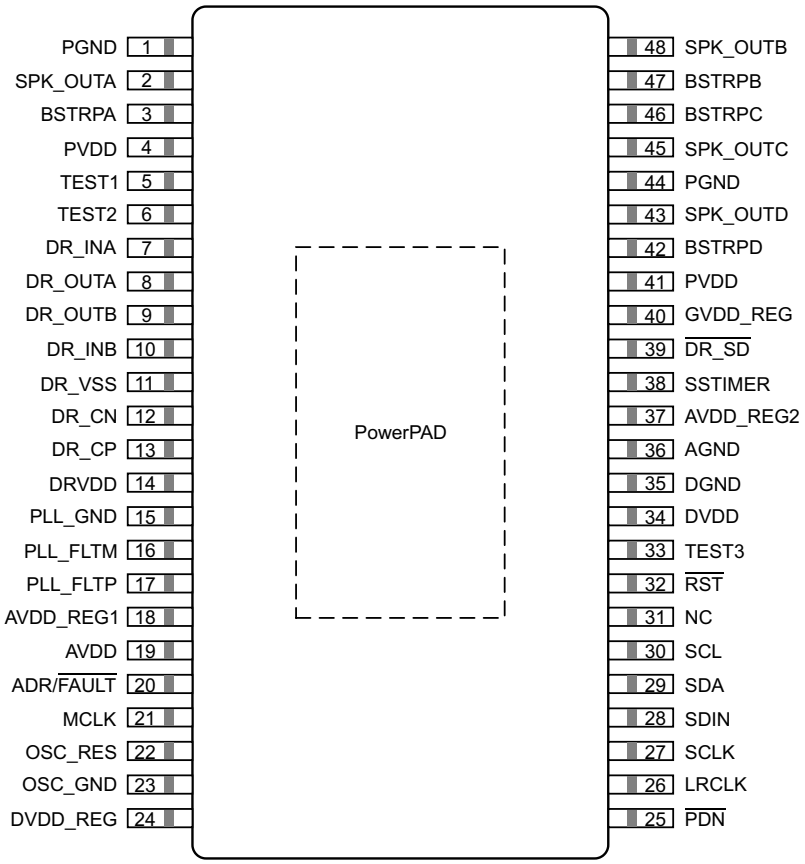

TAS5721
DRVDD
DVDD
AVDD
PVDD
Internal Regulation and Power Distribution
Internal Voltage Supplies
MCLK Monitoring and Watchdog
Power-On Reset (POR)
Digital to PWM Converter (DPC)
3 Ch. PWM Modulator
Noise Shaping
Click and Pop Suppression
Open Loop 4 Channel PWM Amplifier
Sensing and Protection
Temperature Short Circuits PVDD Voltage Output Current
Fault Notification
MCLK
LRCLK
SCLK
SDIN
Serial Audio Port (SAP)
Sample Rate Auto-Detect
PLL
Digital Audio Processor (DAP)
Sample Rate Converter (SRC)
SPK_OUTA
SPK_OUTB
SPK_OUTC
SPK_OUTD
Internal Register/State Machine Interface
I2C Control Port
Charge Pump
Stereo Headphone Amplifier
DR_OUTA
DR_OUTB
SCL
SDA
PDN
RST
DR_CP
DR_CN
DR_VSS
DR_INA
DR_INB
SAP
L
R
BQ1
BQ2
BQ3
BQ4
BQ5
BQ6
BQ7
BQ8
BQ9
BQ10
BQ11
Chan1
Chan2
Chan3
Scale1
Scale2
Mux1
Mux2
Mux3
Mux4
Mux5
Mix1
Vol1
Vol2
Vol3
Vol4
Master
DRC1
DRC2
Mix2
Mix3
Mix4
Graph1
Graph2
Graph3
Pre Output
Post Output
Sample Rate Conv

图 1. DAP 过程结构

PIN ASSIGNMENT AND DESCRIPTIONS

TAS5721
DCA Package
(Top View)



Pin Out

PIN		TYPE(1)	TERMINATION	DESCRIPTION
NAME	NO.			
ADR/FAULT	20	DI/DO	-	Dual function terminal which sets the LSB of the I²C address to 0 if pulled to GND, 1 if pulled to DVDD. If configured to be a fault output by the methods described in I²C Address Selection and Fault Output, this terminal is pulled low when an internal fault occurs. A pull-up or pull-down resistor is required, as is shown in the Typical Application Circuit Diagrams.
AGND	36	P	-	Ground reference for analog circuitry(2)
AVDD	19	P	-	Power supply for internal analog circuitry
AVDD_REG1	18	P	-	Voltage regulator derived from AVDD supply(3)
AVDD_REG2	37	P	-	Voltage regulator derived from AVDD supply(3)
BSTRPx	3, 42, 46, 47	P	-	Connection points for the bootstrap capacitors, which are used to create a power supply for the high-side gate drive of the device
DGND	35	P	-	Ground reference for digital circuitry(2)
DR_CN	12	P	-	Negative terminal for capacitor connection used in headphone amplifier and line driver charge pump
DR_CP	13	P	-	Positive terminal for capacitor connection used in headphone amplifier and line driver charge pump
DR_INx	7, 10	AI	-	Input for channel A or B of headphone amplifier or line driver

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output
(2) This terminal should be connected to the system ground
(3) This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry.

Pin Out (continued)

DR_OUTx	8, 9	AO	-	Output for channel A or B of headphone amplifier or line driver
$\overline{\text{DR\_SD}}$	39	DI	-	Places the headphone amplifier/line driver in shutdown when pulled low.
DR_VSS	11	P	-	Negative supply generated by charge pump for ground centered headphone and line driver output
DRVDD	14	P	-	Power supply for internal headphone and line driver circuitry
DVDD	34	P	-	Power supply for the internal digital circuitry
DVDD_REG	24	P	-	Voltage regulator derived from DVDD supply(3)
GVDD_REG	40	P	-	Voltage regulator derived from PVDD supply(3)
LRCLK	26	DI	Pulldown	Word select clock for the digital signal that is active on the input data line of the serial port
MCLK	21	DI	Pulldown	Master clock used for internal clock tree and sub-circuit and state machine clocking
NC	31	-	-	Not connected inside the device (all no connect terminals should be connected to ground)
OSC_GND	23	P	-	Ground reference for oscillator circuitry (this terminal should be connected to the system ground)
OSC_RES	22	AO	-	Connection point for oscillator trim resistor
$\overline{\text{PDN}}$	25	DI	Pullup	Quick powerdown of the device that is used upon an unexpected loss of PVDD or DVDD power supply in order to quickly transition the outputs of the speaker amplifier to a 50/50 duty cycle. This quick powerdown feature avoids the audible anamolies that would occur as a result of loss of either of the supplies. If this pin is used to place the device into quick powerdown mode, the $\overline{\text{RST}}$ pin of the device must be toggled before the device is brought out of quick powerdown.
PGND	1	P	-	Ground reference for power device circuitry(4)
PLL_FLTM	16	AI/AO	-	Negative connection point for the PLL loop filter components
PLL_FLTP	17	AI/AO	-	Positive connection point for the PLL loop filter components
PLL_GND	15	P	-	Ground reference for PLL circuitry (this terminal should be connected to the system ground)
PowerPAD	-	P	-	Thermal and ground pad thatprovides both an electrical connection to the ground plane and a thermal path to the PCB for heat dissipation. This pad must be grounded to the system ground.
PVDD	4, 41	P	-	Power supply for internal power circuitry
$\overline{\text{RST}}$	32	DI	Pullup	Places the device in reset when pulled low
SCL	30	DI	-	I^2C serial control port clock
SCLK	27	DI	Pulldown	Bit clock for the digital signal that is active on the input data line of the serial data port
SDA	29	DI/DO	-	I^2C serial control port data
SDIN	28	DI	Pulldown	Data line to the serial data port
SPK_OUTx	2, 43, 45, 48	AO	-	Speaker amplifier outputs
SSTIMER	38	AI	-	Connection point for the capacitor that is used by the ramp timing circuit, as described in Output Mode and MUX Selection
TEST1	5	DO	-	Used by TI for testing during device production (this terminal must be left floating)
TEST2	6	DO	-	Used by TI for testing during device production (this terminal must be left floating)
TEST3	33	DI	-	Used by TI for testing during device production (this terminal must be connected to GND)

(4) This terminal should be connected to the system ground

TYPICAL APPLICATION CIRCUITS

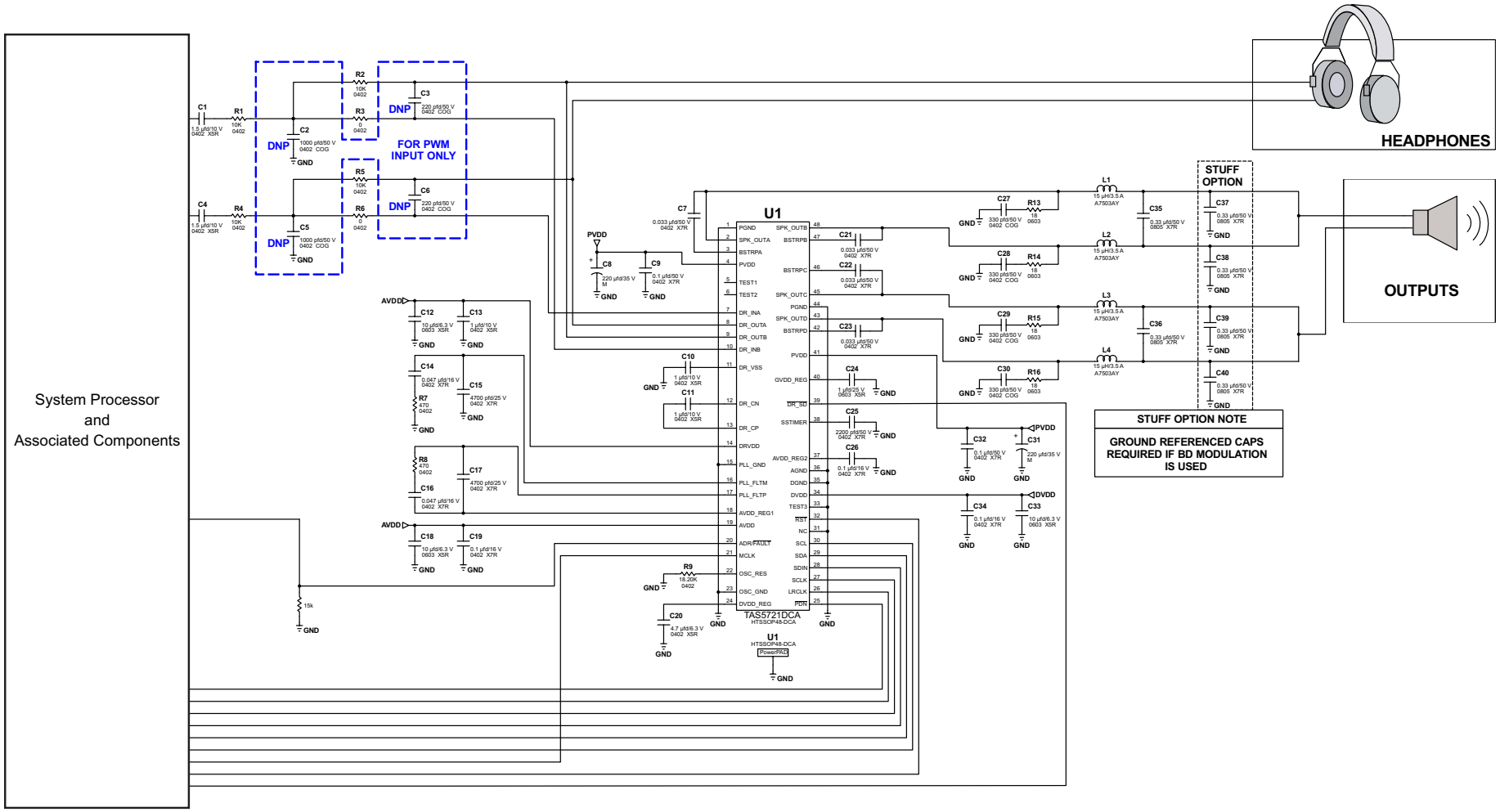


Figure 2. Typical Application Circuit for Mono (PBTL) Configuration

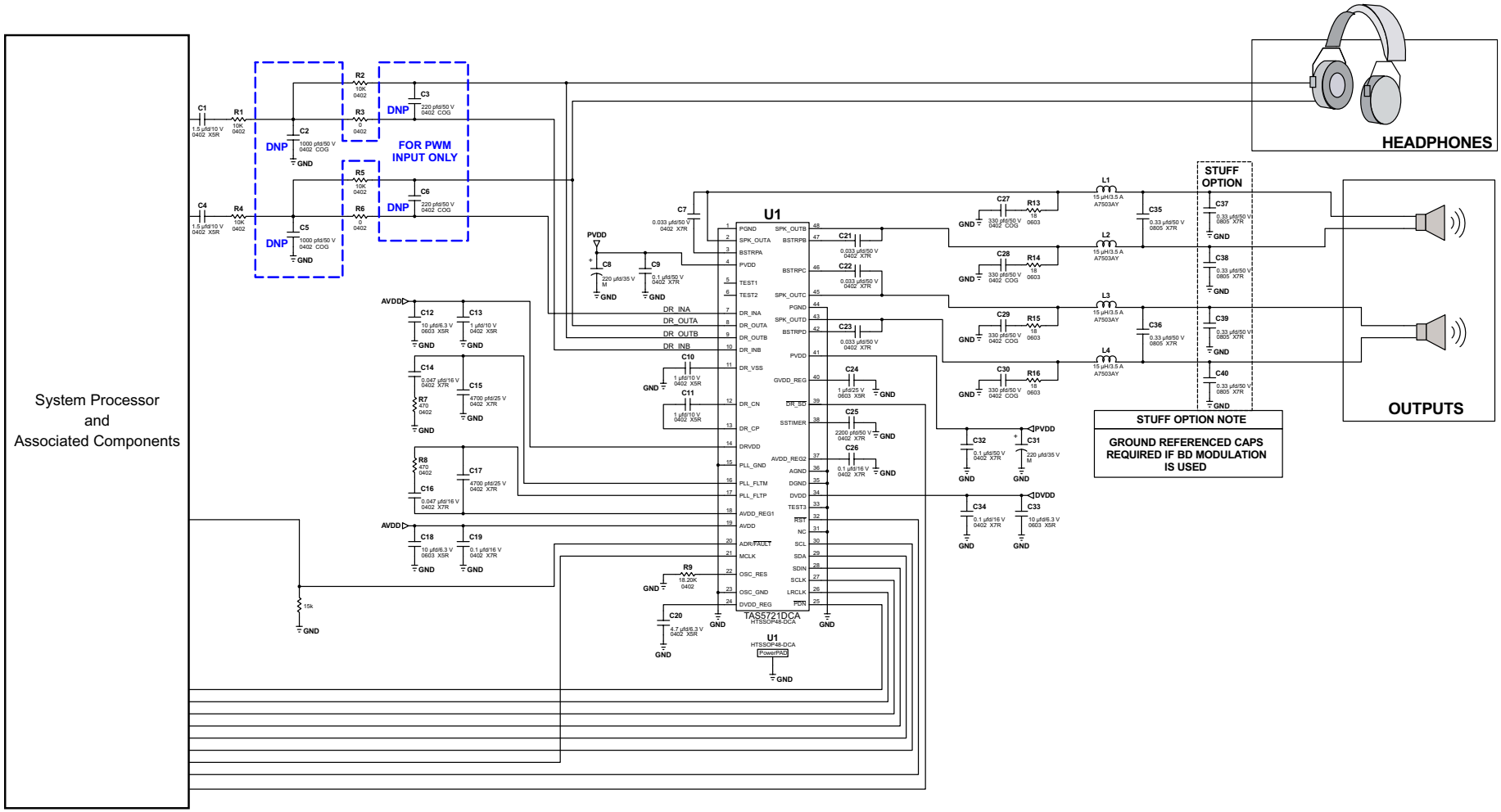


Figure 3. Typical Application Diagram for 2.0 Configuration

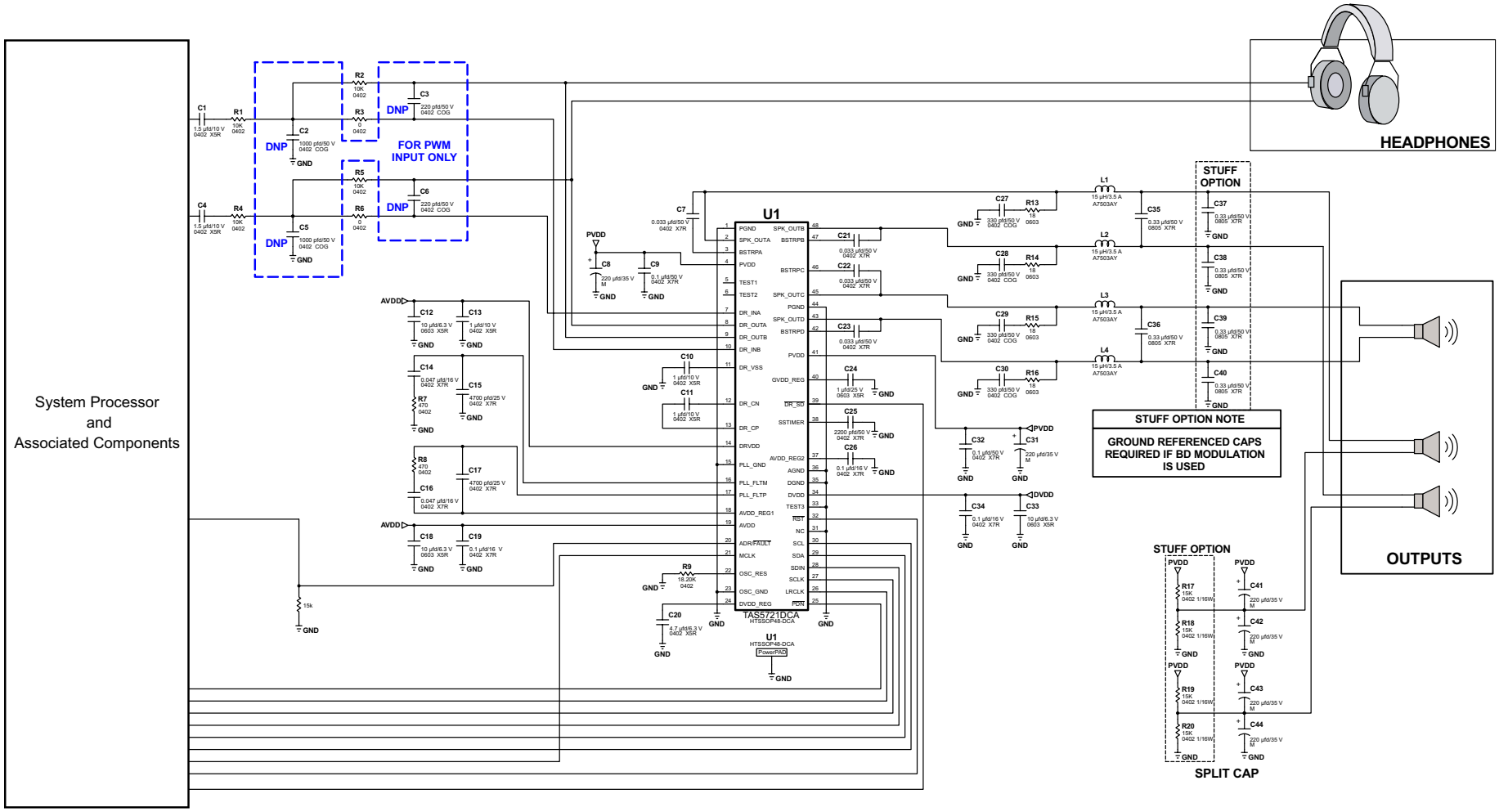


Figure 4. Typical Application Diagram for 2.1 Configuration

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted). (1)

		VALUE	UNIT
Supply voltage	DVDD, AVDD, DRVDD	–0.3 to 3.6	V
	PVDD	–0.3 to 30	V
DR_INx		–0.3 to DRVDD + 6 V	V
Input voltage	3.3-V digital input	–0.5 to DVDD + 0.5	V
	5-V tolerant(2) digital input (except MCLK)	–0.5 to DVDD + 2.5(3)	
	5-V tolerant MCLK input	–0.5 to AVDD + 2.5(3)	
SPK_OUTx to GND		32(4)	V
BSTRPx to GND		39(4)	V
Operating free-air temperature		0 to 85	°C
Storage temperature range, T_{stg}		–40 to 125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are $\overline{PDN}$, $\overline{RST}$, SCLK, LRCLK, MCLK, SDIN, SDA, and SCL.
(3) Maximum pin voltage should not exceed 6 V.
(4) DC voltage + peak AC waveform measured at the pin should be below the allowed limit for all conditions.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
xVDD	Digital, analog, headphone supply voltage		3	3.3	3.6	V
PVDD	Half-bridge supply voltage		8		26.4(1)	V
V_{IH}	High-level input voltage	5-V tolerant	2			V
V_{IL}	Low-level input voltage	5-V tolerant			0.8	V
T_A	Operating ambient temperature range		0		85	°C
T_J (2)	Operating junction temperature range		0		125	°C
R_{SPK} (SE, BTL, and PBTL)	Minimum Supported Speaker Impedance	Output filter: L = 15 µH, C = 330 nF	4	8		Ω
Lo(BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition	10			µH
R_{HP}	Headphone mode load impedance		16		32	Ω
R_{LD}	Line-diver mode load impedance		0.6		10	kΩ

(1) For operation at PVDD levels greater than 18 V, the modulation limit must be set to 93.8% via the control port register 0x10.
(2) Continuous operation above the recommended junction temperature may result in reduced reliability and/or lifetime of the device.

ELECTRICAL CHARACTERISTICS

I/O Pin Characteristics

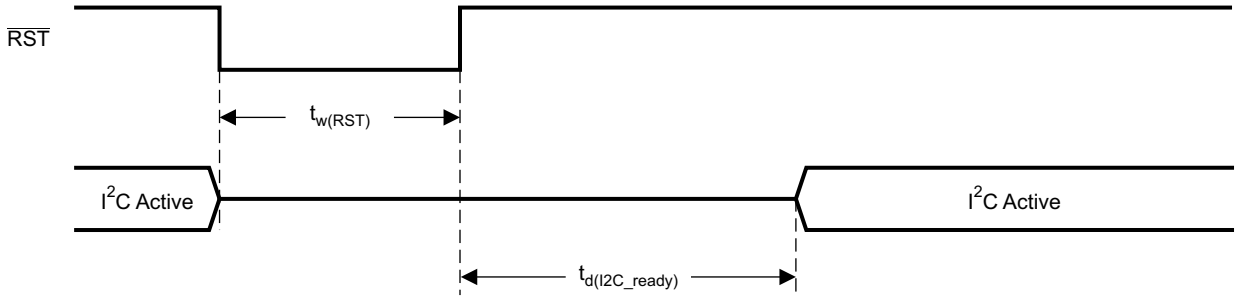
PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	ADR/$\overline{FAULT}$ and SDA	I_{OH} = –4 mA DVDD = AVDD = 3 V	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA DVDD = AVDD = 3 V			0.5	
I_{IL}	Low-level input current	Digital Inputs	$V_I < V_{IL}$; DVDD = AVDD = 3.6 V			75	µA
I_{IH}	High-level input current		$V_I > V_{IH}$; DVDD = AVDD = 3.6 V			75	

I/O Pin Characteristics (continued)

PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	3.3 V supply current	3.3 V supply voltage (DVDD, AVDD)	Normal mode		48	70	mA
			Reset ($\overline{RST}$ = low, $\overline{PDN}$ = high, DR_SD = low)		21	38	
$t_{w(RST)}$	Pulse duration, $\overline{RST}$ active	$\overline{RST}$		100			µs
$t_{d(I2C\_ready)}$	Time before the I^2C port is able communicate after $\overline{RST}$ goes high					12	ms



NOTE: On power up, it is recommended that the TAS5721 $\overline{RST}$ be held LOW for at least 100 µs after DVDD has reached 3 V.

NOTE: If $\overline{RST}$ is asserted LOW while $\overline{PDN}$ is LOW, then $\overline{RST}$ must continue to be held LOW for at least 100 µs after $\overline{PDN}$ is deasserted (HIGH).

Figure 5. Reset Timing

Master Clock Characteristics(1)

PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLK}	MCLK frequency		2.8224		24.576	MHz
	MCLK duty cycle		40%	50%	60%	
$t_{r(MCLK)}$ / $t_{f(MCLK)}$	Rise/fall time for MCLK				5	ns

(1) For clocks related to the serial audio port, please see Serial Audio Port Timing

I²C Serial Control Port Requirements and Specifications

PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	Frequency, SCL	No wait states		400	kHz
$t_{w(H)}$	Pulse duration, SCL high		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low		1.3		µs
t_r	Rise time, SCL and SDA			300	ns
t_f	Fall time, SCL and SDA			300	ns
t_{su1}	Setup time, SDA to SCL		100		ns
t_{h1}	Hold time, SCL to SDA		0		ns
$t_{(buf)}$	Bus free time between stop and start conditions		1.3		µs
t_{su2}	Setup time, SCL to start condition		0.6		µs
t_{h2}	Hold time, start condition to SCL		0.6		µs
t_{su3}	Setup time, SCL to stop condition		0.6		µs
C_L	Load capacitance for each bus line			400	pF

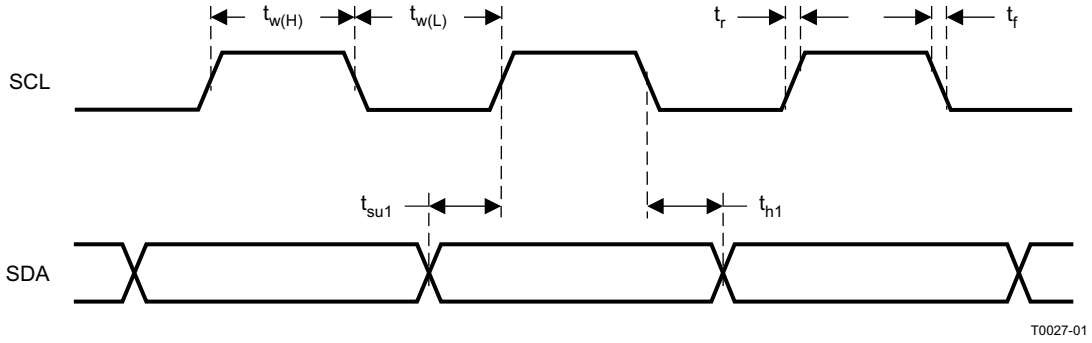


Figure 6. SCL and SDA Timing

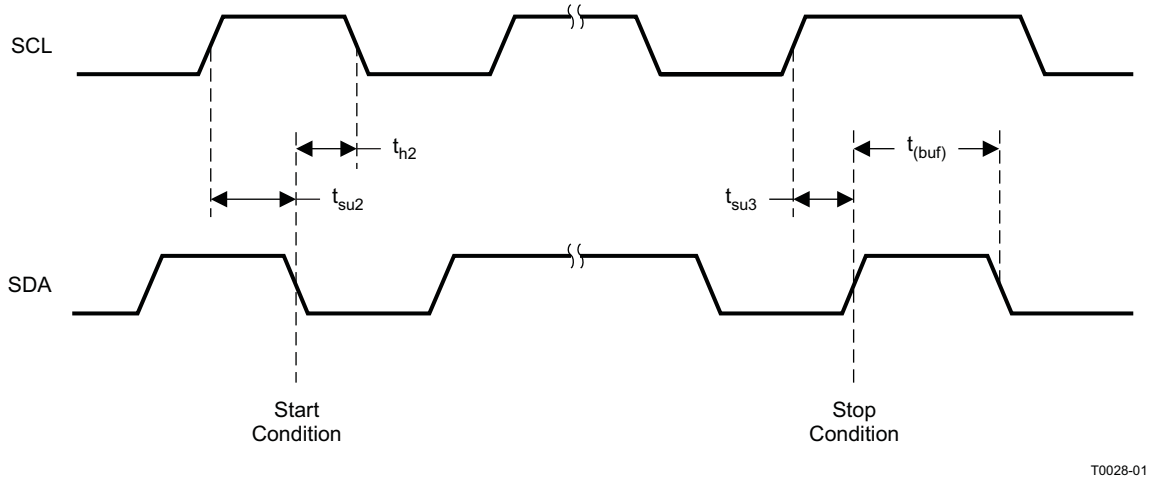


Figure 7. Start and Stop Conditions Timing

Serial Audio Port Timing

PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, audio input signal =1 kHz sine wave, BTL, AD mode, f_S = 48 kHz, R_{SPK} = 8 Ω, AES17 filter, f_{PWM} = 384 kHz, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	Frequency, SCLK 32 × f_S, 48 × f_S, 64 × f_S	C_L = 30 pF	1.024		12.288	MHz
t_{su1}	Setup time, LRCLK to SCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from SCLK rising edge		10			ns
t_{su2}	Setup time, SDIN to SCLK rising edge		10			ns
t_{h2}	Hold time, SDIN from SCLK rising edge		10			ns
	LRCLK frequency		8	48	48	kHz
	SCLK duty cycle		40%	50%	60%	
	LRCLK duty cycle		40%	50%	60%	
	SCLK rising edges between LRCLK rising edges		32		64	SCLK edges
$t_{(edge)}$	LRCLK clock edge with respect to the falling edge of SCLK		–1/4		1/4	SCLK period
t_r/t_f	Rise/fall time for SCLK/LRCLK				8	ns
	LRCLK allowable drift before LRCLK reset				4	MCLK Periods

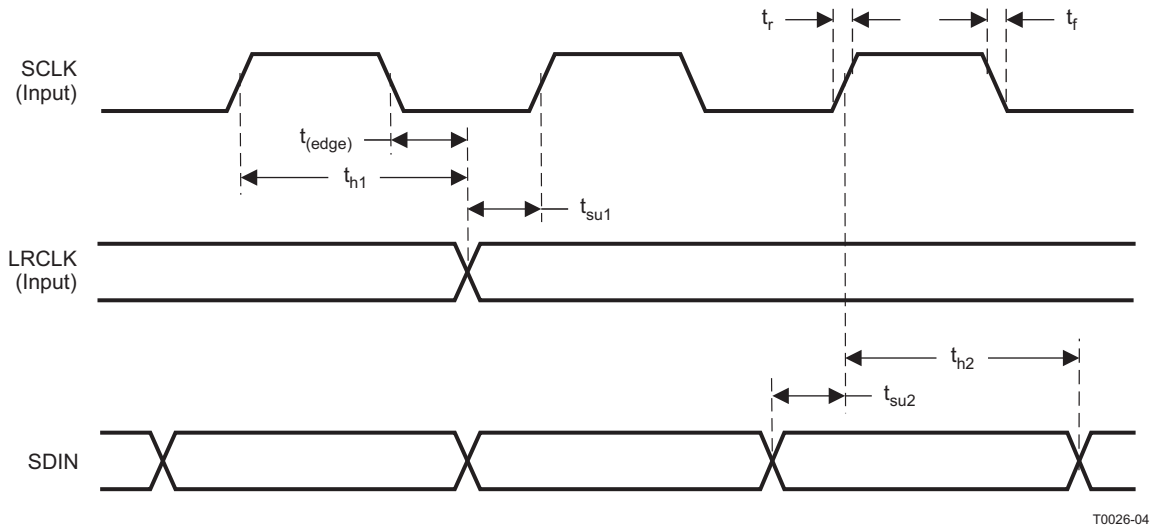


Figure 8. Serial Audio Port Timing

Speaker Amplifier Characteristics

T_A = 25°C, PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, audio input signal =1 kHz sine wave, BTL, AD mode, f_S = 48 kHz, R_{SPK} = 8 Ω, AES17 filter, f_{PWM} = 384 kHz, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Po_{SPK} (BTL)	Power output per channel of speaker amplifier when used in BTL mode (1)	PVDD = 18 V, R_{SPK} = 8Ω, 1-kHz input signal			10		W
		PVDD = 12 V, R_{SPK} = 8Ω, 10% THD+N, 1-kHz input signal			8.8		
		PVDD = 12 V, R_{SPK} = 8Ω, 7% THD+N, 1-kHz input signal			8.3		
		PVDD = 8 V, R_{SPK} = 8Ω, 10% THD+N, 1-kHz input signal			4		
		PVDD = 8 V, R_{SPK} = 8Ω, 7% THD+N, 1-kHz input signal			3.8		
Po_{SPK} (PBTL)	Power output per channel of speaker amplifier when used in PBTL mode (1)	PVDD = 12 V, R_{SPK} = 4Ω, 10% THD+N, 1-kHz input signal			10		
		PVDD = 12 V, R_{SPK} = 4Ω, 7% THD+N, 1-kHz input signal			10		
		PVDD = 18 V, R_{SPK} = 4Ω, 1-kHz input signal			10		
Po_{SPK} (SE)	Power output per channel of speaker amplifier when used in SE mode (1)	PVDD = 12 V, R_{SPK} = 4 Ω, 10% THD+N, 1-kHz input signal			4.3		
		PVDD = 24 V, R_{SPK} = 4 Ω, 10% THD+N, 1-kHz input signal			5.5		
THD+N	Total harmonic distortion + noise	PVDD = 18 V, P_O = 1 W			0.07		%
		PVDD = 12 V, P_O = 1 W			0.11		
		PVDD = 8 V, P_O = 1 W			0.2		
ICN	Idle channel noise	A-weighted			61		μV
	Crosstalk	P_O = 1 W, f = 1 kHz (BD Mode), PVDD = 24 V			58		dB
		P_O =1 W, f = 1 kHz (AD Mode), PVDD = 24 V			48		dB
SNR	Signal-to-noise ratio (2)	A-weighted, f = 1 kHz, maximum power at THD < 1%			106		dB
f_{PWM}	Output switching frequency	11.025/22.05/44.1-kHz data rate ±2%			352.8		kHz
		48/24/12/8/16/32-kHz data rate ±2%			384		
I_{PVDD}	Supply current	No load (PVDD)	Normal mode		32	50	mA
			Reset ($\overline{RST}$ = low, $\overline{PDN}$ = high)		5	8	
$r_{DS(on)}$	Drain-to-source resistance (for each of the Low-Side and High-Side Devices)	T_J = 25°C, includes metallization resistance			200		mΩ
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when drivers are in the high-impedance state to provide bootstrap capacitor charge.			3		kΩ

(1) Power levels are thermally limited.
(2) SNR is calculated relative to 0-dBFS input level.

Headphone Amplifier and Line Driver Characteristics

T_A = 25°C, PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, audio input signal =1 kHz sine wave, BTL, AD mode, f_S = 48 kHz, R_{SPK} = 8 Ω, AES17 filter, f_{PWM} = 384 kHz, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Po_{HP}	Power output per channel of headphone amplifier	DRVDD = 3.3 V (R_{HP} = 32; THD = 1%)		50		mW
AV_{DR}	Gain for headphone amplifier and line driver	Adjustable through R_{in} and R_{fb}		-		dB
SNR_{HP}	Signal-to-noise ratio (headphone mode)	R_{hp} = 32		101		dB
SNR_{LD}	Signal-to-noise ratio (line driver mode)	2-V_{RMS} output		105		dB

Protection Characteristics

T_A = 25°C, PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, audio input signal =1 kHz sine wave, BTL, AD mode, f_S = 48 kHz, R_{SPK} = 8 Ω, AES17 filter, f_{PWM} = 384 kHz, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{uvp(fall)}$	Undervoltage protection limit	PVDD falling		4		V
$V_{uvp(rise)}$	Undervoltage protection limit	PVDD rising		4.1		V
OTE	Overtemperature error threshold			150		°C
ΔOTE	Variation in overtemperature detection circuit			±15		°C
I_{OCE}	Overcurrent limit protection threshold			3.0		A
t_{OCE}	Overcurrent response time			150		ns

THERMAL CHARACTERISTICS

THERMAL METRIC(1)		TAS5721 DCA 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	27.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	20.7	
θ_{JB}	Junction-to-board thermal resistance(4)	13	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.3	
ψ_{JB}	Junction-to-board characterization parameter(6)	6.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.1	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：SPRA953）。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结至电路板的热阻。
(5) 结至顶部的特征参数，(ψ_{JT})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(6) 结至电路板的特征参数，(ψ_{JB})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到了内容接近的说明。

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT POWER vs PVDD IN 2.1 MODE

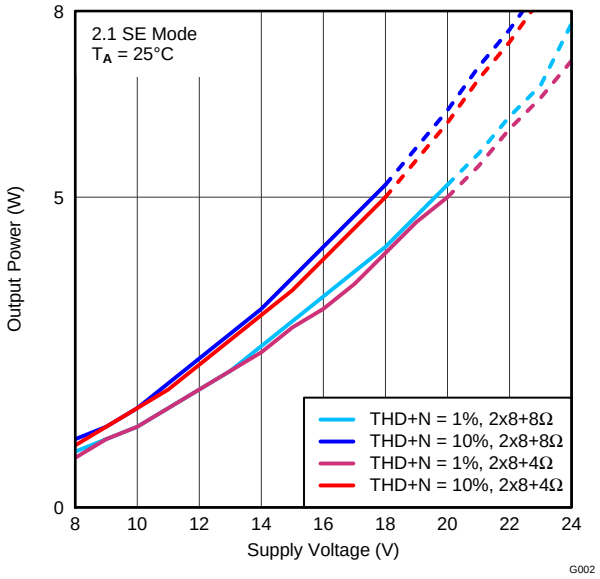


Figure 9.

OUTPUT POWER vs PVDD IN PBTL MODE

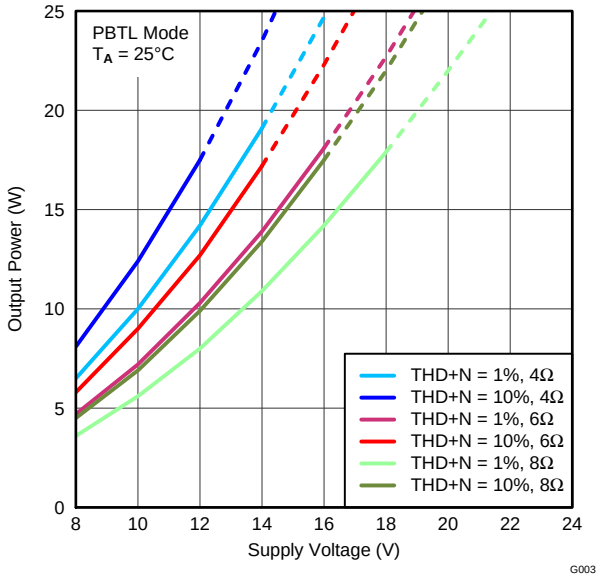


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN 2.0 MODE WITH PVDD = 12 V

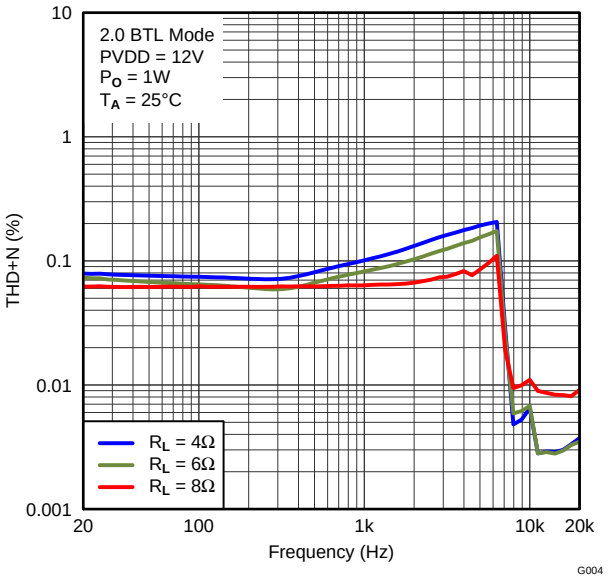


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY in 2.0 MODE WITH PVDD = 18 V

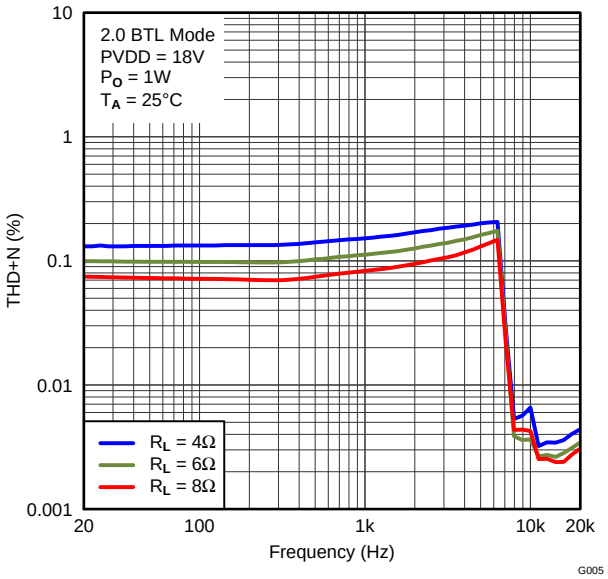


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN 2.0 MODE WITH PVDD = 24 V

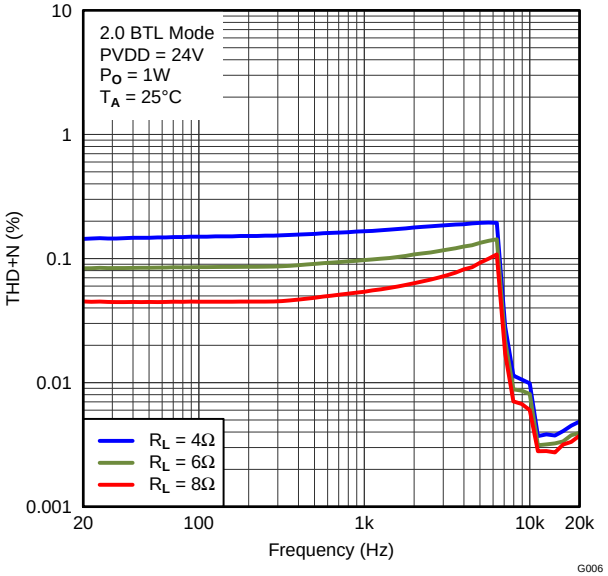


Figure 13.

TOTAL HARMONIC DISTORTION + NOISE vs FEQUENCY IN 2.1 MODE WITH PVDD = 12 V

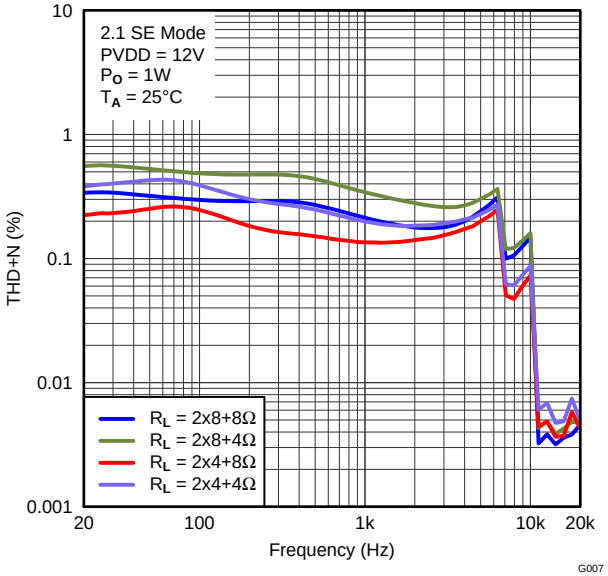


Figure 14.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN 2.1 MODE WITH PVDD = 18 V

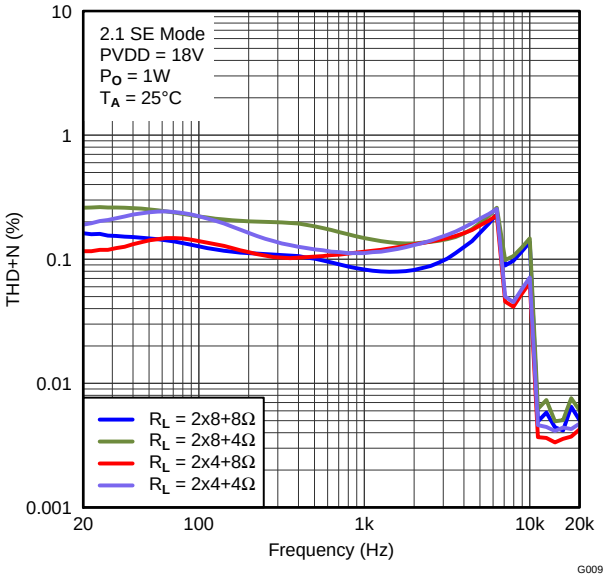


Figure 15.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN 2.1 MODE WITH PVDD = 24 V

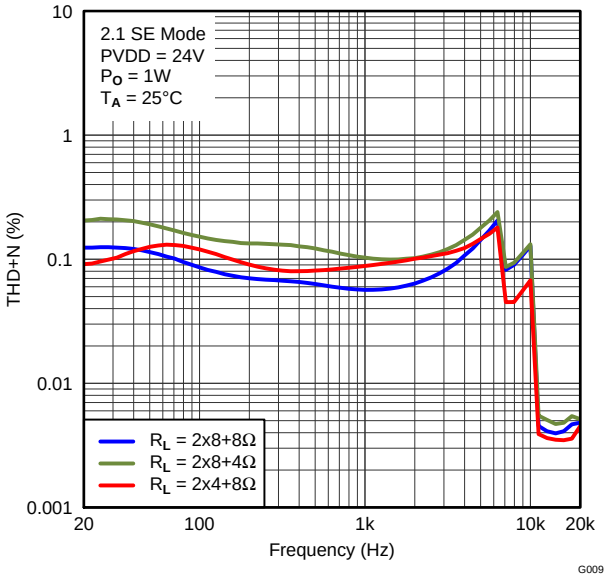


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN PBTL MODE WITH PVDD = 12 V

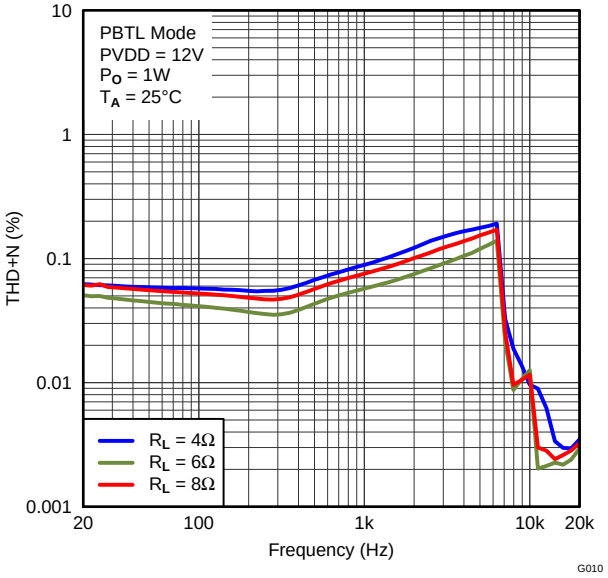


Figure 17.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN PBTL MODE WITH PVDD = 18 V

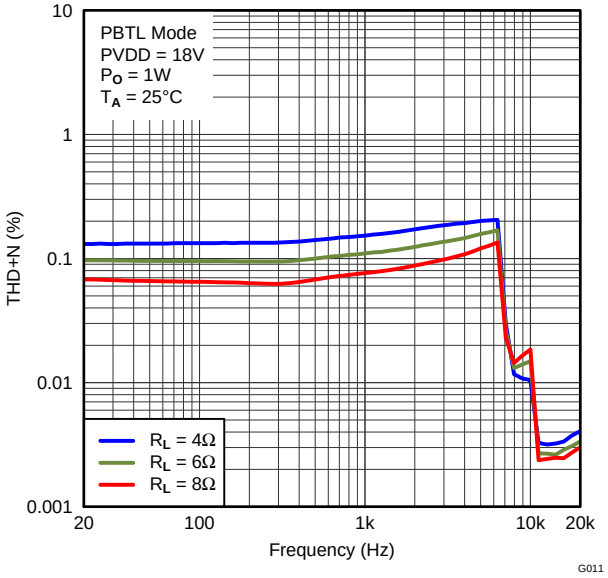


Figure 18.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN PBTL MODE WITH PVDD = 24 V

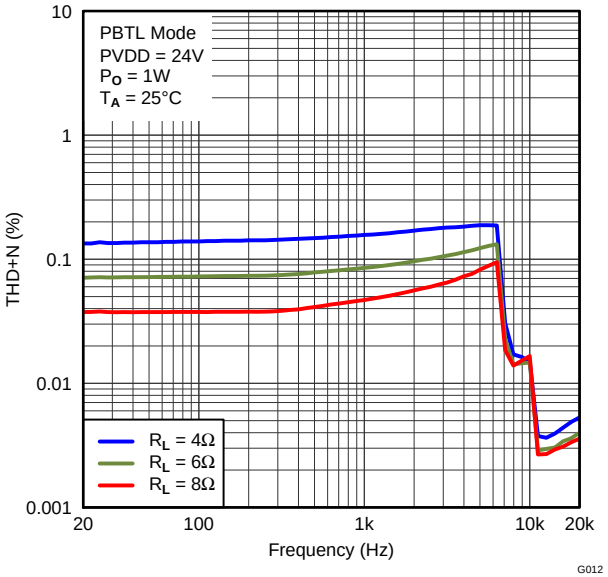


Figure 19.

2.0 IDLE CHANNEL NOISE vs PVDD

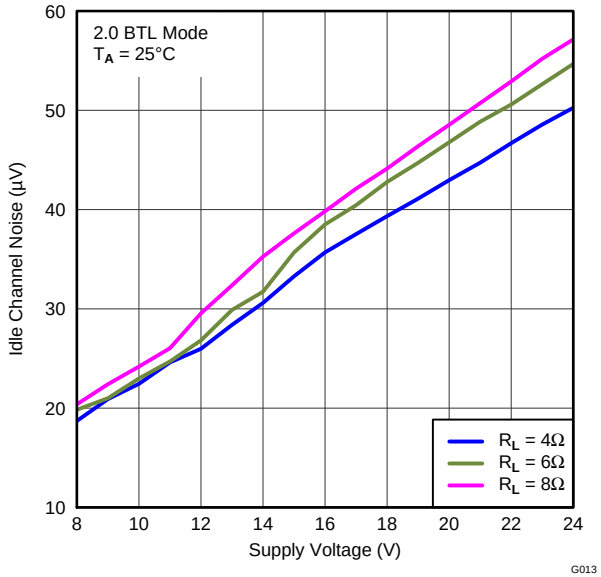


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

2.1 IDLE CHANNEL NOISE vs PVDD

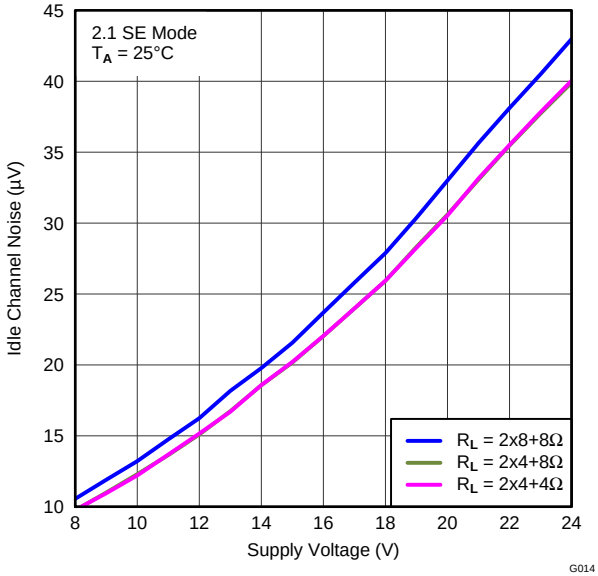


Figure 21.

PBTL IDLE CHANNEL NOISE vs PVDD

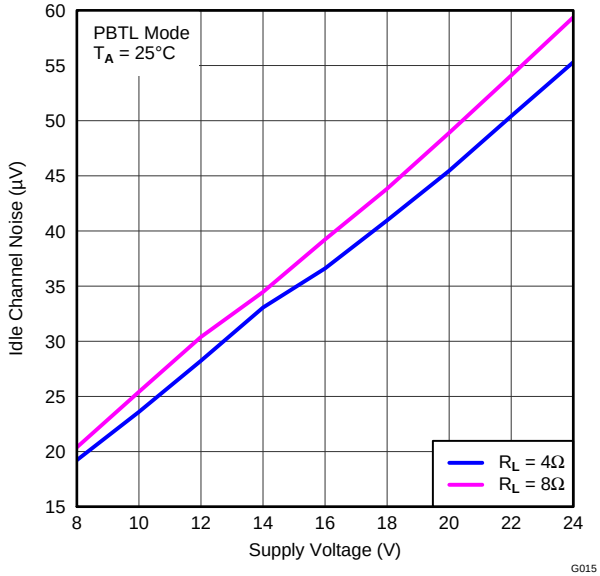


Figure 22.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN 2.0 MODE WITH PVDD = 12 V

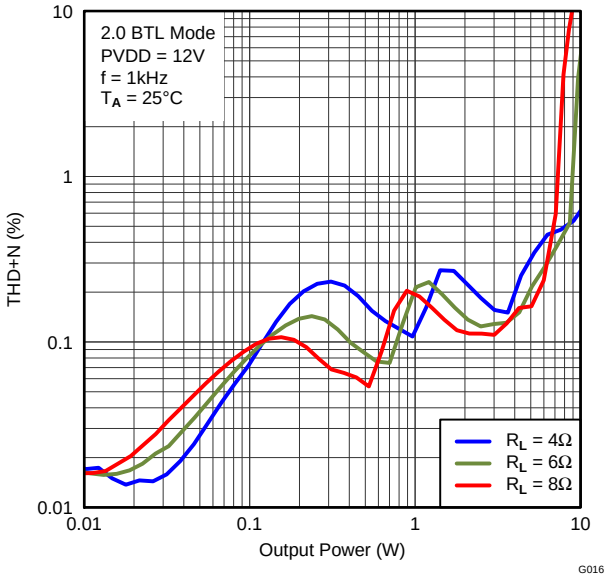


Figure 23.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN 2.0 MODE WITH PVDD = 18 V

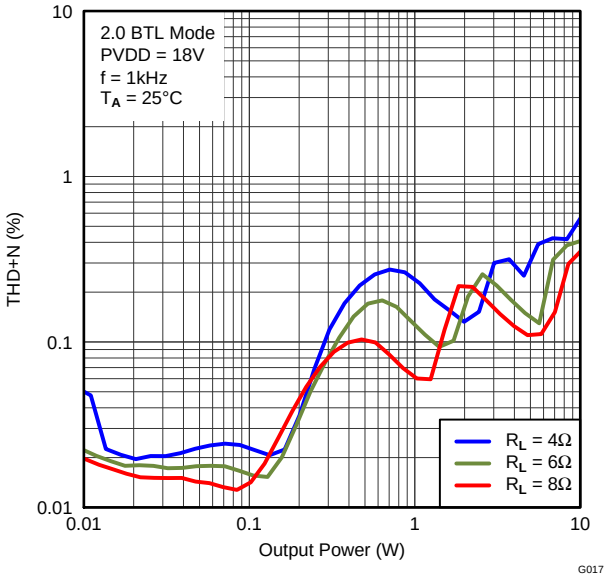


Figure 24.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN 2.0 MODE WITH PVDD = 24 V

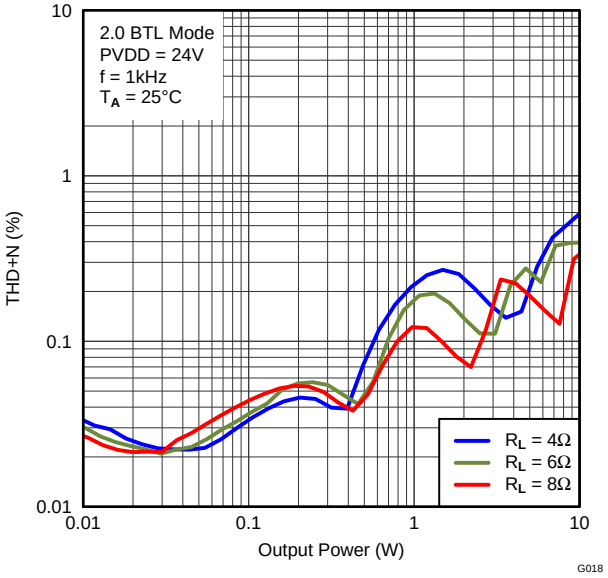


Figure 25.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN 2.1 MODE WITH PVDD = 12 V

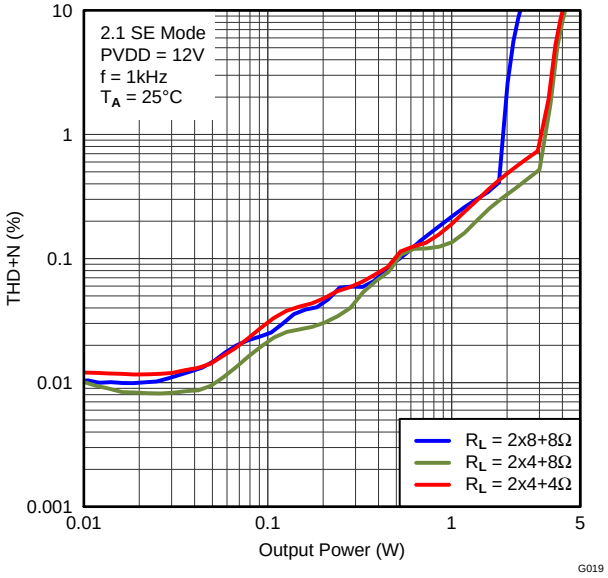


Figure 26.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN 2.1 MODE WITH PVDD = 18 V

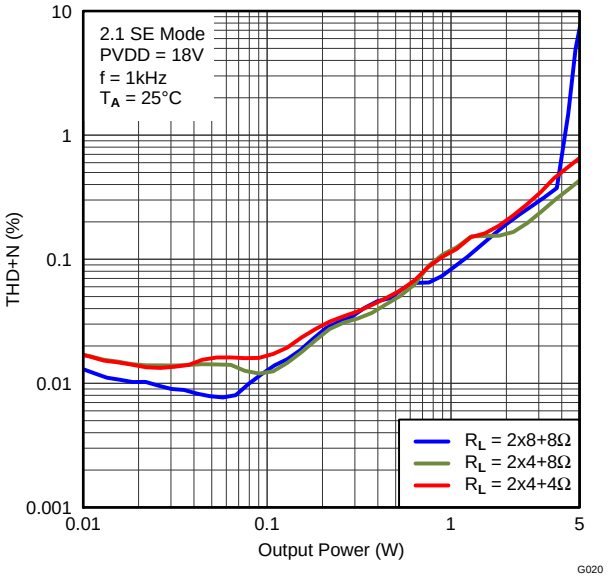


Figure 27.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN 2.1 MODE WITH PVDD = 24 V

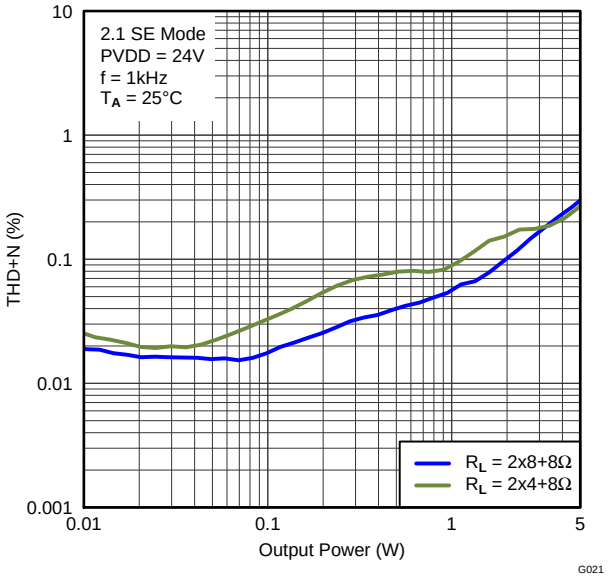


Figure 28.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN PBTL MODE WITH PVDD = 12 V

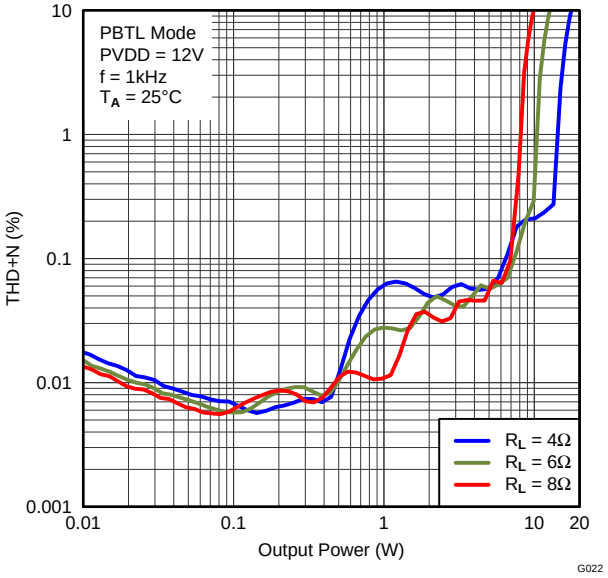


Figure 29.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN PBTL MODE WITH PVDD = 18 V

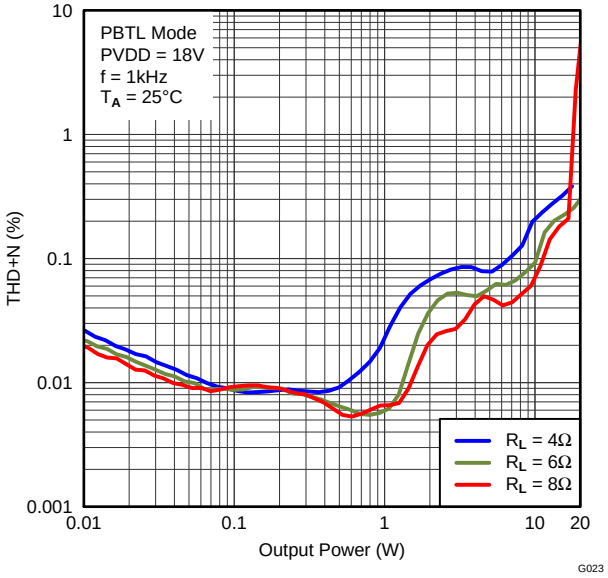


Figure 30.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN PBTL MODE WITH PVDD = 24 V

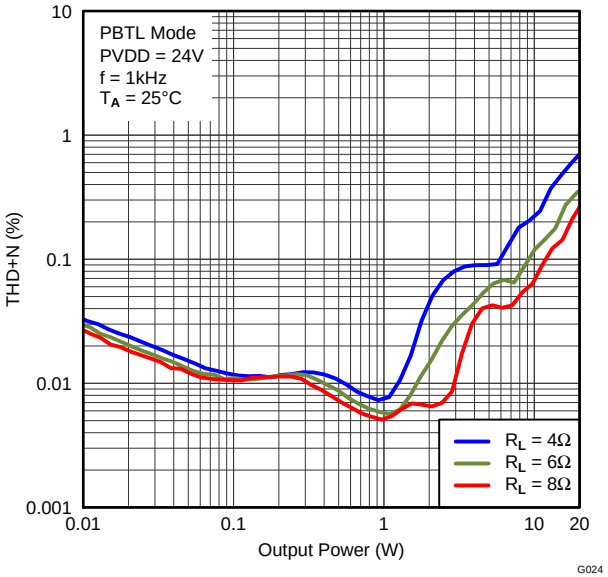
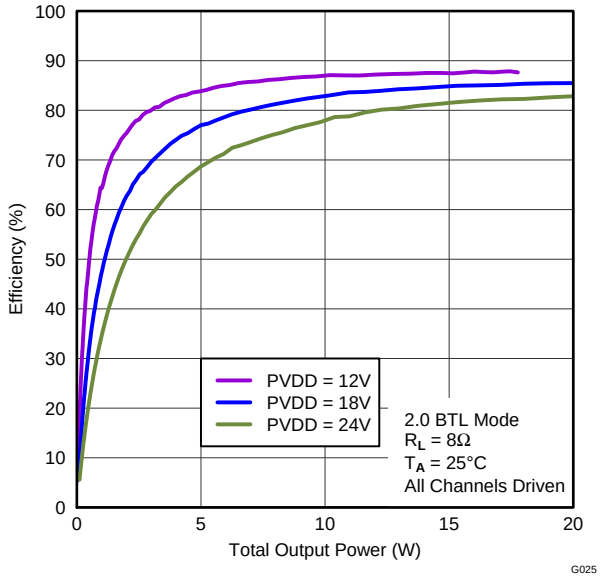


Figure 31.

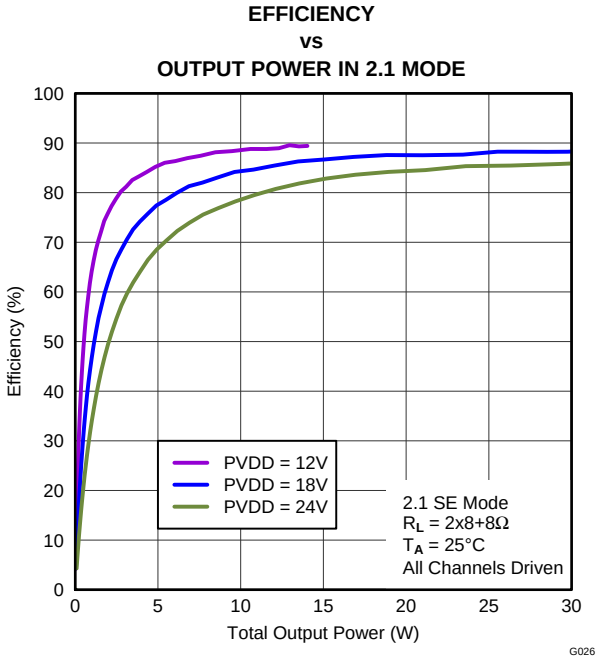
EFFICIENCY vs OUTPUT POWER IN 2.0 MODE



All channels driven

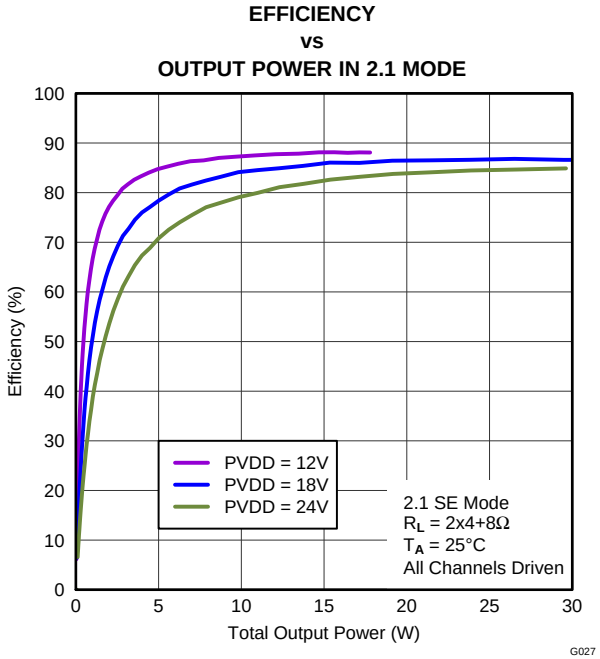
Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



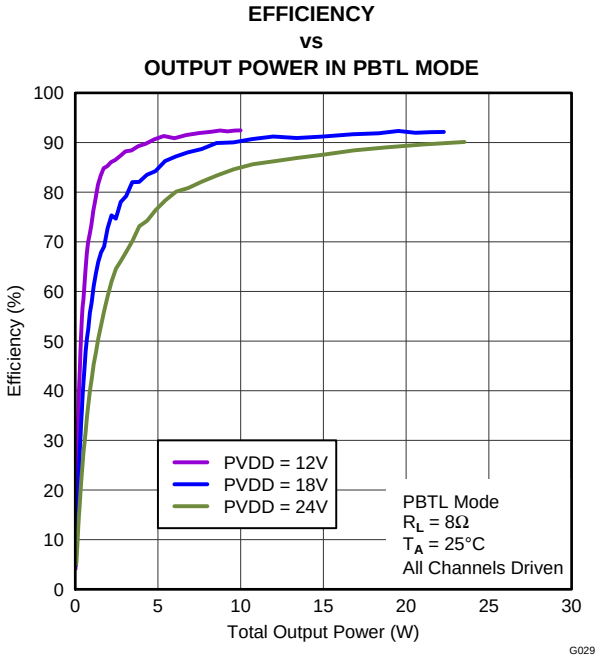
All channels driven

Figure 33.



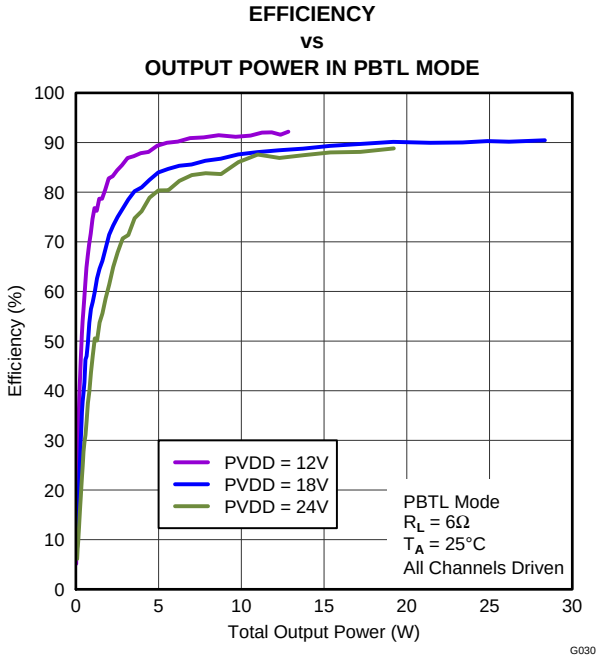
All channels driven

Figure 34.



All channels driven

Figure 35.



All channels driven

Figure 36.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

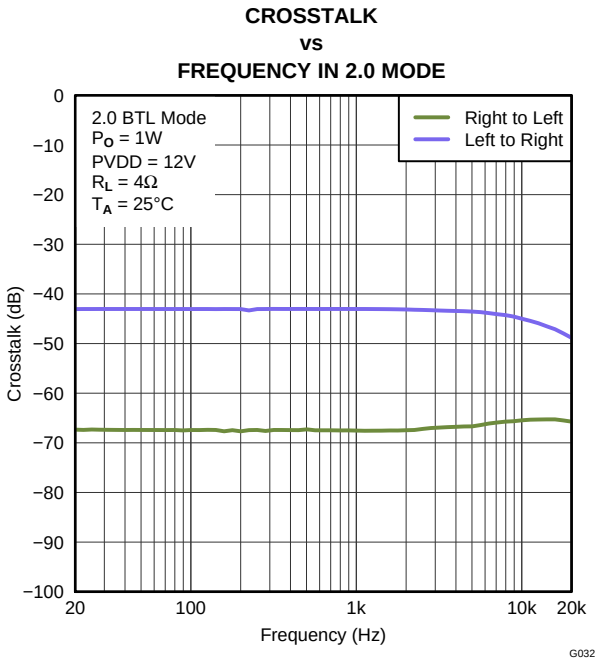


Figure 37.

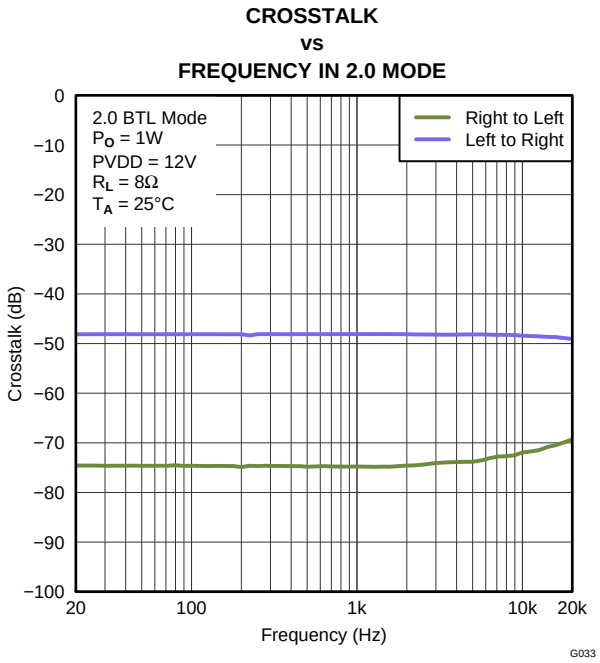


Figure 38.

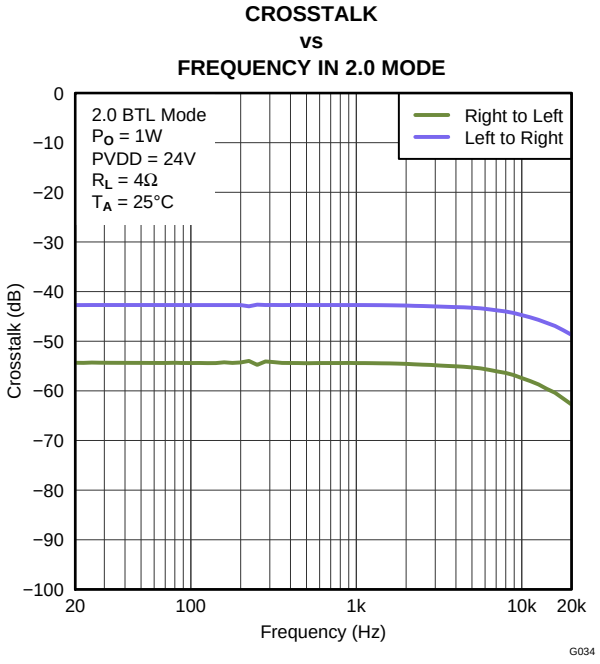


Figure 39.

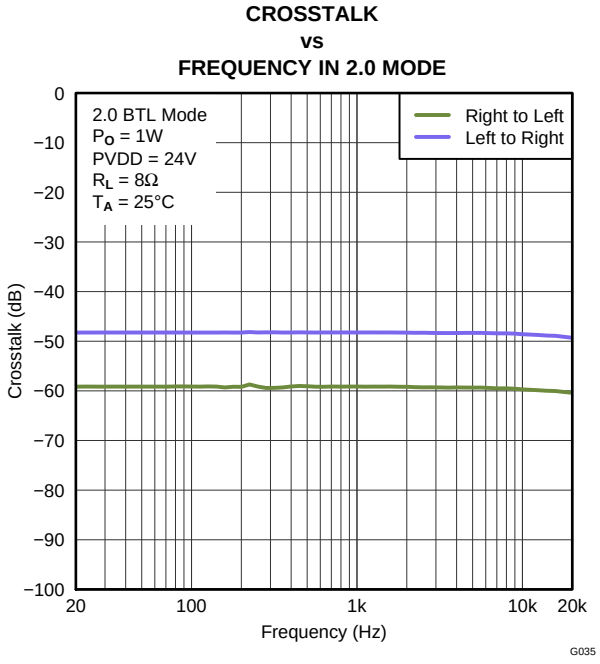


Figure 40.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

CROSSTALK vs FREQUENCY IN 2.1 MODE

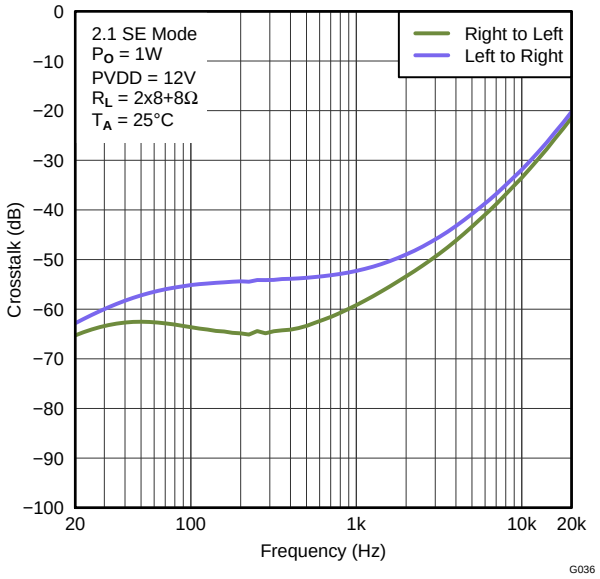


Figure 41.

CROSSTALK vs FREQUENCY IN 2.1 MODE

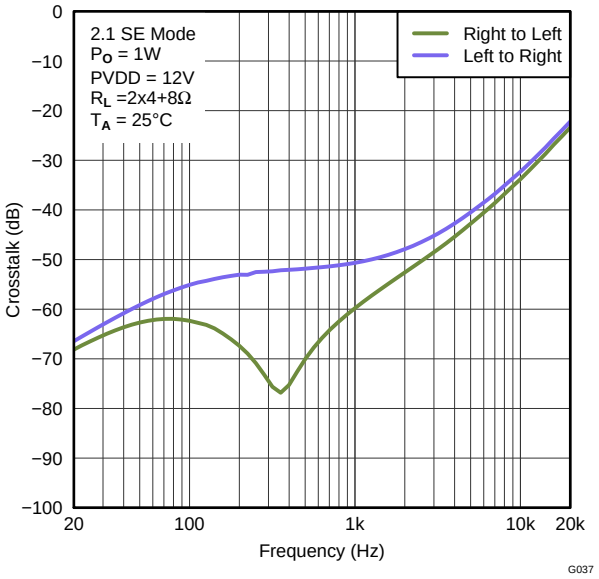


Figure 42.

CROSSTALK vs FREQUENCY IN 2.1 MODE

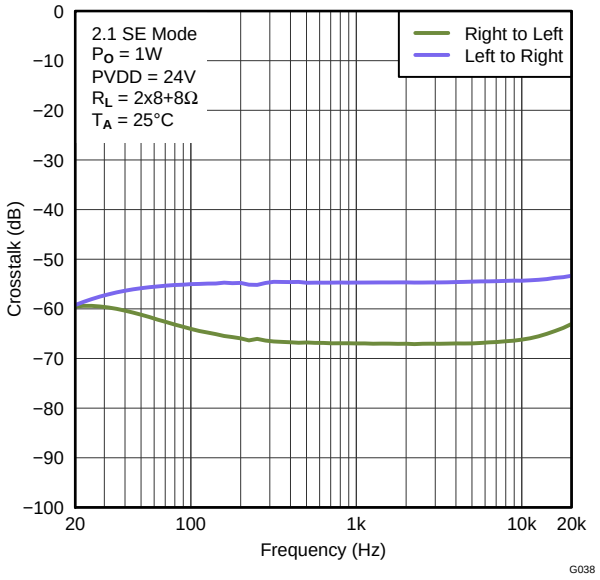


Figure 43.

CROSSTALK vs FREQUENCY IN 2.1 MODE

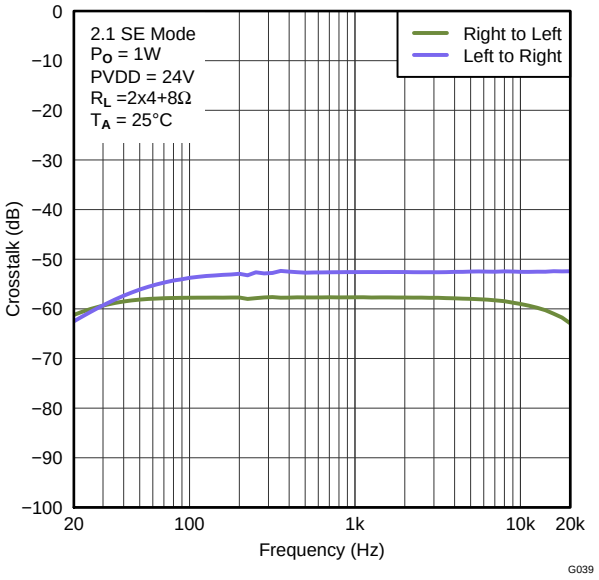


Figure 44.

HEADPHONE TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY HEADPHONE WITH DRVDD = 3.3 V

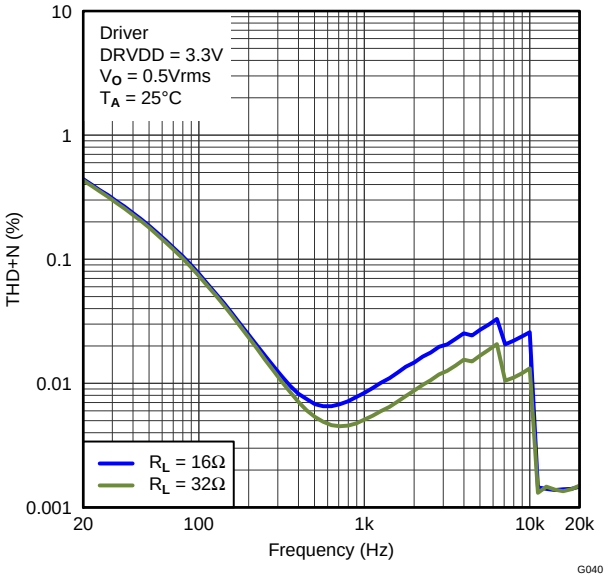


Figure 45.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY HEADPHONE WITH DRVDD = 3.3 V

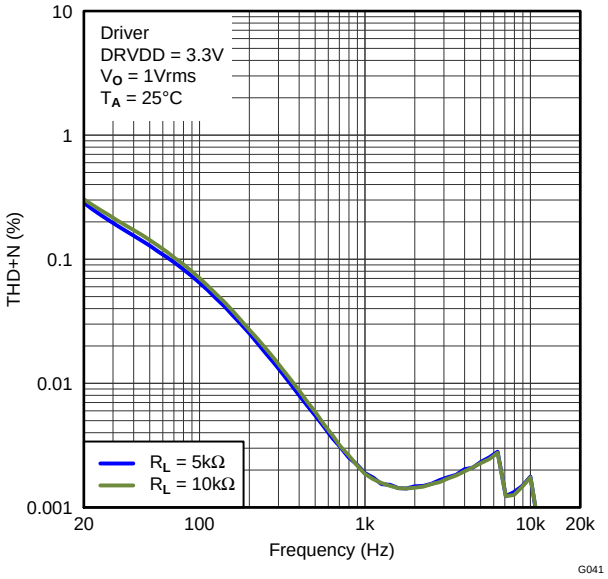


Figure 46.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER HEADPHONE WITH DRVDD = 3.3 V

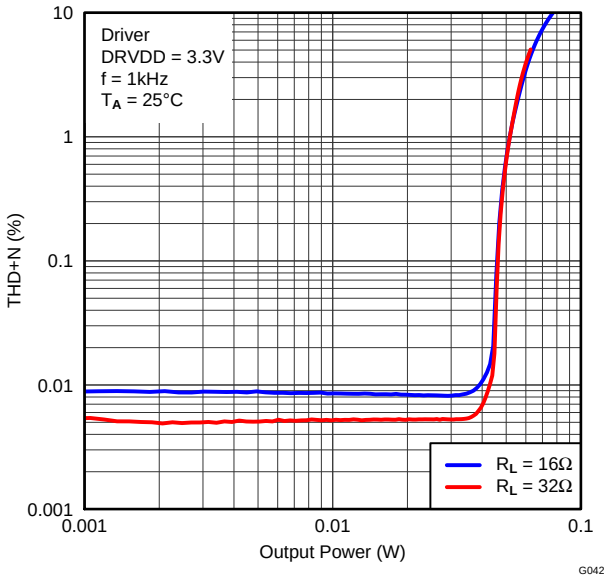


Figure 47.

LINE DRIVER TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE HEADPHONE WITH DRVDD = 3.3 V

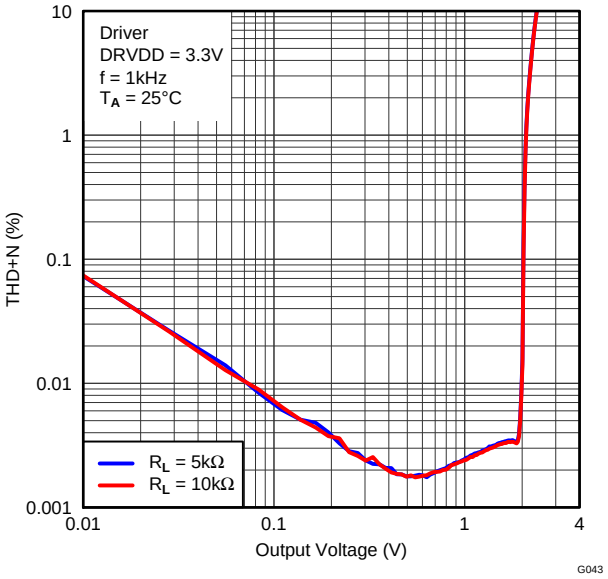


Figure 48.

CROSSTALK vs FREQUENCY HEADPHONE WITH DRVDD = 3.3 V

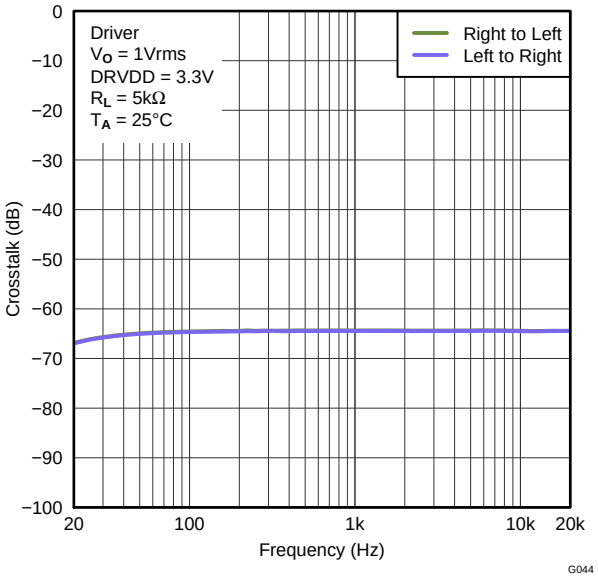


Figure 49.

CROSSTALK vs FREQUENCY HEADPHONE WITH DRVDD = 3.3 V

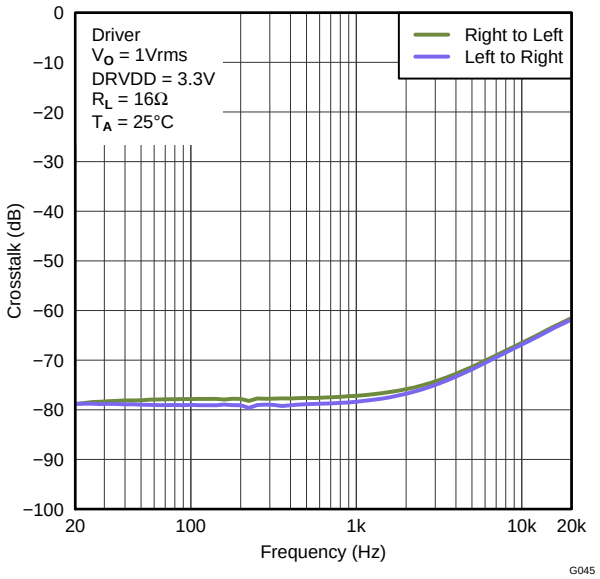


Figure 50.

CROSSTALK vs FREQUENCY HEADPHONE WITH DRVDD = 3.3 V

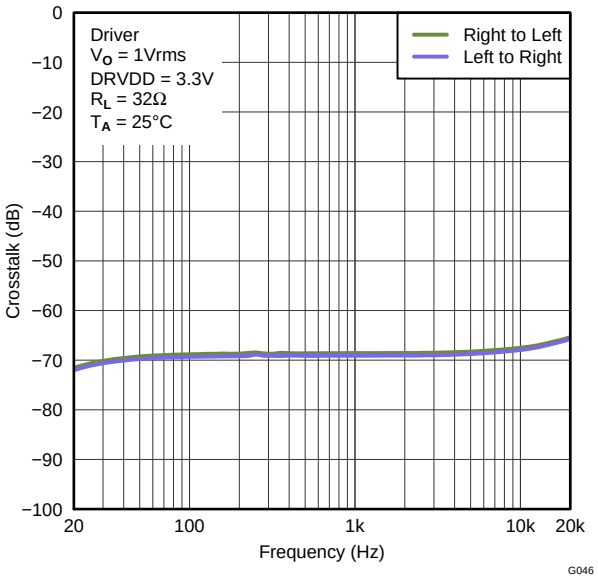


Figure 51.

Serial Control Interface Register Summary

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
			A u indicates unused bits.	
0x00	Clock control register	1	Description shown in subsequent section	0x6C
0x01	Device ID register	1	Description shown in subsequent section	0x00
0x02	Error status register	1	Description shown in subsequent section	0x00
0x03	System control register 1	1	Description shown in subsequent section	0xA0
0x04	Serial data interface register	1	Description shown in subsequent section	0x05
0x05	System control register 2	1	Description shown in subsequent section	0x40
0x06	Soft mute register	1	Description shown in subsequent section	0x00
0x07	Master volume	1	Description shown in subsequent section	0xFF (mute)
0x08	Channel 1 vol	1	Description shown in subsequent section	0x30 (0 dB)
0x09	Channel 2 vol	1	Description shown in subsequent section	0x30 (0 dB)
0x0A	Channel 3 vol	1	Description shown in subsequent section	0x30 (0 dB)
0x0B–0x0D		1	Reserved(1)	
0x0E	Volume configuration register	1	Description shown in subsequent section	0x91
0x0F		1	Reserved(1)	
0x10	Modulation limit register	1	Description shown in subsequent section	0x02
0x11	IC delay channel 1	1	Description shown in subsequent section	0xAC
0x12	IC delay channel 2	1	Description shown in subsequent section	0x54
0x13	IC delay channel 3	1	Description shown in subsequent section	0xAC
0x14	IC delay channel 4	1	Description shown in subsequent section	0x54
0x15–0x18		1	Reserved(1)	
0x19	PWM channel shutdown group register	1	Description shown in subsequent section	0x30
0x1A	Start/stop period register	1	Description shown in subsequent section	0x0F
0x1B	Oscillator trim register	1	Description shown in subsequent section	0x82
0x1C	BKND_ERR register	1	Description shown in subsequent section	0x02
0x1D–0x1F		1	Reserved(1)	
0x20	Input MUX register	4	Description shown in subsequent section	0x0001 7772
0x21	Ch 4 source select register	4	Description shown in subsequent section	0x0000 4303
0x22–0x24		4	Reserved(1)	
0x25	PWM MUX register	4	Description shown in subsequent section	0x0102 1345
0x26–0x28		4	Reserved(1)	
0x29	ch1_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2A	ch1_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

(1) Reserved registers should not be accessed.

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x2B	ch1_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2C	ch1_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2D	ch1_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2E	ch1_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2F	ch1_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x30	ch2_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x31	ch2_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x32	ch2_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x33	ch2_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x34	ch2_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x35	ch2_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x36	ch2_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x37–0x39		4	Reserved (2)	
0x3A	DRC1 ae (3)	8	u[31:26], ae[25:0]	0x0080 0000
	DRC1 (1 – ae)		u[31:26], (1 – ae)[25:0]	0x0000 0000
0x3B	DRC1 aa	8	u[31:26], aa[25:0]	0x0080 0000
	DRC1 (1 – aa)		u[31:26], (1 – aa)[25:0]	0x0000 0000
0x3C	DRC1 ad	8	u[31:26], ad[25:0]	0x0080 0000
	DRC1 (1 – ad)		u[31:26], (1 – ad)[25:0]	0x0000 0000
0x3D	DRC2 ae	8	u[31:26], ae[25:0]	0x0080 0000
	DRC 2 (1 – ae)		u[31:26], (1 – ae)[25:0]	0x0000 0000
0x3E	DRC2 aa	8	u[31:26], aa[25:0]	0x0080 0000
	DRC2 (1 – aa)		u[31:26], (1 – aa)[25:0]	0x0000 0000
0x3F	DRC2 ad	8	u[31:26], ad[25:0]	0x0080 0000
	DRC2 (1 – ad)		u[31:26], (1 – ad)[25:0]	0x0000 0000
0x40	DRC1-T	4	T1[31:0] (9.23 format)	0xFDA2 1490
0x41	DRC1-K	4	u[31:26], K1[25:0]	0x0384 2109
0x42	DRC1-O	4	u[31:26], O1[25:0]	0x0008 4210
0x43	DRC2-T	4	T2[31:0] (9.23 format)	0xFDA2 1490
0x44	DRC2-K	4	u[31:26], K2[25:0]	0x0384 2109
0x45	DRC2-O	4	u[31:26], O2[25:0]	0x0008 4210
0x46	DRC control	4	Description shown in subsequent section	0x0000 0000
0x47–0x4F		4	Reserved (2)	
0x50	Bank switch control	4	Description shown in subsequent section	0x0F70 8000
0x51	Ch 1 output mixer	12	Ch 1 output mix1[2]	0x0080 0000
			Ch 1 output mix1[1]	0x0000 0000
			Ch 1 output mix1[0]	0x0000 0000
0x52	Ch 2 output mixer	12	Ch 2 output mix2[2]	0x0080 0000
			Ch 2 output mix2[1]	0x0000 0000
			Ch 2 output mix2[0]	0x0000 0000

(2) Reserved registers should not be accessed.
(3) ae stands for ∝ of energy filter, aa stands for ∝ of attack filter and ad stands for ∝ of decay filter and 1- ∝ = ω.

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x53	Ch 1 input mixer	16	Ch 1 input mixer[3]	0x0080 0000
			Ch 1 input mixer[2]	0x0000 0000
			Ch 1 input mixer[1]	0x0000 0000
			Ch 1 input mixer[0]	0x0080 0000
0x54	Ch 2 input mixer	16	Ch 2 input mixer[3]	0x0080 0000
			Ch 2 input mixer[2]	0x0000 0000
			Ch 2 input mixer[1]	0x0000 0000
			Ch 2 input mixer[0]	0x0080 0000
0x55	Channel 3 input mixer	12	Channel 3 input mixer [2]	0x0080 0000
			Channel 3 input mixer [1]	0x0000 0000
			Channel 3 input mixer [0]	0x0000 0000
0x56	Output post-scale	4	u[31:26], post[25:0]	0x0080 0000
0x57	Output pre-scale	4	u[31:26], pre[25:0] (9.17 format)	0x0002 0000
0x58	ch1 BQ[7]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x59	ch1 BQ[8]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5A	Subchannel BQ[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5B	Subchannel BQ[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5C	ch2 BQ[7]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5D	ch2 BQ[8]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5E	pseudo_ch2 BQ[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x5F		4	Reserved(4)	
0x60	Channel 4 (subchannel) output mixer	8	Ch 4 output mixer[1]	0x0000 0000
			Ch 4 output mixer[0]	0x0080 0000
0x61	Channel 4 (subchannel) input mixer	8	Ch 4 input mixer[1]	0x0040 0000
			Ch 4 input mixer[0]	0x0040 0000
0x62	IDF post scale	4	Post-IDF attenuation register	0x0000 0080
0x63–0xF7			Reserved(4)	0x0000 0000
0xF8	Device address enable register	4	Write F9 A5 A5 A5 in this register to enable write to device address update (0xF9)	0x0000 0000
0xF9	Device address Update Register	4	u[31:8], New Dev Id[7:1] , ZERO[0] (New Dev Id (7:1) defines the new device address	0X0000 0036
0xFA–0xFF		4	Reserved(4)	0x0000 0000

(4) Reserved registers should not be accessed.

All DAP coefficients are 3.23 format unless specified otherwise.

DETAILED REGISTER DESCRIPTIONS

CLOCK CONTROL REGISTER (0x00)

The clocks and data rates are automatically determined by the TAS5721. The clock control register contains the auto-detected clock status. Bits D7–D5 reflect the sample rate. Bits D4–D2 reflect the MCLK frequency. The device accepts a 64 f_S or 32 f_S SCLK rate for all MCLK ratios, but accepts a 48 f_S SCLK rate for MCLK ratios of 192 f_S and 384 f_S only.

Table 1. Clock Control Register (0x00)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	–	–	–	–	–	f_S = 32-kHz sample rate
0	0	1	–	–	–	–	–	Reserved(1)
0	1	0	–	–	–	–	–	Reserved(1)
0	**1**	**1**	**–**	**–**	**–**	–	**–**	**f_S = 44.1/48-kHz sample rate (2)**
1	0	0	–	–	–	–	–	fs = 16-kHz sample rate
1	0	1	–	–	–	–	–	fs = 22.05/24-kHz sample rate
1	1	0	–	–	–	–	–	fs = 8-kHz sample rate
1	1	1	–	–	–	–	–	fs = 11.025/12-kHz sample rate
–	–	–	0	0	0	–	–	MCLK frequency = 64 × f_S (3)
–	–	–	0	0	1	–	–	MCLK frequency = 128 × f_S (3)
–	–	–	0	1	0	–	–	MCLK frequency = 192 × f_S (4)
–	**–**	**–**	**0**	**1**	**1**	**–**	**–**	**MCLK frequency = 256 × f_S** (2) (5)
–	–	–	1	0	0	–	–	MCLK frequency = 384 × f_S
–	–	–	1	0	1	–	–	MCLK frequency = 512 × f_S
–	–	–	1	1	0	–	–	Reserved(1)
–	–	–	1	1	1	–	–	Reserved(1)
–	–	–	–	–	–	**0**	–	**Reserved(1)** (2)
–	**–**	**–**	–	**–**	**–**	**–**	**0**	**Reserved**(1) (2)

(1) Reserved registers should not be accessed.
(2) Default values are in **bold**.
(3) Only available for 44.1-kHz and 48-kHz rates.
(4) Rate only available for 32/44.1/48-kHz sample rates
(5) Not available at 8 kHz

DEVICE ID REGISTER (0x01)

The device ID register contains the ID code for the firmware revision

Table 2. Device ID Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	Identification code

ERROR STATUS REGISTER (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.

Error Definitions:

- MCLK Error : MCLK frequency is changing. The number of MCLKs per LRCLK is changing.
- SCLK Error: The number of SCLKs per LRCLK is changing.
- LRCLK Error: LRCLK frequency is changing.
- Frame Slip: LRCLK phase is drifting with respect to internal frame sync.

Table 3. Error Status Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	-	–	–	–	–	–	–	MCLK error
–	1	–	–	–	–	–	–	PLL autolock error
–	–	1	–	–	–	–	–	SCLK error
–	–	–	1	–	–	–	–	LRCLK error
–	–	–	–	1	–	–	–	Frame slip
–	–	–	–	–	1	–	–	Clip indicator
–	–	–	–	–	–	1	–	Overcurrent, overtemperature, overvoltage or undervoltage errors
–	–	–	–	–	–	–	**0**	**Reserved**
0	**0**	**0**	**0**	**0**	**0**	**0**	–	**No errors** (1)

(1) Default values are in **bold**.

SYSTEM CONTROL REGISTER 1 (0x03)

The system control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.
If 1, the dc-blocking filter (–3 dB cutoff < 1 Hz) for each channel is enabled (default).

Bit D5: If 0, use soft unmute on recovery from clock error. This is a slow recovery. Unmute takes the same time as the volume ramp defined in register 0x0E.
If 1, use hard unmute on recovery from clock error (default). This is a fast recovery, a single step volume ramp

Bits D1–D0: Select de-emphasis

Table 4. System Control Register 1 (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	PWM high-pass (dc blocking) disabled
1	–	–	–	–	–	–	–	**PWM high-pass (dc blocking) enabled** (1)
–	**0**	–	–	–	–	–	–	**Reserved** (1)
–	–	0	–	–	–	–	–	Soft unmute on recovery from clock error
–	–	**1**	–	–	–	–	–	**Hard unmute on recovery from clock error** (1)
–	–	–	**0**	–	–	–	–	**Reserved** (1)
–	–	–	–	**0**	–	–	–	**Reserved** (1)
–	–	–	–	–	**0**	–	–	**Reserved**(1)
–	–	–	–	–	–	**0**	**0**	**No de-emphasis** (1)
–	–	–	–	–	–	0	1	De-emphasis for f_S = 32 kHz
–	–	–	–	–	–	1	0	De-emphasis for f_S = 44.1 kHz
–	–	–	–	–	–	1	1	De-emphasis for f_S = 48 kHz

(1) Default values are in **bold**.

SERIAL DATA INTERFACE REGISTER (0x04)

As shown in Table 5, the TAS5721 supports nine serial data modes. The default is 24-bit, I^2S mode,

Table 5. Serial Data Interface Control Register (0x04) Format

RECEIVE SERIAL DATA INTERFACE FORMAT	WORD LENGTH	D7–D4	D3	D2	D1	D0
Right-justified	16	0000	0	0	0	0
Right-justified	20	0000	0	0	0	1
Right-justified	24	0000	0	0	1	0
I^2S	16	000	0	0	1	1
I^2S	20	0000	0	1	0	0
I^2S (1)	**24**	**0000**	**0**	**1**	**0**	**1**
Left-justified	16	0000	0	1	1	0
Left-justified	20	0000	0	1	1	1
Left-justified	24	0000	1	0	0	0
Reserved		0000	1	0	0	1
Reserved		0000	1	0	1	0
Reserved		0000	1	0	1	1
Reserved		0000	1	1	0	0
Reserved		0000	1	1	0	1
Reserved		0000	1	1	1	0
Reserved		0000	1	1	1	1

(1) Default values are in **bold**.

SYSTEM CONTROL REGISTER 2 (0x05)

When bit D6 is set low, the system exits all channel shutdown and starts playing audio; otherwise, the outputs are shut down (hard mute).

Table 6. System Control Register 2 (0x05)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Mid-Z ramp disabled** (1)
1	–	–	–	–	–	–	–	Mid-Z ramp enabled
–	0	–	–	–	–	–	–	Exit all-channel shutdown (normal operation)
–	**1**	–	–	–	–	–	–	**Enter all-channel shutdown (hard mute)(1)**
–	–	–	–	–	**0**	–	–	**2.0 mode [2.0 BTL]** (1)
–	–	–	–	–	1	–	–	2.1 mode [2 SE + 1 BTL]
–	–	–	–	–	–	**0**	–	**ADR/$\overline{\text{FAULT}}$ pin is configured as to serve as an address input only(1)**
–	–	–	–	–	–	1	–	ADR/$\overline{\text{FAULT}}$ pin is configured as fault output
–	–	**0**	**0**	**0**	**–**	**–**	**0**	**Reserved (1)**

(1) Default values are in **bold**.

SOFT MUTE REGISTER (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

Table 7. Soft Mute Register (0x06)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	–	–	–	**Reserved** (1)
–	–	–	–	–	**0**	–	–	**Soft unmute channel 3** (1)
–	–	–	–	–	1	–	–	Soft mute channel 3
–	–	–	–	–	–	**0**	–	**Soft unmute channel 2** (1)
–	–	–	–	–	–	1	–	Soft mute channel 2
–	–	–	–	–	–	–	**0**	**Soft unmute channel 1** (1)
–	–	–	–	–	–	–	1	Soft mute channel 1

(1) Default values are in **bold**.

VOLUME REGISTERS (0x07, 0x08, 0x09, 0x0A)

Step size is 0.5 dB

Master volume	– 0x07 (default is mute)
Channel-1 volume	– 0x08 (default is 0 dB)
Channel-2 volume	– 0x09 (default is 0 dB)
Channel-3 volume	– 0x0A (default is 0 dB)

Table 8. Volume Registers (0x07, 0x08, 0x09, 0x0A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	24 dB
0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0 dB (default for individual channel volume) (1)**
1	1	1	1	1	1	1	0	–103 dB
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**Soft mute (default for the master volume)(1)**

(1) Default values are in **bold**.

VOLUME CONFIGURATION REGISTER (0x0E)

Bits D2–D0: Volume slew rate (Used to control volume change and MUTE ramp rates). These bits control the number of steps in a volume ramp. Volume steps occur at a rate that depends on the sample rate of the I^2S data as follows:

Sample Rate (KHz)	Approximate Ramp Rate
8/16/32	125 us/step
11.025/22.05/44.1	90.7 us/step
12/24/48	83.3 us/step

Table 9. Volume Control Register (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	**–**	**–**	**1**	**0**	–	–	–	**Reserved (1)**
–	**0**	–	–	–	–	–	–	**Subchannel (ch4) volume = ch1 volume(2)(1)**
–	1	–	–	–	–	–	–	Subchannel volume = register 0x0A(2)
–	–	**0**	–	–	–	–	–	**Ch3 volume = ch2 volume(1)**
–	–	1	–	–	–	–	–	Ch3 volume = register 0x0A
–	–	–	–	–	0	0	0	Volume slew 512 steps (43-ms volume ramp time at 48 kHz)
–	–	–	–	–	**0**	**0**	**1**	**Volume slew 1024 steps (85-ms volume ramp time at 48 kHz) (1)**
–	–	–	–	–	0	1	0	Volume slew 2048 steps (171- ms volume ramp time at 48 kHz)
–	–	–	–	–	0	1	1	Volume slew 256 steps (21-ms volume ramp time at 48 kHz)
–	–	–	–	–	1	X	X	Reserved

(1) Default values are in **bold**.
(2) Bits 6:5 can be changed only when volume is in MUTE [master volume = MUTE (register 0x07 = 0xFF)].

MODULATION LIMIT REGISTER (0x10)

The modulation limit is the maximum duty cycle of the PWM output waveform. It is important to note that for any applications with PVDD greater than 18 V, the maximum modulation index must be set to 93.8%.

Table 10. Modulation Limit Register (0x10)

D7	D6	D5	D4	D3	D2	D1	D0	MODULATION LIMIT
–	–	–	–	–	0	0	0	99.2%
–	–	–	–	–	0	0	1	98.4%
–	–	–	–	–	**0**	**1**	**0**	**97.7%** (1)
–	–	–	–	–	0	1	1	96.9%
–	–	–	–	–	1	0	0	96.1%
–	–	–	–	–	1	0	1	95.3%
–	–	–	–	–	1	1	0	94.5%
–	–	–	–	–	1	1	1	93.8%
0	**0**	**0**	**0**	**0**	–	–	–	**RESERVED**

(1) Default values are in **bold**.

INTERCHANNEL DELAY REGISTERS (0x11, 0x12, 0x13, and 0x14)

Internal PWM channels 1, 2, $\overline{1}$, and $\overline{2}$ are mapped into registers 0x11, 0x12, 0x13, and 0x14.

Table 11. Channel Interchannel Delay Register Format

SUBADDRESS	D7	D6	D5	D4	D3	D2	D1	D0	Delay = (value) × 4 DCLKs
0x11	**1**	**0**	**1**	**0**	**1**	**1**	–	–	**Default value for channel 1** (1)
0x12	**0**	**1**	**0**	**1**	**0**	**1**	–	–	**Default value for channel 2** (1)
0x13	**1**	**0**	**1**	**0**	**1**	**1**	–	–	**Default value for $\overline{\text{channel 1}}$** (1)
0x14	**0**	**1**	**0**	**1**	**0**	**1**	–	–	**Default value for $\overline{\text{channel 2}}$** (1)
RANGE OF VALUES FOR 0x11 - 0x14									
	0	0	0	0	0	0	–	–	Minimum absolute delay, 0 DCLK cycles
	0	1	1	1	1	1	–	–	Maximum positive delay, 31 × 4 DCLK cycles
	1	0	0	0	0	0	–	–	Maximum negative delay, –32 × 4 DCLK cycles
							0	**0**	**RESERVED**

(1) Default values are in **bold**.

The ICD settings have high impact on audio performance (for example, dynamic range, THD+N, crosstalk, and so forth). Therefore, appropriate ICD settings must be used. By default, the device has ICD settings for AD mode. If used in BD mode, then update these registers before coming out of all-channel shutdown.

REGISTER	AD MODE	BD MODE
0x11	AC	B8
0x12	54	60
0x13	AC	A0
0x14	54	48

PWM SHUTDOWN GROUP REGISTER (0x19)

Settings of this register determine which PWM channels are active. The value should be 0x30 for BTL mode and 0x3A for PBTL mode. The default value of this register is 0x30. The functionality of this register is tied to the state of bit D6 in the system control register.

This register defines which channels belong to the shutdown group (SDG). If a 1 is set in the shutdown group register, that particular channel is **not** started following an exit *out of all-channel shutdown* command (if bit D6 is set to 0 in system control register 2, 0x05).

Table 12. Shutdown Group Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Reserved** (1)
–	**0**	–	–	–	–	–	–	**Reserved** (1)
–	–	**1**	–	–	–	–	–	**Reserved** (1)
–	–	–	**1**	–	–	–	–	**Reserved** (1)
–	–	–	–	**0**	–	–	–	**PWM channel 4 does not belong to shutdown group.** (1)
–	–	–	–	1	–	–	–	PWM channel 4 belongs to shutdown group.
–	–	–	–	–	**0**	–	–	**PWM channel 3 does not belong to shutdown group.** (1)
–	–	–	–	–	1	–	–	PWM channel 3 belongs to shutdown group.
–	–	–	–	–	–	**0**	–	**PWM channel 2 does not belong to shutdown group.** (1)
–	–	–	–	–	–	1	–	PWM channel 2 belongs to shutdown group.
–	–	–	–	–	–	–	**0**	**PWM channel 1 does not belong to shutdown group.** (1)
–	–	–	–	–	–	–	1	PWM channel 1 belongs to shutdown group.

(1) Default values are in **bold**.

START/STOP PERIOD REGISTER (0x1A)

This register is used to control the soft-start and soft-stop period following an enter/exit all channel shut down command or change in the $\overline{PDN}$ state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and I^2S clock stability.

Table 13. Start/Stop Period Register (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**–**	**–**	–	–	–	–	–	**SSTIMER enabled**(1)
1	–	–	–	–	–	–	–	SSTIMER disabled
–	**0**	**0**	–	–	–	–	–	**Reserved** (1)
–	–	–	0	0	–	–	–	No 50% duty cycle start/stop period
–	–	–	0	1	0	0	0	16.5-ms 50% duty cycle start/stop period
–	–	–	0	1	0	0	1	23.9-ms 50% duty cycle start/stop period
–	–	–	0	1	0	1	0	31.4-ms 50% duty cycle start/stop period
–	–	–	0	1	0	1	1	40.4-ms 50% duty cycle start/stop period
–	–	–	0	1	1	0	0	53.9-ms 50% duty cycle start/stop period
–	–	–	0	1	1	0	1	70.3-ms 50% duty cycle start/stop period
–	–	–	0	1	1	1	0	94.2-ms 50% duty cycle start/stop period
–	–	–	**0**	**1**	**1**	**1**	**1**	**125.7-ms 50% duty cycle start/stop period**(1)
–	–	–	1	0	0	0	0	164.6-ms 50% duty cycle start/stop period
–	–	–	1	0	0	0	1	239.4-ms 50% duty cycle start/stop period
–	–	–	1	0	0	1	0	314.2-ms 50% duty cycle start/stop period
–	–	–	1	0	0	1	1	403.9-ms 50% duty cycle start/stop period
–	–	–	1	0	1	0	0	538.6-ms 50% duty cycle start/stop period
–	–	–	1	0	1	0	1	703.1-ms 50% duty cycle start/stop period
–	–	–	1	0	1	1	0	942.5-ms 50% duty cycle start/stop period
–	–	–	1	0	1	1	1	1256.6-ms 50% duty cycle start/stop period
–	–	–	1	1	0	0	0	1728.1-ms 50% duty cycle start/stop period
–	–	–	1	1	0	0	1	2513.6-ms 50% duty cycle start/stop period
–	–	–	1	1	0	1	0	3299.1-ms 50% duty cycle start/stop period
–	–	–	1	1	0	1	1	4241.7-ms 50% duty cycle start/stop period
–	–	–	1	1	1	0	0	5655.6-ms 50% duty cycle start/stop period
–	–	–	1	1	1	0	1	7383.7-ms 50% duty cycle start/stop period
–	–	–	1	1	1	1	0	9897.3-ms 50% duty cycle start/stop period
–	–	–	1	1	1	1	1	13,196.4-ms 50% duty cycle start/stop period

(1) Default values are in **bold**.

OSCILLATOR TRIM REGISTER (0x1B)

The TAS5721 PWM processor contains an internal oscillator to support autodetect of I^2S clock rates. This reduces system cost because an external reference is not required. TI recommends a reference resistor value of that shown in the Typical Application Circuit Diagrams. The circuit that uses this resistor should be calibrated or trimmed after each time the device is reset.

Writing 0x00 to register 0x1B enables the trim that was programmed at the factory. It is important to note that after writing the value 0x00 to the trim register, the register will repor the value 0xC0, to indicate the trim process is complete.

Table 14. Oscillator Trim Register (0x1B)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	**Reserved** (1)
–	**0**	–	–	–	–	–	–	**Oscillator trim not done (read-only)** (1)
–	1	–	–	–	–	–	–	Oscillator trim done (read only)
–	–	**0**	**0**	**0**	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	0	–	Select factory trim (Write a 0 to select factory trim; default is 1.)
–	–	–	–	–	–	**1**	–	**Factory trim disabled** (1)
–	–	–	–	–	–	–	**0**	**Reserved** (1)

(1) Default values are in **bold**.

BKND_ERR REGISTER (0x1C)

When a backend error signal is received from the internal power stage, the power stage is reset stopping all PWM activity. Subsequently, the modulator waits approximately for the time listed in Table 15 before attempting to restart the power stage.

Table 15. BKND_ERR Register (0x1C)(1)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	X	Reserved
–	–	–	–	**0**	**0**	**1**	**0**	**Set back-end reset period to 299 ms** (2)
–	–	–	–	0	0	1	1	Set back-end reset period to 449 ms
–	–	–	–	0	1	0	0	Set back-end reset period to 598 ms
–	–	–	–	0	1	0	1	Set back-end reset period to 748 ms
–	–	–	–	0	1	1	0	Set back-end reset period to 898 ms
–	–	–	–	0	1	1	1	Set back-end reset period to 1047 ms
–	–	–	–	1	0	0	0	Set back-end reset period to 1197 ms
–	–	–	–	1	0	0	1	Set back-end reset period to 1346 ms
–	–	–	–	1	0	1	X	Set back-end reset period to 1496 ms
–	–	–	–	1	1	X	X	

(1) This register can be written only with a non-reserved value. Also this register can be only be written once after the device is reset. If a different value is desired, the device must be reset before changing 0x1C again.
(2) Default values are in **bold**.

INPUT MULTIPLEXER REGISTER (0x20)

This register controls the modulation scheme (AD or BD mode) as well as the routing of I^2S audio to the internal channels.

Table 16. Input Multiplexer Register (0x20)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	-	-	-	**Reserved (1)**
					0			**Polarity of Ch3 is not inverted**
					1			Polarity of Ch3 is inverted
						0		**Polarity of Ch2 is not inverted**
						1		Polarity of Ch2 is inverted
							0	**Polarity of Ch1 is not inverted**
							1	Polarity of Ch1 is inverted
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	–	–	–	–	–	–	–	**Channel-1 AD mode (1)**
1	–	–	–	–	–	–	–	Channel-1 BD mode
–	**0**	**0**	**0**	–	–	–	–	**SDIN-L to channel 1 (1)**
–	0	0	1	–	–	–	–	SDIN-R to channel 1
–	0	1	0	–	–	–	–	Reserved
–	0	1	1	–	–	–	–	Reserved
–	1	0	0	–	–	–	–	Reserved
–	1	0	1	–	–	–	–	Reserved
–	1	1	0	–	–	–	–	Ground (0) to channel 1
–	1	1	1	–	–	–	–	Reserved
–	–	–	–	**0**	–	–	–	**Channel 2 AD mode (1)**
–	–	–	–	1	–	–	–	Channel 2 BD mode
–	–	–	–	–	0	0	0	SDIN-L to channel 2
–	–	–	–	–	**0**	**0**	**1**	**SDIN-R to channel 2 (1)**
–	–	–	–	–	0	1	0	Reserved
–	–	–	–	–	0	1	1	Reserved
–	–	–	–	–	1	0	0	Reserved
–	–	–	–	–	1	0	1	Reserved
–	–	–	–	–	1	1	0	Ground (0) to channel 2
–	–	–	–	–	1	1	1	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**Reserved (1)**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
				0				Sub channel in 2.1 mode, AD modulation
				1				Sub channel in 2.1 mode, BD modulation
0	**1**	**1**	**1**	**-**	**0**	**1**	**0**	**Reserved (1)**

(1) Default values are in **bold**.

CHANNEL 4 SOURCE SELECT REGISTER (0x21)

This register selects the channel 4 source.

Table 17. Subchannel Control Register (0x21)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**1**	**0**	**0**	**0**	**0**	**1**		**Reserved** (1)
–	–	–	–	–	–	**–**	0	(L + R)/2
–	–	–	–	–	–	–	**1**	**Left-channel post-BQ** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Reserved** (1)

(1) Default values are in **bold**.

PWM OUTPUT MUX REGISTER (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21–D20: Selects which PWM channel is output to OUT_A

Bits D17–D16: Selects which PWM channel is output to OUT_B

Bits D13–D12: Selects which PWM channel is output to OUT_C

Bits D09–D08: Selects which PWM channel is output to OUT_D

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 4 = 0x03. **See for details.**

Table 18. PWM Output Mux Register (0x25)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**Reserved**(1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	–	–	–	–	–	–	**Reserved**(1)
–	**–**	**0**	**0**	–	–	–	–	**Multiplex PWM 1 to OUT_A** (1)
–	–	0	1	–	–	–	–	Multiplex PWM 2 to OUT_A
–	–	1	0	–	–	–	–	Multiplex PWM 3 to OUT_A
–	–	1	1	–	–	–	–	Multiplex PWM 4 to OUT_A
–	–	–	–	**0**	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	0	0	Multiplex PWM 1 to OUT_B
–	–	–	–	–	–	0	1	Multiplex PWM 2 to OUT_B
–	–	–	–	–	–	**1**	**0**	**Multiplex PWM 3 to OUT_B** (1)
–	–	–	–	–	–	1	1	Multiplex PWM 4 to OUT_B
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	–	–	–	–	–	–	**Reserved** (1)
–	–	0	0	–	–	–	–	Multiplex PWM 1 to OUT_C
–	–	**0**	**1**	–	–	–	–	**Multiplex PWM 2 to OUT_C**(1)

(1) Default values are in **bold**.

Table 18. PWM Output Mux Register (0x25) (continued)

–	–	1	0	–	–	–	–	Multiplex PWM 3 to OUT_C
–	–	1	1	–	–	–	–	Multiplex PWM 4 to OUT_C
–	–	–	–	**0**	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	0	0	Multiplex PWM 1 to OUT_D
–	–	–	–	–	–	0	1	Multiplex PWM 2 to OUT_D
–	–	–	–	–	–	1	0	Multiplex PWM 3 to OUT_D
–	–	–	–	–	–	**1**	**1**	**Multiplex PWM 4 to OUT_D** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**Reserved**(1)

DRC CONTROL (0x46)

Each DRC can be enabled independently using the DRC control register. The DRCs are disabled by default.

Table 19. DRC Control Register

D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved** (1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**0**	**–**	**–**	–	–	–	–	**Reserved** (1)
–	–	**0**	–	–	–	–	–	**Disable complementary (1–H) low-pass filter generation** (1)
–	–	1	–	–	–	–	–	Enable complementary (1–H) low-pass filter generation
–	–	–	**0**	–	–	–	–	
–	–	–	1	–	–	–	–	
				0	**0**			**Reserved** (1)
–	–	–	–	–	–	**0**	–	**DRC2 turned OFF** (1)
–	–	–	–	–	–	1	–	DRC2 turned ON
–	–	–	–	–	–	–	**0**	**DRC1 turned OFF** (1)
–	–	–	–	–	–	–	1	DRC1 turned ON

(1) Default values are in **bold**.

BANK SWITCH AND EQ CONTROL (0x50)

The bank switching feature is described in detail in section BANK SWITCHING.

Table 20. Bank Switching Command

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	–	–	–	–	–	–	–	**32 kHz, does not use bank 3 (1)**
1	–	–	–	–	–	–	–	32 kHz, uses bank 3
–	**0**	–	–	–	–	–	–	**Reserved(1)**
–	–	**0**	–	–	–	–	–	**Reserved(1)**
–	–	–	**0**	–	–	–	–	**44.1/48 kHz, does not use bank 3 (1)**
–	–	–	1	–	–	–	–	44.1/48 kHz, uses bank 3
–	–	–	–	0	–	–	–	16 kHz, does not use bank 3
–	–	–	–	**1**	–	–	–	**16 kHz, uses bank 3 (1)**
–	–	–	–	–	0	–	–	22.025/24 kHz, does not use bank 3
–	–	–	–	–	**1**	–	–	**22.025/24 kHz, uses bank 3 (1)**
–	–	–	–	–	–	0	–	8 kHz, does not use bank 3
–	–	–	–	–	–	**1**	–	**8 kHz, uses bank 3 (1)**
–	–	–	–	–	–	–	0	11.025 kHz/12, does not use bank 3
–	–	–	–	–	–	–	**1**	**11.025/12 kHz, uses bank 3 (1)**

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
0	–	–	–	–	–	–	–	**32 kHz, does not use bank 2 (1)**
1	–	–	–	–	–	–	–	32 kHz, uses bank 2
–	**1**	–	–	–	–	–	–	**Reserved (1)**
–	–	**1**	–	–	–	–	–	**Reserved (1)**
–	–	–	0	–	–	–	–	44.1/48 kHz, does not use bank 2
–	–	–	**1**	–	–	–	–	**44.1/48 kHz, uses bank 2 (1)**
–	–	–	–	**0**	–	–	–	**16 kHz, does not use bank 2 (1)**
–	–	–	–	1	–	–	–	16 kHz, uses bank 2
–	–	–	–	–	**0**	–	–	**22.025/24 kHz, does not use bank 2 (1)**
–	–	–	–	–	1	–	–	22.025/24 kHz, uses bank 2
–	–	–	–	–	–	**0**	–	**8 kHz, does not use bank 2 (1)**
–	–	–	–	–	–	1	–	8 kHz, uses bank 2
–	–	–	–	–	–	–	**0**	**11.025/12 kHz, does not use bank 2 (1)**
–	–	–	–	–	–	–	1	11.025/12 kHz, uses bank 2

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	–	–	–	–	–	–	–	32 kHz, does not use bank 1
1	–	–	–	–	–	–	–	**32 kHz, uses bank 1 (1)**
–	**0**	–	–	–	–	–	–	**Reserved(1)**
–	–	**0**	–	–	–	–	–	**Reserved(1)**
–	–	–	**0**	–	–	–	–	**44.1/48 kHz, does not use bank 1 (1)**
–	–	–	1	–	–	–	–	44.1/48 kHz, uses bank 1
–	–	–	–	**0**	–	–	–	**16 kHz, does not use bank 1 (1)**
–	–	–	–	1	–	–	–	16 kHz, uses bank 1
–	–	–	–	–	**0**	–	–	**22.025/24 kHz, does not use bank 1 (1)**
–	–	–	–	–	1	–	–	22.025/24 kHz, uses bank 1
–	–	–	–	–	–	**0**	–	**8 kHz, does not use bank 1 (1)**
–	–	–	–	–	–	1	–	8 kHz, uses bank 1
–	–	–	–	–	–	–	**0**	**11.025/12 kHz, does not use bank 1 (1)**
–	–	–	–	–	–	–	1	11.025/12 kHz, uses bank 1

(1) Default values are in **bold**.

Table 20. Bank Switching Command (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0								**EQ ON**
1	–	–	–	–	–	–	–	EQ OFF (bypass BQ 0-7 of channels 1 and 2)
–	**0**	–	–	–	–	–	–	**Reserved** (2)
–	–	**0**	–	–	–	–	–	**Ignore bank-mapping in bits D31–D8.Use default mapping.** (2)
		1						Use bank-mapping in bits D31–D8.
–	–	–	**0**	–	–	–	–	**L and R can be written independently.** (2)
–	–	–	1	–	–	–	–	L and R are ganged for EQ biquads; a write to left-channel BQ is also written to right-channel BQ. (0x29–0x2F is ganged to 0x30–0x36.Also 0x58–0x5B is ganged to 0x5C–0x5F)
–	–	**–**	**–**	**0**	–	–	–	**Reserved** (2)
–	–	–	–	–	**0**	**0**	**0**	**No bank switching. All configuration of the BiQuads are applied directly to the DAP** (2)
–	–	–	–	–	0	0	1	Configure bank 1 (32 kHz by default)
–	–	–	–	–	0	1	0	Configure bank 2 (44.1/48 kHz by default)
–	–	–	–	–	0	1	1	Configure bank 3 (other sample rates by default)
–	–	–	–	–	1	0	0	Automatic bank selection
–	–	–	–	–	1	0	1	Reserved
–	–	–	–	–	1	1	X	Reserved

(2) Default values are in **bold**.

DETAILED DESCRIPTION AND THEORY OF OPERATION

POWER SUPPLY

To facilitate system design, the TAS5721 needs only a 3.3-V supply in addition to the PVDD power-stage supply. The required sequencing of the power supplies is shown in the Recommended Use Model section. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, for example, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BSTRPx) and power-stage supply pins (PVDD). The gate drive voltage (GVDD_REG) is derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BSTRPx) to the power-stage output pin (SPK_OUTx). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. As shown in the Typical Application Circuits section, it is recommended to use ceramic capacitors, for the bootstrap supply pins. These capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD pin is decoupled with a ceramic capacitor placed as close as possible to each supply pin, as shown in the Typical Application Circuits section.

The TAS5721 is fully protected against erroneous power-stage turn-on due to parasitic gate charging.

I^2C Address Selection and Fault Output

ADR/$\overline{\text{FAULT}}$ is an input pin during power up. It can be pulled HIGH or LOW through a resistor as shown in the Typical Application Circuits section in order to set the I^2C address. Pulling this pin HIGH through the resistor results in setting the I^2C 7-bit address to 0011011 (0x36), and pulling it LOW through the resistor results in setting the address to 0011010 (0x34).

During power up, the address of the device is latched in, freeing up the ADR/$\overline{\text{FAULT}}$ pin to be used as a fault notification output. When configured as a fault output, the pin will go low when a fault occurs and will return to it's default state when register 0x02 is cleared. The device will pull the fault pin low for over-current, over-temperature, over-voltage lock-out, and under-voltage lock-out.

DEVICE PROTECTION SYSTEM

Overcurrent (OC) Protection With Current Limiting

The device has independent, fast reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by a protection system. If the high-current condition situation persists, a protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. After the power stage enters into this state, the power stage will attempt to restart after a period of time defined in register 0x1C. If the high-current condition persists, the device will begin the shutdown and retry sequence again. The device will return to normal operation once the fault condition is removed. Current limiting and overcurrent protection are not independent for half-bridges. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

Overtemperature Protection

The TAS5721 has an overtemperature-protection system. If the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and ADR/FAULT, if configured as an output, being asserted low. The TAS5721 recovers automatically once the temperature drops approximately 30 °C.

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5721 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit ensures that all circuits are fully operational when the PVDD and AVDD supply voltages reach 4.1 V and 2.7 V, respectively. Although PVDD and AVDD are independently monitored, a supply voltage drop below the UVP threshold on AVDD or on either PVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and ADR/FAULT, if configured as an output, being asserted low.

CLOCK, AUTO DETECTION, AND PLL

The TAS5721 is a slave device. It accepts MCLK, SCLK, and LRCLK. The digital audio processor (DAP) supports all the sample rates and MCLK rates that are defined in the Clock Control Register section.

The TAS5721 checks to verify that SCLK is a specific value of 32 f_S, 48 f_S, or 64 f_S. The DAP only supports a 1 × f_S LRCLK. The timing relationship of these clocks to SDIN is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable, out of range, or absent) to produce the internal clock (DCLK) running at 512 times the PWM switching frequency.

The DAP can autodetect and set the internal clock control logic to the appropriate settings for all supported clock rates as defined in the clock control register.

TAS5721 has robust clock error handling that uses the built-in trimmed oscillator clock to quickly detect changes/errors. Once the system detects a clock change/error, it will mute the audio (through a single step mute) and then force PLL to operate in a reduced capacity using the internal oscillator as a reference clock. Once the clocks are stable, the system will auto detect the new rate and revert to normal operation. During this process, the default volume will be restored in a single step (also called hard unmute) by default. If desired, the unmuting process can be programmed to ramp back slowly (also called soft unmute) as defined in volume register (0x0E).

SERIAL DATA INTERFACE

Serial data is input on SDIN. The PWM outputs are derived from SDIN. The TAS5721 DAP accepts serial data in 16-, 20-, or 24-bit left-justified, right-justified, and I^2S serial data formats.

PWM Section

The TAS5721 DAP device uses noise-shaping and sophisticated non-linear correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts 24-bit PCM data from the DAP and outputs up to three PWM audio output channels.

The PWM modulation block has individual channel dc blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz. Individual channel de-emphasis filters for 44.1- and 48-kHz are included and can be enabled and disabled.

Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%. It is important to note that for any applications with PVDD greater than 18 V, the maximum modulation index must be set to 93.8%.

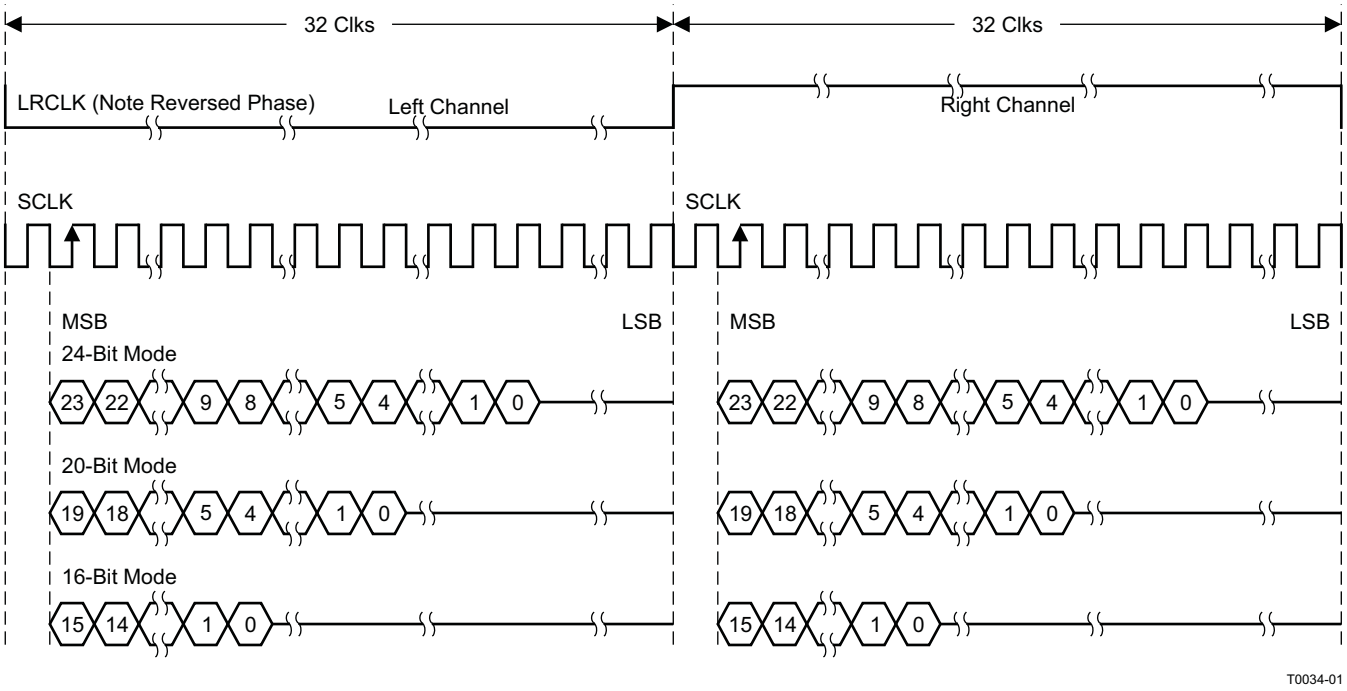
SERIAL INTERFACE CONTROL AND TIMING

The I^2S mode is set by writing to register 0x04.

I²S Timing

I²S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

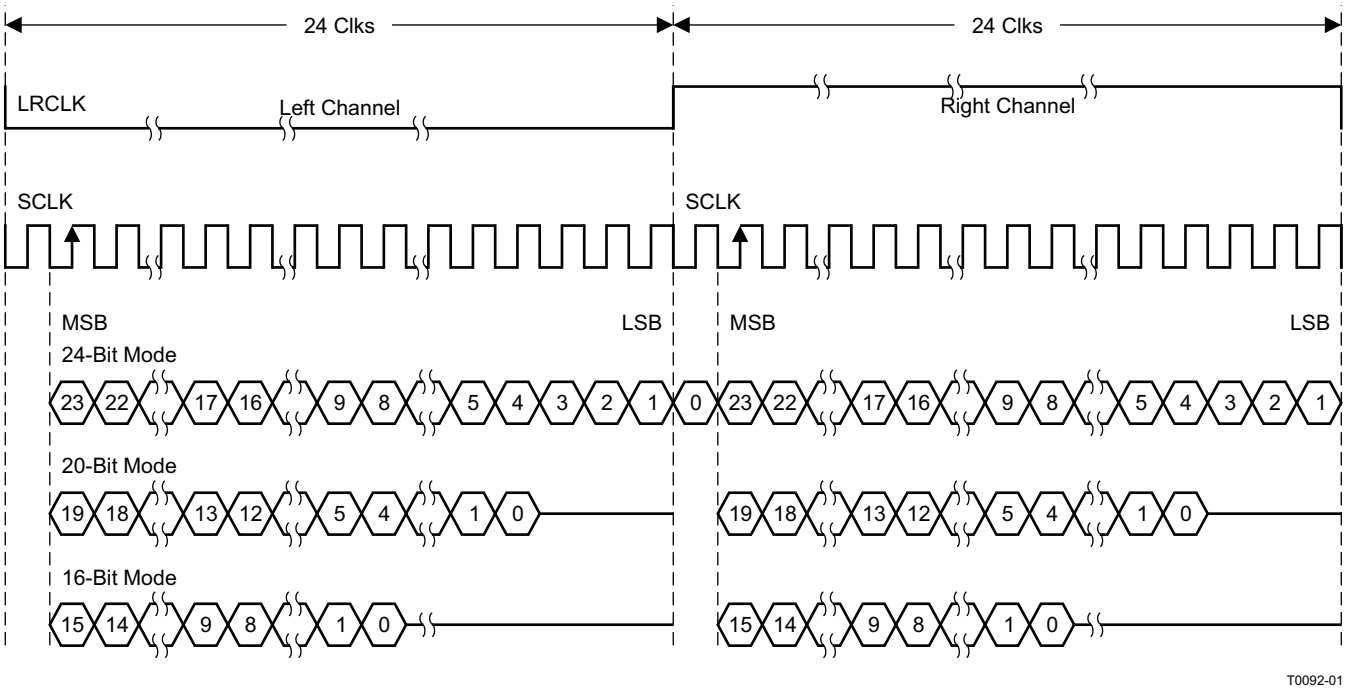
2-Channel I²S (Philips Format) Stereo Input



NOTE: All data presented in 2s-complement form with MSB first.

Figure 52. I²S 64-f_S Format

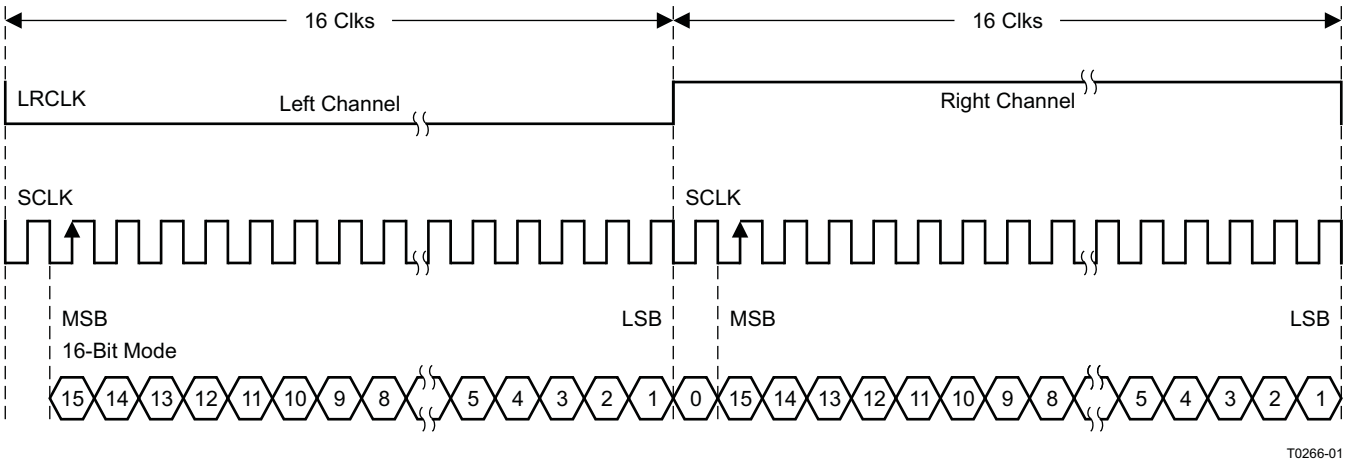
2-Channel I²S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)



NOTE: All data presented in 2s-complement form with MSB first.

Figure 53. I²S 48-f_S Format

2-Channel I²S (Philips Format) Stereo Input



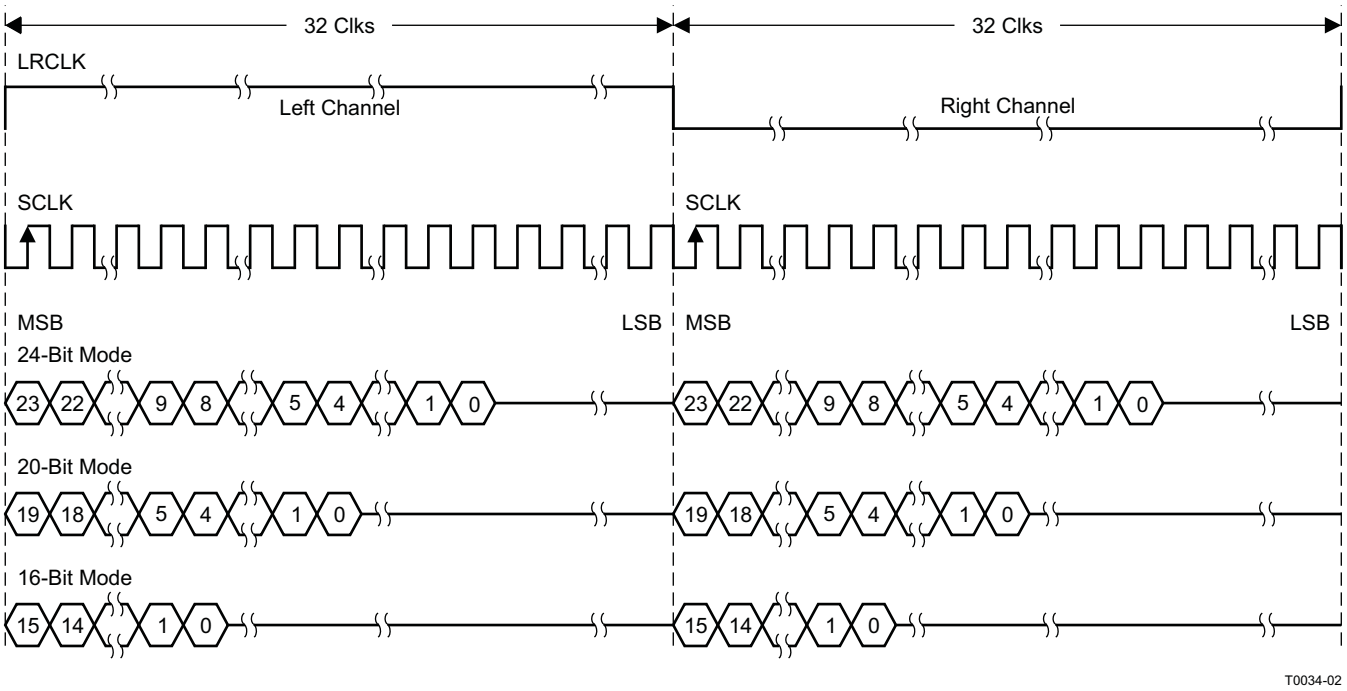
NOTE: All data presented in 2s-complement form with MSB first.

Figure 54. I²S 32-f_S Format

Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

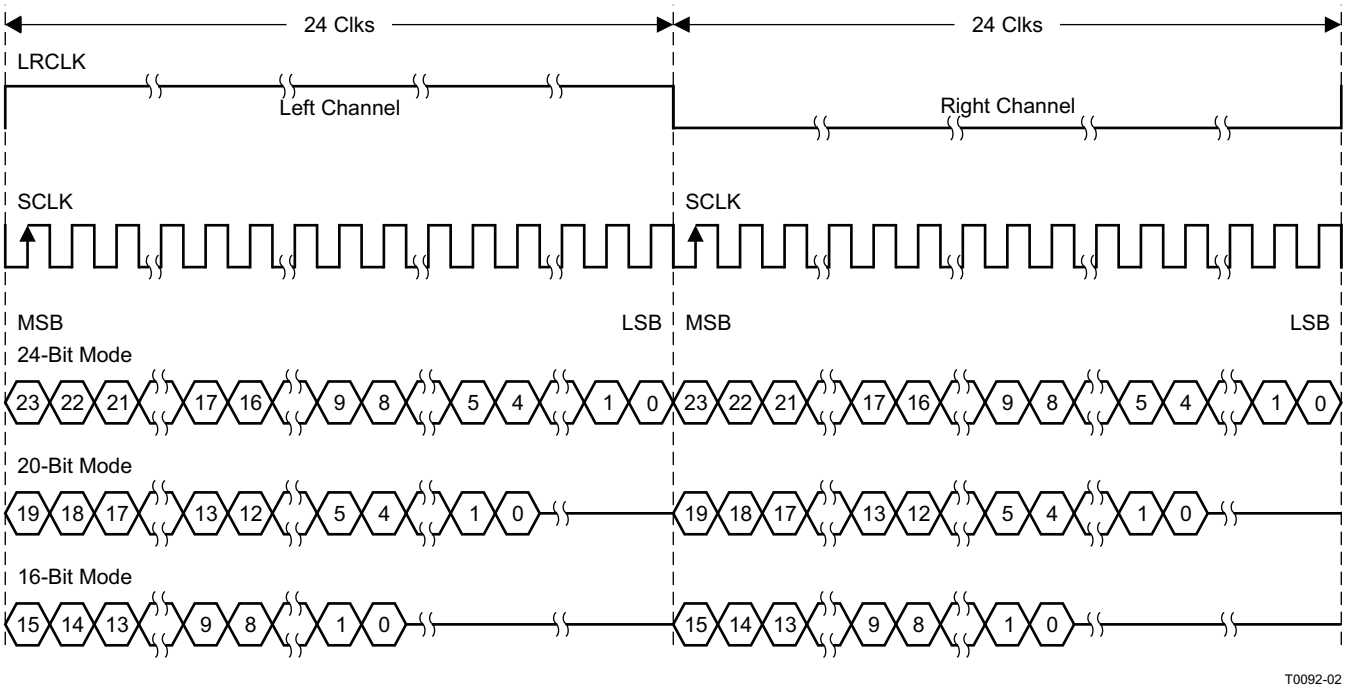
2-Channel Left-Justified Stereo Input



NOTE: All data presented in 2s-complement form with MSB first.

Figure 55. Left-Justified 64-f_S Format

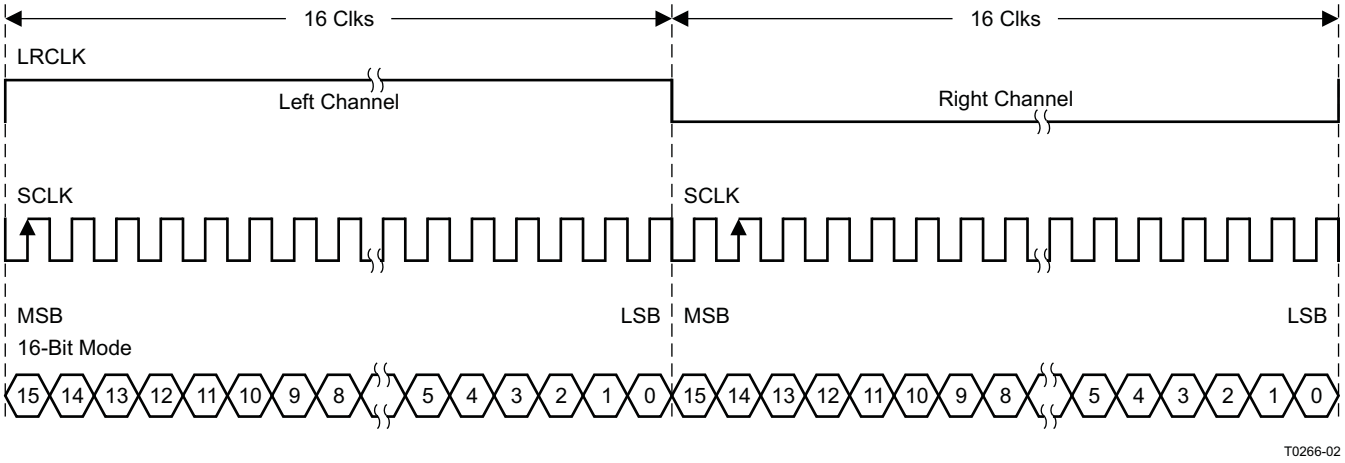
2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)



NOTE: All data presented in 2s-complement form with MSB first.

Figure 56. Left-Justified 48-f_S Format

2-Channel Left-Justified Stereo Input



NOTE: All data presented in 2s-complement form with MSB first.

Figure 57. Left-Justified 32-f_S Format

Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input

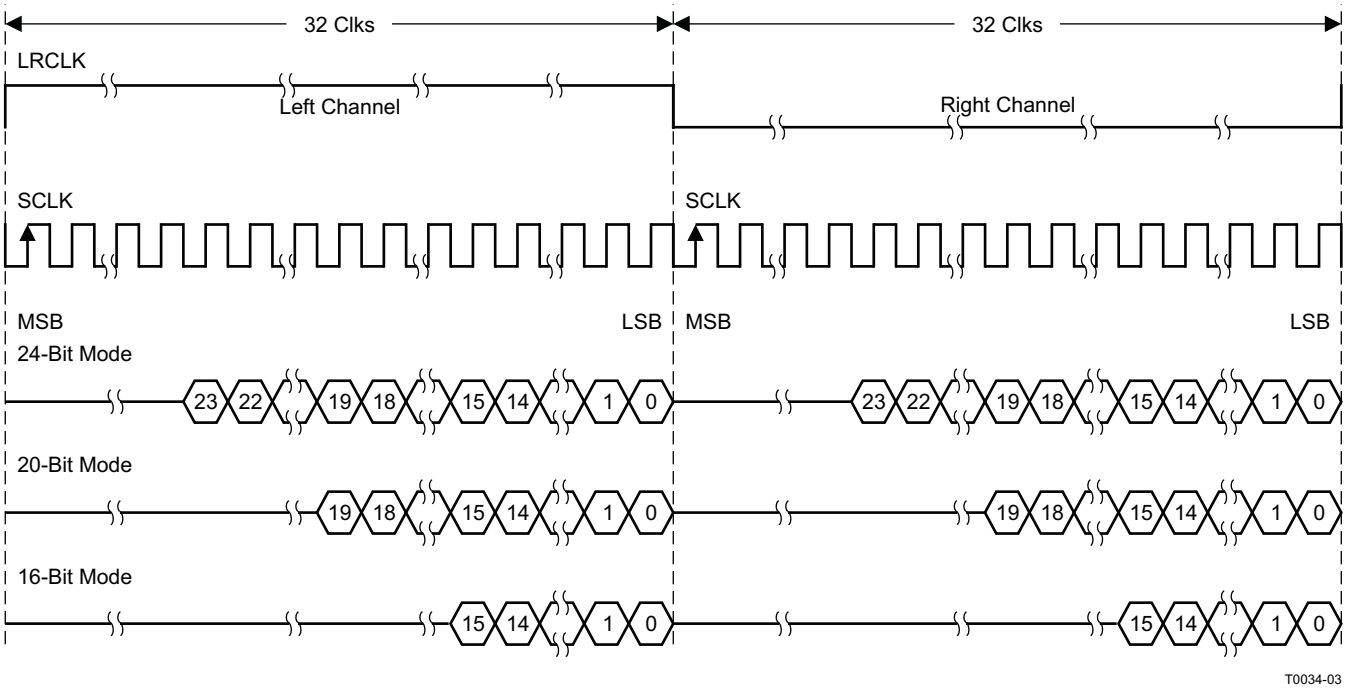


Figure 58. Right Justified 64-f_S Format

2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)

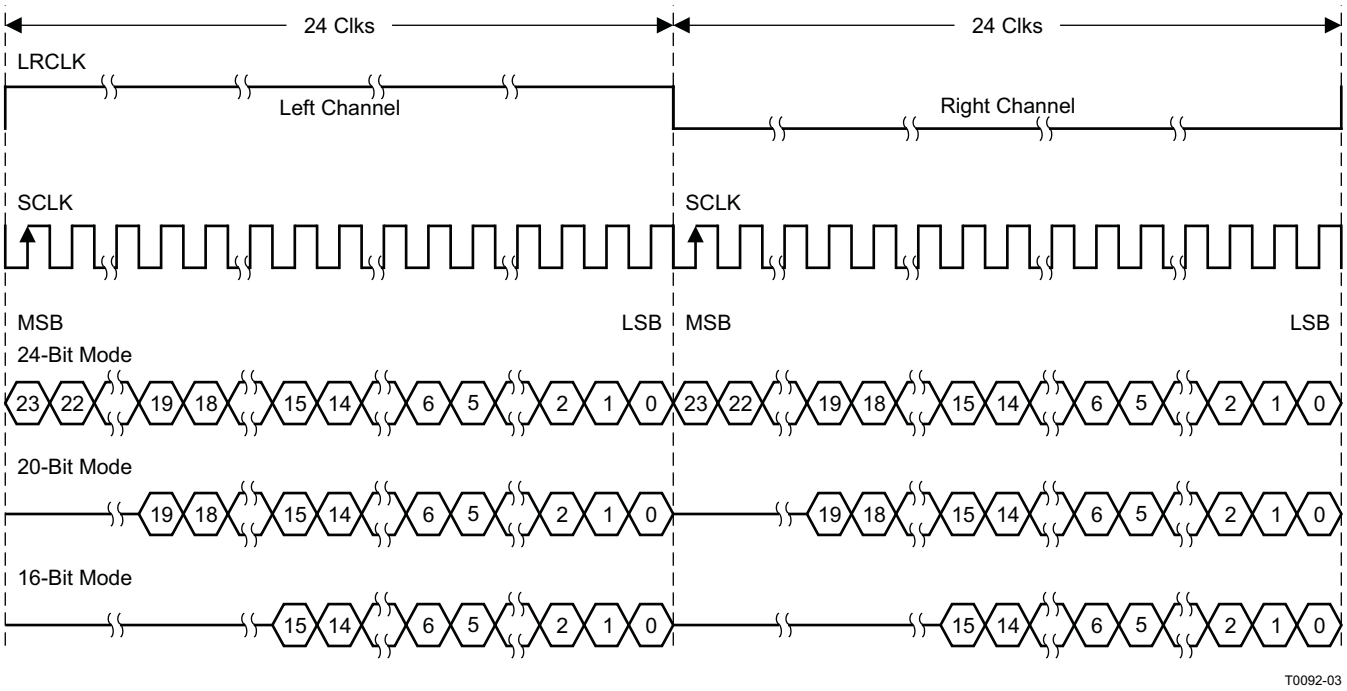


Figure 59. Right Justified 48-f_S Format

2-Channel Right-Justified (Sony Format) Stereo Input

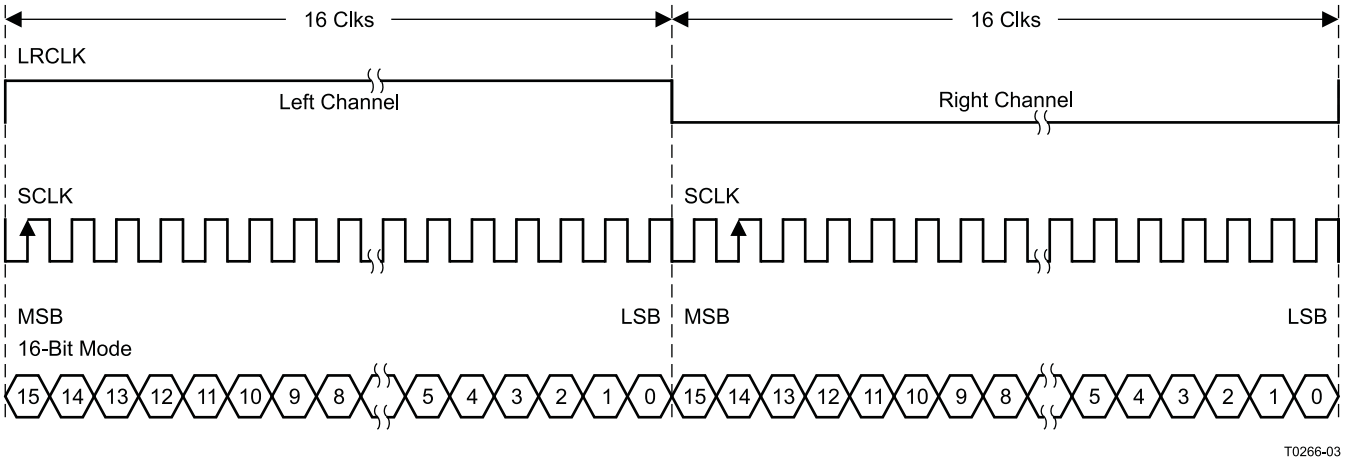


Figure 60. Right Justified 32-f_S Format

I²C SERIAL CONTROL INTERFACE

The TAS5721 DAP has a bidirectional inter-integrated circuit (I²C) interface that is compatible with the I²C bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single and multiple byte write and read operations. This is a slave only device that does not support a multimaster bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum) and the fast I²C bus operation (400 kHz maximum). The DAP performs all I²C operations without I²C wait cycles.

General I²C Operation

The I²C bus employs two signals to communicate between integrated circuits in a system: (data) SDA and (clock) SCL. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 61. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5721 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

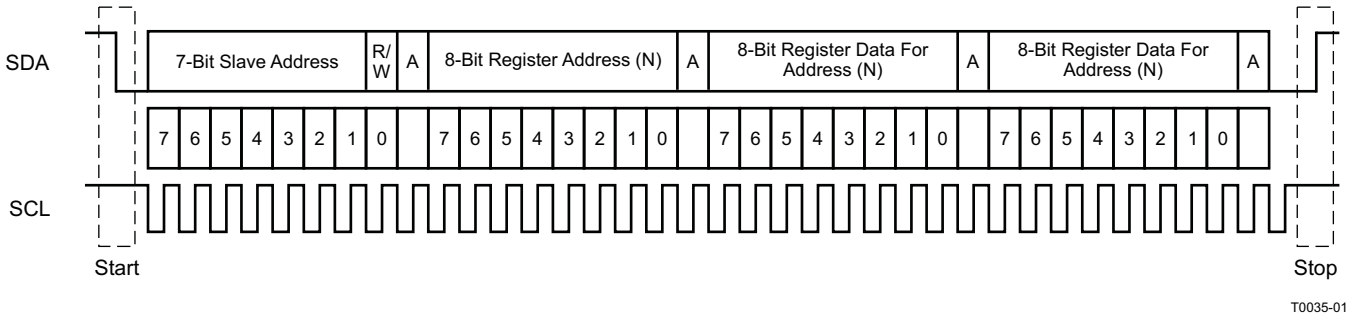


Figure 61. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 61.

Pin ADR/$\overline{FAULT}$ defines the I²C device address. An external 15-kΩ pull down on this pin gives a device address of 0x34 and a 15-kΩ pull up gives a device address of 0x36. The 7-bit address is 0011011 (0x36) or 0011010 (0x34).

I²C Device Address Change Procedure

- Write to device address change enable register, 0xF8 with a value of 0xF9 A5 A5 A5.
- Write to device register 0xF9 with a value of 0x0000 00XX, where XX is the new address.
- Any writes after that should use the new device address XX.

Single- and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for subaddresses 0x00 to 0x1F. However, for the subaddresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. For example, if a write command is received for a biquad subaddress, the DAP expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded.

Supplying a subaddress for each subaddress transaction is referred to as random I^2C addressing. The TAS5721 also supports sequential I^2C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I^2C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5721. For I^2C sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 62, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit will be a 0. After receiving the correct I^2C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5721 internal memory address being accessed. After receiving the address byte, the TAS5721 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5721 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

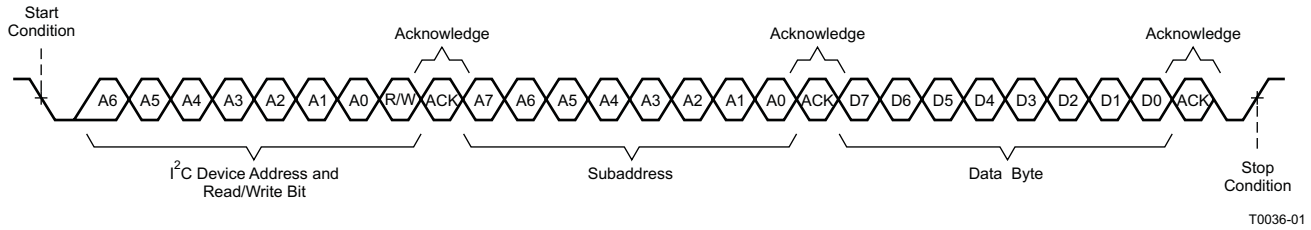


Figure 62. Single-Byte Write Transfer

Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 63. After receiving each data byte, the TAS5721 responds with an acknowledge bit.

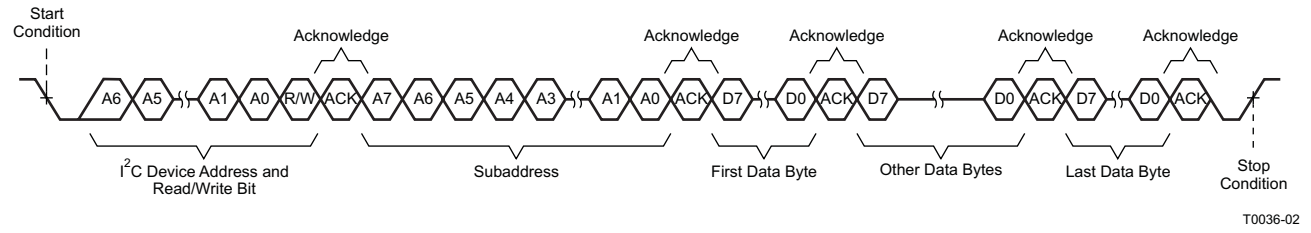


Figure 63. Multiple-Byte Write Transfer

Single-Byte Read

As shown in Figure 64, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5721 address and the read/write bit, TAS5721 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5721 address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5721 again responds with an acknowledge bit. Next, the TAS5721 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

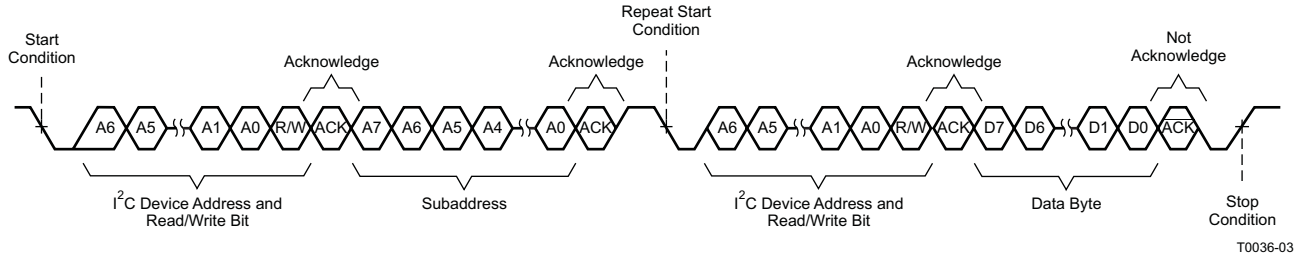


Figure 64. Single-Byte Read Transfer

Multiple-Byte Read

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TAS5721 to the master device as shown in Figure 65. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

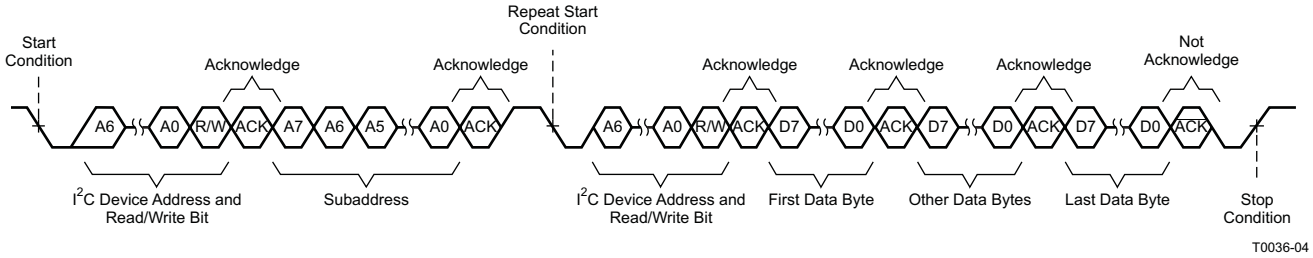


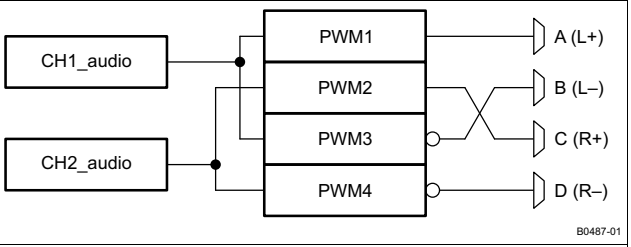
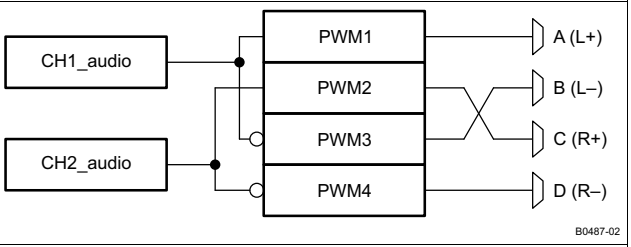
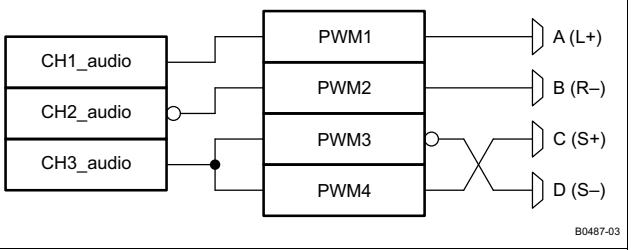
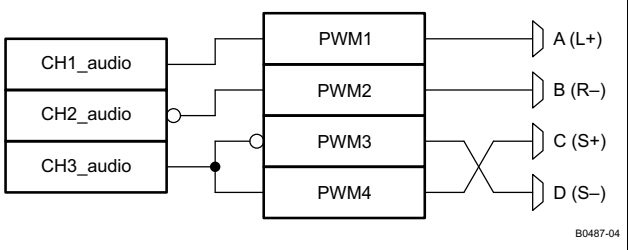
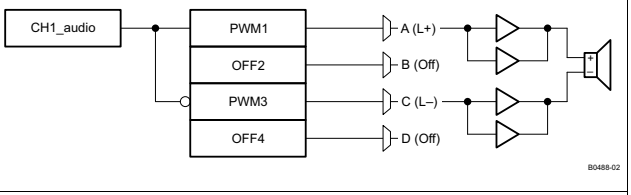
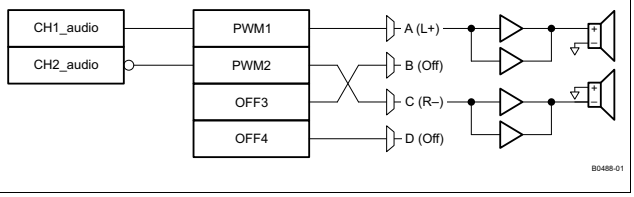
Figure 65. Multiple Byte Read Transfer

Output Mode and MUX Selection

The TAS5721 is a highly configurable device, capable of operating in 2.0, Single Device 2.1 and parallel bridge tied load (PBTL) configurations. Addtionally, the modulation scheme can be changed for the channels to operate either in AD or BD Modulation mode. While many configurations are possible because of this flexibility, the majority of use cases uses will operate in one of the configurations shown below. For ease of use and reduced complexity, the figure below outlines both the register settings and the output configurations required to set the device up for operation in these various modes.

The output configuration quick reference table below highlights the controls that are required to configure the device for various operational modes. Please note that other controls, which are not directly related to the output configuration muxes may also be required. For example, the Inter Channel Delay (ICD) settings will likely need to be modified to optimize for idle channel noise, cross-talk, and distortion performance for each of these considerations, in addition to start and stop time and others. Please consult the respective registers for these controls to optimize for various other peformance parameters and use cases.

Table 21. Output Configuration Quick Reference

Output Configuration	Modulation Mode	Register Settings	Block Diagram
2.0 (Stereo BTL)	AD for Both Outputs	0x20[23] = 0 0x20[19] = 0 0x20[15:8] = 0x77 0x05[7] = 0 0x05[2] = 0 0x25[23:8] = 0x0213 0x1A[7:0] = 0x0F	
	BD for Both Outputs	0x20[23] = 1 0x20[19] = 1 0x20[15:8] = 0x77 0x05[7] = 0 0x05[2] = 0 0x25[23:8] = 0x0213 0x1A[7:0] = 0x0A	
Single Device 2.1 (Stereo Single Ended + Mono BTL) Note: In these described configurations, the polarity of the signal being sent to SPK_OUTB is inverted. For this reason, care should be taken to ensure that the speakers are connected as shown in the block diagram.	AD for Both SE Outputs AD for Single BTL Output	0x20[23] = 0 0x20[19] = 0 0x20[3] = 0 0x05[7] = 1 0x05[2] = 1 0x25[23:8] = 0x0132 0x1A[7:0] = 0x95 0x20[7:4] = 0x7 0x21[8] = 0 0x20[25] = 1	
	AD for both SE Outputs BD for Single BTL Output	0x20[23] = 0 0x20[19] = 0 0x20[3] = 1 0x05[7] = 1 0x05[2] = 1 0x25[23:8] = 0x0132 0x1A[7:0] = 0x95 0x20[7:4] = 0x7 0x21[8] = 0 0x20[25] = 1	
1.0 Mono PBTL	AD	0x05[7] = 0 0x05[5] = 0 0x05[2] = 0 0x19[7:0] = 0x3A 0x1A[7:0] = 0x0F 0x20[23] = 0 0x20[15:12] = 0x7 0x25[23:8] = 0x0123	
	BD	0x05[7] = 0 0x05[5] = 0 0x05[2] = 0 0x19[7:0] = 0x3A 0x1A[7:0] = 0x0A 0x20[23] = 1 0x20[15:12] = 0x7 0x25[23:8] = 0x0123	

2.1-Mode Support

The TAS5721 uses a special *mid-Z ramp* sequence to reduce click and pop in SE-mode and 2.1-mode operation. To enable the mid-Z ramp, register 0x05 bit D7 must be set to 1. To enable 2.1 mode, register 0x05 bit D2 must be set to 1. The SSTIMER pin should be left floating in this mode.

Supply Pumping and Polarity Inversion

The high degree of correlation between the left and right channels of a stereo audio signal dictates that, when the left audio signal is positive, the right audio signal tends to be positive as well. When the Class D is configured for single-ended operation (as would be the case for Single Device 2.1 Operation), this results in both outputs drawing current from the supply rail "in phase". Similarly, when the left audio signal is negative, the right audio signal tends to be negative as well. For single-ended operation, both outputs will likewise force current into the ground rail. This can lead to a phenomenon called "supply pumping" in which the capacitances on the PVDD rail begin to store charge- raising the voltage level of PVDD as well. This noise injection onto the rail is in phase with and at a similar frequency of the signal being produced by the amplifier output stage. This phenomenon can cause issues for other devices attached to the PVDD rail. The problem does not occur for BTL outputs since outputs of both polarities are always present for each channel.

To combat supply pumping in 2.1 Mode, the device has an integrated speaker-mode volume negation feature, which, essentially introduces a polarity inversion (shift by 180°) to any of the given channels. By setting the correct bit in 0x20[31:24], it is possible to invert the polarity of the DAP channels that drive the PWM modulator blocks. This allows, for instance, the left channel to operate with its default polarity, while the right channel could have its polarity inverted to balance current flow into and out of the supplies. This procedure could have an adverse implication on the stereo imaging of the audio system because, if the speakers in the system are connected in the same manner as they would be connected when being driven by traditional BTL channels, the phase of the signals being sent to the speakers is 180° out of phase. In order to prevent this from occurring, the speaker on the negated channel must be connected "backwards" (i.e. the Class D signal for the negated channel gets connected to the negative speaker terminal and the positive terminal is grounded). In this way, supply pumping is reduced while keeping the effective signal polarity the same. The table above includes register settings which enable the polarity inversion, so care should be taken to adjust the polarity of the speakers if this feature is left enabled. Of course this feature can be left disabled if desired, provided the supply pumping phenomenon doesn't cause any other system level issues

PBTL-Mode Support

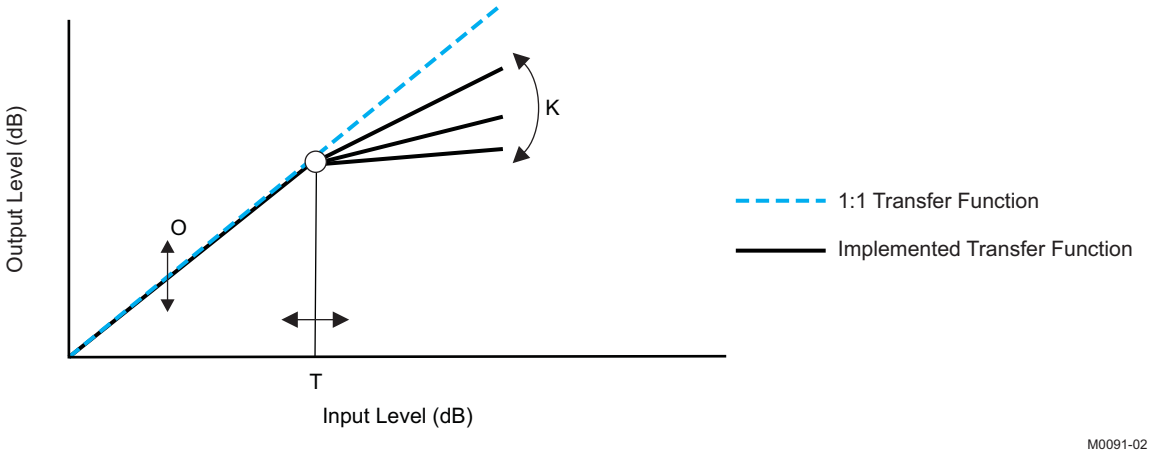
The TAS5721 supports parallel BTL (PBTL) mode with OUT_A/OUT_B (and OUT_C/OUT_D) connected after the LC filter. In order to put the part in PBTL configuration, the PWM output multiplexers should be updated to set the device in PBTL mode. Output Mux Register (0x25) should be written with a value of 0x01 10 32 45. Also, the PWM shutdown register (0x19) should be written with a value of 0x3A.

Dynamic Range Control (DRC)

The DRC scheme has a single threshold, offset, and slope (all programmable). There is one ganged DRC for the left/right channels and one DRC for the subchannel.

The DRC input/output diagram is shown in Figure 66.

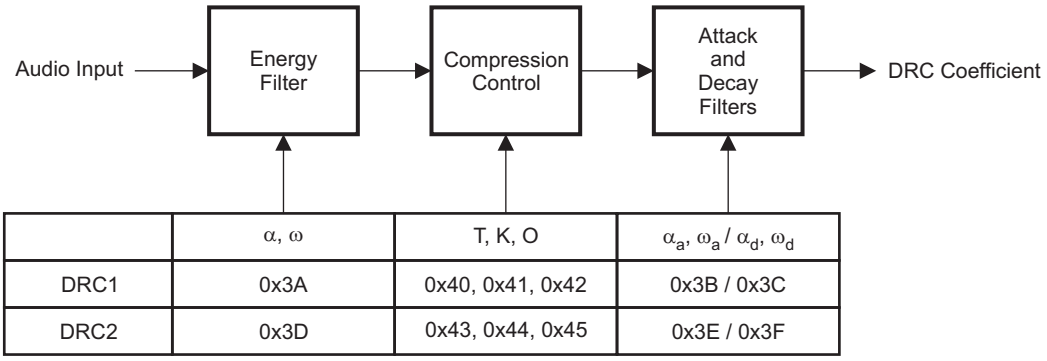
Refer to GDE software tool for more description on T, K, and O parameters.



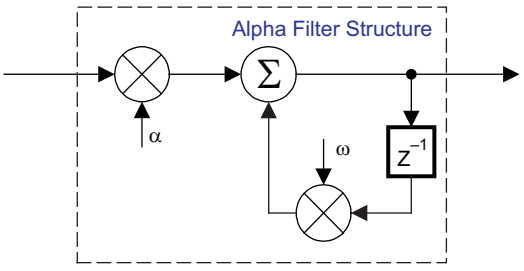
Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

- Each DRC has adjustable threshold, offset, and compression levels.
- Programmable energy, attack, and decay time constants
- *Transparent compression*: compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

Figure 66. Dynamic Range Control



	α, ω	T, K, O	α_a, ω_a / α_d, ω_d
DRC1	0x3A	0x40, 0x41, 0x42	0x3B / 0x3C
DRC2	0x3D	0x43, 0x44, 0x45	0x3E / 0x3F



NOTE:
$\omega = 1 - \alpha$

T = 9.23 format, all other DRC coefficients are 3.23 format

Figure 67. DRC Structure

BANK SWITCHING

The TAS5721 uses an approach called *bank switching* together with automatic sample-rate detection. All processing features that must be changed for different sample rates are stored internally in three banks. The user can program which sample rates map to each bank. By default, bank 1 is used in 32-kHz mode, bank 2 is used in 44.1- or 48-kHz mode, and bank 3 is used for all other rates. Combined with the clock-rate autodetection feature, bank switching allows the TAS5721 to detect automatically a change in the input sample rate and switch to the appropriate bank without any MCU intervention.

An external controller configures bankable locations (0x29-0x36, 0x3A-0x3F, and 0x58-0x5F) for all three banks during the initialization sequence.

If auto bank switching is enabled (register 0x50, bits 2:0) , then the TAS5721 automatically swaps the coefficients for subsequent sample rate changes, avoiding the need for any external controller intervention for a sample rate change.

By default, bits 2:0 have the value 000; indicating that bank switching is disabled. In that state, updates to bankable locations take immediate effect. A write to register 0x50 with bits 2:0 being 001, 010, or 011 brings the system into the coefficient-bank-update state *update bank1*, *update bank2,* or *update bank3*, respectively. Any subsequent write to bankable locations updates the coefficient banks stored outside the DAP. After updating all the three banks, the system controller should issue a write to register 0x50 with bits 2:0 being 100; this changes the system state to automatic bank switching mode. In automatic bank switching mode, the TAS5721 automatically swaps banks based on the sample rate.

Command sequences for updating DAP coefficients can be summarized as follows:

1. **Bank switching disabled (default):** DAP coefficient writes take immediate effect and are not influenced by subsequent sample rate changes.

   OR

   Bank switching enabled:

   (a) Update bank-1 mode: Write "001" to bits 2:0 of reg 0x50. Load the 32 kHz coefficients.
   (b) Update bank-2 mode: Write "010" to bits 2:0 of reg 0x50. Load the 48 kHz coefficients.
   (c) Update bank-3 mode: Write "011" to bits 2:0 of reg 0x50. Load the other coefficients.
   (d) Enable automatic bank switching by writing "100" to bits 2:0 of reg 0x50.

26-Bit 3.23 Number Format

All mixer gain coefficients are 26-bit coefficients using a 3.23 number format. Numbers formatted as 3.23 numbers means that there are 3 bits to the left of the decimal point and 23 bits to the right of the decimal point. This is shown in Figure 68 .

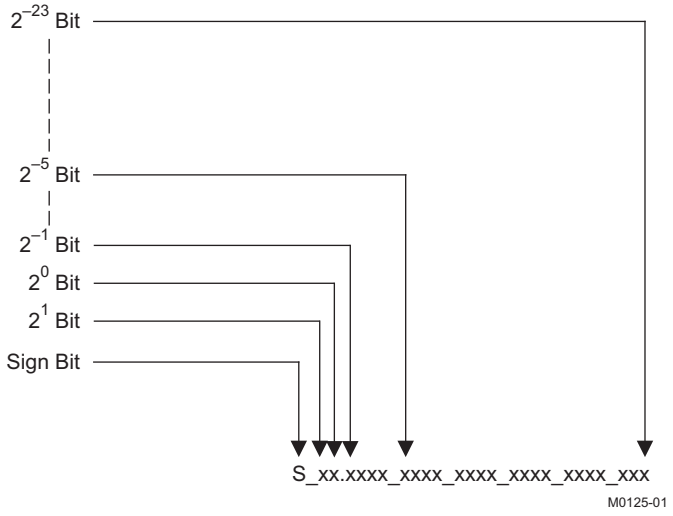


Figure 68. 3.23 Format

The decimal value of a 3.23 format number can be found by following the weighting shown in Figure 68. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 69 applied to obtain the magnitude of the negative number.

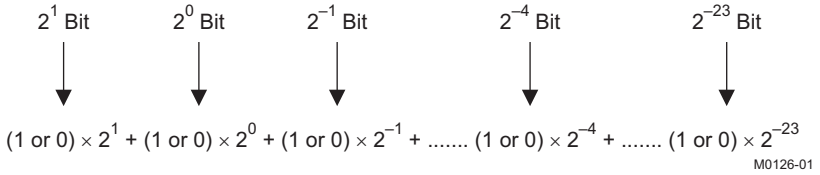


Figure 69. Conversion Weighting Factors—3.23 Format to Floating Point

Gain coefficients, entered via the I^2C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in Figure 70

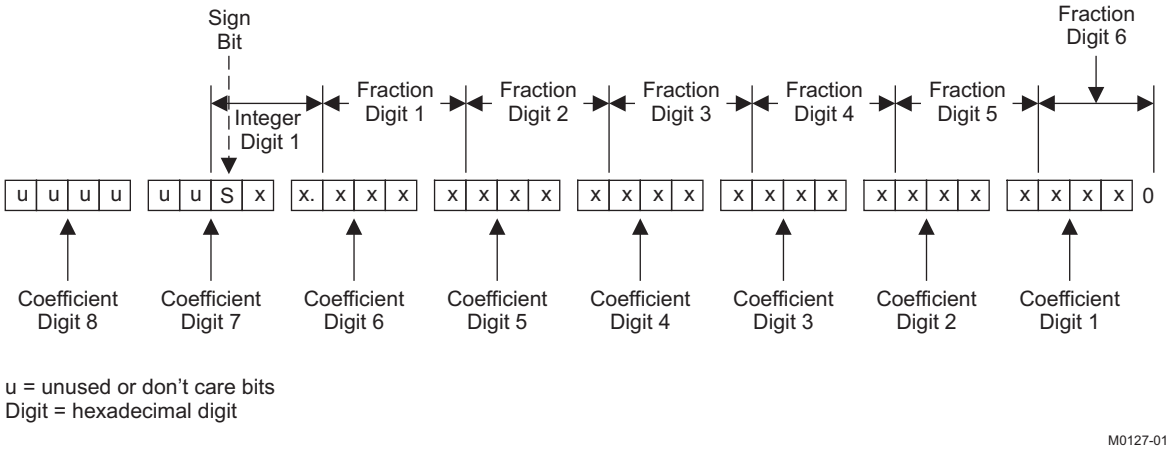


Figure 70. Alignment of 3.23 Coefficient in 32-Bit I^2C Word

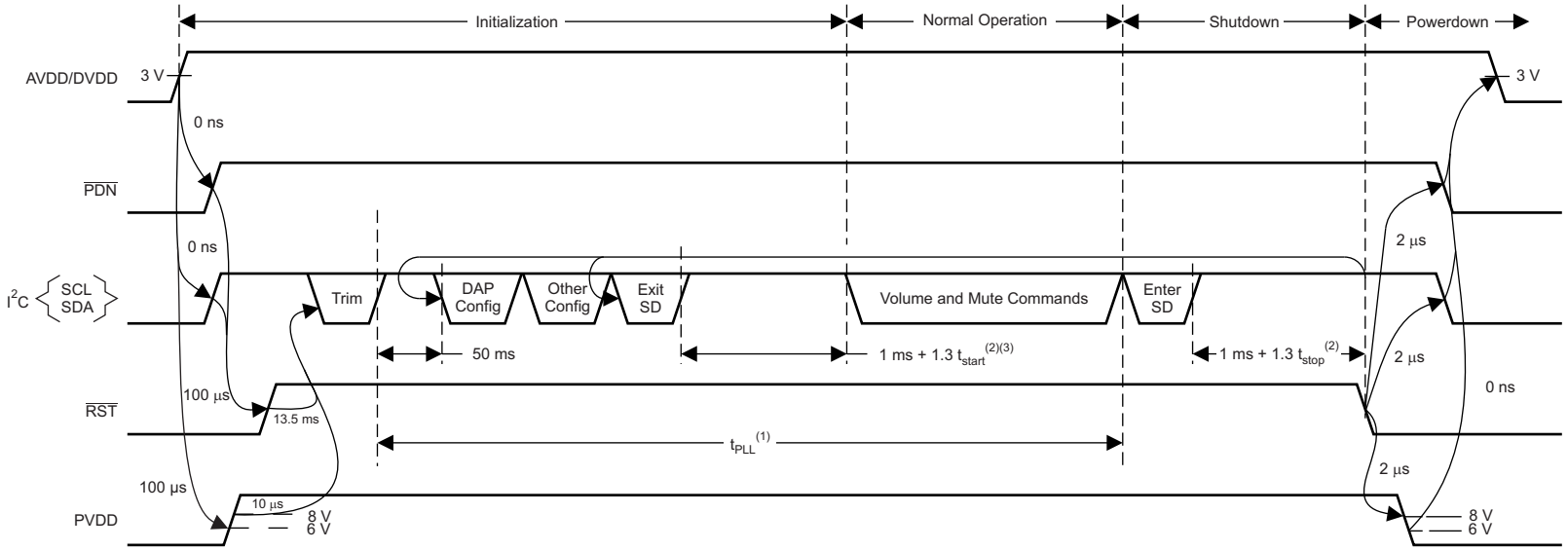
Table 22. Sample Calculation for 3.23 Format

dB	Linear	Decimal	Hex (3.23 Format)
0	1	8,388,608	0080 0000
5	1.7782794	14,917,288	00E3 9EA8
–5	0.5623413	4,717,260	0047 FACC
X	$L = 10^{(X/20)}$	D = 8,388,608 × L	H = dec2hex (D, 8)

Table 23. Sample Calculation for 9.17 Format

dB	Linear	Decimal	Hex (9.17 Format)
0	1	131,072	2 0000
5	1.77	231,997	3 8A3D
–5	0.56	73,400	1 1EB8
X	$L = 10^{(X/20)}$	D = 131,072 × L	H = dec2hex (D, 8)

Recommended Use Model



(1) t_{PLL} has to be greater than 240 ms + 1.3 t_{start}.
This constraint only applies to the first trim command following AVDD/DVDD power-up.
It does not apply to trim commands following subsequent resets.
(2) t_{start}/t_{stop} = PWM start/stop time as defined in register 0X1A
(3) When Mid-Z ramp is enabled (for 2.1 mode), t_{start} = 300 ms

T0419-07

Figure 71. Recommended Command Sequence

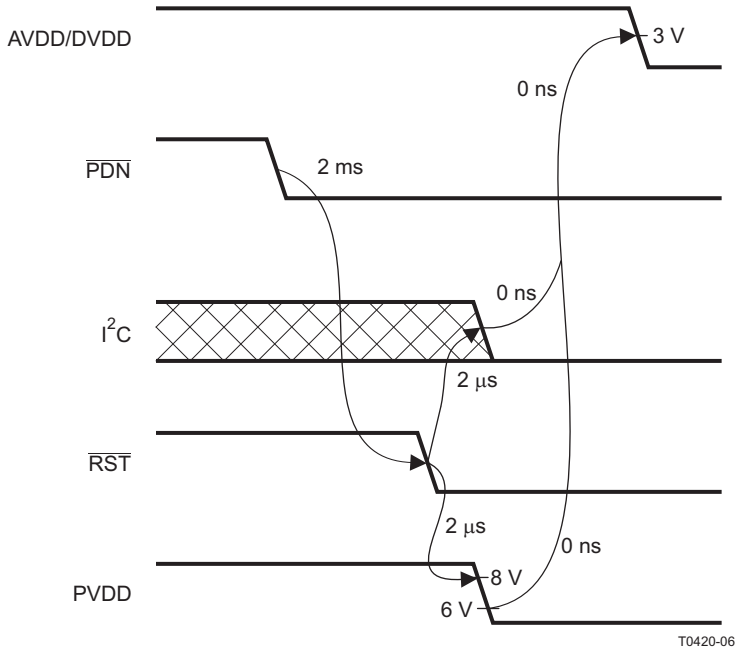


Figure 72. Power Loss Sequence

Recommended Command Sequences

Initialization Sequence

Use the following sequence to power-up and initialize the device:

1. Hold all digital inputs low and ramp up AVDD/DVDD to at least 3 V.
2. Initialize digital inputs and PVDD supply as follows:
   - Drive $\overline{RST}$ = 0, $\overline{PDN}$ = 1, and other digital inputs to their desired state while ensuring that all are never more than 2.5 V above AVDD/DVDD. Wait at least 100 µs, drive $\overline{RST}$ = 1, and wait at least another 13.5 ms.
   - Ramp up PVDD to at least 8 V while ensuring that it remains below 6 V for at least 100 µs after AVDD/DVDD reaches 3 V. Then wait at least another 10 µs.
3. Trim oscillator (write 0x00 to register 0x1B) and wait at least 50 ms.
4. Configure the DAP via I^2C (see Users's Guide for typical values).
5. Configure remaining registers.
6. Exit shutdown (sequence defined below).

Normal Operation

The following are the only events supported during normal operation:

1. Writes to master/channel volume registers.
2. Writes to soft mute register.
3. Enter and exit shutdown (sequence defined below).

Note: Event 3 is not supported for 240 ms + 1.3 × t_{start} after trim following AVDD/DVDD powerup ramp (where t_{start} is 300 ms when mid-Z ramp is enabled and is otherwise specified by register 0x1A).

Shutdown Sequence

Enter:

1. Write 0x40 to register 0x05.
2. Wait at least 1 ms + 1.3 × t_{stop} (where t_{stop} is specified by register 0x1A).
3. If desired, reconfigure by returning to step 4 of initialization sequence.

Exit:

1. Write 0x00 to register 0x05 (exit shutdown command may not be serviced for as much as 240 ms after trim following AVDD/DVDD powerup ramp).
2. Wait at least 1 ms + 1.3 × t_{start} (where t_{start} is 300 ms when mid-Z ramp is enabled and is otherwise specified by register 0x1A).
3. Proceed with normal operation.

Power-Down Sequence

Use the following sequence to powerdown the device and its supplies:

1. If time permits, enter shutdown (sequence defined above); else, in case of sudden power loss, assert $\overline{PDN}$ = 0 and wait at least 2 ms.
2. Assert $\overline{RST}$ = 0.
3. Drive digital inputs low and ramp down PVDD supply as follows:
   - Drive all digital inputs low after $\overline{RST}$ has been low for at least 2 µs.
   - Ramp down PVDD while ensuring that it remains above 8 V until $\overline{RST}$ has been low for at least 2 µs.
4. Ramp down AVDD/DVDD while ensuring that it remains above 3 V until PVDD is below 6 V and that it is never more than 2.5 V below the digital inputs.

USING HEADPHONE AMPLIFIER OR LINE DRIVER IN TAS5721

This device has a stereo output which can be used as a line driver or a headphone driver that can output 2-Vrms stereo. An audio system can be set up for different applications using this device.

USING HEADPHONE AMPLIFIER IN TAS5721

The device can be represented as shown in Figure 73: analog inputs (single-ended) as DR_INA (pin 7) and DR_INB (pin 10) with the outputs DR_OUTA (pin 8) and DR_OUTB (pin 9).

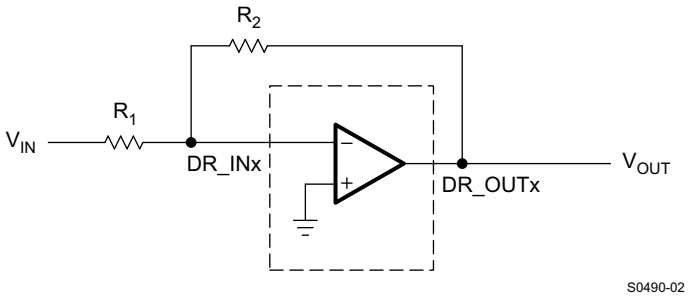


Figure 73. Headphone/Line Driver with Analog Input

$\overline{DR\_SD}$ pin can be used to turn ON or OFF the headphone amplifier and line driver.

Speaker channels are independent of headphone and line driver in this mode.

USING LINE DRIVER AMPLIFIER IN TAS5721

Single-supply headphone and line driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 74 illustrates the conventional line driver amplifier connection to the load and output signal.

DC blocking capacitors for headphone amps are often large in value, and a mute circuit is needed during power up to minimize click and pop for both headphone and line driver. The output capacitors and mute circuits consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

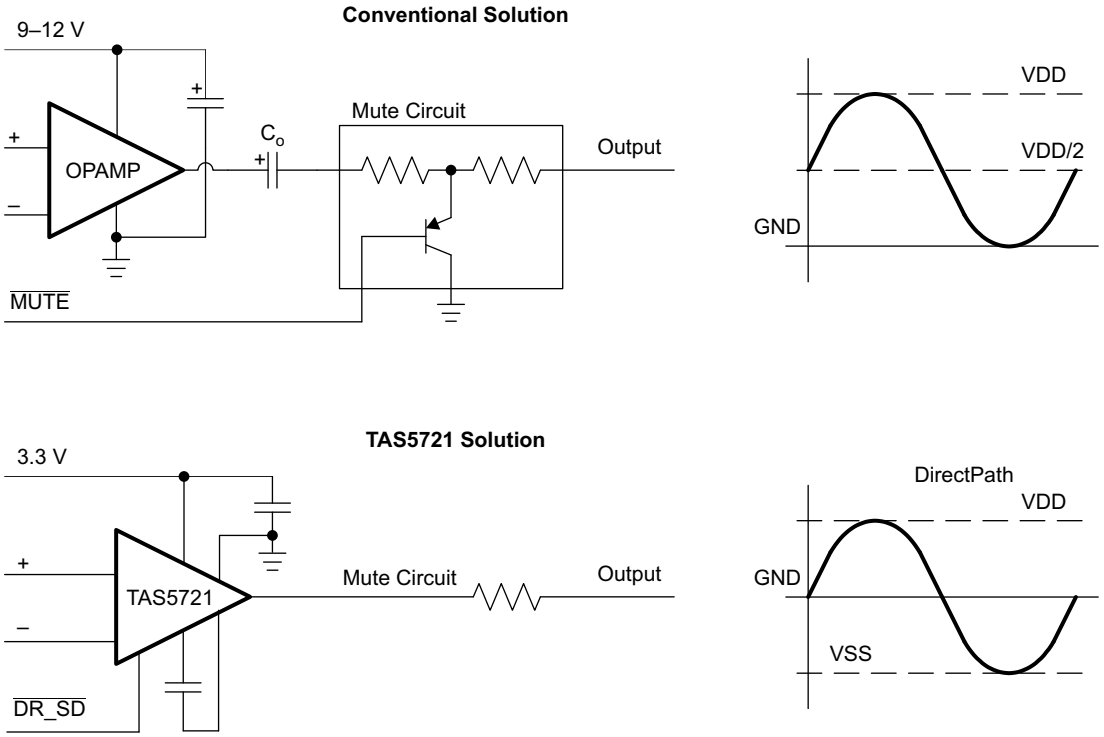


Figure 74. Conventional and DirectPath HP and Line Driver

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail, combining this with the built in click and pop reduction circuit, the DirectPath amplifier requires no output dc blocking capacitors.

The bottom block diagram and waveform of Figure 74 illustrate the ground-referenced headphone and line driver architecture. This is the architecture of the TAS5721.

COMPONENT SELECTION

Charge Pump

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The capacitor connected to the DR_VSS pin must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1 µF is typical. Capacitor values that are smaller than 1 µF are not recommended for the DR_VSS pin as they will limit the negative voltage swing when driving low impedance loads.

Decoupling Capacitors

The TAS5721 is a DirectPath amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device PVDD leads works best. Placing this decoupling capacitor close to the TAS5721 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device. Please refer to the TAS5721 for the recommended layout for these components.

Gain Setting Resistors Ranges

The gain setting resistors, R_{in} and R_{fb}, must be chosen so that noise, stability and input capacitor size of the TAS5721 is kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{in}. Selecting values that are too low demands a large input ac-coupling capacitor, C_{IN}. Selecting values that are too high increases the noise of the amplifier. Table 24 lists the recommended resistor values for different gain settings.

Table 24. Recommended Resistor Values

INPUT RESISTOR VALUE, R_{in}	FEEDBACK RESISTOR VALUE, R_{fb}	DIFFERENTIAL INPUT GAIN	INVERTING INPUT GAIN	NON INVERTING INPUT GAIN
10 kΩ	10 kΩ	1 V/V	–1 V/V	2 V/V
10 kΩ	15 kΩ	1.5 V/V	–1.5 V/V	2.5 V/V
10 kΩ	20 kΩ	2 V/V	–2 V/V	3 V/V
4.7 kΩ	47 kΩ	10 V/V	–10 V/V	11 V/V

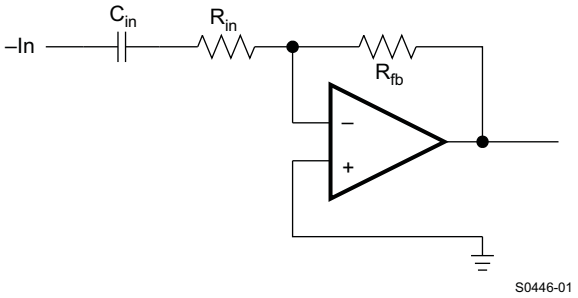


Figure 75. Inverting Gain Configuration

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the TAS5721. These capacitors block the DC portion of the audio source and allow the TAS5721 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC gain to 1, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{in}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 24, then the frequency and/or capacitance can be determined when one of the two values is given.

$$fc_{in} = \frac{1}{2\pi \times R_{in} \times C_{in}} \qquad C_{in} = \frac{1}{2\pi \times fc_{in} \times R_{in}} \tag{1}$$

Using the TAS5721 as a Second Order Filter

Several audio DACs used today require an external low-pass filter to remove out of band noise. This is possible with the TAS5721 as it can be used like a standard OPAMP. Several filter topologies can be implemented, both single ended and differential. In the figure below a Multi Feed Back (MFB), with differential input and single ended input is shown.

An AC-coupling capacitor to remove DC-content from the source is shown. It serves to block any DC content from the source and lowers the DC-gain to 1, helping reduce the output dc-offset to a minimum.

The component values can be calculated with the help of the TI FilterPro™ program available on the TI website at: focus.ti.com

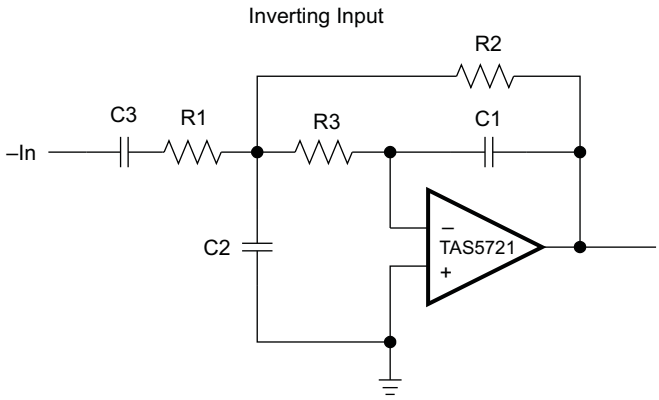


Figure 76. Second-Order Active Low-Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling cap. The C2 can be split in two with the midpoint connected to GND; this can increase the common-mode attenuation.

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{\text{DR\_SD}}$ low during power supply ramp up and down. The pin should be kept low until the input AC-coupling capacitors are fully charged before asserting the $\overline{\text{DR\_SD}}$ pin high, this way proper precharge of the AC-coupling capacitors is performed and pop-less power up is achieved. Figure 77 illustrates the preferred sequence.

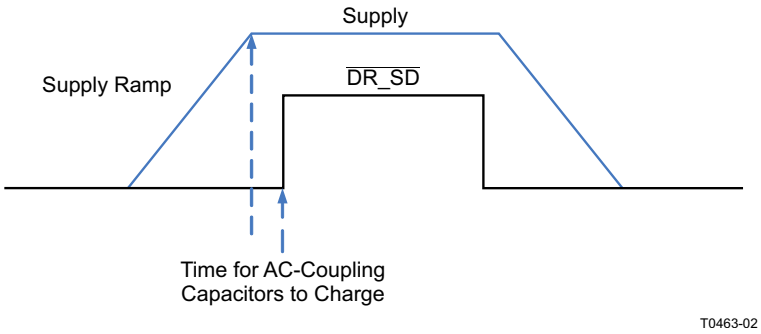


Figure 77. Power Up or Down Sequence

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5721DCA	ACTIVE	HTSSOP	DCA	48	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5721	Samples
TAS5721DCAR	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5721	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

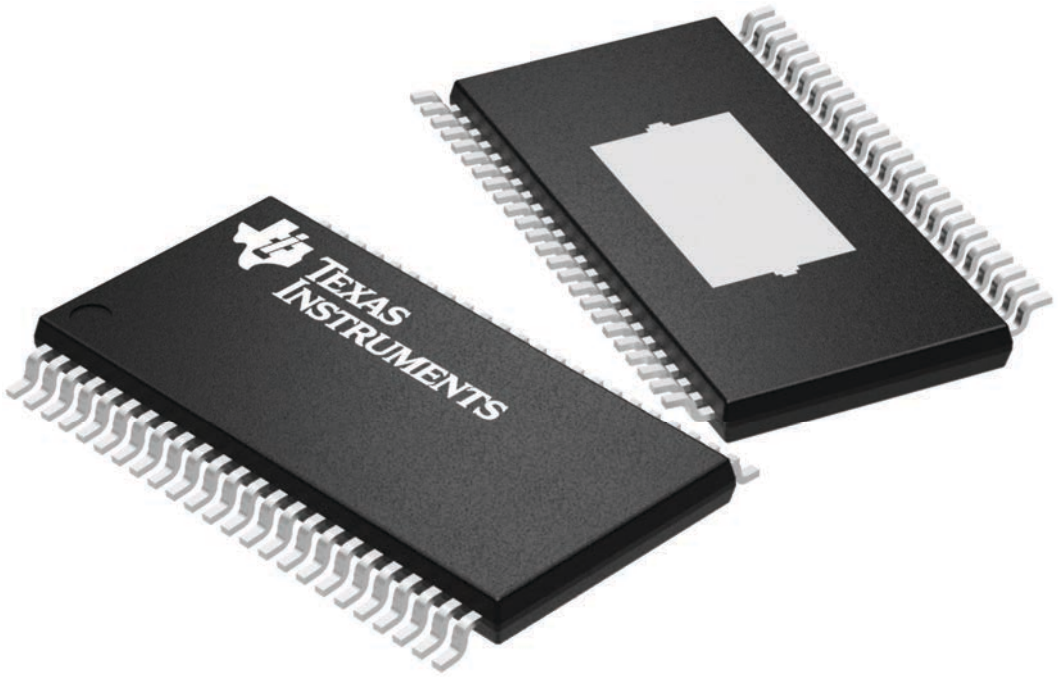
DCA 48

HTSSOP - 1.2 mm max height

12.5 x 6.1, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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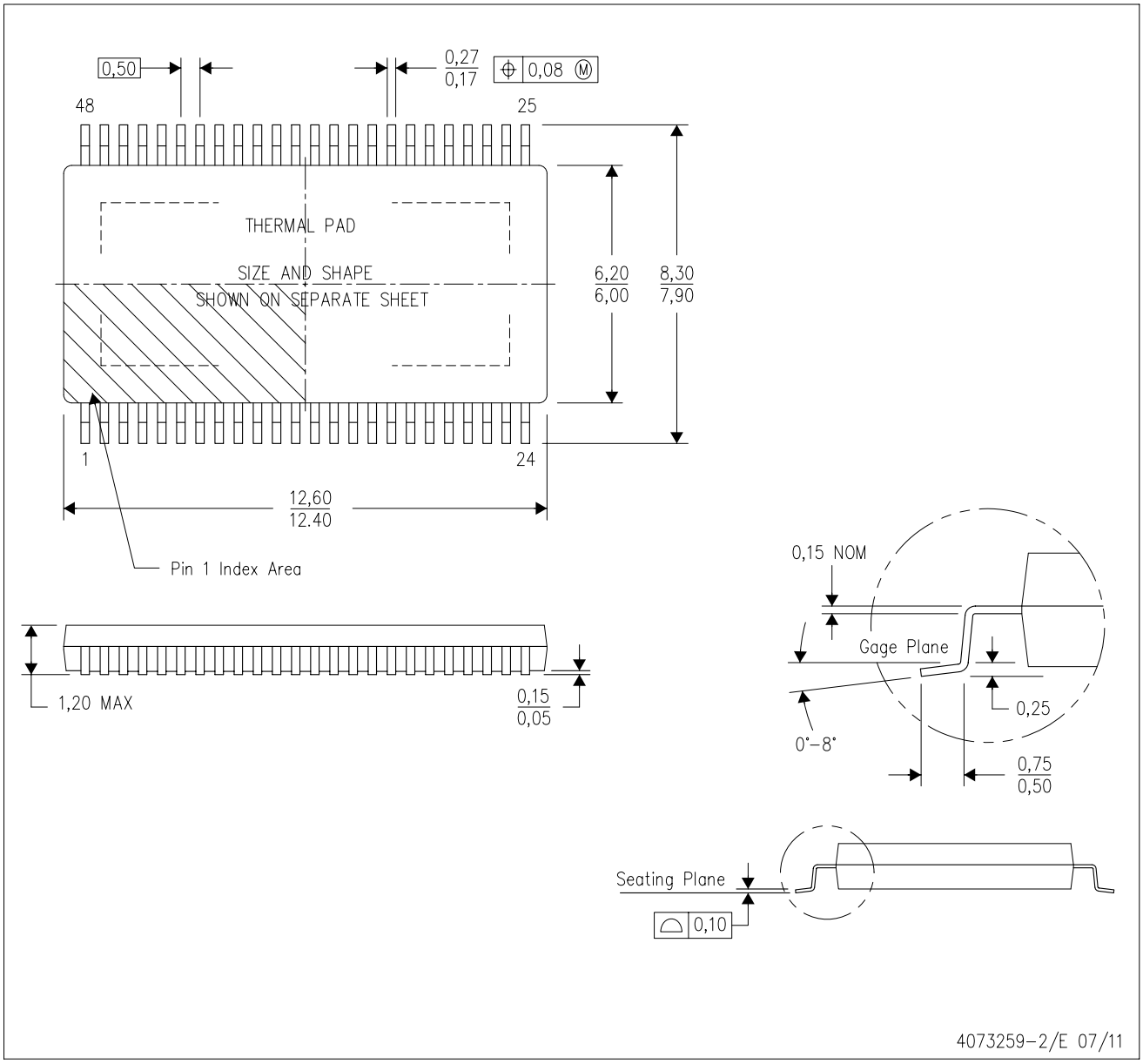
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

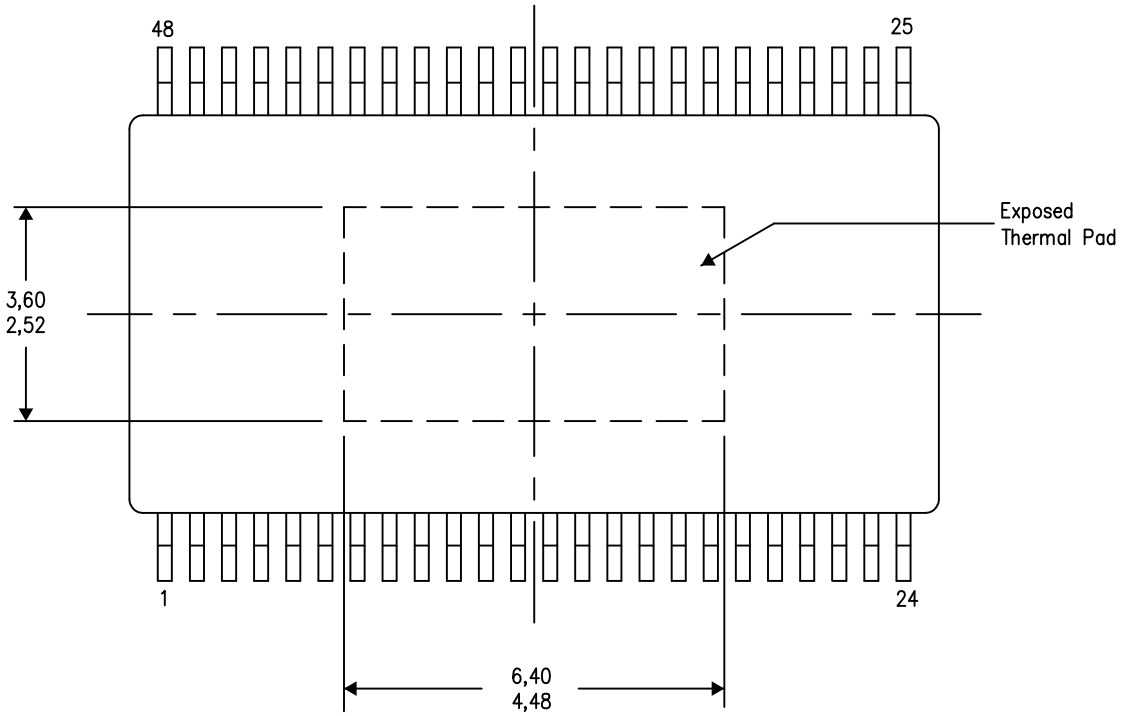
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

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NOTE: A. All linear dimensions are in millimeters

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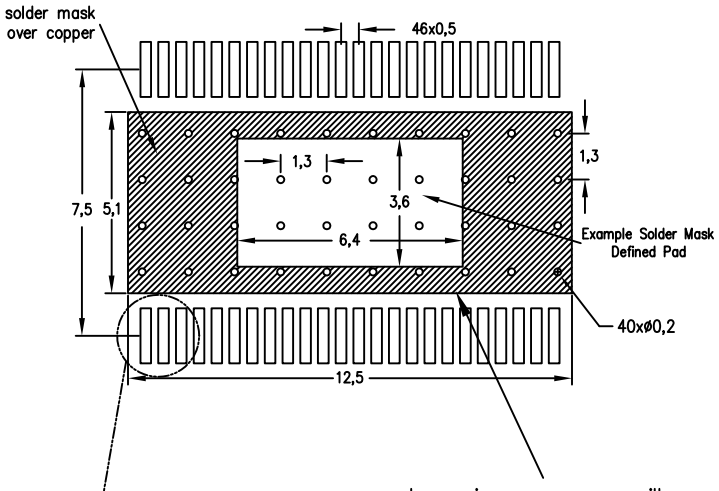
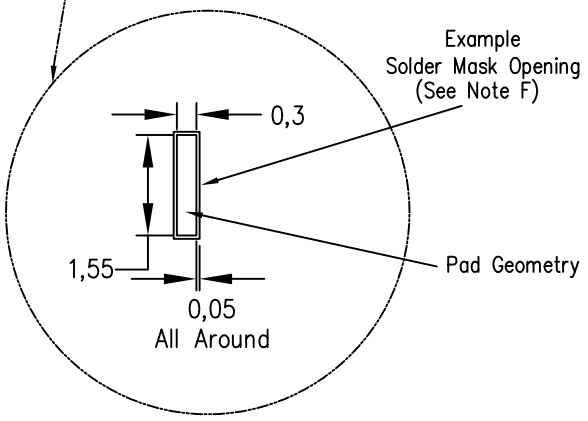
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

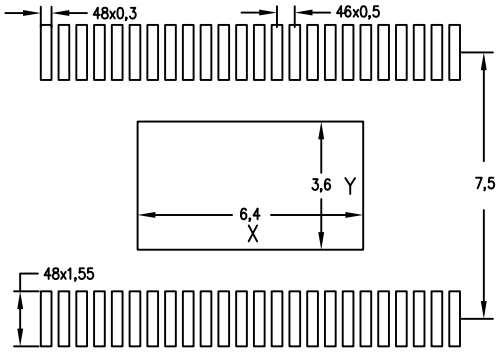


Increasing copper area will
enhance thermal performance
(See Note D)

Example
Non Soldermask Defined Pad



Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



(See Note E)

Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.21	4.06
0.127mm	6.40	3.60
0.152mm	5.85	3.29
0.178mm	5.41	3.04

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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