TCA9509 电平转换 I²C 和 SMBUS 总线中继器

1 特性

- 双通道双向缓冲器
- 与 I²C 总线和 SMBus 兼容
- B 侧的工作电源电压范围为 2.7V 至 5.5V
- A 侧的工作电源电压范围为 0.9V 至 5.5V
- 从 0.9V 至 5.5V 和 2.7V 至 5.5V 的电压电平转换
- 高电平有效中继器使能输入
- 低电压端口 A 上无需使用外部上拉电阻器
- 漏极开路 I²C I/O
- 5.5V 耐压 I²C 和使能输入支持混合模式信号操作
- 无闭锁操作
- 适应标准模式和快速模式 I²C 器件和多个控制器
- 支持中继器上的仲裁及时钟延伸
- 断电高阻抗 I²C 总线引脚
- 支持 400kHz 快速 I²C 总线运行速度
- 可采用
  - 1.6mm × 1.6mm、0.4mm 高度、0.5mm 间距 QFN 封装
  - 3mm × 3mm 业界通用 MSOP 封装
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 带电器件模型 (C101)

2 应用

- 服务器
- 路由器（电信交换设备）
- 工业设备
- 产品包含多个 I²C 目标和/或长 PCB 布线

3 说明

TCA9509 是一款适用于 I²C/SMBus 系统的 I²C 总线/SMBus 中继器。此器件还可在混合模式应用中提供低电压（低至 0.9V）和较高电压（2.7V 至 5.5V）间的双向电压电平转换（上行转换/下行转换）。电平转换期间，这个器件在不损失系统性能的情况下可扩展 I²C 和相似的总线系统。

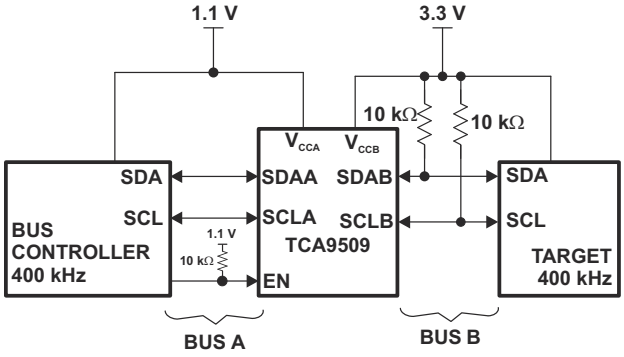
TCA9509 可缓冲 I²C 总线上的串行数据 (SDA) 和串行时钟 (SCL) 信号，因此支持 B 侧 400pF 的总线电容。这款器件也可用于将总线隔离为电压和电容两部分。

TCA9509 具有两类驱动器：A 侧驱动器和 B 侧驱动器。所有输入和 B 侧 I/O 都能够承受 5.5V 的过压。当器件未通电时（VCCB 和/或 VCCA = 0V），A 侧 I/O 也能承受 5.5V 的过压。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TCA9509	VSSOP (8)	3.00mm × 3.00mm
	X2QFN (8)	1.60mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (December 2017) to Revision D (April 2021) **Page**

- 将数据表中的术语*主站和从站* 更改为*控制器和目标* 1
- Changed I_{CC} Quiescent supply current for V_{CCB} MIN value from 0.5 mA to 0.20 mA and the TYP value from 0.9 mA to 0.5 mA in the *Electrical Characteristics* table 6
- Changed text From: "Multiple B-sides of TCA9509 s..." To: "Multiple B-sides of TCA9509..." 13

Changes from Revision B (January 2012) to Revision C (December 2017) **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- Added junction temperature to the *Absolute Maximum Ratings* 5
- Changed thermal information for RVH and DGK packages 6
- Changed V_{ILC}, added Test Conditions with new MIN and TYP values in the *Electrical Characteristics* table 6
- Updated Bus A (0.9-V to 5.5-V Bus) Waveform 7
- Updated Bus B (2.7-V to 5.5-V Bus) Waveform 7

Changes from Revision A (October 2011) to Revision B (January 2012) **Page**

- 向数据表添加了 DGK 封装和封装信息 1

Changes from Revision * (August 2011) to Revision A (October 2011) **Page**

- 将文档中多个实例的 V_{CCA} 工作电压下限更正为 0.9V 1
- 更改了“特性”B 侧的“工作电源电压范围”值错误将“B 侧 0.9V 至 5.5V”更改为“B 侧 2.7V 至 5.5V” 1
- 更改了“特性”A 侧的“工作电压范围”值错误将“A 侧 2.7V 至 V_{CCB} - 1V”更改为“A 侧 0.9V 至 V_{CCB} - 1V” 1

5 Description (continued)

The bus port B drivers are compliant with SMBus I/O levels, while the A-side uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. The A-side uses a 1 mA current source for pull-up and a 200 Ω pull-down driver. This results in a LOW on the A-side accommodating smaller voltage swings. The output pull-down on the A-side internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the A-side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the B-side drives a hard LOW and the input level is set at 0.3 of SMBus or I^2C-bus voltage level which enables B side to connect to any other I^2C-bus devices or buffer.

The TCA9509 drivers are not enabled unless V_{CCA} is above 0.8 V and V_{CCB} is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

6 Pin Configuration and Functions

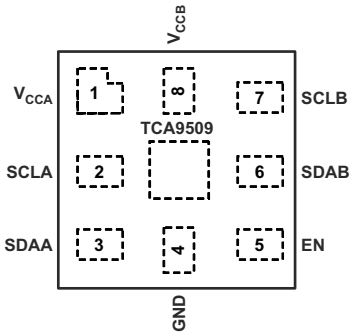


图 6-1. RVH Package, 8-Pin X2QFN, Top View

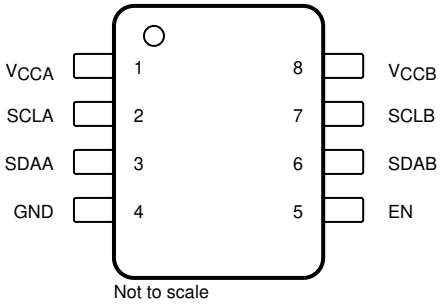


图 6-2. DGK Package, 8-Pin VSSOP, Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{CCA}	1	Supply	A-side supply voltage (0.9 V to 5.5 V)
SCLA	2	I/O	Serial clock bus, A side.
SDAA	3	I/O	Serial data bus, A side.
GND	4	Supply	Supply ground
EN	5	Input	Active-high repeater enable input
SDAB	6	I/O	Serial data bus, B side. Connect to V_{CCB} through a pull-up resistor.
SCLB	7	I/O	Serial clock bus, B side. Connect to V_{CCB} through a pull-up resistor.
V_{CCB}	8	Supply	B-side and device supply voltage (2.7 V to 5.5 V)
Thermal Attach Pad	-	-	Thermal Attach Pad is not electrically connected and it is recommended to be attached to GND for best thermal performance. This is for the RVH package only.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		–0.5	6	V
V_{CCA}	Supply voltage		–0.5	6	V
V_I	Enable input voltage(2)		–0.5	6	V
$V_{I/O}$	I^2C bus voltage(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
P_d	Max power dissipation			100	mW
T_J	Junction temperature			125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.9(1)	5.5	V
V_{CCB}	Supply voltage, B-side bus		2.7	5.5	V
V_{IH}	High-level input voltage	SDAA, SCLA	0.7 × V_{CCA}	V_{CCA}	V
		SDAB, SCLB	0.7 × V_{CCB}	5.5	
		EN	0.7 × V_{CCA}	5.5	
V_{IL}	Low-level input voltage	SDAA, SCLA	–0.5	0.3	V
		SDAB, SCLB	–0.5	0.3 × V_{CCB}	
		EN	–0.5	0.3 × V_{CCA}	
I_{OL}	Low-level output current	SDAA, SCLA		10	µA
		SDAB, SCLB		6	mA
T_A	Operating free-air temperature		–40	85	°C

(1) Low-level supply voltage

7.4 Thermal Information

THERMAL METRIC[1]		TCA9509		UNIT
		RVH (X2QFN)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	160.3	222.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	109.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	115.9	144.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	34.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	116.2	142.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	80.5	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Electrical Characteristics

V_{CCB} = 2.7 V to 5.5 V, V_{CCA} = 0.9 V to (V_{CCB}-1), T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA	–1.5		–0.5	V
V_{OL}	Low-level output voltage	SDAA, SCLA	I_{OL} = 10 µA, V_{ILA} = V_{ILB} = 0 V, V_{CCA} = 0.9 to 1.2 V		0.18	0.25	V
		SDAA, SCLA	I_{OL} = 20 µA, V_{ILA} = V_{ILB} = 0 V, 1.2V < V_{CCA} ≤ (V_{CCB} – 1 V)		0.2	0.3	
V_{OL} – V_{ILc}	Low-level input voltage below low-level output voltage	SDAA, SCLA			50		mV
V_{ILc}	SDA and SCL low-level input voltage contention	SDAA, SCLA	V_{CCA} ≥ 1.5 V and V_{CCB} ≥ 3.15 V	110	150		mV
			V_{CCA} < 1.5 V or V_{CCB} < 3.15 V	50	100		
V_{OLB}	Low-level output voltage	SDAB, SCLB	I_{OL} = 6 mA		0.1	0.2	V
I_{CC}	Quiescent supply current for V_{CCA}		All port A Static high	0.25	0.45	0.9	mA
			All port A Static low	1.25			
I_{CC}	Quiescent supply current for V_{CCB}		All port B Static high	0.2	0.5	1.1	mA
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}			±1	µA
			V_I = 0.2 V			10	
		SDAA, SCLA	V_I = V_{CCA}			±1	
			V_I = 0.2 V			10	
		EN	V_I = V_{CCB}			±1	
			V_I = 0.2 V			–10	
I_{OH}	High-level output leakage current	SDAB, SCLB	V_O = 3.6 V			10	µA
		SDAA, SCLA				10	
C_{IOA}	I/O capacitance of A-side	SCLA, SDAA	V_I = 0 V		6.5	7	pF
C_{IOB}	I/O capacitance of B-side	SCLB, SDAB	V_I = 0 V	5.5		6.2	pF

7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition(1)	100		ns
t_h	Hold time, EN high after Stop condition(1)	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

7.7 I²C Interface Timing Requirements

T_A = – 40°C to 85°C (unless otherwise noted)

PARAMETER			V_{CCA} (INPUT)	V_{CCB} (OUTPUT)	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PHL}	Propagation delay	port A to port B	1.9 V	5 V	EN High	123.1	127.2	132.8	ns
		port B to port A				88.1	88.8	89.8	
t_{PLH}	Propagation delay	port A to port B	1.9 V	5 V	EN High	122.6	125.7	131.7	ns
		port B to port A				123	124.1	126.9	
t_{rise}	Transition time	port A	1.9 V	5 V	EN High	40.1	40.9	41.9	ns
		port B				57.3	57.5	58.4	
t_{fall}	Transition time	port A	1.9 V	5 V	EN High	14.5	16.4	17.9	ns
		port B				18.7	19.4	20.2	
t_{PLH2}	Propagation delay 50% of initial low on Port A to 1.5 V on Port B	port A to port B	1.9 V	5 V		176	177.3	178	ns
f_{MAX}	Maximum switching frequency					400			KHz

(1) Typical values were measured with V_{CCA} = V_{CCB} = 2.7 V at T_A = 25°C, unless otherwise noted.

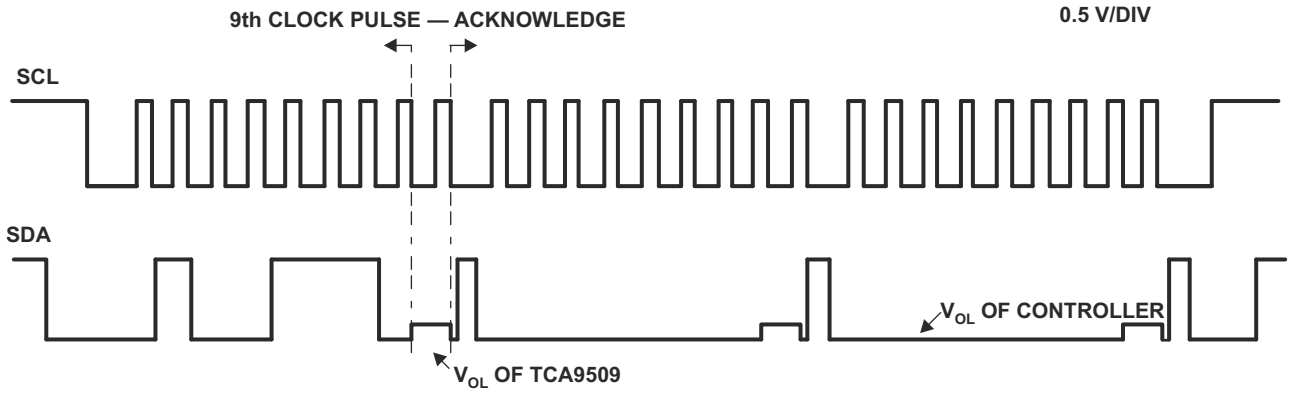


图 7-1. Bus A (0.9-V to 5.5-V Bus) Waveform

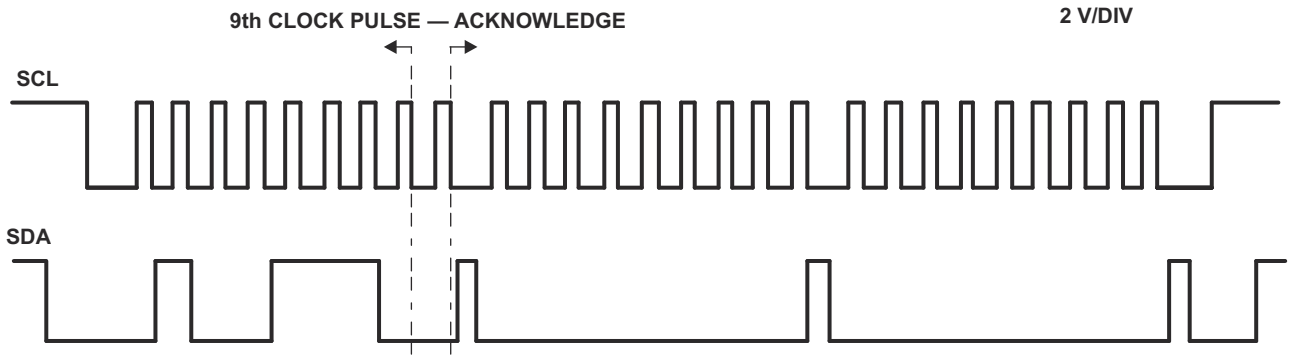
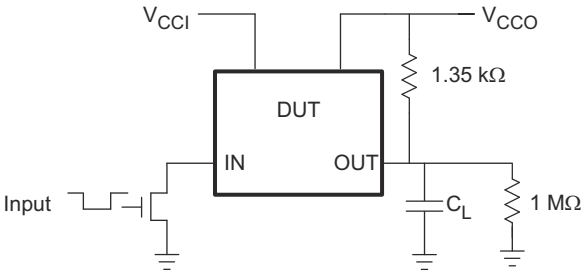
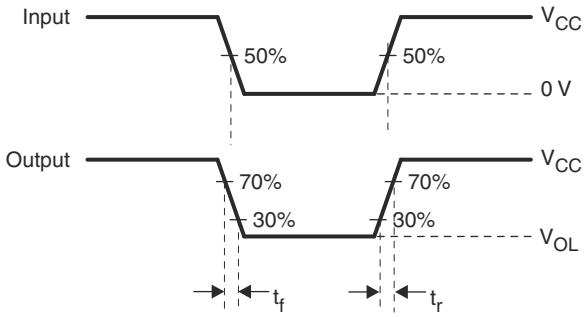


图 7-2. Bus B (2.7-V to 5.5-V Bus) Waveform

8 Parameter Measurement Information



PIN	C_L
SCLA, SDAA (A-side)	50 pF
SDAB, SCLB (B-side)	50 pF



A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
B. C_L includes probe and jig capacitance.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, Z_O = 50 Ω, slew rate ⩾ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

图 8-1. Test Circuit and Voltage Waveforms

9 Detailed Description

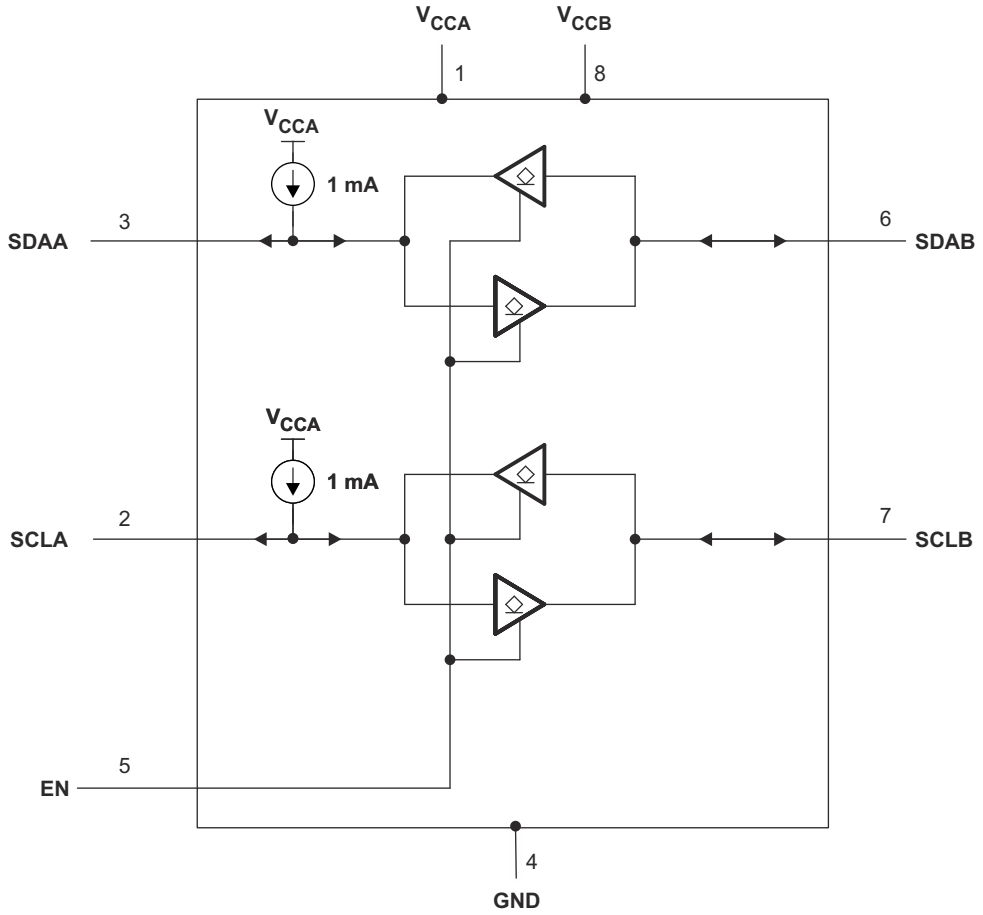
9.1 Overview

This TCA9509 integrated circuit is an I^2C bus/SMBus Repeater for use in I^2C/SMBus systems. It can also provide bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I^2C and similar bus systems to be extended, without degradation of performance even during level shifting.

The TCA9509 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I^2C bus, thus allowing 400-pF bus capacitance on the B-side. This device can also be used to isolate two halves of a bus for voltage and capacitance.

The TCA9509 has two types of drivers – A-side drivers and B-side drivers. All inputs and B-side I/O’s are overvoltage tolerant to 5.5V. The A-side I/O’s are overvoltage tolerant to 5.5 V when the device is unpowered (V_{CCB} and/or V_{CCA} = 0V).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Two-Channel Bidirectional Buffer

The TCA9509 is a two-channel bidirectional buffer with level-shifting capabilities, featuring an integrated current source on the A-side.

9.3.2 Integrated A-Side Current Source

The A-side ports of the TCA9509 feature an integrated 1 mA current source, eliminating the need for external pull-up resistors on SDAA and SCLA.

9.3.3 Standard Mode and Fast Mode Support

The TCA9509 supports standard mode as well as fast mode I^2C. The maximum system operating frequency will depend on system design and delays added by the repeater.

9.4 Device Functional Modes

表 9-1 lists the functional modes for the TCA9509.

表 9-1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TCA9509 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the B-side of the TCA9509 is pulled low by a driver on the I^2C bus and the falling edge goes below 0.3 V_{CCB}, it causes the internal driver on the A-side to turn on, causing the A-side to pull down to about 0.2 V (V_{OL}). When the A-side of the TCA9509 falls, a comparator detects the falling edge and causes the internal driver on the B-side to turn on and pull the B-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to 图 7-1. If the bus controller in 图 10-1 were to write to the target through the TCA9509, waveforms shown in 图 7-2 would be observed on the B bus. This looks like a normal I^2C bus transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the A-side bus of the TCA9509, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9509. After the eighth clock pulse, the data line is pulled to the V_{OL} of the controller device, which is close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9509 for a short delay, while the B-bus side rises above 0.3 V_{CCB} and then continues high. It is important to note that any arbitration or clock stretching events require that the low level on the A-bus side at the input of the TCA9509 (V_{IL}) be at or below V_{ILC} to be recognized by the TCA9509 and then transmitted to the B-bus side.

10.2 Typical Application

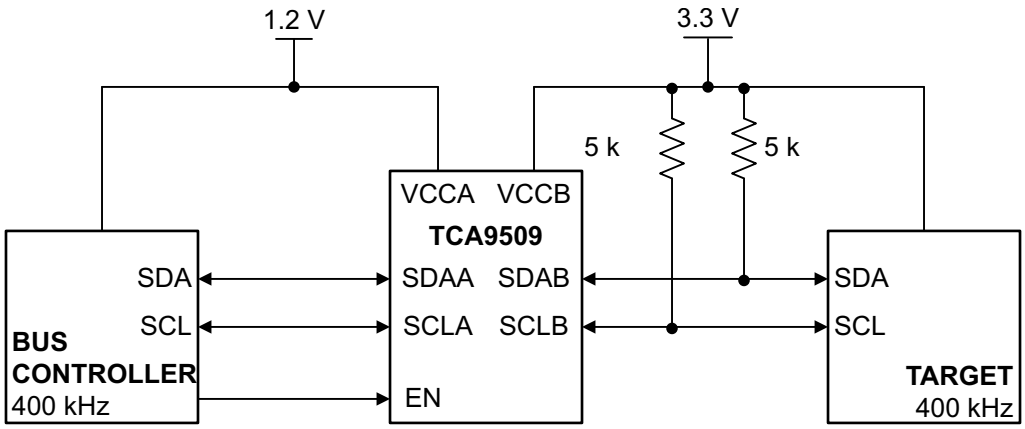


图 10-1. Typical Application, A-side Connected to controller

10.2.1 Design Requirements

A typical application is shown in 图 10-1. In this example, the system controller is running on a 1.2-V I^2C bus, and the target is connected to a 3.3-V bus. Both buses run at 400 kHz. Controller devices can be placed on either bus. For the level translating application, the following should be true: $V_{CCA} \leq (V_{CCB} - 1\ V)$

- V_{CCA} = 0.9 V to 5.5 V
- V_{CCB} = 2.7 to 5.5 V
- A-side ports must not be connected together

- Pullup resistors should not be placed on the A-side ports

10.2.2 Detailed Design Procedure

10.2.2.1 Clock Stretching Support

The TCA9509 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the target and controller. This is best done by increasing the pull-up resistor value on B-side ports.

10.2.2.2 V_{ILC} and Pulldown Strength Requirements

For the TCA9509 to function correctly, all devices on the A-side must be able to pull the A-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the A-side must be below V_{ILC} min.

The V_{OL} can be adjusted by changing the I_{OL}through the device which is set by the pull-up resistance value. The pull-up resistance on the A-side must be carefully selected to ensure that the logic levels will be transferred correctly to the B-side.

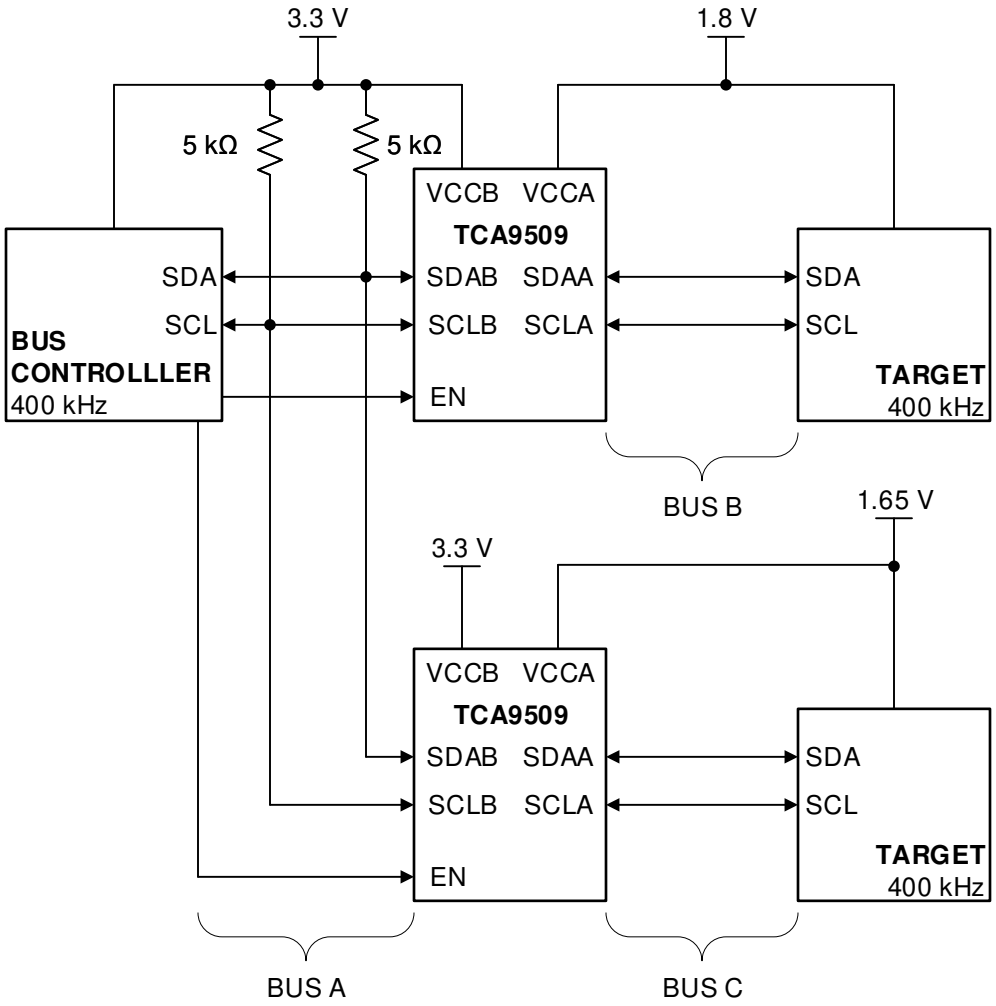


图 10-2. Typical Star Application

Multiple B-sides of TCA9509 can be connected in a star configuration, allowing all nodes to communicate with each other. The A-sides should not be connected together when used in a star/parallel configuration.

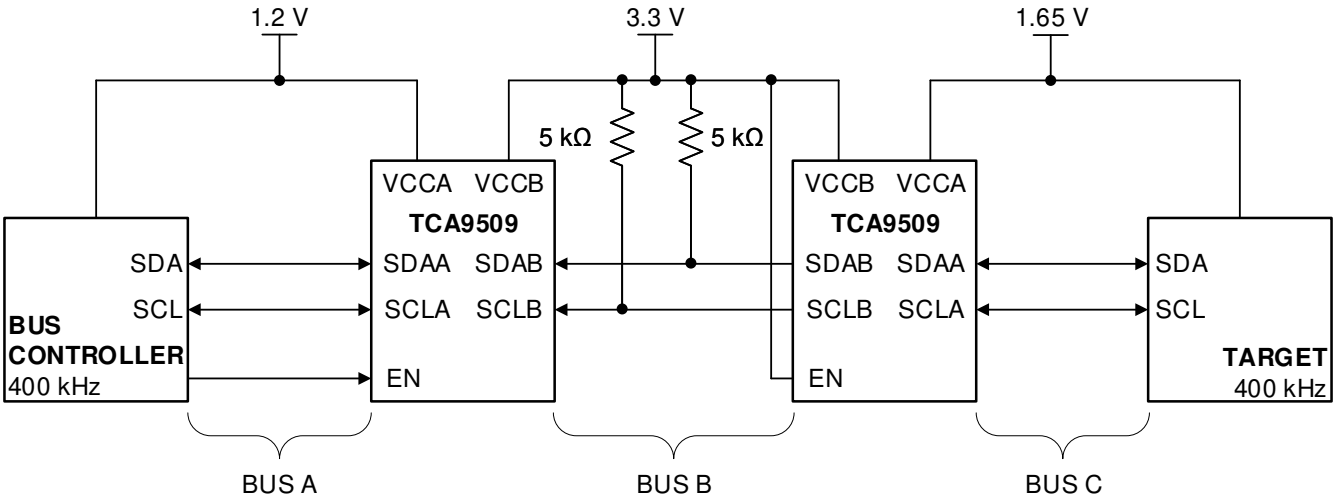


图 10-3. Typical Series Application, Two B-Sides Connected Together

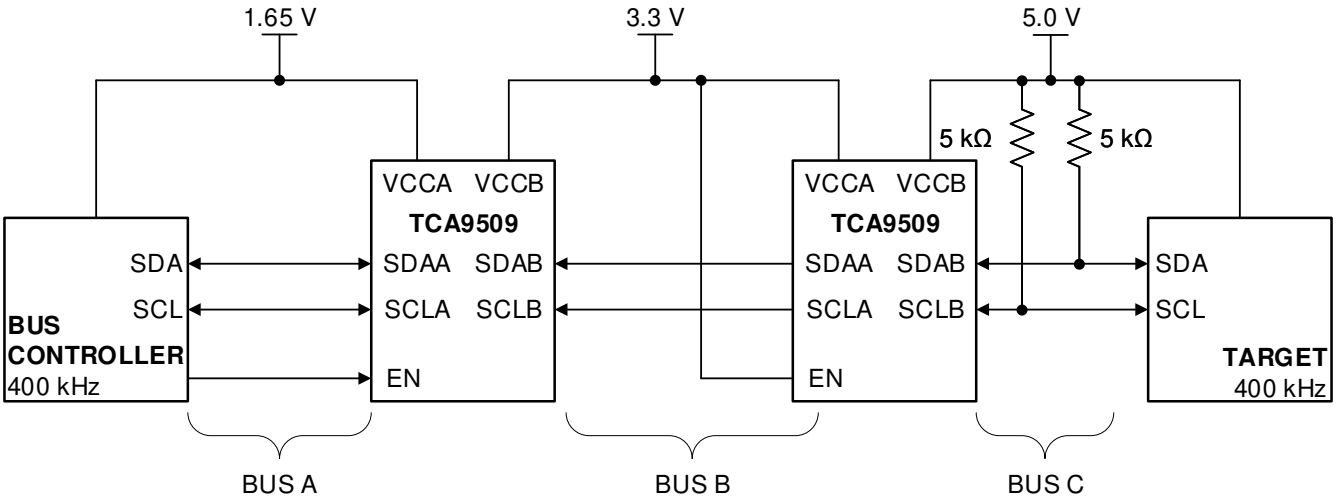


图 10-4. Typical Series Application, A-side Connected to B-Side

To further extend the I^2C bus for long traces/cables, multiple TCA9509 devices can be connected in series as long as the A-side is connected to the B-side and $V_{CCA} \leq (V_{CCB} - 1\ V)$ must also be met. Series connections can also be made by connecting both B-sides together while following power supply rule $V_{CCA} \leq (V_{CCB} - 1\ V)$. I^2C bus target devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

11 Power Supply Recommendations

V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9509 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. After power up and with the EN high, a low level on the B-side (below 0.3 × V_{CCB}) turns the corresponding A-side driver (either SDA or SCL) on and drives the A-side down to approximately 0.2 V. When the B-side rises above 0.3 × V_{CCB}, the A-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the A-side falls first and goes below 0.3 × V_{CCA}, the B-side driver is turned on and the B-side pulls down to 0 V. The A-side pull-down is not enabled unless the A-side voltage goes below 0.4 V. If the A-side low voltage does not go below 0.5 V, the B-side driver turns off when the A-side voltage is above 0.7 × V_{CCA}. If the A-side low voltage goes below 0.4 V, the A-side pull-down driver is enabled, and the A-side is able to rise to only 0.5 V until the B-side rises above 0.3 × V_{CCB}.

A 100 nF a decoupling capacitor should be placed as close to the V_{CCA} and V_{CCB} pins in order to provide proper filtering of supply noise.

12 Layout

12.1 Layout Guidelines

There are no special layout procedures required for the TCA9509.

It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

12.2 Layout Example

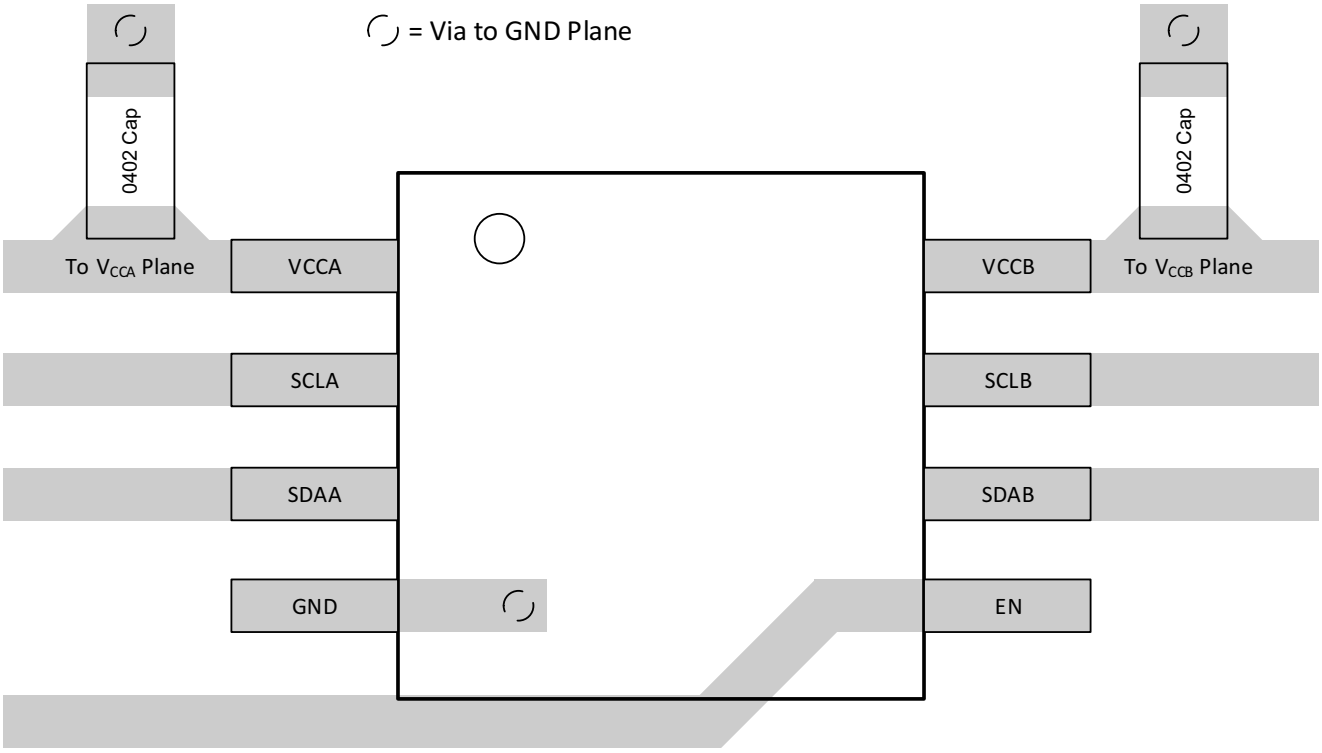


图 12-1. Example Layout

13 Device and Documentation Support

13.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.3 Trademarks

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13.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9509DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 85	(7KO, 7KQ)	Samples
TCA9509MRVHR	ACTIVE	X2QFN	RVH	8	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K	Samples
TCA9509RVHR	ACTIVE	X2QFN	RVH	8	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	7K	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

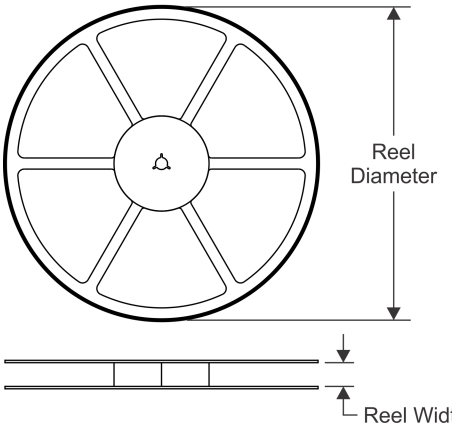
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

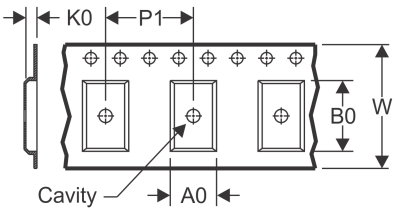
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

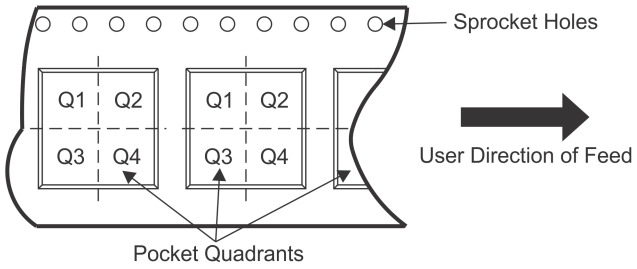


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

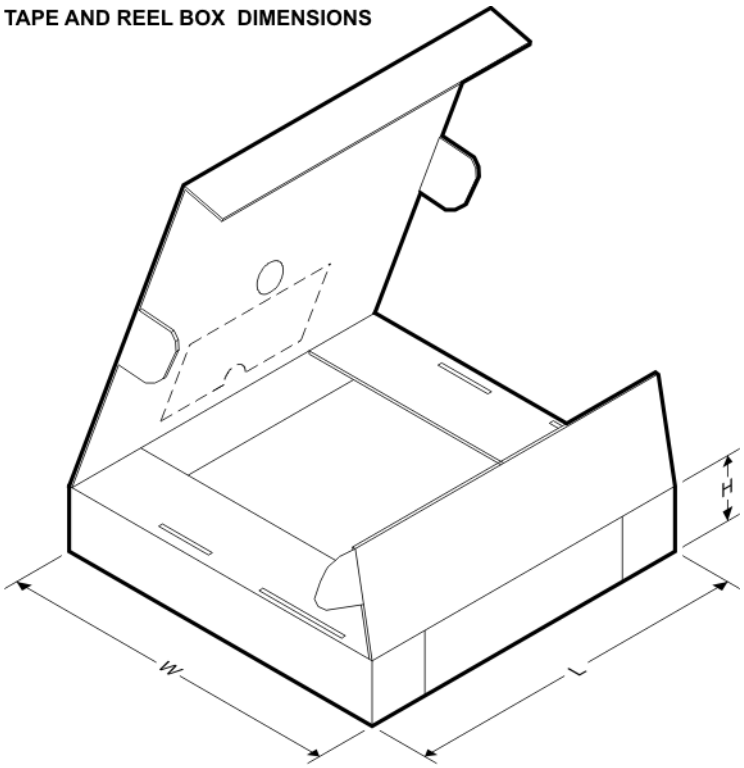
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9509DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TCA9509MRVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q1
TCA9509RVHR	X2QFN	RVH	8	5000	180.0	8.4	1.8	1.8	0.5	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

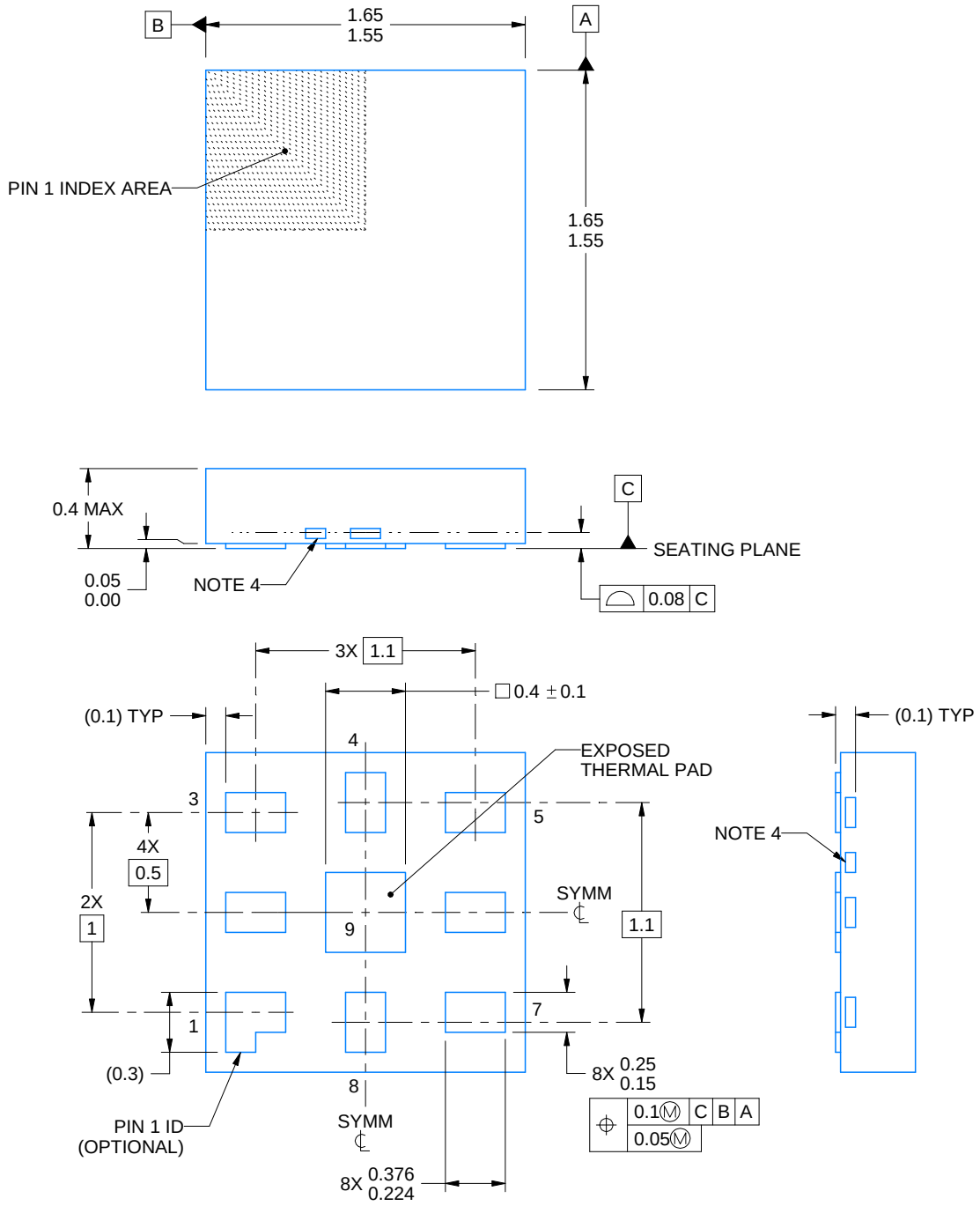
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9509DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TCA9509MRVHR	X2QFN	RVH	8	5000	183.0	183.0	20.0
TCA9509RVHR	X2QFN	RVH	8	5000	202.0	201.0	28.0

PACKAGE OUTLINE

RVH0008A

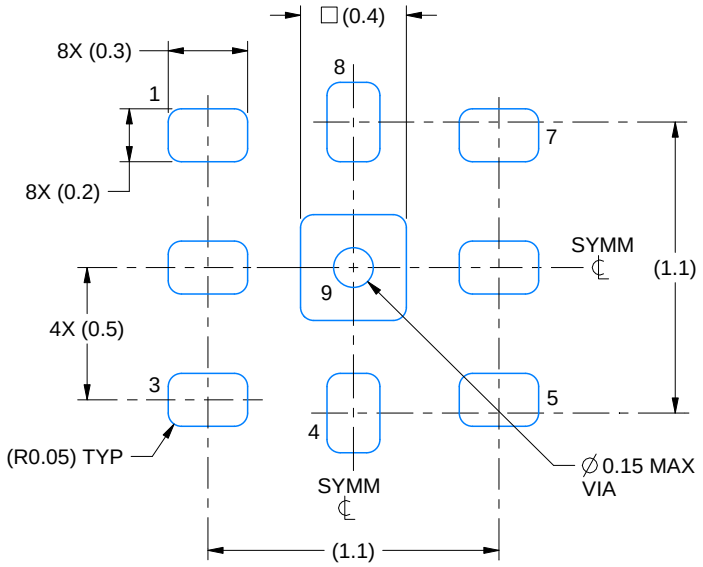
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

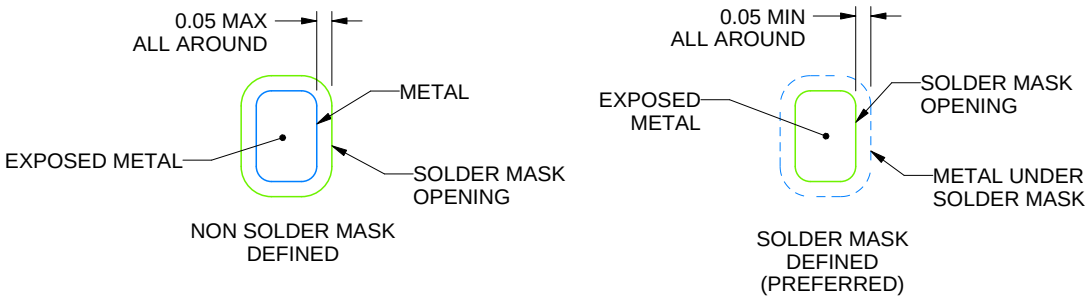


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed tie bars may vary in size and location.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:35X



SOLDER MASK DETAILS

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NOTES: (continued)

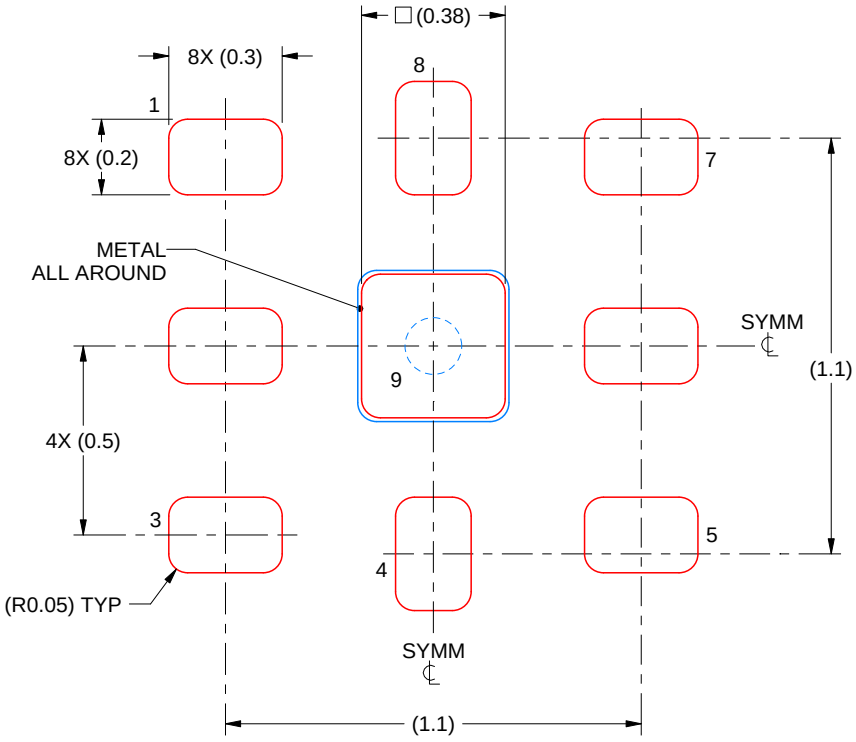
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RVH0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

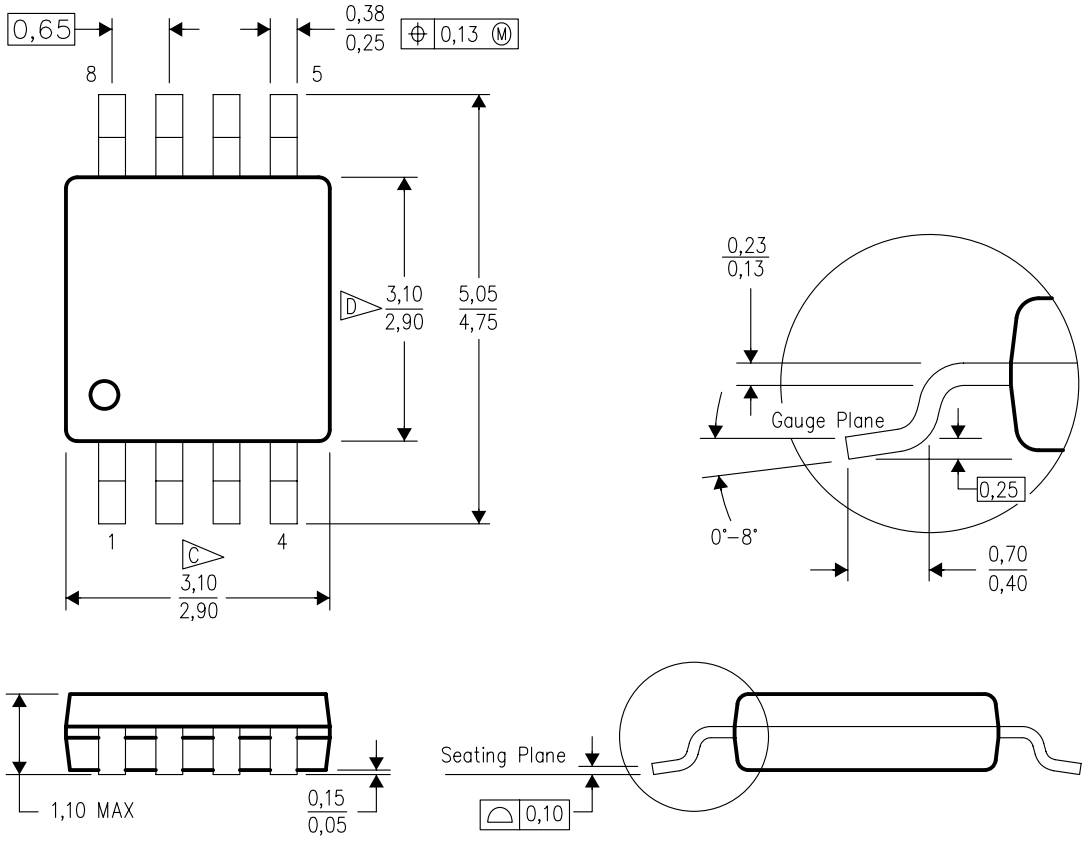
EXPOSED PAD 9
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4219153/B 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

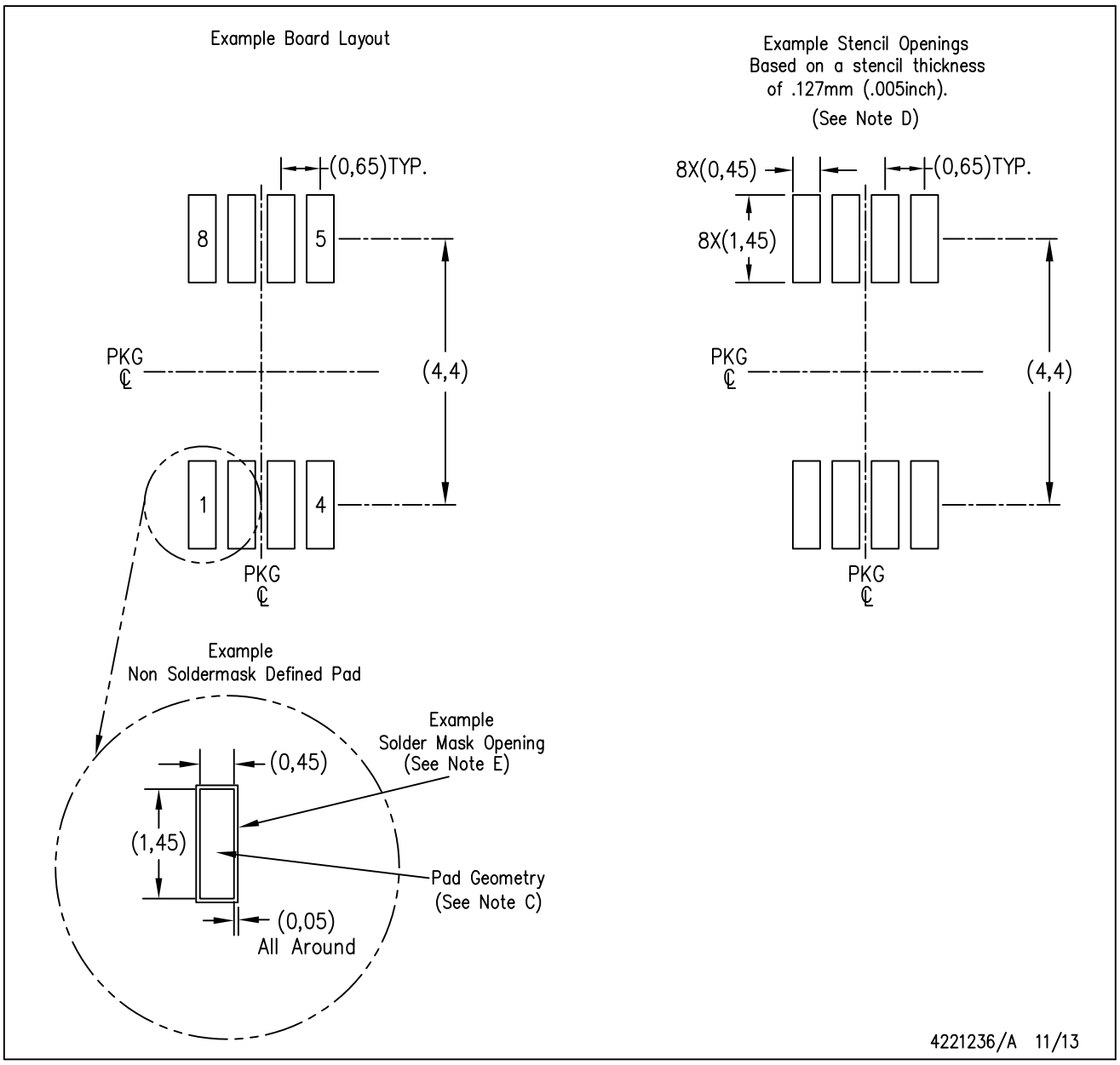
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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