采用小型封装且具有低残余电压和集成浪涌保护功能的 TIOL112 和 TIOL112x IO-Link 器件收发器

1 特性

- 7V 至 36V 电源电压
- PNP、NPN 或 IO-Link 可配置输出
  - IEC 61131-9 COM1、COM2 和 COM3 数据速率支持
- 功能安全型
  - 可提供用于功能安全系统设计的文档
- 与 TIOL111(x) 引脚兼容，并提升了性能
  - 在 200mA 条件下，残余电压低，为 0.5V（典型值）
  - 有效驱动器电流限制能力
  - 改善了封装的热性能
  - 更低的驱动器压摆率，以减少过冲：最大 750ns
- 使系统更加稳健的集成保护特性
  - 可配置驱动器过流限制：50mA 至 350mA
  - L+、CQ 和 L- 上高达 65V 的有效反极性保护
  - 过流、过热和 UVLO 的故障指示灯
  - 电感性负载的安全快速消磁功能
  - 工作环境温度：-40°C 至 125°C
- L+ 和 CQ 上的集成式 EMC 保护
  - ±8 kV IEC 61000-4-2 ESD 接触放电
  - ±4kV IEC 61000-4-4 电气快速瞬变
  - ±1.2kV/500Ω IEC 61000-4-5 浪涌
- 较大电容性负载驱动能力
- < 2μA CQ 泄露电流
- < 1.5mA 静态电源电流
- 集成式 LDO 选项可支持高达 20mA 的电流
  - TIOL1123：3.3V LDO
  - TIOL1125：5V LDO
  - TIOL1123L (YAH)：可选 3.3V/5V 输出
- 远程唤醒指示和唤醒生成
- 节省空间的小型封装选项
  - 3mm x 3mm 10 引脚 VSON 封装：与 TIOL111 引脚兼容
  - 2.45 mm x 1.7 mm DSBGA 封装

2 应用

- 现场发送器和执行器
- 工厂自动化
- 过程自动化
- 远程 IO 中的 IO-Link PHY

3 说明

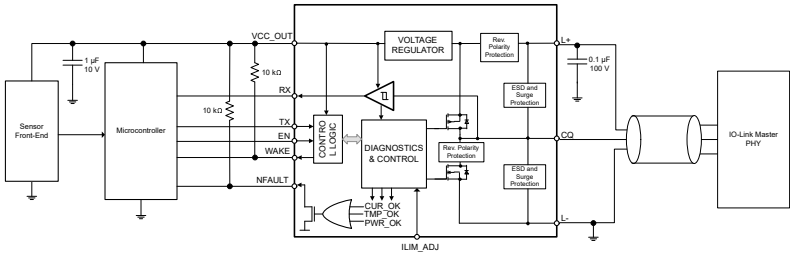
TIOL112(x) 系列收发器使用 IO-Link 接口实现工业双向点到点通信。当此器件通过一个三线制接口连接至一个 IO-Link 主器件时，主器件能够发起通信并与远程节点交换数据，而此时 TIOL112(x) 则用作一个用于通信的完整物理层。

这些器件能够承受高达 1.2kV (500Ω) 的 IEC 61000-4-5 浪涌，并集成反向极性保护功能。只需通过一个简单的引脚可编程接口，便可轻松连接到控制器电路。可使用外部电阻器配置输出电流限值。TIOL112(x) 可配置为生成唤醒脉冲并用于 IO-link 主应用。针对欠压、过流和过热情况提供了故障报告和内部保护功能。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TIOL112	VSON (10)	3.00mm x 3.00mm
TIOL1123		
TIOL1125		
TIOL112	DSBGA (12)	2.45mm x 1.70mm
TIOL1123		

(1) 如需了解所有可订购器件，请参阅数据表末尾的可订购产品附录。



典型应用图

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4 Revision History

Changes from Revision B (December 2022) to Revision C (January 2023) **Page**

- 删除了*器件信息*表中 DSBGA 封装的*预告信息*注释 ... 1

Changes from Revision A (April 2022) to Revision B (December 2022) **Page**

- Removed the conditional note 2 from the *IEC Ratings - ESD Specifications* table that specified 4.5kV when EN=TX=HIGH ... 5
- Changed the description of $I_{(VCC\_OUT)}$ from: (TIOL112L only) to: TIOL1123(L), TIOL1125 only in the *Recommended Operating Conditions* table ... 5
- Changed 图 6-4 and 图 6-6 ... 9
- Added application curves Figure 9-6 and Figure 9-7 showing inductive load demagnetization ... 24

Changes from Revision * (February 2022) to Revision A (April 2022) **Page**

- 删除了*器件信息*表中 VSON 封装的 TIOL112 和 TIOL1125 *预告信息*注释 ... 1

5 Pin Configuration and Functions

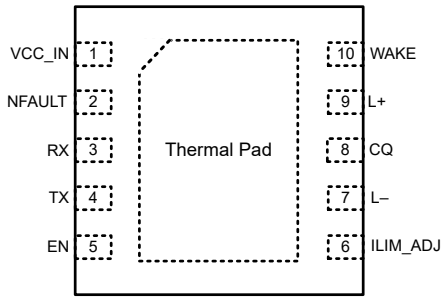


图 5-1. TIOL112
DRC (VSON), 10-Pin
(Top View)

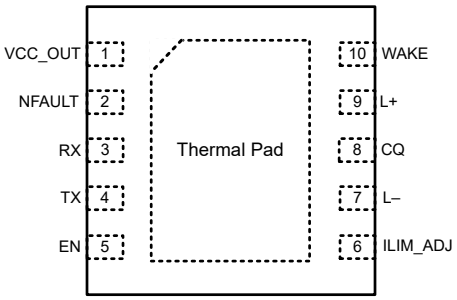


图 5-2. TIOL1123, TIOL1125
DRC (VSON), 10-Pin
(Top View)

表 5-1. Pin Functions (VSON Package)

PIN NO	PIN NAME		TYPE	DESCRIPTION
	TIOL112	TIOL1123 TIOL1125		
1	VCC_IN	VCC_OUT	P	VCC_IN (TIOL112): External 3.3-V or 5-V logic supply input pin. VCC_OUT (TIOL1123, TIOL1125): 3.3-V or 5-V linear regulator output
2	NFAULT	NFAULT	O	Fault indicator output signal to the microcontroller. A low level indicates either an over- current, an undervoltage supply or an overtemperature condition.
3	RX	RX	O	Receive data output to the local microcontroller
4	TX	TX	I	Transmit data input from the local microcontroller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
5	EN	EN	I	Driver enable input signal from the local microcontroller. Logic low sets the CQ output at Hi-Z. Weak internal pull-down.
6	ILIM_ADJ	ILIM_ADJ	I	Input for current limit adjustment. Connect resistor R_{SET} between ILIM_ADJ and L-.
7	L-	L-	GND	IO-Link ground potential
8	CQ	CQ	I/O	IO-Link data signal (bidirectional)
9	L+	L+	P	IO-Link supply voltage (24 V nominal)
10	WAKE	WAKE	O	Wake-up indicator to the local microcontroller. Open-drain output, connect this pin via pull-up resistor to VCC_IN/OUT.
	Thermal Pad	Thermal Pad	—	Connect to L- for optimal thermal and electrical performance

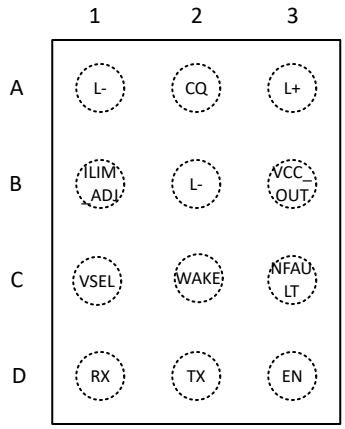


图 5-3. TIOL1123L YAH (DSBGA), 12-Pin (Top View)

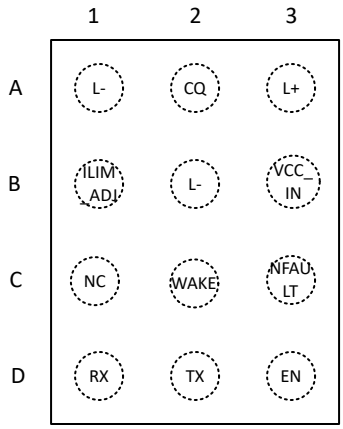


图 5-4. TIOL112 YAH (DSBGA), 12-Pin (Top View)

表 5-2. Pin Functions (DSBGA)

PIN NO	PIN NAME		TYPE	DESCRIPTION
	TIOL112	TIOL1123L		
B3	VCC_IN	VCC_OUT	P	**VCC_IN (TIOL112)**: External 3.3-V or 5-V logic supply input pin. **VCC_OUT (TIOL1123)**: 3.3-V or 5-V linear regulator output
C3	NFAULT	NFAULT	O	Fault indicator output signal to the microcontroller. A low level indicates either an over- current, an undervoltage supply or an overtemperature condition.
D1	RX	RX	O	Receive data output to the local controller
D2	TX	TX	I	Transmit data input from the local controller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
D3	EN	EN	I	Driver enable input signal from the local controller. Logic low sets the CQ output at Hi-Z. Weak internal pull-down.
B1	ILIM_ADJ	ILIM_ADJ	O	Input for current limit adjustment. Connect resistor R_{SET} between ILIM_ADJ and L-.
A1, B2	L-	L-	GND	IO-Link ground potential
A2	CQ	CQ	I/O	IO-Link data signal (bidirectional)
A3	L+	L+	P	IO-Link supply voltage (24 V nominal)
C1	NC	VSEL	I	**TIOL112 (NC):** Leave floating. Do not connect. **TIOL1123 (VSEL)**: Connect to GND for 5V LDO output. Please leave this pin floating for 3.3V LDO output. VSEL has an internal pull-up of 1 MΩ
C2	WAKE	WAKE	O	Wake-up indicator to the local controller. Open-drain output, connect this pin via pull-up resistor to VCC_IN/OUT.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	Steady state voltage for L+ and CQ	–65	65	V
	Transient pulse width < 100 µs for L+ and CQ	–70	70	V
Voltage difference	$\lvert V_{(L+)} - V_{(CQ)} \rvert$		65	V
Logic supply voltage (TIOL112)	VCC_IN	–0.3	6	V
Input logic voltage	TX, EN, VSEL	–0.3	min(VCC_IN+ 0.3, 6)	V
Output current	RX, WAKE, NFAULT	–5	5	mA
Storage temperature, T_{stg}		-55	170	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute maximum ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime. All voltages are with reference to the L- pin, unless otherwise specified.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±4000	V
$V_{(ESD)}$	Electrostatic discharge	Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	All pins	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), L+, CQ and L- (1)	±8,000	V
	Electrostatic discharge	IEC 61000-4-5, 1.2 µs/50 µs Surge with 500 Ω in series, L+, CQ and L- (1)	±1,200	
	Electrostatic discharge	IEC 61000-4-4 EFT (Fast transient or burst), L+, CQ and L- (1)	±4,000	

(1) Minimum 100-nF capacitor is required between L+ and L-. Minimum 1-µF capacitor is required between VCC_IN/VCC_OUT and L-.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(L+)}$	Supply voltage		7	24	36	V
$V_{(VCC\_IN)}$	Logic level input voltage (TIOL112 only)	3.3 V configuration	3	3.3	3.6	V
		5 V configuration	4.5	5	5.5	V
R_{SET}	External resistor for CQ current limit		0		110	kΩ
$1/t_{BIT}$	Data rate (Communication mode)				250	kbps
$I_{(VCC\_OUT)}$	LDO output current (TIOL1123(L), TIOL1125 only)				20	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Junction temperature				150	°C

6.5 Thermal Information

THERMAL METRIC(1)		TIOL112, TIOL1123, TIOL1125	TIOL112, TIOL1123L	UNIT
		DRC (10 Pins)	YAH (12 Pins)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	79.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.9	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.9	19.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.8	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at L_+ = 24 V, V_{VCC_IN} = 3.3 V, V_{VCC_OUT} = 3.3 V and T_A = 25 ℃ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (L+)						
$I_{(L+)}$	Quiescent supply current	EN = LOW, no load		1	1.5	mA
		EN = HIGH, no load		2	2.95	mA
LOGIC-LEVEL INPUTS (EN, TX, VSEL)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2			V
R_{PD}	Pull-down (EN) resistance			100		kΩ
R_{PU}	Pull-up (TX) resistance			200		kΩ
R_{PU}	Pull-up (VSEL) resistance			1000		kΩ
CONTROL OUTPUTS (WAKE, NFAULT)						
V_{OL}	Output logic low voltage	I_O = 4 mA			0.5	V
I_{OZ}	Output high impedance leakage	Output in Hi-Z, V_O = 0 V or VCC_IN/OUT	–1		1	µA
DRIVER OUTPUT (CQ)						
$R_{DS(ON)}$	High-side driver on-resistance			2.5	4.5	Ω
$V_{DS(ON)}$	High-side driver residual voltage	I = 200 mA		0.5	0.9	V
		I = 100 mA		0.25	0.5	V
$R_{DS(ON)}$	Low-side driver on-resistance			2.5	4.5	Ω
$V_{DS(ON)}$	Low-side driver residual voltage	I = 200 mA		0.5	0.9	V
		I = 100 mA		0.25	0.5	V
$I_{OZ(CQ)}$	CQ leakage	EN = LOW, 0 ≤ $V_{(CQ)}$ ≤ ($V_{(L+)}$ - 0.1 V)	–2		2	µA
I_{LLM}	CQ load discharge current	EN = LOW, R_{SET} = 0 to 5 kΩ (2), $V_{(CQ)}$ >= 5 V	5		15	mA
$I_{O(LIM)}$	Driver output current limit	R_{SET} = 110 kΩ ; $V_{(CQ)}$= (V_{L+} - 3) V or 3 V	35	50	70	mA
		R_{SET} = 10 kΩ	300	350	400	mA
		R_{SET} = 0 to 5 kΩ (2) $V_{(CQ)}$= (V_{L+} - 3) V or 3 V T_J < $T_{(SDN)}$ or t < 200 µs (3)	500			mA
		(Fast-detect mode) R_{SET} = OPEN(1) $V_{(CQ)}$= (V_{L+} - 3) V or 3 V	260	330	400	mA
RECEIVER INPUT (CQ)						
$V_{(THH)}$	Input threshold “H”	$V_{(L+)}$ > 18 V, EN= LOW	10.5		13	V
$V_{(THL)}$	Input threshold “L"		8		11.5	V
$V_{(HYS)}$	Receiver Hysteresis ($V_{(THH)}$ - $V_{(THL)}$)			0.75		V
$V_{(THH)}$	Input threshold “H”	$V_{(L+)}$ < 18 V, EN= LOW	See Note (4)		See Note (5)	V

6.6 Electrical Characteristics (continued)

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at L_+ = 24 V, V_{VCC_IN} = 3.3 V, V_{VCC_OUT} = 3.3 V and T_A = 25 ℃ unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(THL)}$	Input threshold "L"	$V_{(L+)}$ < 18 V, EN= LOW		See Note (6)		See Note (7)	V
$V_{(HYS)}$	Receiver Hysteresis ($V_{(THH)}$ - $V_{(THL)}$)				0.75		V
V_{OL}	RX output low voltage	I_{OL} = 4 mA				0.4	V
V_{OH}	RX output high voltage	I_{OL} = – 4 mA		VCC_IN/ OUT – 0.5			V
PROTECTION CIRCUITS							
$V_{(UVLO)}$	L+ under voltage lockout	L+ falling; NFAULT = Hi-Z		6	6.3		V
		L+ rising; NFAULT = LOW			6.5	6.8	V
$V_{(UVLO,HYS)}$	L+ under voltage hysteresis	Rising to falling threshold		200			mV
$V_{(UVLO\_IN)}$	VCC_IN under voltage lockout (No LDO option)	VCC_IN falling; NFAULT = Hi-Z			2.3		V
		VCC_IN rising; NFAULT = LOW			2.5		V
$V_{(UVLO,HYS)}$	VCC_IN under voltage hysteresis (No LDO option)	Rising to falling threshold			190		mV
$T_{(WRN)}$	Thermal warning	Die temperature T_J		125			°C
$T_{(SDN)}$	Thermal shutdown			150	160		°C
$T_{(HYS)}$	Thermal hysteresis for shutdown				14		°C
$T_{(WRN)}$	Thermal hysteresis for warning	Die temperature T_J			14		°C
I_{REV}	Leakage current in reverse polarity	EN=LOW, TX=x; $V_{(CQ)}$ < $V_{(L-)}$ or $V_{(CQ)}$ > $V_{(L+)}$, up to |36 V|				60	µA
		EN=LOW, TX=x; $V_{(CQ)}$ < $V_{(L-)}$ or $V_{(CQ)}$ > $V_{(L+)}$, up to |65 V|				110	µA
		EN = HIGH, TX = LOW; $V_{(CQ\ to\ L+)}$ = 3 V				640	µA
		EN = HIGH, TX = HIGH; $V_{(CQ\ to\ L-)}$ = -3 V				10	µA
LINEAR REGULATOR (LDO)							
$V_{(VCC\_OUT)}$	Voltage regulator output	TIOL1125, TIOL1123L (5V)		4.75	5	5.25	V
		TIOL1123, TIOL1123L (3.3V)		3.13	3.3	3.46	V
$V_{(DROP)}$	Voltage regulator drop-out voltage ($V_{(L+)}$ – $V_{(VCC\_OUT)}$)	I_{CC} = 20 mA load current	TIOL1125, TIOL1123L (5V)		0.75	1.9	V
			TIOL1123, TIOL1123L (3.3V)		0.75	2.3	V
REG	Line regulation ($dV_{(VCC\_OUT)}$/ dV(L+))	$I_{(VCC\_OUT)}$ = 1 mA				1.7	mV/V
L_{REG}	Load regulation ($dV_{(VCC\_OUT)}$/ $V_{(VCC\_OUT)}$)	$V_{(L+)}$ = 24 V, $I_{(VCC\_OUT)}$ = 100 µA to 20 mA				1%	
PSSR	Power Supply Rejection Ratio	100 kHz, $I_{(VCC\_OUT)}$ = 20 mA			40		dB

(1) Current fault indication will be active. Current fault auto recovery will be de-activated.
(2) Current fault indication and current fault auto recovery will be de-activated.
(3) If operating continuosly with this current limit, ensure that the current through the device does not cause the T_J to be greater than $T_{(SDN)}$ for a given ambient temperature and thermal porperty of the system. For pulse durations t < 200 µs, the device can source or sink current of at least 500 mA across the recommended operating conditions. For YAH (DSBGA) package, this parameter is specified by design and characterization.
(4) V_{THH} (min) = 5 V + (11/18) [$V_{(L+)}$ - 8 V]
(5) V_{THH} (max) = 6.5 V + (13/18) [$V_{(L+)}$ - 8 V]
(6) V_{THL} (min) = 4 V + (8/18) [$V_{(L+)}$ -8 V]
(7) V_{THL} (max) = 6 V + (11/18) [$V_{(L+)}$ -8 V]

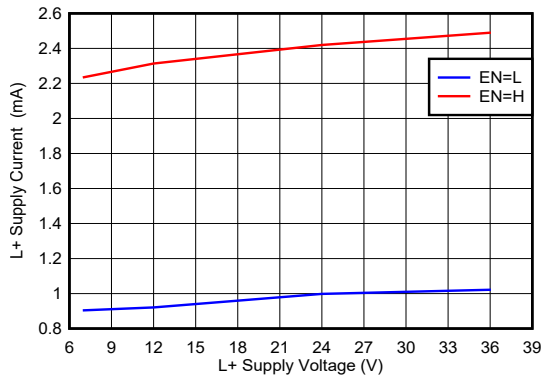
6.7 Switching Characteristics

Over recommended operating conditions and recommended free-air temperature range (unless otherwise noted). Typical values are at L_+ = 24 V, V_{VCC_IN} = 3.3 V, V_{VCC_OUT} = 3.3 V and T_A = 25 ℃ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_{PLH}, t_{PHL}	Driver propagation delay	See 图 7-1 See 图 7-2 See 图 7-3 R_L = 2 kΩ C_L = 5 nF $R_{(SET)}$ = 10 kΩ		600	1200	ns
$t_{P(skew)}$	Driver propagation delay skew. | t_{PLH} - t_{PHL} |			75		ns
t_{PZH}, t_{PZL}	Driver enable delay				4	µs
t_{PHZ}, t_{PLZ}	Driver disable delay				4	µs
t_r, t_f	Driver output rise, fall time		200		700	ns
$\|t_r - t_f\|$	Difference in rise and fall time			50		ns
t_{WU1}	Wake-up recognition begin	See 图 7-5	45	60	75	µs
t_{WU2}	Wake-up recognition end		85	100	145	µs
t_{pWAKE}	Wake-up output delay				150	µs
t_{SC}	Current fault blanking time		175	200		µs
t_{pSC}	Current fault indication delay				280	µs
t_{WUL}	Wake output pulse duration on wake detection in EN=L mode	See 图 7-6	175	225	285	µs
t_{SCEN}	Current fault driver re-enable wait time			15		ms
$t_{(UVLO)}$	CQ re-enable delay after UVLO (1)	$V_{(UVLO)}$ rising threshold crossing time to CQ enable time	10	30	50	ms
RECEIVER						
t_{ND}	Noise suppression time (2)				250	ns
t_{PLH}, t_{PHL}	Receiver propagation delay	See 图 7-4 15-pF load on RX,		150	300	ns

(1) CQ output remains Hi-Z for this time
(2) Noise suppression time is defined as the permissible duration of a receive signal above/below the detection threshold without detection taking place.

6.8 Typical Characteristics



No Load TX = Open T_A = 25°C

图 6-1. Supply Current vs Supply Voltage

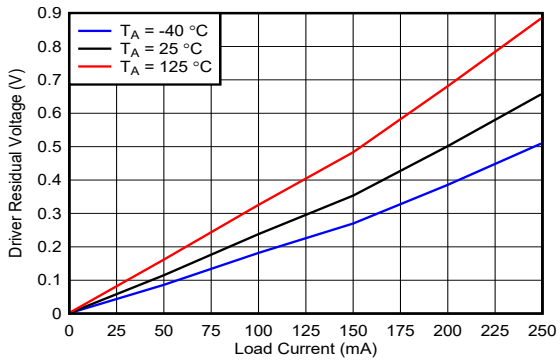


图 6-2. Residual Voltage vs Load Current: High Side

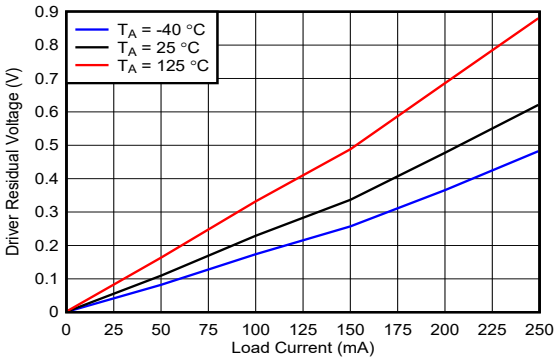
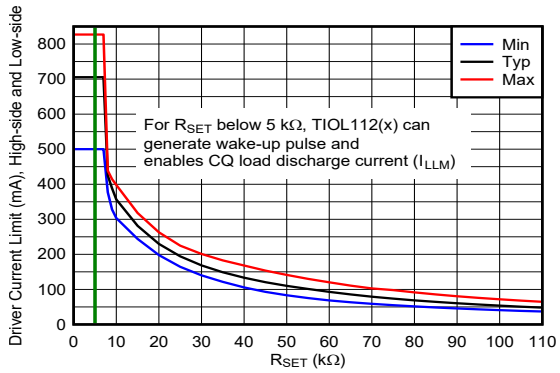
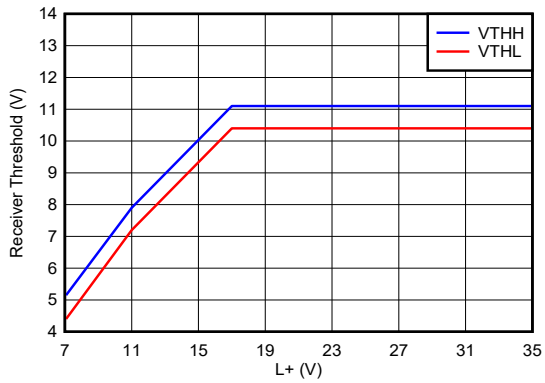


图 6-3. Residual Voltage vs Load Current: Low Side



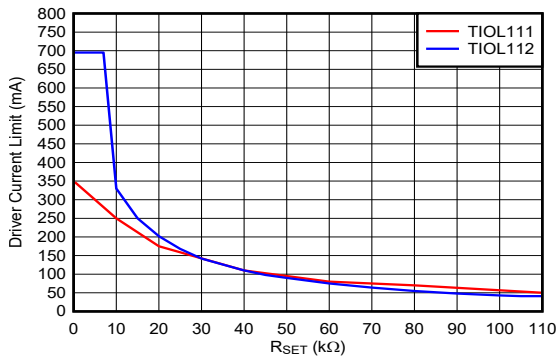
For R_{SET} in the 0-5 kΩ range, TIOL112(x) can source/sink 500 mA required for wake-up pulse generation in IO-link applications. For R_{SET} in the 0-5 kΩ range, TIOL112(x) also activates a pull-down current source (I_{LLM}) when the driver is disabled. Min and max curves specified by design and characterization across temperature and process variation.
T_A = 25°C (typ curve)

图 6-4. Current Limit vs R_{SET}



T_A = 25°C

图 6-5. Receiver Threshold Boundaries



T_A = 25°C

图 6-6. Current limit vs R_{SET}: TIOL112(x) vs TIOL111(x)

7 Parameter Measurement Information

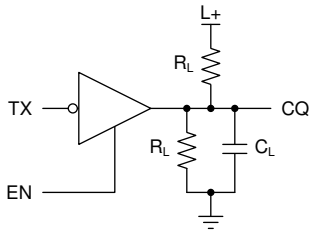


图 7-1. Test Circuit for Driver Switching

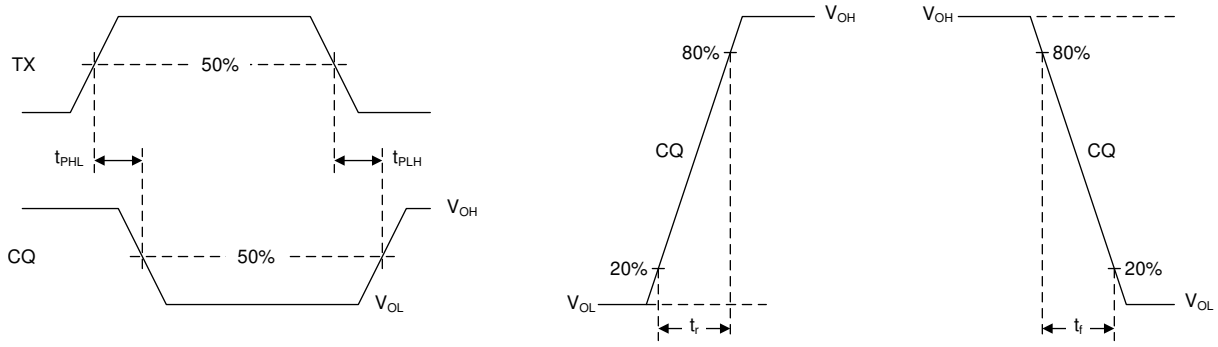


图 7-2. Waveforms for Driver Output Switching Measurements

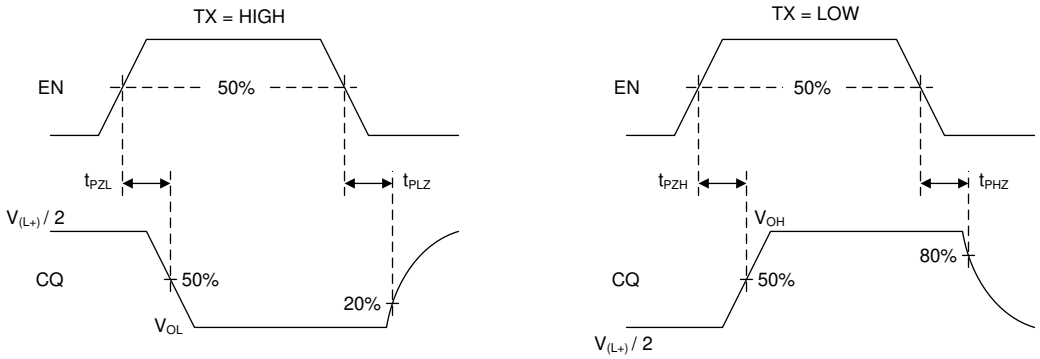


图 7-3. Waveforms for Driver Enable or Disable Time Measurements

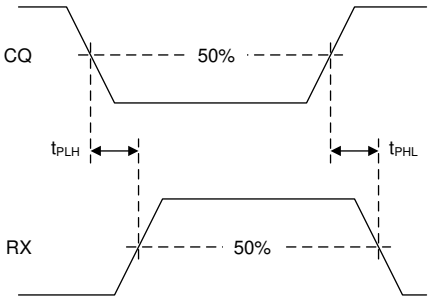
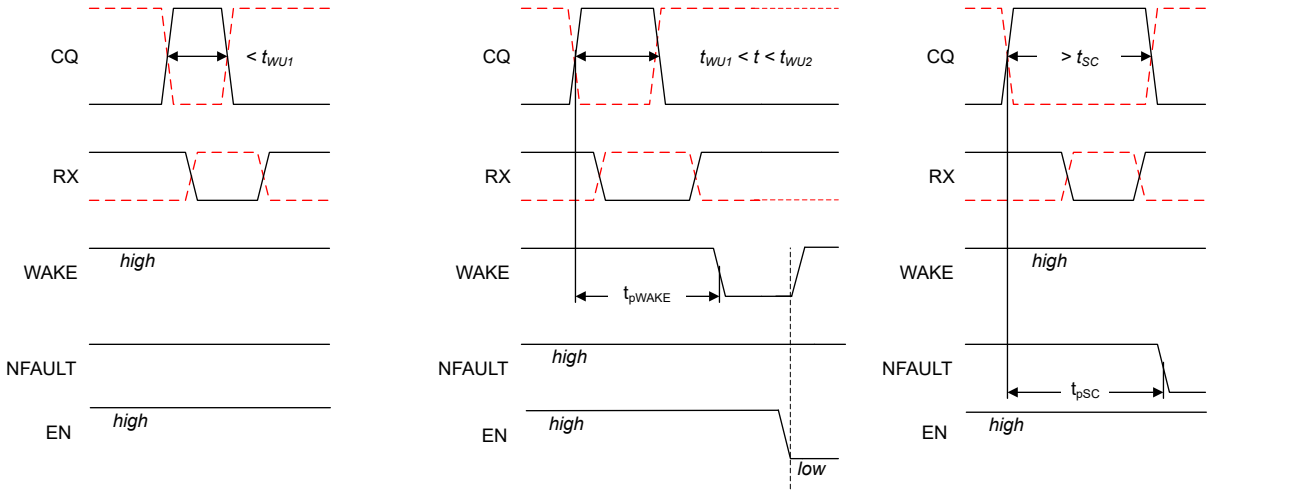


图 7-4. Receiver Switching Measurements



a) Over-current due to transient　　b) Valid Wake-up pulse　　c) Over-current due to fault condition

图 7-5. Overcurrent and Wake Conditions for EN = H and ILIM_ADJ = 10 kΩ to 110 kΩ, TX = H (Full Lines); and TX = L (Red Dotted Lines)

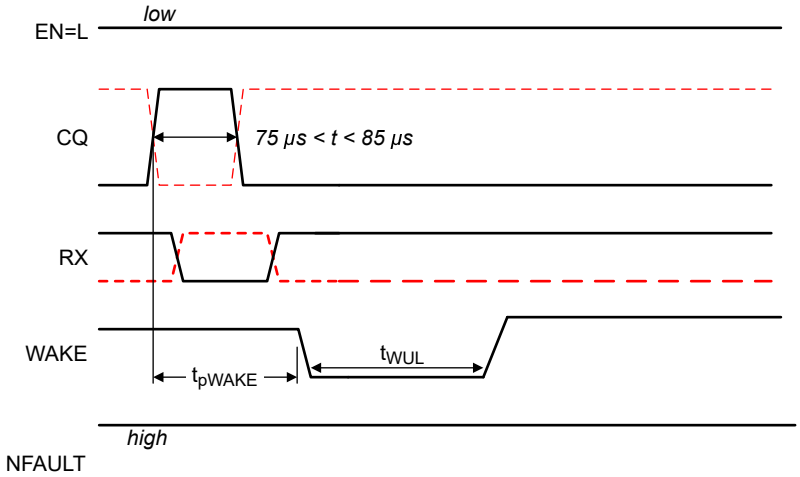
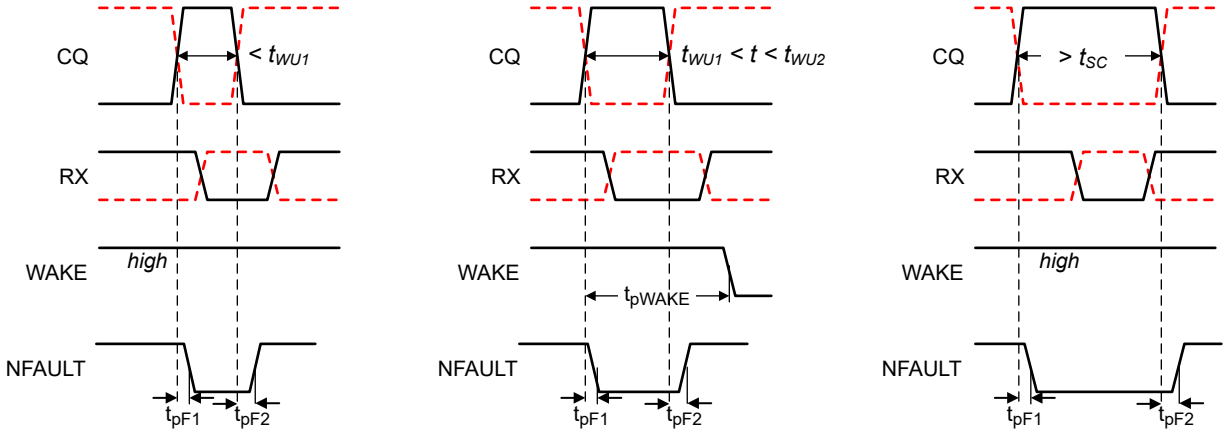


图 7-6. Wake Conditions for EN = L, RX = H (Full Lines); and RX = L (Red Dotted Lines)



a) Over-current due to transient　　b) Valid Wake-up pulse　　c) Over-current due to fault condition

图 7-7. Overcurrent and Wake Conditions for EN = H and ILIM_ADJ is floating, TX = H (Full Lines); and TX = L (Red Dotted Lines)

8 Detailed Description

8.1 Overview

图 8-1 shows that the TIOL112 or TIOL112x driver output (CQ) can be used in either push-pull, high-side, or low-side configuration using the enable (EN) and transmit data (TX) input pins. The internal receiver converts the 24-V signal on the CQ line to standard logic levels on the receive data (RX) pin. A simple parallel interface is used to receive/transmit data and status information between the device and the local controller.

These devices have integrated IEC 61000-4-4/5 EFT and surge protection. In addition, tolerance to ±70-V transients enables flexibility to choose from a wider range of TVS diodes if an application requires higher levels of protection. These integrated robustness features will simplify the system level design by reducing external protection circuitry.

TIOL112 or TIOL112x transceivers implement protection features for overcurrent, overvoltage and over-temperature conditions. The devices also provide a current-limit setting of the driver output current using an external resistor.

The devices derive the low-voltage supply from the IO-Link L+ voltage (24 V nominal) via an internal linear regulator to provide power to the local controller and sensor circuitry.

8.2 Functional Block Diagrams

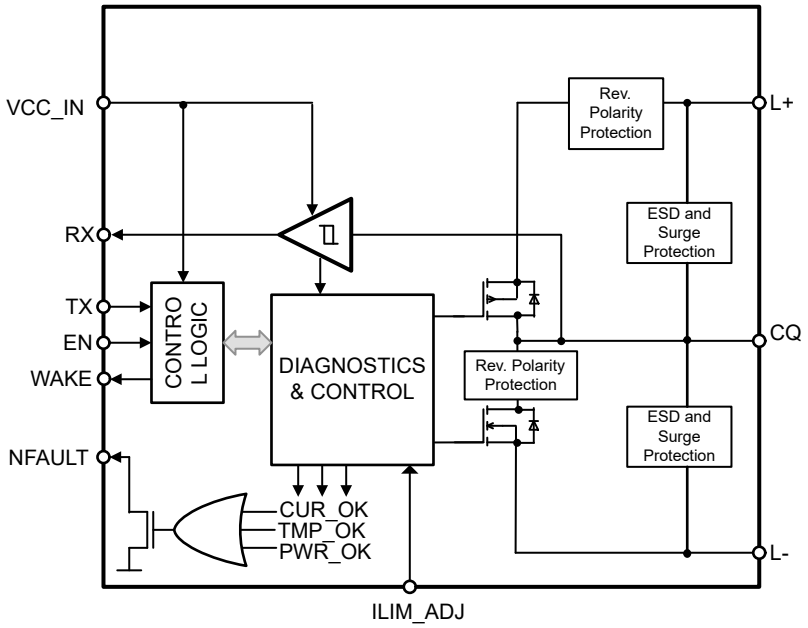


图 8-1. Block Diagram TIOL112

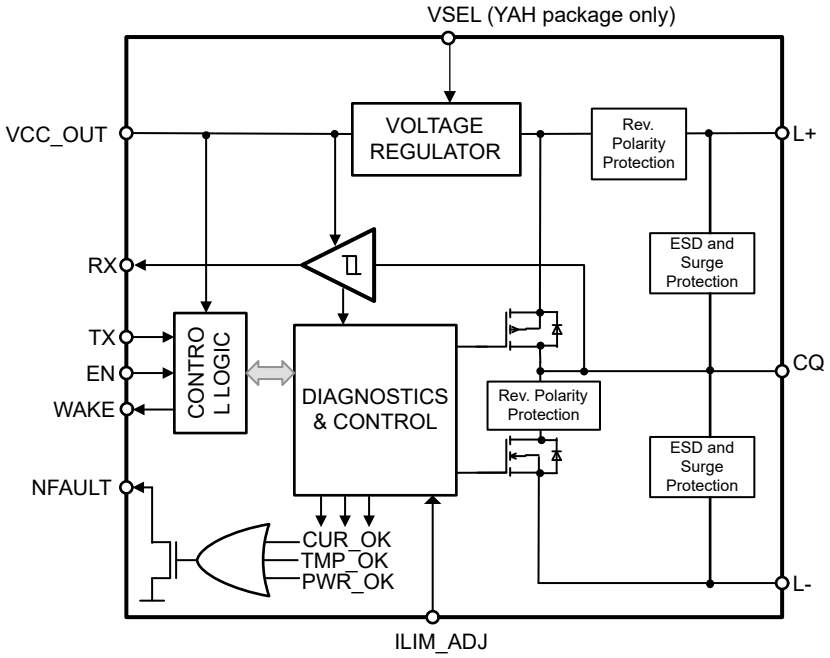


图 8-2. Block Diagram TIOL1123(L), TIOL1125

8.3 Feature Description

8.3.1 Wake-Up Detection

The TIOL112(x) may be operated in IO-Link mode or Standard Input / Output (SIO) mode. If the device is in SIO mode and the IO-link master node wants to initiate communication with the device node, the master drives the CQ line to the opposite of its present state, and will either sink or source the current (≥ 500 mA) for the wake-up duration (typically 80 µs) depending on the CQ logic level as per the IO-Link specification. The TIOL112(x) detects this as a wake-up condition and communicates to the local microcontroller via the WAKE pin. The IO-Link communication specification requires the device node to switch to receive mode within 500 µs after receiving the wake-up signal.

For overcurrent conditions shorter or longer than a valid wake-up pulse, the WAKE pin remains in a high-impedance (inactive) state. This is illustrated in 图 7-5.

If the driver of TIOL112(x) is disabled (EN = L), any change in CQ logic level for duration $t_{WU1} < t < t_{WU2}$ is detected as a wake-up event and WAKE asserts low for the duration of t_{WUL}. This is illustrated in 图 7-6. Please refer to 表 8-4 for the summary of the conditions for Wake-Up detection.

8.3.2 Current Limit Configuration

The output current can be configured with an external resistor on ILIM_ADJ pin. The highest current limit setting with an external resistor of 10 kΩ provides a minimum of 300 mA over the operating temperature and voltage range.

Output disable due to current fault and current fault auto recovery features can be disabled by floating ILIM_ADJ pin. However, the current fault indication is still active in this configuration. This feature is useful when driving large capacitances.

When ILIM_ADJ pin is shorted to ground, the TIOL112(x) is configured to be in the IO-link master mode. In this mode, the TIOL112(x) can source or sink minimum of 500 mA to generate a wake-up request. In addition, the TIOL112(x) enables a small current sink of 5 mA (minimum). The current fault indication, output disable, and auto recovery features are disabled in this mode.

表 8-1. Current Limit Configuration

ILIM_ADJ Pin Condition	CQ Current Limit (Min.)	NFAULT Indication During Current Fault	Output Disable and Auto Recovery
R_{SET} resistor to L- (10 kΩ to 110 kΩ)	Variable (35 mA to 300 mA)	Yes	Yes
Connected to L- (R_{SET} 0 to 5 kΩ)	500 mA	No	No
OPEN	260 mA	Yes	No

8.3.3 Current Fault Detection, Indication and Auto Recovery

If the output current at CQ exceeds the internally-set current limit $I_{O(LIM)}$ for a duration longer than t_{SC}, the NFAULT pin is driven logic low to indicate a fault condition. The output is turned off, but the LDO continues to function. The output periodically retries to check if the output is still in the over current condition. In this mode, the output is switched on for t_{SC} in t_{SCEN} intervals. Current fault auto recovery mode can be disabled by setting ILIM_ADJ = OPEN. See 表 8-5. Toggling EN will clear NFAULT.

8.3.4 Thermal Warning, Thermal Shutdown

If the die temperature exceeds $T_{(WRN)}$, the NFAULT flag is held low indicating a potential over temperature problem. When the T_J exceeds $T_{(SDN)}$, The output is disabled but the LDO remains operational. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal circuit re-enables the driver, subject to the state of the EN and TX pins.

8.3.5 Fault Reporting (NFAULT)

NFAULT is driven low if either a current fault condition is detected, die temperature has exceeded $T_{(WRN)}$ or supply has dropped below the UVLO threshold. NFAULT returns to high-impedance as soon as all three fault conditions clear.

NFAULT = [CUR_OK && PWR_OK && TMP_OK]

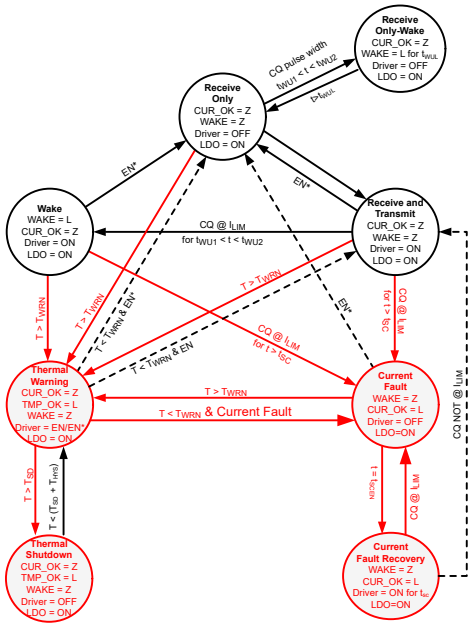


图 8-3. Device State Diagram

8.3.6 Transceiver Function Tables

表 8-2. Driver Function

EN	TX	CQ	COMMENT
L / Open	X	Hi-Z	Device is in ready-to-receive state
H	L	H	CQ is sourcing current (high-side drive)
H	H / Open	L	CQ is sinking current (low-side drive)

表 8-3. Receiver Function

CQ VOLTAGE	RX	COMMENT
$V_{(CQ)} < V_{(THL)}$	H	Normal receive mode, input low
$V_{(THL)} < V_{(CQ)} < V_{(THH)}$	?	Indeterminate output, may be either high or low
$V_{(THH)} < V_{(CQ)}$	L	Normal receive mode, input high
Open	?	Indeterminate output, may be either high or low

表 8-4. Wake-Up Function ($t_{WU1} < t < t_{WU2}$)

EN	TX	CQ CURRENT	WAKE	COMMENT
L / Open	X	X	Asserts low for t_{WUL}	Device asserts low for t_{WUL} if RX output changes high-to-low or low-to-high for $t_{WU1} < t < t_{WU2}$
H	H / Open	$\lvert I_{(CQ)} \rvert \geqslant 500$ mA	L	Device receives high-level wake-up request over the IO-Link bus
H	L	$\lvert I_{(CQ)} \rvert \geqslant 500$ mA	L	Device receives low-level wake-up request over the IO-Link bus

表 8-5. Current Limit Indicator Function ($t > t_{SC}$)

EN	TX	CQ CURRENT	NFAULT	COMMENT
H	H / Open	$\lvert I_{(CQ)} \rvert > I_{O(LIM)}$	L	CQ current exceeds the set limit for over t_{SC}
		$\lvert I_{(CQ)} \rvert < I_{O(LIM)}$	Z	Normal operation
H	L	$\lvert I_{(CQ)} \rvert > I_{O(LIM)}$	L	CQ current exceeds the set limit for over t_{SC}
		$\lvert I_{(CQ)} \rvert < I_{O(LIM)}$	Z	Normal operation
L / Open	X	X	Z	Driver is disabled, Current limit indicator is inactive

备注

Current limit indicator function is disabled when ILIM_ADJ is connected to GND (or $R_{SET} < 5$ kΩ

8.3.7 The Integrated Voltage Regulator (LDO)

The TIOL1123 and TIOL1125 each have an integrated linear voltage regulator (LDO) which can supply power to external components. The voltage regulator is specified for L+ voltages in the range of 7 V to 36 V with respect to L-. The LDO is capable of delivering up to 20 mA.

In the DSBGA (YAH) package, TIOL1123L offers pin-configurable LDO output via VSEL pin. When VSEL is connected to GND, VCC_OUT is configured to provide a 5-V output. When VSEL is left floating, VCC_OUT provides a 3.3-V output.

表 8-6. LDO Output Configuration via VSEL pin (YAH Package)

VSEL pin connection	VCC_OUT
Connected to L-	5 V
Floating	3.3 V

The LDO is designed to be stable with standard ceramic capacitors with values of 1 μF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1 Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1 μF.

The voltage regulator has an internal 35-mA current limit to protect against initial startup inrush current due to large decoupling capacitors and accidental short circuit conditions.

8.3.8 Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the L+, CQ and L- pins. The maximum voltage between any of the pins may not exceed 65 V DC at any time.

图 8-4 and 图 8-5 shows all the possible connection combinations.

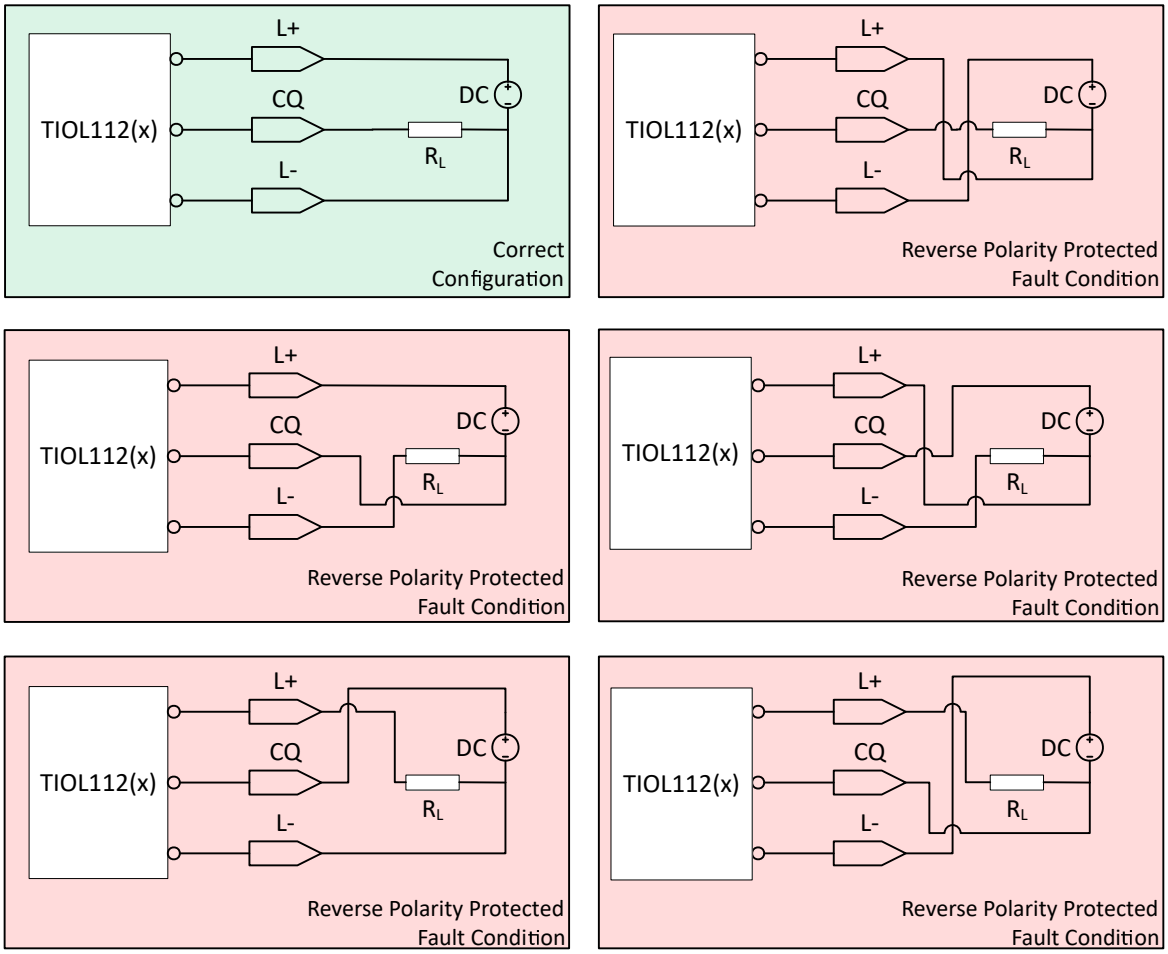


图 8-4. High-Side Driver Configuration

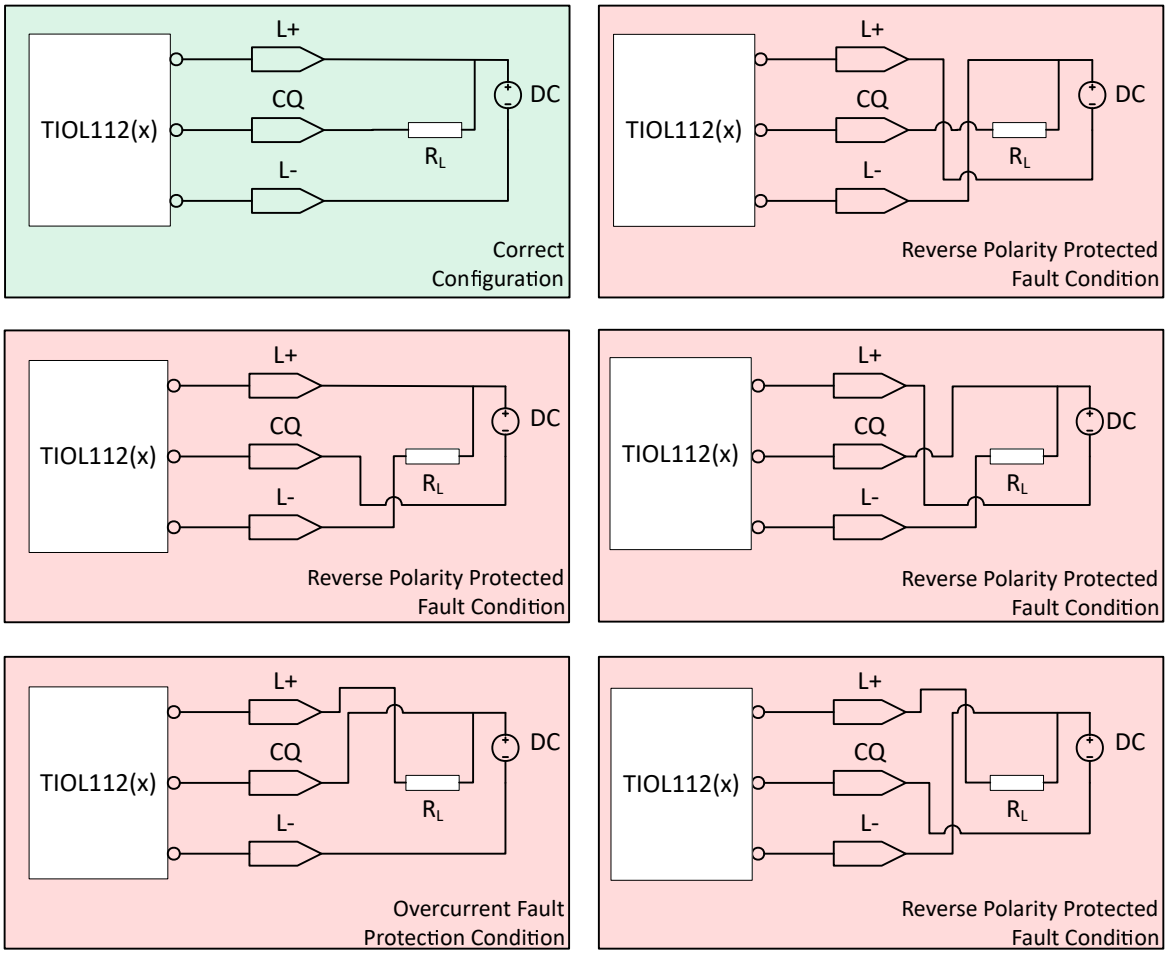
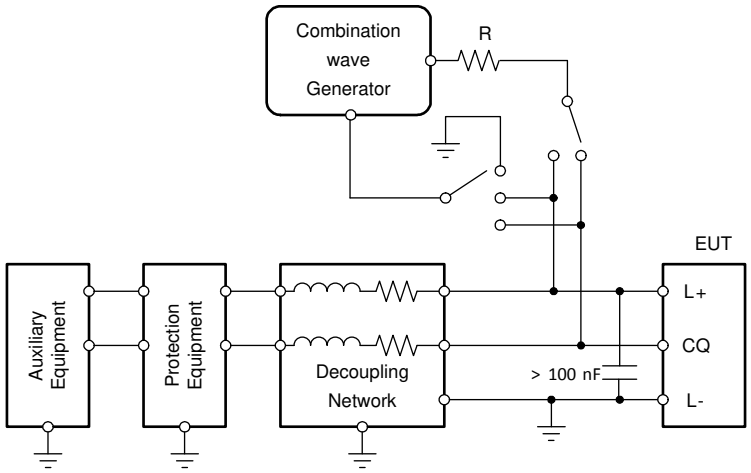


图 8-5. Low-Side Driver Configuration

8.3.9 Integrated Surge Protection and Transient Waveform Tolerance

The L+ and CQ pins of the device are capable of withstanding up to 1.2 kV of 1.2/50 – 8/20 μs IEC 61000-4-5 surge with a source impedance of 500 Ω. The surge testing should be performed with a minimum 100 nF supply decoupling capacitor between L+ and L-, and 1 μF between VCC_IN/OUT and L-.

External TVS diodes may be required for higher transient protection levels. The system designer should ensure that the maximum clamping voltage of the external diodes should be < 65 V at the desired current level. The device is capable of withstanding up to ±70-V transient pulses < 100 μs.



1.2/50 – 8/20 μs CWG
R = 500 Ω

图 8-6. Surge Test Setup

8.3.10 Power Up Sequence (TIOL112)

VCC_IN and L+ domains can be powered up in any sequence. In the event of L+ is powered and VCC_IN is not, the CQ pin will remain in high impedance.

8.3.11 Undervoltage Lock-Out (UVLO)

The device enters UVLO if the L+ voltage falls below $V_{(UVLO)}$. (For the device without the integrated LDO, the device monitors VCC_IN in addition to L+. UVLO happens if either supply falls below the threshold.)

As soon as the supply falls below $V_{(UVLO)}$, NFAULT is pulled low, and the driver (CQ) is disabled (Hi-Z). Receiver performance is not specified in this mode.

When the supply rises above $V_{(UVLO)}$, NFAULT returns to Hi-Z (given no other fault conditions present). The CQ output is turned on after $t_{(UVLO)}$ delay.

8.4 Device Functional Modes

These devices can operate in three different modes.

8.4.1 NPN Configuration (N-Switch SIO Mode)

Set TX pin high (or open) and use EN pin as control for realizing the function of an N-switch (low-side configuration) on CQ.

8.4.2 PNP Configuration (P-Switch SIO Mode)

Set TX pin low and use EN pin as control for realizing the function of a P-switch (high-side configuration) on CQ.

8.4.3 Push-Pull, Communication Mode

Set EN pin high and toggle TX as control for realizing the function of a push-pull output on CQ. 表 8-7, 表 8-8 and 表 8-9 summarize the pin configurations to accomplish the functional modes.

表 8-7. NPN Mode

EN	TX	CQ
L / Open	H / Open	Hi-Z
H	H / Open	N-Switch

表 8-8. PNP Mode

EN	TX	CQ
L / Open	L	Hi-Z
H	L	P-Switch

表 8-9. Push-Pull, Communication Mode

EN	TX	CQ
L / Open	X	Hi-Z
H	H	N-Switch
H	L	P-Switch

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

When TIOL112(x) is connected to an IO-Link master through a three-wire interface (图 9-1), the master can initiate communication and exchange data with a remote node with the TIOL112(x) IO-Link transceiver acting as a complete physical layer for the communication.

9.2 Typical Application

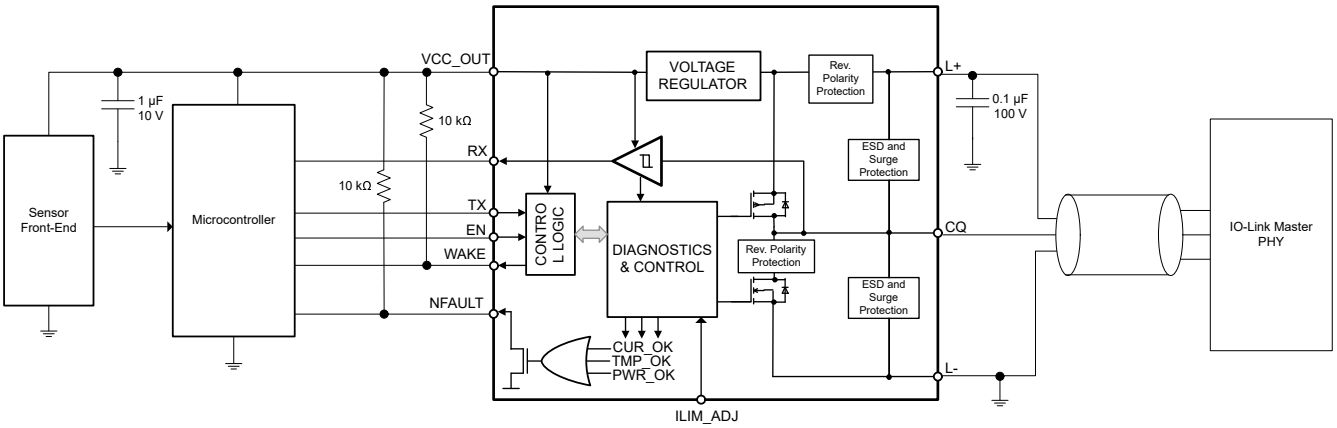


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

TIOL112 and TIOL112x IO-Link transceivers can be used to communicate using the IO-Link protocol, or as standard digital outputs to either sense or drive a wide range of sensors and loads. 表 9-1 shows recommended components for a typical system design.

表 9-1. Design Parameters

PARAMETERS	Design Requirement	TIOL112(x) Specification
Input voltage range (L+)	24 V (typ), 30 V (max)	7 V to 36 V
Output current (CQ)	200 mA	Choose 250 mA limit with R_{SET} = 27 kΩ
LDO Output voltage	5 V	Choose TIOL1125; VCC_OUT = 5 V
LDO output current	5 mA	$I_{(VCC\_OUT)}$: Up to 20 mA
Pull-up resistors for NFAULT and WAKE	10 kΩ	10 kΩ
L+ decoupling capacitor	0.1 µF / 100 V	0.1 µF / 100 V
LDO output capacitor	1 µF / 10 V	1 µF / 10 V
Maximum Ambient Temperature, T_A	105 °C	TIOL112 can support up to T_A of 125 °C if $T_J < T_{(SDN)}$

9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Junction Temperature Check

For a 200 mA current limit:

- Choose driver output current limit, $I_{O(LIM)}$ = 250 mA (allowing for current limit tolerance); R_{SET} = 27 kΩ
- The maximum voltage drop across the high-side switch at 250 mA current is $V_{DS(ON)}$ = 1.1 V.

This causes a power consumption of:

$$PD_{OP} = V_{DS(ON)} \times I_{O(LIM)} = 1.1\,V \times 250\,mA = 275\,mW \quad (1)$$

For a 5 mA LDO current output,

$$PD_{LDO} = \left(V_{L+} - V_{VCC_{OUT}}\right) \times I_{VCC\_OUT} = (30 - 5)V \times 5\,mA = 125\,mW \quad (2)$$

Total power dissipation,

$$PD = PD_{LDO} + PD_{OP} = 275\,mW + 125\,mW = 400\,mW \quad (3)$$

Multiply this value with the Junction-to-ambient thermal resistance of θ_{JA} = 45.9 °C/W (taken from the *Thermal Information table* table) to receive the difference between junction temperature, T_J, and ambient temperature, T_A:

$$\Delta T = T_J - T_A = PD \times \theta_{JA} = 400\,mW \times 45.9\,{}^{\circ}\!C/W = 18.36\,{}^{\circ}\!C \quad (4)$$

Add this value to the maximum ambient temperature of T_A = 105°C to receive the final junction temperature:

$$T_J = T_A + \Delta T = T_A + PD \times \theta_{JA} = 105\,{}^{\circ}\!C + 400\,mW \times 45.9\,{}^{\circ}\!C/W = 105\,{}^{\circ}\!C + 18.36\,{}^{\circ}\!C = 123.36\,{}^{\circ}\!C \quad (5)$$

As long as T_J is below the recommended maximum value of 150°C, no thermal shutdown will occur. However, the junction temperature is closer to T_{WRN} and thermal warning may be generated if the junction temperature rises above T_{WRN}.

Note that the modeling of the complete system may be necessary to predict junction temperature in smaller PCBs and/or enclosures without air flow.

9.2.2.2 Driving Capacitive Loads

These devices are capable of driving capacitive loads on the CQ output. Assuming a pure capacitive load without series/parallel resistance, the maximum capacitance that can be charged without triggering current fault can be calculated as:

$$C_{LOAD} = \frac{[I_{O(LIM)} \text{ x } t_{SC}]}{V_{(L+)}} \quad (6)$$

To drive higher capacitive loads and avoid overcurrent condition disabling the driver, it is recommended leave ILIM_ADJ pin floating. With ILIM_ADJ floating, TIOL112(x) indicates overcurrent fault without blanking time delay (t_{SC}) but does not disable the driver. Another approach is to drive high capacitive loads with a series resistor between the CQ output and the load to avoid overcurrent condition. Capacitive loads can be connected to L- or L+.

9.2.2.3 Driving Inductive Loads

The TIOL112(x) family is capable of magnetizing and demagnetizing large inductive loads. These devices contain internal circuitry that enables fast and safe demagnetization when configured as either P-switch or N-switch mode.

In P-switch configuration, the load inductor L is magnetized when the CQ output is driven high. When the PNP is turned off, there is a significant amount of negative inductive kick back at the CQ pin. This voltage is safely clamped internally at about -15 V.

Similarly, in N-switch configuration, the load inductor L is magnetized when the CQ output is driven low. When the NPN is turned off, there is a significant amount of positive inductive kick back at the CQ pin. This voltage is safely clamped internally at about 15 V.

The equivalent protection circuits are shown in 图 9-2 and 图 9-3. The minimum value of the resistive load R can be calculated as:

$$R = \frac{V_{(L+)}}{I_{O(LIM)}} \quad (7)$$

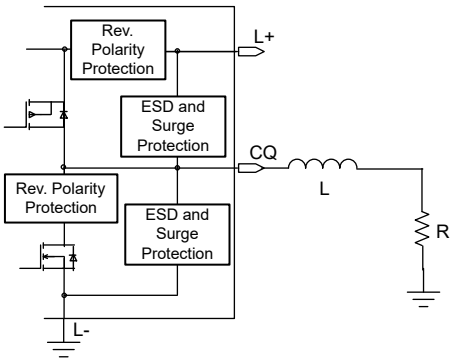


图 9-2. P-Switch Mode

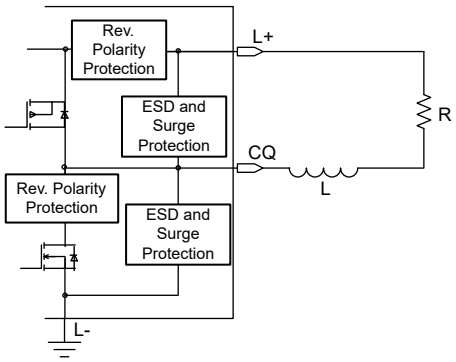


图 9-3. N-Switch Mode

9.2.3 Application Curves

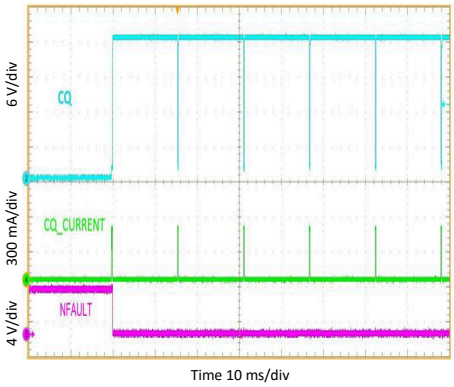


图 9-4. CQ in Current Fault Auto Recovery, Low Side Mode

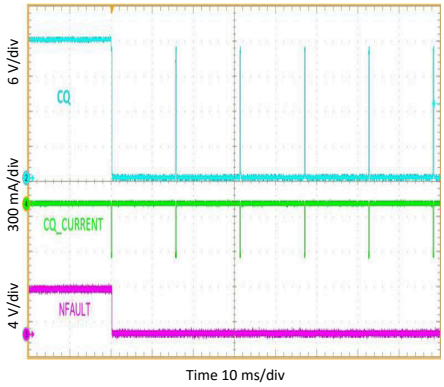


图 9-5. CQ in Current Fault Auto Recovery, High Side Mode

L+ = 36 V L = 1.5 H R_L = 360 Ω R_{SET} = 10 kΩ T_A = 25 °C

图 9-6. CQ Driving Inductive Load, Low Side Mode (NPN mode)

L+ = 36 V L=1.5 H R_L = 360 Ω R_{SET} = 10 kΩ T_A = 25 °C

图 9-7. CQ Driving Inductive Load, High Side Mode (PNP mode)

NFAULT is indicated for the duration of charging and discharging of the capacitor but driver is not disabled when ILIM_ADJ is floating

L+ = 24 V C_L = 20 µF R_L = 100 Ω R_{SET} = 1 MΩ (ILIM_ADJ Floating) T_A = 25 °C

图 9-8. CQ Driving Capacitive Load, Push-Pull Mode

9.3 Power Supply Recommendations

The TIOL112 and TIOL112x transceivers are designed to operate from a 24-V nominal supply at L+, which can vary by +12 V and -17 V from the nominal value to remain within the device recommended supply voltage range of 7 V to 36 V. This supply should be buffered with at least a 100-nF/100-V capacitor.

9.4 Layout

9.4.1 Layout Guidelines

- Use of a 4-layer board is recommended for good heat conduction. Use layer 1 (top layer) for control signals, layer 2 as power ground layer for L-, layer 3 for the 24-V supply plane (L+), and layer 4 for the regulated output supply (VCC_IN/OUT).
- Connect the thermal pad to L- with maximum amount of thermal vias for best thermal performance.
- Use entire planes for L+, VCC_IN/OUT and L- to assure minimum inductance.
- The L+ terminal must be decoupled to ground with a low-ESR ceramic decoupling capacitor. The recommended minimum capacitor value is 100 nF. The capacitor must have a voltage rating of 50 V minimum (100 V depending on max sensor supply fault rating) and an X5R or X7R dielectric.
- The optimum placement of the capacitor is closest to the transceiver’ s L+ and L- terminals to reduce supply drops during large supply current loads. See 图 9-9 for a PCB layout example.
- Connect all open-drain control outputs via 10 kΩ pull-up resistors to the VCC_IN/OUT plane to provide a defined voltage potential to the system controller inputs when the outputs are high-impedance.
- Connect the R_{SET} resistor between ILIM_ADJ and L-.
- Decouple the regulated output voltage at VCC_IN/OUT to ground with a low-ESR, ≥ 1-µF, ceramic decoupling capacitor. The capacitor should have a voltage rating of 10 V minimum and an X5R or X7R dielectric.

9.4.2 Layout Example

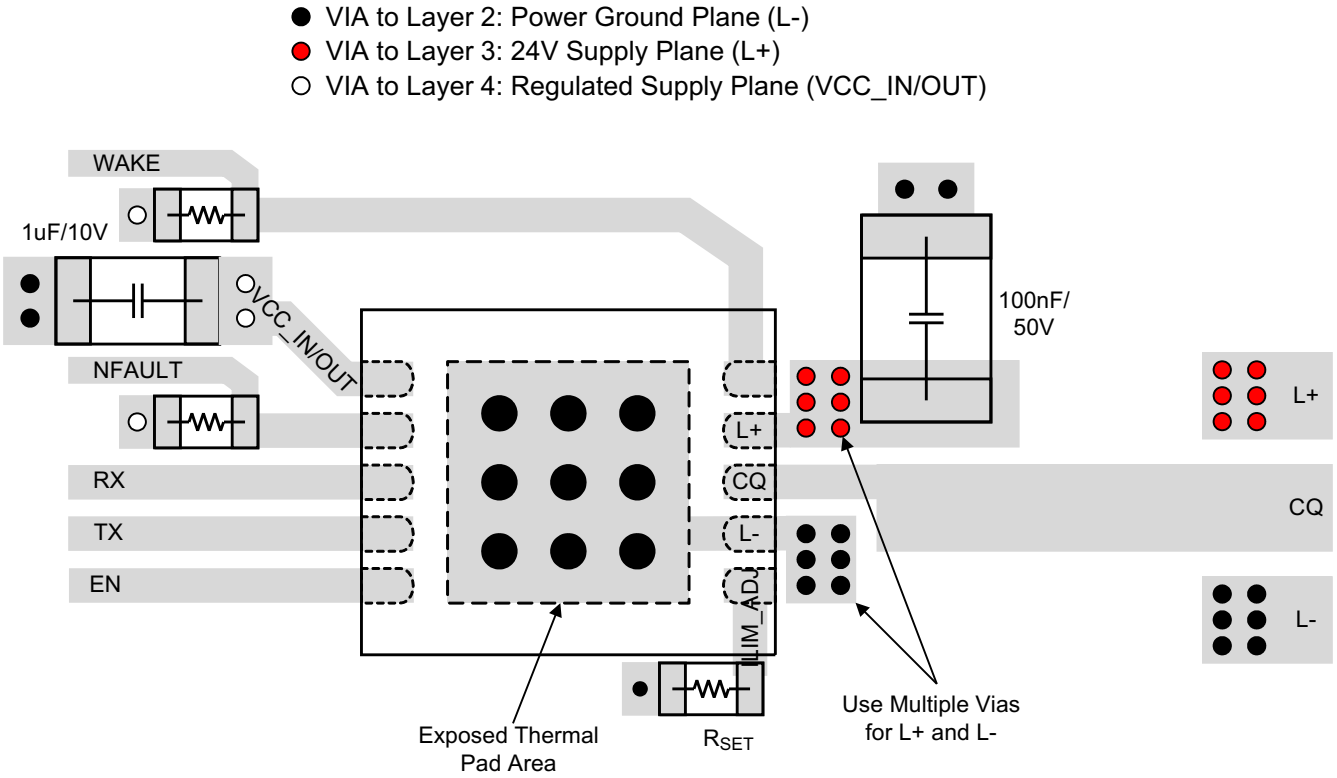


图 9-9. Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

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10.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIOL1123DRCR	ACTIVE	VSON	DRC	10	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1123	Samples
TIOL1123LYAHR	ACTIVE	DSBGA	YAH	12	1500	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T1123L	Samples
TIOL1125DRCR	ACTIVE	VSON	DRC	10	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1125	Samples
TIOL112DRCR	ACTIVE	VSON	DRC	10	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	112	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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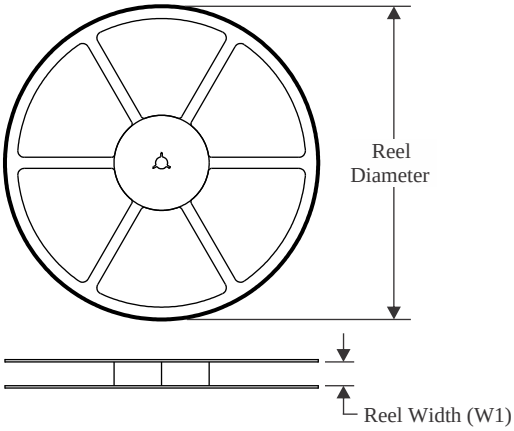
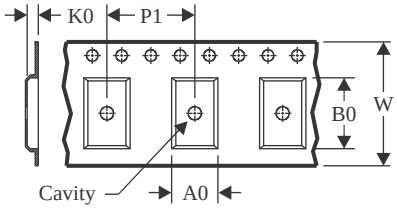
TAPE AND REEL INFORMATION

REEL DIMENSIONS

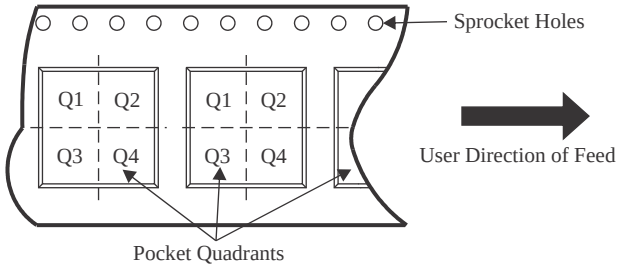


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

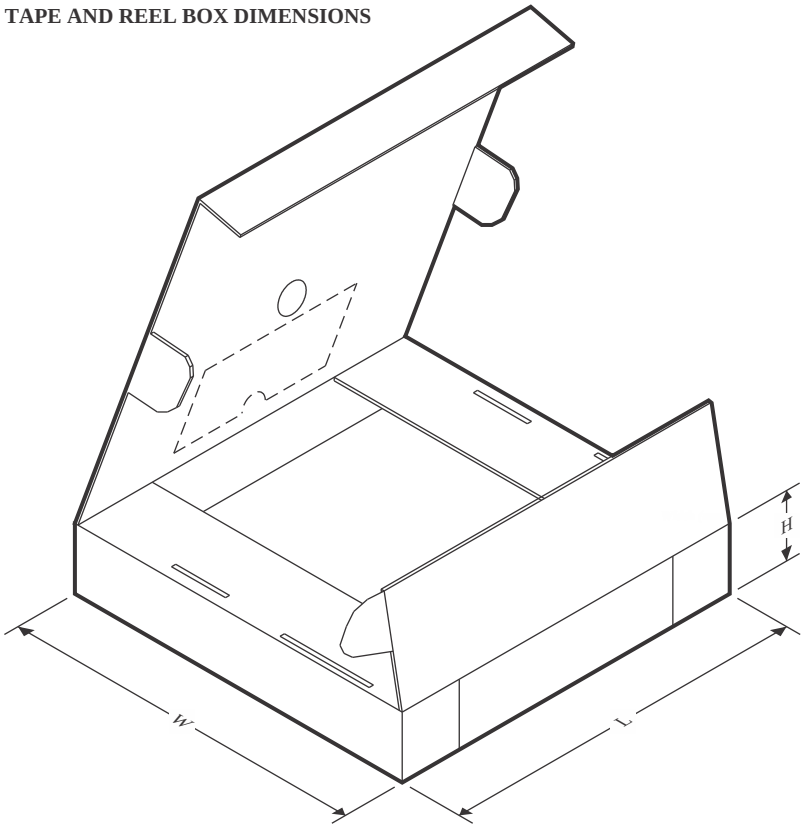
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TIOL1123DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TIOL1123LYAHR	DSBGA	YAH	12	1500	180.0	8.4	1.88	2.63	0.53	4.0	8.0	Q1
TIOL1125DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TIOL112DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TIOL1123DRCR	VSON	DRC	10	5000	367.0	367.0	35.0
TIOL1123LYAHR	DSBGA	YAH	12	1500	182.0	182.0	20.0
TIOL1125DRCR	VSON	DRC	10	5000	367.0	367.0	35.0
TIOL112DRCR	VSON	DRC	10	5000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

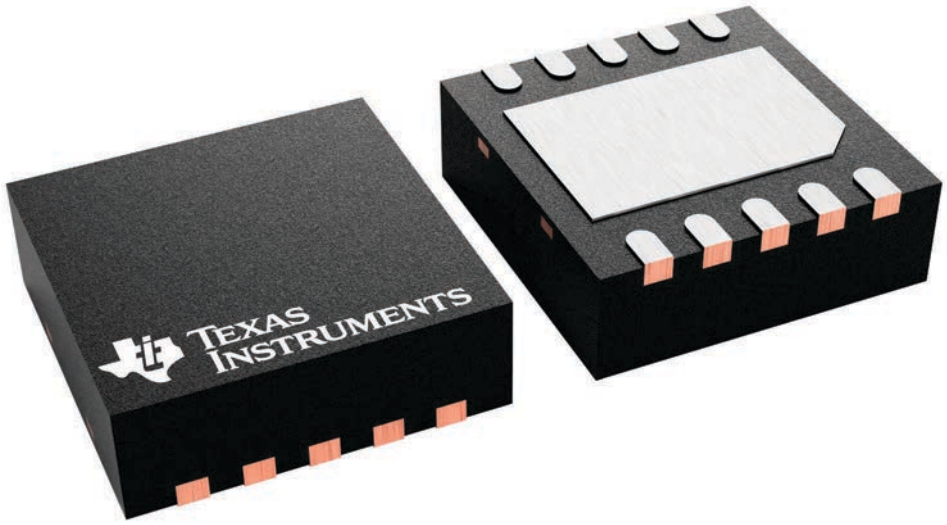
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



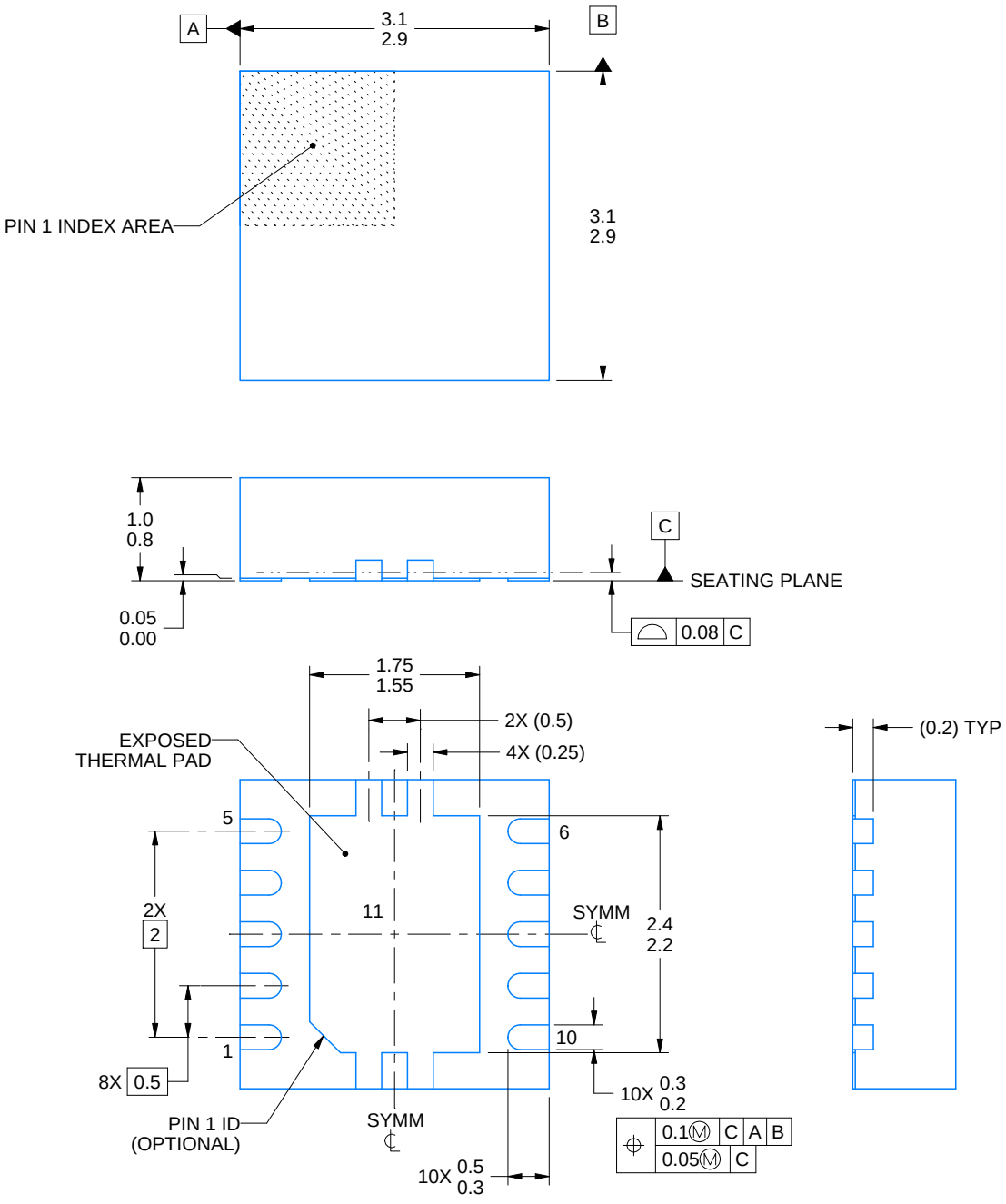
4226193/A

DRC0010V

PACKAGE OUTLINE

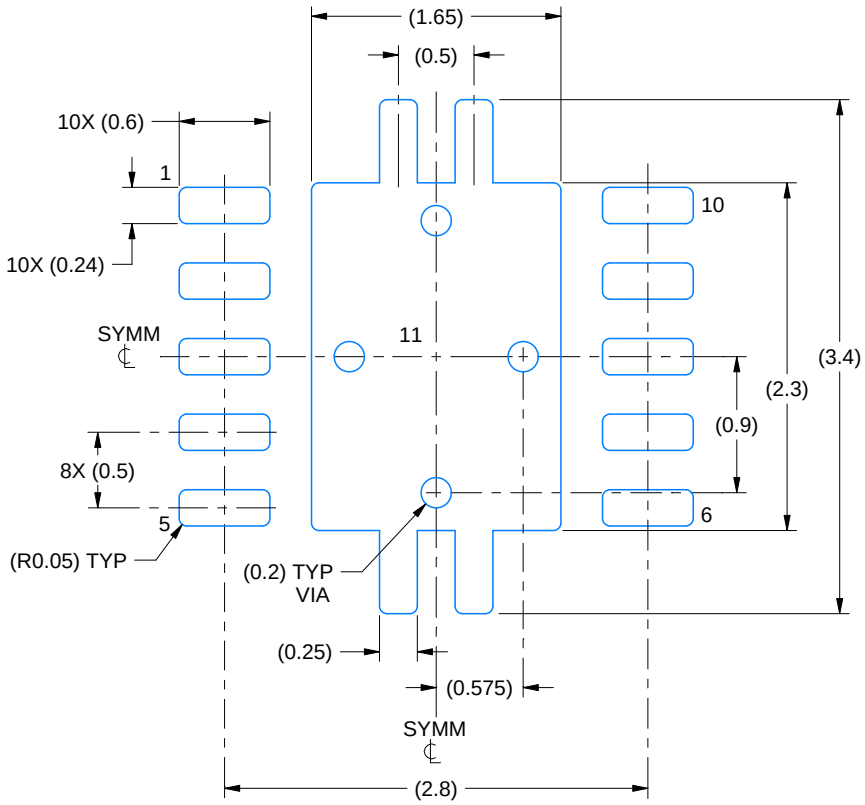
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

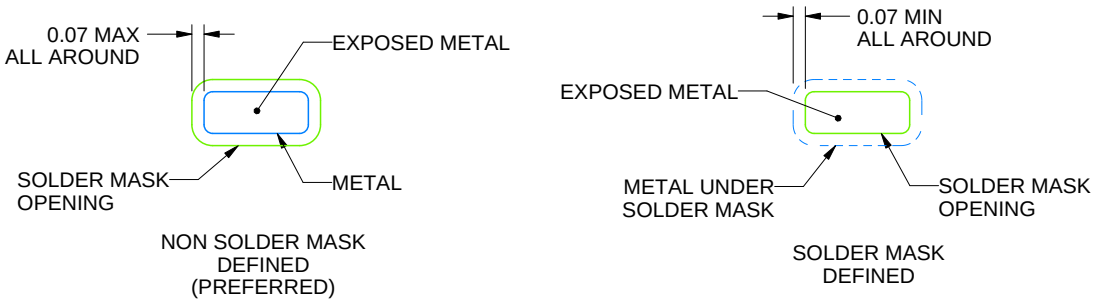


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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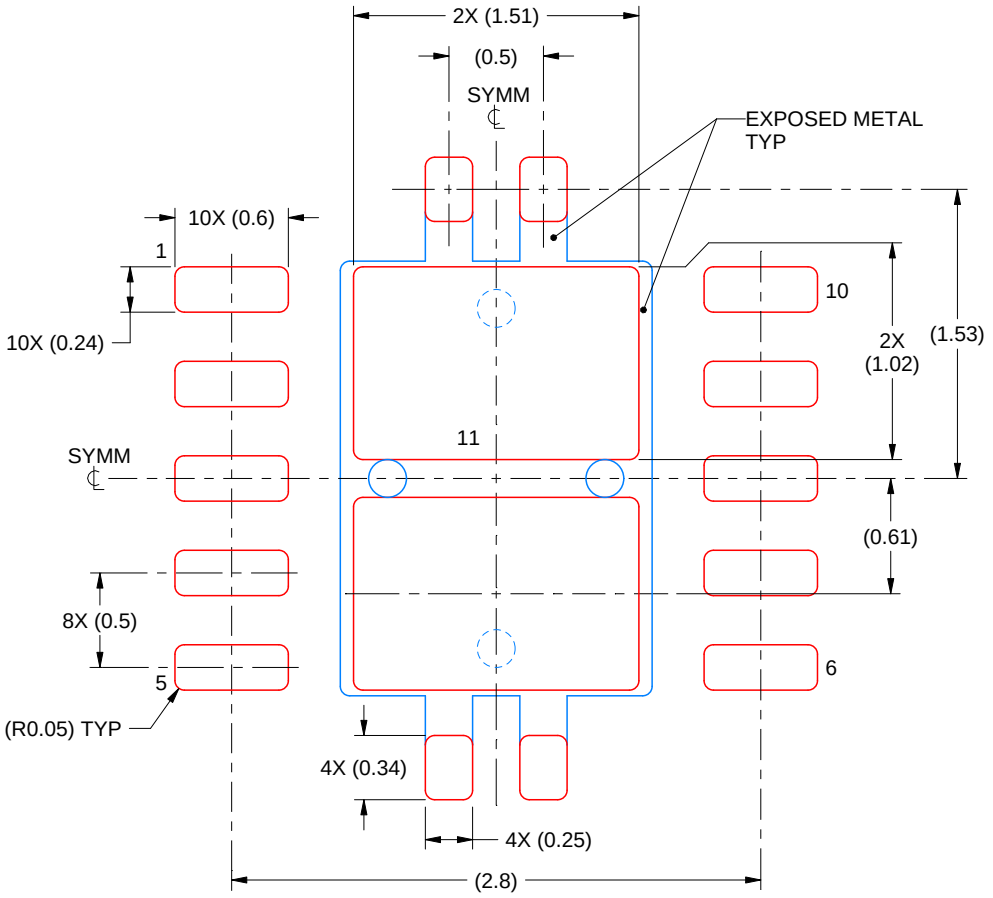
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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