

## 具有集成浪涌保护功能的 TIOS101、TIOS101x 数字传感器输出驱动器

### 1 特性

- 提供功能安全
  - 可帮助进行功能安全系统设计的文档：  
[TIOS101](#)、[TIOS1013](#)、[TIOS1015](#)
- 7V 至 36V 电源电压
- PNP、NPN 或推挽可配置输出
- 在 250mA 条件下，残余电压低，为 1.75V
- 50mA 至 350mA 可配置电流限制
- 耐受  $\pm 65V$  瞬态电压（时间低于 100 $\mu s$ ）
- VCC、OUT 和 GND 上高达 60V 的反极性保护
- VCC 和 OUT 上有集成式 EMC 保护
  - $\pm 16kV$  IEC 61000-4-2 ESD 接触放电
  - $\pm 4kV$  IEC 61000-4-4 电气快速瞬变
  - $\pm 1.2kV/500\Omega$  IEC 61000-4-5 浪涌
- 高达 1.5H 电感负载的快速消磁功能
- 大电容负载驱动能力
- < 2.2mA 静态电源电流
- 集成式 LDO 选项可支持高达 20mA 的电流
  - TIOS101：无 LDO
  - TIOS1013：3.3V LDO
  - TIOS1015：5V LDO
- 过热警告和热保护
- 故障指示灯
- 工作环境温度：-40°C 至 125°C
- 2.5mm x 3mm 10 引脚 VSON 封装

### 2 应用

- 接近开关
- 电容式和电感式传感器
- 数字输出

### 3 说明

TIOS101(x) 器件可配置为高侧、低侧或推挽驱动器。这些器件能够承受高达 1.2kV (500 $\Omega$ ) 的 IEC 61000-4-5 浪涌，并具有集成反向极性保护。

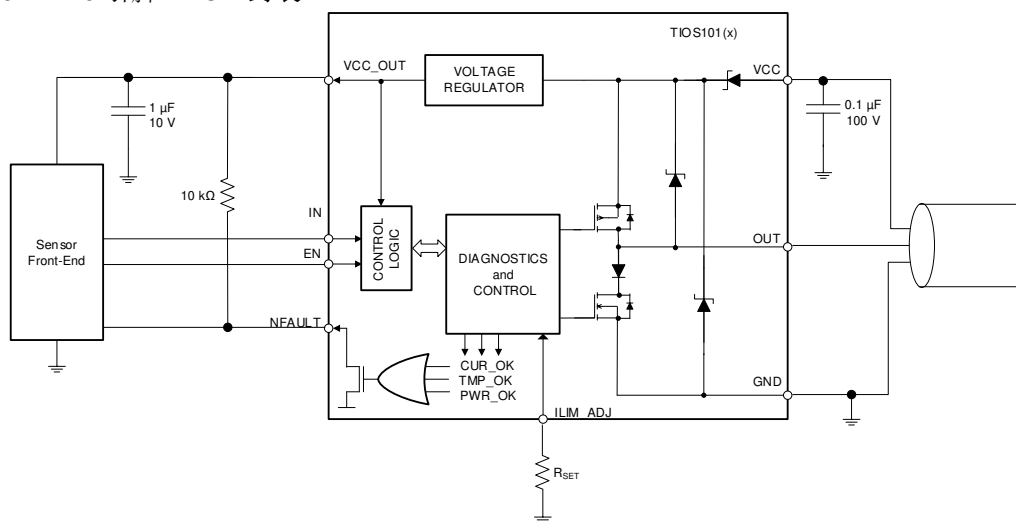
只需通过一个简单的引脚可编程接口，便可轻松连接到控制器电路。输出电流限制可使用外部电阻器进行配置。

此外，它们提供了故障报告和内部保护功能，可应对欠压、过流和过热条件。

#### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 (标称值)
TIOS101	VSON (10)	2.50mm x 3.00mm
TIOS1013		
TIOS1015		

(1) 如需了解所有可订购器件，请参阅数据表末尾的可订购产品附录。



典型应用图



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## 4 Revision History

Changes from Revision B (June 2019) to Revision C (February 2021)	Page
• 向特性列表添加了“功能安全”.....	1

Changes from Revision A (August 2018) to Revision B (June 2019)	Page
• 向数据表添加了器件编号 TIOS1013 和 TIOS1015.....	1
• 将所有 TIOS101-3 更改为 TIOS1013 并将 TIOS101-5 更改为 TIOS1015.....	1
• 将特性从“VCC 上高达 55V 的反极性保护”更改为“VCC 上高达 60V 的反极性保护”.....	1
• Changed the Supply voltage values From: MIN = - 55 V, MAX = 50 V To: MIN = - 60 V, MAX = 60 V in the <i>Absolute Maximum Ratings</i> .....	4
• Changed the Voltage difference Max value From: 55 V To: 60 V in the <i>Absolute Maximum Ratings</i> .....	4
• Changed  55 V  To:  60 V  in the Leakage current Test Conditions in the Electrical Characteristics.....	5
• Changed text From: "not exceed 55 V DC at any time." To: "not exceed 60 V DC at any time." in the <i>Reverse Polarity Protection</i> section.....	13

Changes from Revision * (July 2017) to Revision A (August 2018)	Page
• Changed the <i>Thermal Information</i> table values.....	5

## 5 Pin Configuration and Functions

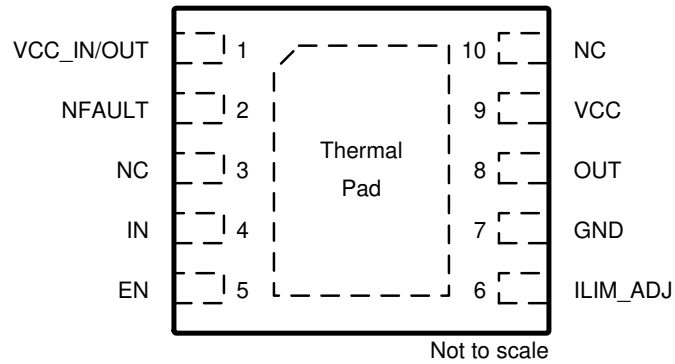


图 5-1. DMW Package, 10-Pin (VSON), Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	8	O	Switch output
VCC	9	POWER	Supply voltage (24 V nominal)
GND	7	POWER	Device ground
EN	5	I	Driver enable input signal from the local controller. Logic low sets the OUT output at Hi-Z. Weak internal pull-down.
IN	4	I	Transmit data input from the local controller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
VCC_IN/OUT	1	POWER	3.3-V or 5-V linear regulator output; external 3.3-V or 5-V logic supply input for option without LDO.
ILIM_ADJ	6	I	Input for current limit adjustment. Connect resistor $R_{SET}$ between ILIM_ADJ and GND.
NFAULT	2	OPEN-DRAIN	Fault indicator output signal to the microcontroller. A low level indicates either an over-current, an undervoltage in supply or an overtemperature condition. Connect this pin via pull-up resistor to VCC_IN/OUT.
NC	3, 10	—	No internal connection.
Thermal Pad	—	—	Connect to GND plane for optimal thermal and electrical performance

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
Supply voltage	Steady state voltage for VCC and OUT	- 60	60	V
	Transient pulse width < 100 μs for VCC and OUT	- 65	65	V
Voltage difference	V <sub>(VCC)</sub> - V <sub>(OUT)</sub>		60	V
Logic supply voltage (TIOS101)	VCC_IN	- 0.3	6	V
Input logic voltage	IN, EN, ILIM_ADJ	- 0.3	6	V
Output current	NFAULT	- 5	5	mA
Storage temperature, T <sub>stg</sub>		-55	170	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with reference to the GND pin, unless otherwise specified.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Contact discharge, per IEC 61000-4-2 <sup>(2)</sup> <sup>(3)</sup>	±16000	
		Electrical fast transient, per IEC 61000-4-4 <sup>(2)</sup>	±4000	
		Surge protection with 500 Ω, per IEC 61000-4-5; 1.2/50 μs <sup>(2)</sup>	±1200	
		All pins		
		Pins VCC, OUT and GND		

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- Minimum 100-nF capacitor is required between VCC and GND. Minimum 1-μF capacitor is required between VCC\_IN/OUT and GND.
- Passing level is ±4500 V if the device is powered and EN=IN=HIGH.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>(VCC)</sub>	Supply voltage	7	24	36	V
V <sub>(VCC_IN)</sub>	Logic level input voltage (TIOS101 only)	3.3 V configuration	3.3	3.6	V
		5 V configuration	4.5	5.5	V
R <sub>SET</sub>	External resistor for OUT current limit	0		100	kΩ
1/t <sub>BIT</sub>	Signaling rate (push-pull mode)			250	kbps
I <sub>(VCC_OUT)</sub>	LDO output current (TIOS1013 and TIOS1015 only)			20	mA
T <sub>A</sub>	Operating ambient temperature	- 40		125	°C
T <sub>J</sub>	Junction temperature			150	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TIOS101(x)	UNIT
		DMW (10 Pins)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	13.4	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	40.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	25.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES (VCC)</b>						
$I_{(VCC)}$	Quiescent supply current	EN = LOW, no load		1.5	2.2	mA
		EN = HIGH, no load		2	2.7	mA
<b>LOGIC-LEVEL INPUTS (EN, IN)</b>						
$V_{IL}$	Input logic low voltage				0.8	V
$V_{IH}$	Input logic high voltage		2			V
$R_{PD}$	Pull-down (EN) resistance			100		k $\Omega$
$R_{PU}$	Pull-up (IN) resistance			200		k $\Omega$
<b>CONTROL OUTPUT (NFAULT)</b>						
$V_{OL}$	Output logic low voltage	$I_O = 4$ mA			0.5	V
$I_{OZ}$	Output high impedance leakage	Output in Hi-Z, $V_O = 0$ V or VCC_IN/OUT	-1		1	$\mu$ A
<b>DRIVER OUTPUT (OUT)</b>						
$V_{DS(ON)}$	High-side driver residual voltage	$I = 250$ mA			1.75	V
		$I = 200$ mA			1.5	V
		$I = 100$ mA			1.1	V
	Low-side driver residual voltage	$I = 250$ mA			1.75	V
		$I = 200$ mA			1.5	V
		$I = 100$ mA			1.1	V
$I_P$	OUT pull-up/down current	EN = LOW, IN = LOW, pull-down current	40	50	80	$\mu$ A
		EN = LOW, IN = HIGH, pull-up current	40	50	80	$\mu$ A
$I_{O(LIM)}$	Driver output current limit	$R_{SET} = 100$ k $\Omega$	35	50	70	mA
		$R_{SET} = 0$ k $\Omega$	300	350	400	mA
		$R_{SET} = OPEN^{(1)}$	300	350	400	mA
<b>PROTECTION CIRCUITS</b>						
$V_{(UVLO)}$	VCC under voltage lockout	VCC falling; NFAULT = Hi-Z			6	V
		VCC rising; NFAULT = LOW			6.5	V
$V_{(UVLO,HYS)}$	VCC under voltage hysteresis	Rising to falling threshold	100			mV
$V_{(UVLO,IN)}$	VCC_IN under voltage lockout (No LDO option)	VCC_IN falling; NFAULT = Hi-Z		2.4		V
		VCC_IN rising; NFAULT = LOW		2.5		V
$V_{(UVLO,HYS)}$	VCC_IN under voltage hysteresis (No LDO option)	Rising to falling threshold		100		mV
$T_{(WRN)}$	Thermal warning		125			°C
$T_{(SDN)}$	Thermal shutdown	Die temperature $T_J$	150	160		°C
$T_{(HYS)}$	Thermal hysteresis for shutdown			10		°C

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{REV}$	Leakage current in reverse polarity	$V_{(OUT)} < V_{(VCC)}$ or $V_{(OUT)} > V_{(VCC)}$ up to  36 V			50	$\mu A$
		$V_{(OUT)} < V_{(OUT)}$ or $V_{(OUT)} > V_{(VCC)}$ up to  60 V			80	$\mu A$
		EN = HIGH, IN = LOW; $V_{(OUT \text{ to } VCC)} = 3 \text{ V}$			550	$\mu A$
		EN = HIGH, IN = HIGH; $V_{(OUT \text{ to } GND)} = -3 \text{ V}$			10	$\mu A$
<b>LINEAR REGULATOR (LDO)</b>						
$V_{(VCC\_OUT)}$	Voltage regulator output	TIOS1015	4.75	5	5.25	V
		TIOS1013	3.13	3.3	3.46	V
$V_{(DROP)}$	Voltage regulator drop-out voltage ( $V_{(VCC)} - V_{(VCC\_OUT)}$ )	$I_{CC} = 20 \text{ mA}$ load current	TIOS1015		1.9	V
			TIOS1013		2.3	V
REG	Line regulation ( $dV_{(VCC\_OUT)}/dV_{(VCC)}$ )	$I_{(VCC\_OUT)} = 1 \text{ mA}$			1.7	mV/V
$L_{REG}$	Load regulation ( $dV_{(VCC\_OUT)}/V_{(VCC\_OUT)}$ )	$V_{(VCC)} = 24 \text{ V}$ , $I_{(VCC\_OUT)} = 100 \mu A$ to 20 mA			1%	
PSSR	Power Supply Rejection Ratio	100 kHz, $I_{(VCC\_OUT)} = 20 \text{ mA}$		40		dB

(1) Current fault indication will be active. Current fault auto recovery will be de-activated.

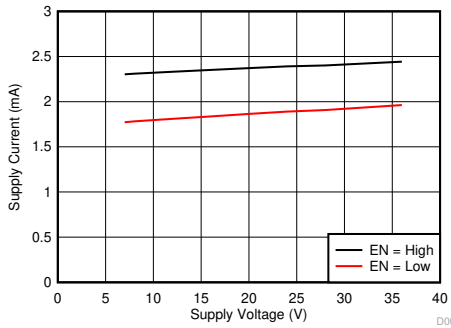
## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{PLH}$ , $t_{PHL}$	Driver propagation delay	See <a href="#">图 7-1</a> See <a href="#">图 7-2</a> See <a href="#">图 7-3</a> $R_L = 2 \text{ k}\Omega$ $C_L = 5 \text{ nF}$ $R_{(SET)} = 0 \Omega$		600	800	ns	
$t_{P(skew)}$	Driver propagation delay skew. $ t_{PLH} - t_{PHL} $			100		ns	
$t_{PZH}$ , $t_{PZL}$	Driver enable delay					4	$\mu s$
$t_{PHZ}$ , $t_{PLZ}$	Driver disable delay					4	$\mu s$
$t_r$ , $t_f$	Driver output rise, fall time					150	ns
$ t_r - t_f $	Difference in rise and fall time					50	ns
$t_{SC}$	Current fault blanking time			175	200		$\mu s$
$t_{pSC}$	Current fault indication delay					260	$\mu s$
$t_{SCEN}$	Current fault driver re-enable wait time			15		ms	
$t_{(UVLO)}$	OUT re-enable delay after UVLO <sup>(1)</sup>	$V_{(UVLO)}$ rising threshold crossing time to OUT enable time	10	30	50	ms	

(1) OUT output remains Hi-Z for this time

## 6.7 Typical Characteristics



No load IN = OPEN 25°C

图 6-1. Supply Current vs Supply Voltage

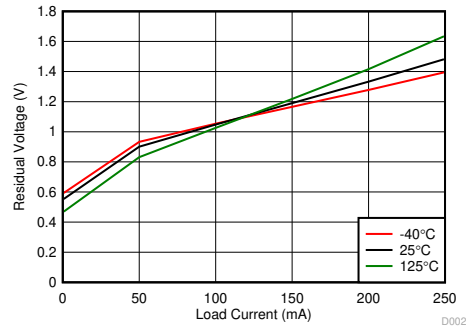


图 6-2. Residual Voltage vs Load Current: High Side

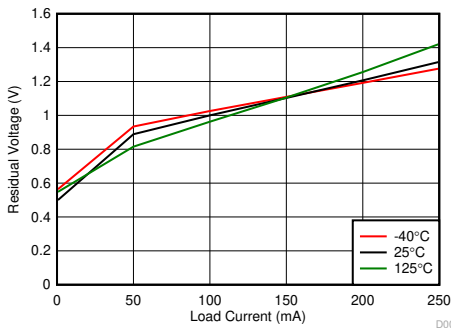


图 6-3. Residual Voltage vs Load Current: Low Side

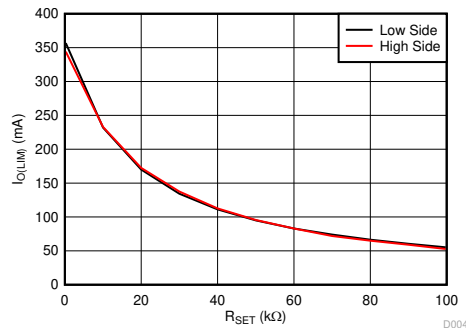


图 6-4. Current Limit vs R<sub>SET</sub>

## 7 Parameter Measurement Information

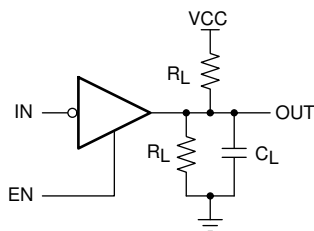


图 7-1. Test Circuit for Driver Switching

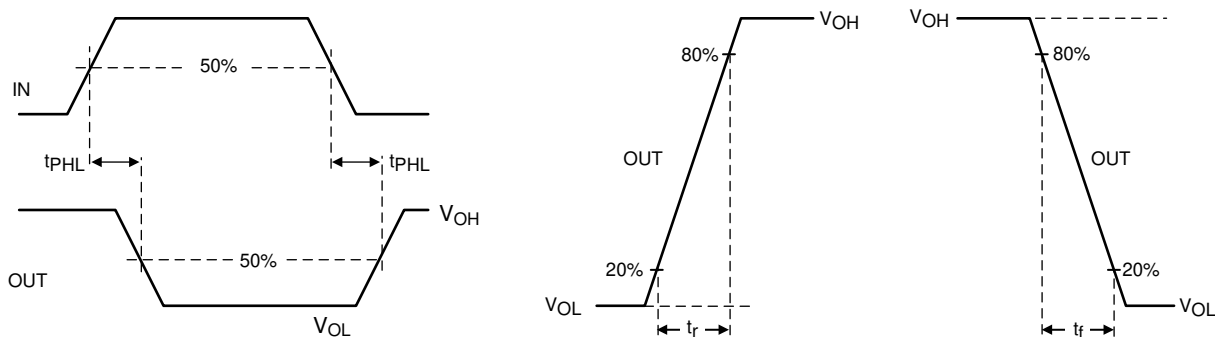


图 7-2. Waveforms for Driver Output Switching Measurements

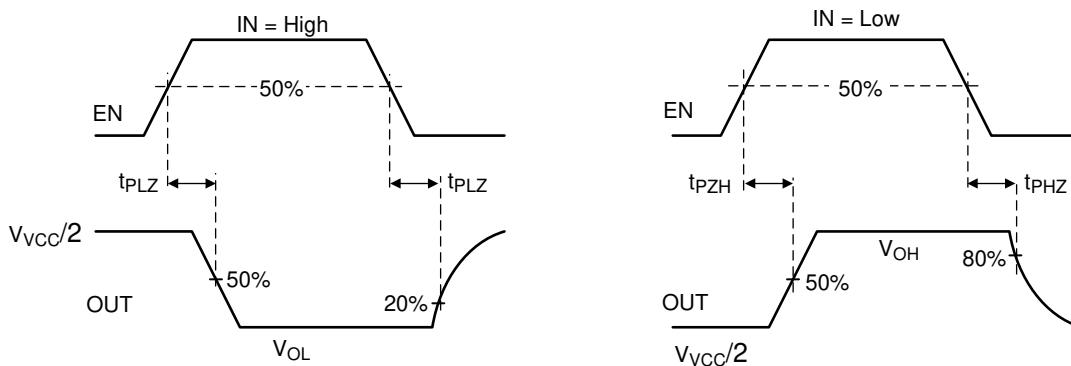


图 7-3. Waveforms for Driver Enable or Disable Time Measurements



## 8 Detailed Description

### 8.1 Overview

Figure 8-1 shows that the device driver output (OUT) can be used in a push-pull, high-side, or low-side configuration using the enable (EN) and transmit data (IN) input pins. OUT can drive resistive, large capacitive or large inductive loads.

TIOS101 and TIOS101x devices have integrated IEC 61000-4-4/5 EFT and surge protection. In addition, tolerance to  $\pm 65\text{-V}$  transients enables flexibility to choose from a wider range of TVS diodes if an application requires higher levels of protection. These integrated robustness features will simplify the system-level design by reducing the external protection circuitry.

These devices implement protection features for over-current, over-voltage and over-temperature conditions. The devices also provide a current-limit setting of the driver output current using an external resistor.

The TIOS101x devices derive the low voltage supply from the typical 24 V industrial supply via an internal linear regulator to provide power to the local controller and sensor circuitry.

### 8.2 Functional Block Diagrams

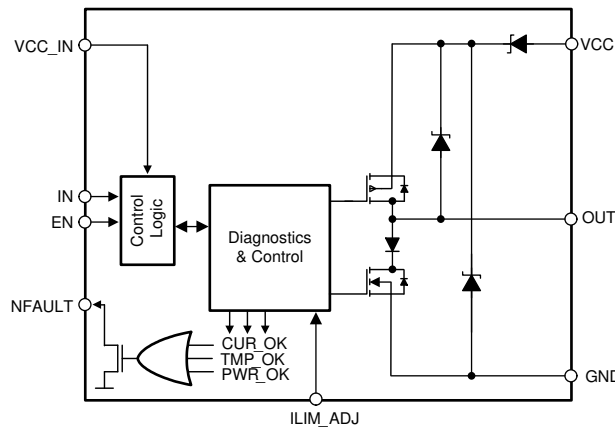


Figure 8-1. Block Diagram, TIOS101

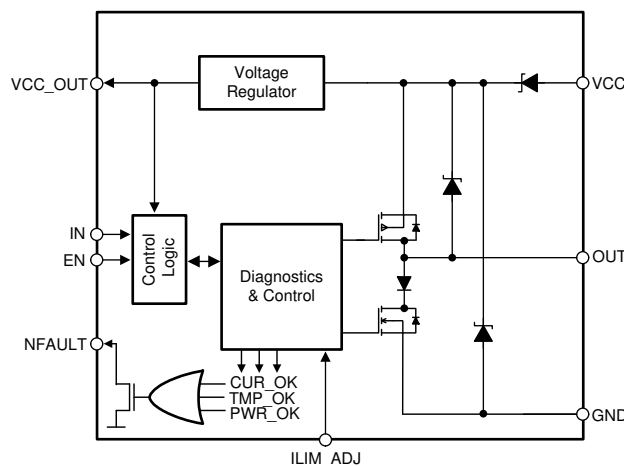


Figure 8-2. Block Diagram, TIOS101x

## 8.3 Feature Description

### 8.3.1 Current Limit Configuration

The output current can be configured with an internal resistor on ILIM\_ADJ pin. The maximum settable current limit is 300 mA. This maximum setting specifies a minimum of 300 mA over temperature and voltage.

Output disable due to current fault and current fault auto recovery features can be disabled by floating ILIM\_ADJ pin. However, the current fault indication is still active in this configuration. This feature is useful when driving large capacitances.

表 8-1. Current Limitation

ILIM_ADJ Pin Condition	OUT Current Limit	NFAULT Indication During Fault	Output Disable and Auto Recovery
R <sub>SET</sub> resistor to GND	Variable	Yes	Yes
Connected to GND	300 mA	Yes	Yes
OPEN	300 mA	Yes	No

### 8.3.2 Current Fault Detection, Indication and Auto Recovery

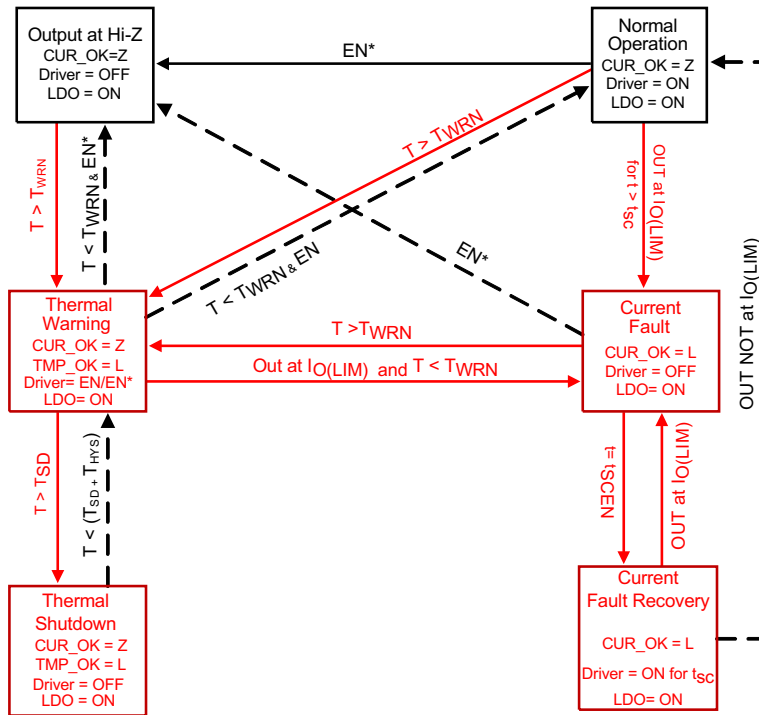
If the output current at OUT exceeds the internally set current limit  $I_{O(LIM)}$  for a duration longer than  $t_{SC}$ , the NFAULT pin is driven logic low to indicate a fault condition. The output is turned off, but the LDO continues to function. The output periodically retries to check if the output is still in the over current condition. In this mode, the output is switched on for  $t_{SC}$  in  $t_{SCEN}$  intervals. Current fault auto recovery mode can be disabled by setting ILIM\_ADJ = OPEN. See 表 8-3. Toggling EN will clear NFAULT.

### 8.3.3 Thermal Warning, Thermal Shutdown

If the die temperature exceeds  $T_{(WRN)}$ , the NFAULT flag is held low indicating a potential over temperature problem. When the  $T_J$  exceeds  $T_{(SDN)}$ , The output is disabled but the LDO remains operational. As soon as the temperature drops below the temperature threshold (and after  $T_{(HYS)}$ ), the internal circuit re-enables the driver, subject to the state of the EN and IN pins.

### 8.3.4 Fault Reporting (NFAULT)

NFAULT is driven low if either a current fault condition is detected, die temperature has exceeded  $T_{(WRN)}$  or supply has dropped below the UVLO threshold. NFAULT returns to high-impedance as soon as all three fault conditions clear.



$$NFAULT = [CUR\_OK \&\& PWR\_OK \&\& TMP\_OK]$$

图 8-3. Device State Diagram

### 8.3.5 Device Function Tables

表 8-2. Driver Function

EN	IN	OUT	COMMENT
L / Open	X	Hi-Z	Device is in ready-to-receive state
H	L	H	OUT is sourcing current (high-side drive)
H	H / Open	L	OUT is sinking current (low-side drive)

表 8-3. Current Limit Indicator Function ( $t > t_{SC}$ )

EN	IN	OUT CURRENT	NFAULT	COMMENT
H	H / Open	$ I_{(OUT)}  > I_{O(LIM)}$	L	OUT current exceeds the set limit for over $t_{SC}$
		$ I_{(OUT)}  < I_{O(LIM)}$	Z	Normal operation
H	L	$ I_{(OUT)}  > I_{O(LIM)}$	L	OUT current exceeds the set limit for over $t_{SC}$
		$ I_{(OUT)}  < I_{O(LIM)}$	Z	Normal operation
L / Open	X	X	Z	Driver is disabled, current limit indicator is inactive

### 8.3.6 The Integrated Voltage Regulator (LDO)

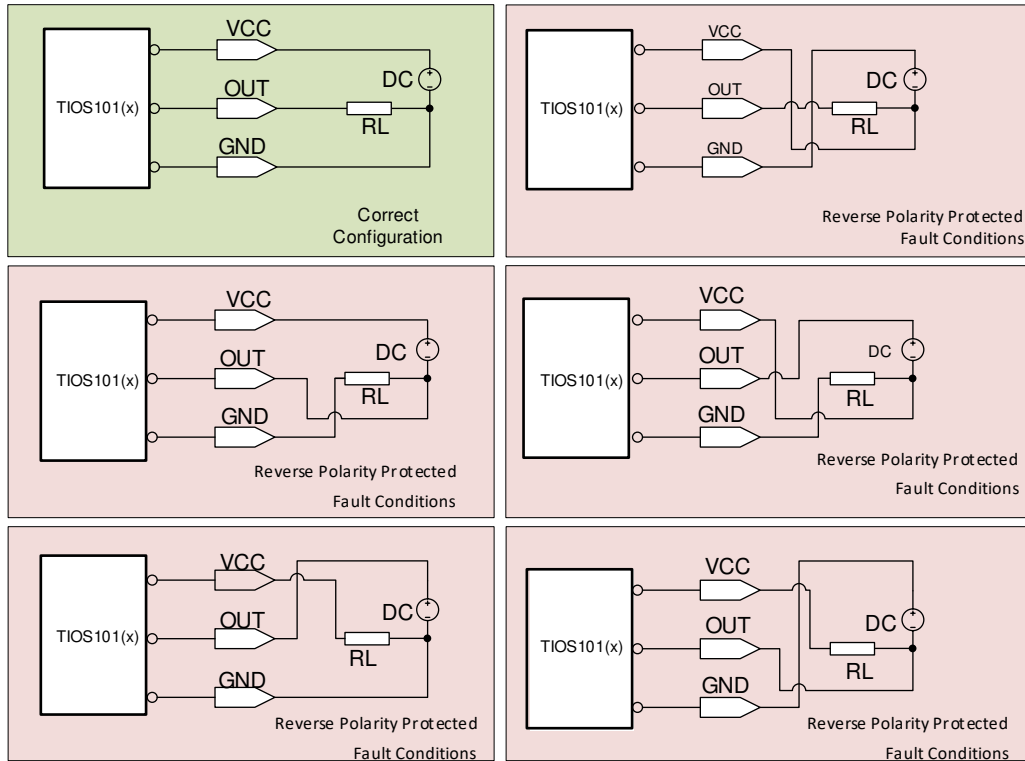
The TIOS1013 and TIOS1015 each have an integrated linear voltage regulator (LDO) which can supply power to external components. The voltage regulator is specified for VCC voltages in the range of 7 V to 36 V with respect to GND. The LDO is capable of delivering up to 20 mA. The LDO output is current limited to 35-mA to limit the inrush current onto VCC\_OUT decoupling capacitors during initial power up.

The LDO is designed to be stable with standard ceramic capacitors with values of 1  $\mu$ F or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1  $\Omega$ . With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1  $\mu$ F.

### 8.3.7 Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the VCC, OUT and GND pins. The maximum voltage between any of the pins may not exceed 60 V DC at any time.

图 8-4 和 图 8-5 shows all the possible connection combinations.



**图 8-4. High-Side Driver Configuration**

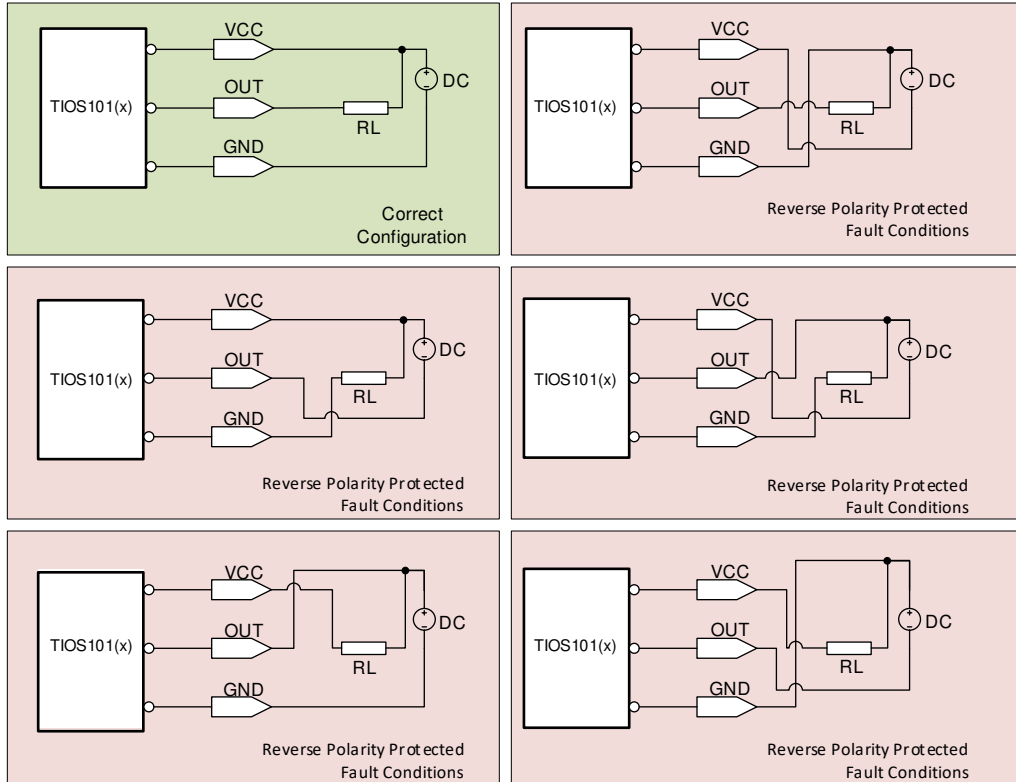
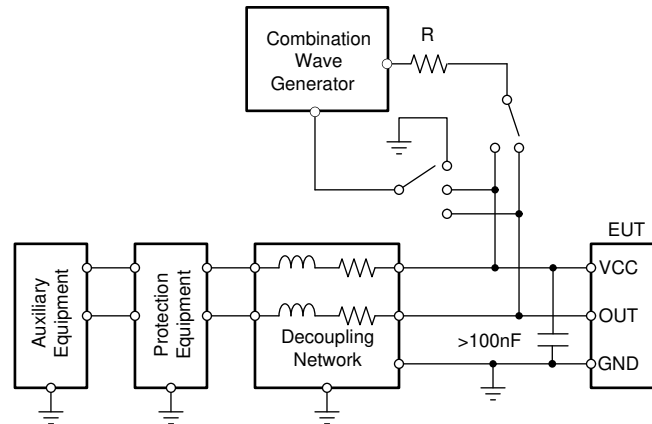


图 8-5. Low-Side Driver Configuration

### 8.3.8 Integrated Surge Protection and Transient Waveform Tolerance

The VCC and OUT pins of the device are capable of withstanding up to 1.2 kV of 1.2/50 - 8/20  $\mu$ s IEC 61000-4-5 surge with a source impedance of 500  $\Omega$ . The surge testing should be performed with a minimum 100 nF supply decoupling capacitor between VCC and GND, and 1  $\mu$ F between VCC\_IN/OUT and GND.

External TVS diodes may be required for higher transient protection levels. The system designer should ensure that the maximum clamping voltage of the external diodes should be < 65 V at the desired current level. The device is capable of withstanding up to  $\pm$ 65-V transient pulses < 100  $\mu$ s.



1.2/50 - 80/20  $\mu$ s CWG  
R = 500  $\Omega$

**图 8-6. Surge Test Setup**

### 8.3.9 Power Up Sequence

VCC\_IN and VCC domains can be powered up in any sequence. In the event of VCC is powered and VCC\_IN is not, the OUT pin remains in high impedance.

### 8.3.10 Undervoltage Lock-Out (UVLO)

The device enters UVLO if the VCC voltage falls below  $V_{(UVLO)}$ . (For the device without the integrated LDO, the device monitors VCC\_IN in addition to VCC. UVLO happens if either supply falls below the threshold.)

As soon as the supply falls below  $V_{(UVLO)}$ , NFAULT is pulled low, the LDO is turned off and the OUT output is disabled (Hi-Z). Receiver performance is not specified in this mode.

When the supply rises above  $V_{(UVLO)}$ , NFAULT returns to Hi-Z (given no other fault conditions present) and the LDO will be enabled immediately. The OUT output will be turned on after  $T_{(UVLO)}$  delay.

## 8.4 Device Functional Modes

These devices can operate in three different modes.

### 8.4.1 NPN Configuration (N-Switch Mode)

Set IN pin high (or open) and use EN pin as control for realizing the function of an N-switch (low-side configuration) on OUT.

### 8.4.2 PNP Configuration (P-Switch Mode)

Set IN pin low and use EN pin as control for realizing the function of a P-switch (high-side configuration) on OUT.

### 8.4.3 Push-Pull Mode

Set EN pin high and toggle IN as control for realizing the function of a push-pull output on OUT. 表 8-4, 表 8-5, and 表 8-6 summarize the pin configurations to accomplish the functional modes.

表 8-4. NPN Mode

EN	IN	OUT
L / Open	H / Open	Hi-Z
H	H / Open	N-Switch

表 8-5. PNP Mode

EN	IN	OUT
L / Open	L	Hi-Z
H	L	P-Switch

表 8-6. Push-Pull Mode

EN	IN	OUT
L / Open	X	Hi-Z
H	H / Open	N-Switch
H	L	P-Switch



## 9 Application Information Disclaimer

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

TIOS101 and TIOS101x are robust 24-V digital drivers for industrial sensors.

### 9.2 Typical Application

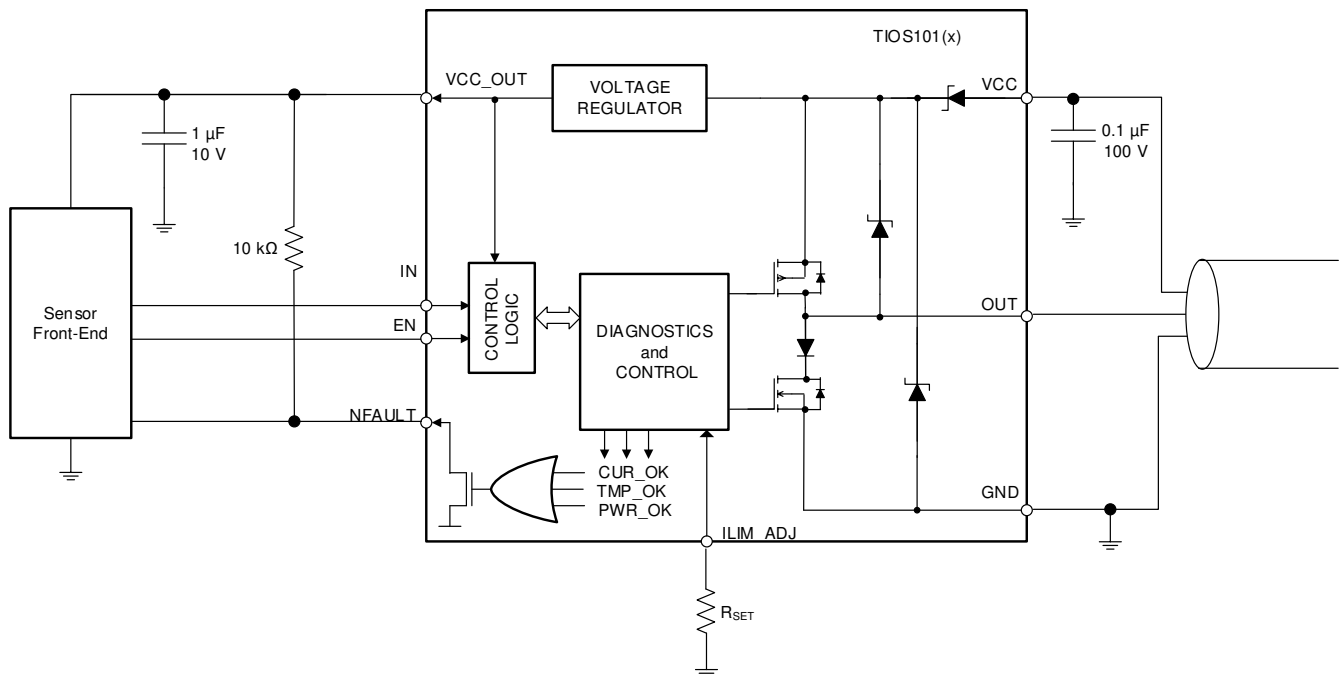


图 9-1. Typical Application Schematic

#### 9.2.1 Design Requirements

表 9-1 shows recommended components for a typical system design.

表 9-1. Design Parameters

PARAMETERS	VALUE
Input voltage range (VCC)	24 V, 30 V (max)
Output current (OUT)	200 mA
Output voltage (VCC_OUT), Pick TIOS1015	5 V
Maximum LDO output current (I <sub>VCC(OUT)</sub> )	5 mA
Pull-up resistors for NFAULT	10 kΩ
VCC decoupling capacitor	0.1 µF / 100 V
LDO output capacitor	1 µF / 10 V
ILIM_ADJ resistor (R <sub>SET</sub> )	10 kΩ
Maximum Ambient Temperature, T <sub>A</sub>	105°C

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Maximum Junction Temperature Check

For a 200 mA current limit:

- The maximum driver output current limit,  $I_{O(LIM)} = 250$  mA (allowed for current limit tolerance).
- The maximum voltage drop across the high-side switch is given with  $V_{DS(ON)} = 1.75$  V.

This causes a power consumption of:

$$PD_{OP} = V_{DS(ON)} \times I_{O(LIM)} = 1.75V \times 250 \text{ mA} = 437.5 \text{ mW} \quad (1)$$

For a 5 mA LDO current output,

$$PD_{LDO} = (V_{L+} - V_{VCC\_OUT}) \times I_{VCC\_OUT} = (30 - 5)V \times 5 \text{ mA} = 125 \text{ mW} \quad (2)$$

Total power dissipation,

$$PD = PD_{OP} + PD_{LDO} = 437.5 \text{ mW} + 125 \text{ mW} = 562.5 \text{ mW} \quad (3)$$

Multiply this value with the Junction-to-ambient thermal resistance of  $\theta_{JA} = 68.1^\circ\text{C/W}$  (taken from the [# 6.4](#) table) to receive the difference between junction temperature,  $T_J$ , and ambient temperature,  $T_A$ :

$$\Delta T = T_J - T_A = PD \times \theta_{JA} = 562.5 \text{ mW} \times 68.1^\circ\text{C/W} = 38.3^\circ\text{C} \quad (4)$$

Add this value to the maximum ambient temperature of  $T_A = 105^\circ\text{C}$  to receive the final junction temperature:

$$T_{J-max} = T_{A-max} + \Delta T = 105^\circ\text{C} + 38.3^\circ\text{C} = 143.3^\circ\text{C} \quad (5)$$

As long as  $T_{J-max}$  is below the recommended maximum value of  $150^\circ\text{C}$ , no thermal shutdown will occur. However, thermal warning may occur as the junction temperature is greater than  $T_{WRN}$ .

Note that the modeling of the complete system may be necessary to predict junction temperature in smaller PCBs and/or enclosures without air flow.

### 9.2.2.2 Driving Capacitive Loads

These devices are capable of driving capacitive loads on the OUT output. Assuming a pure capacitive load without series/parallel resistance, the maximum capacitance that can be charged without triggering current fault can be calculated as:

$$C_{LOAD} = \frac{[I_{O(LIM)} \times t_{SC}]}{V_{(VCC)}} \quad (6)$$

Higher capacitive loads can be driven if a series resistor is connected between the OUT and the load. Capacitive loads can be connected to VCC and GND.

### 9.2.2.3 Driving Inductive Loads

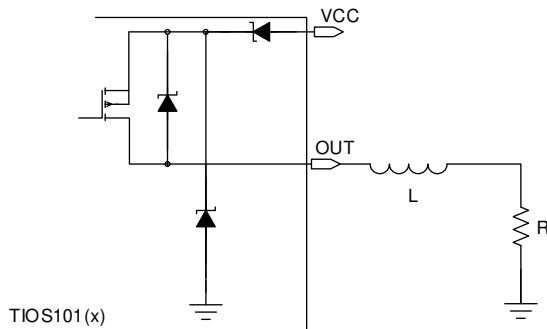
The TIOS101(x) family is capable of magnetizing and demagnetizing inductive loads up to 1.5 H. These devices contain internal circuitry that enables fast demagnetization when configured as either P-switch or N-switch mode.

In P-switch configuration, the load inductor L is magnetized when the OUT pin is driven high. When the PNP is turned off, there is a significant amount of negative inductive kick back at the OUT pin. This voltage is clamped internally at about -75 V.

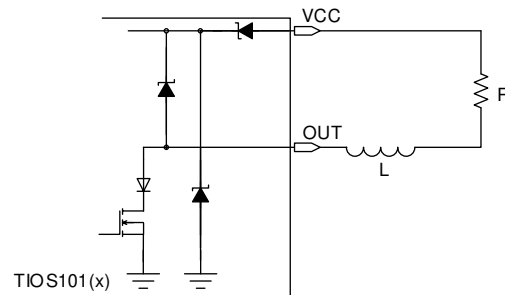
Similarly in N-switch configuration, the load inductor L is magnetized when the OUT pin is driven low. When the NPN is turned off, there is a significant amount of positive inductive kick back at the OUT pin. This voltage is clamped internally at about 75 V.

The equivalent protection circuits are shown in [图 9-2](#) and [图 9-3](#). The minimum value of the resistive load R can be calculated as:

$$R = \frac{V_{(VCC)}}{I_{O(LIM)}} \quad (7)$$

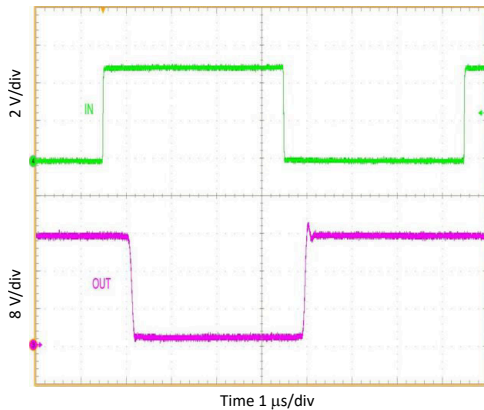


**图 9-2. PNP Mode**



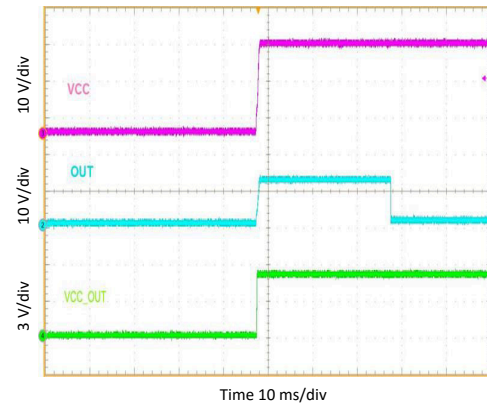
**图 9-3. NPN Mode**

### 9.2.3 Application Curves

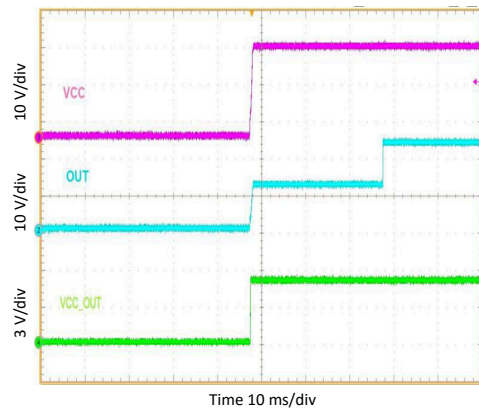


125 kHz

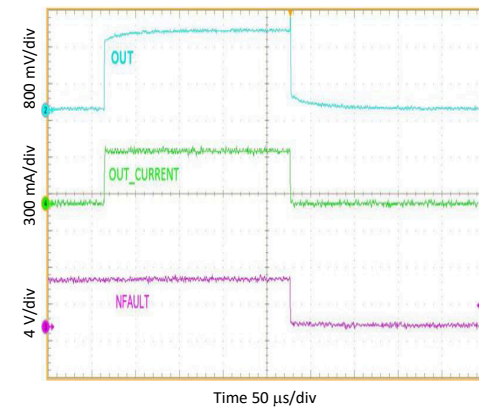
**图 9-4. OUT in Push-Pull Mode**



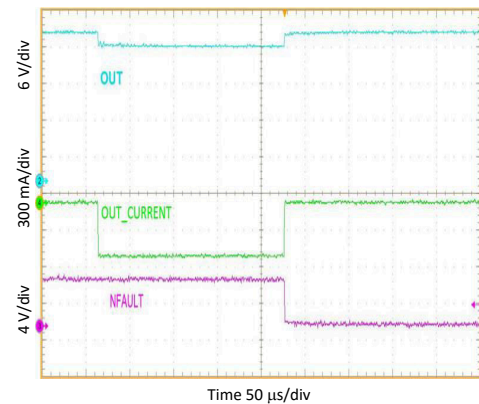
**图 9-5. OUT Power Up Delay, Low Side Mode**



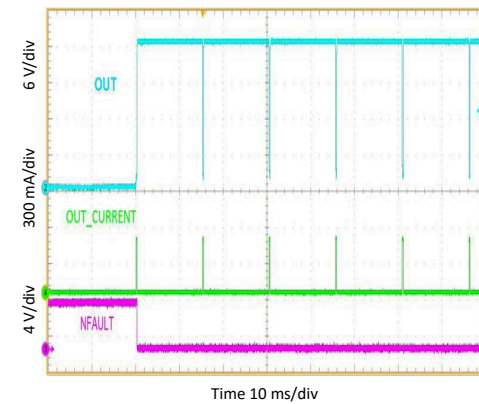
**图 9-6. OUT Power Up Delay, High Side Mode**



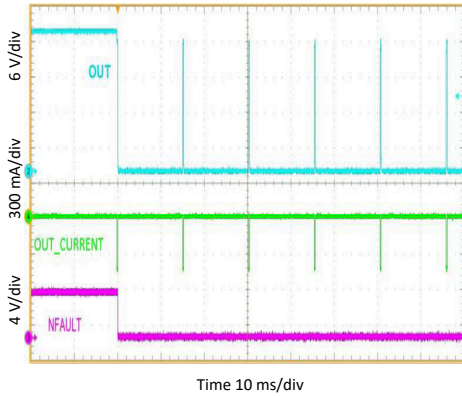
**图 9-7. OUT In Current Fault, Low Side Mode**



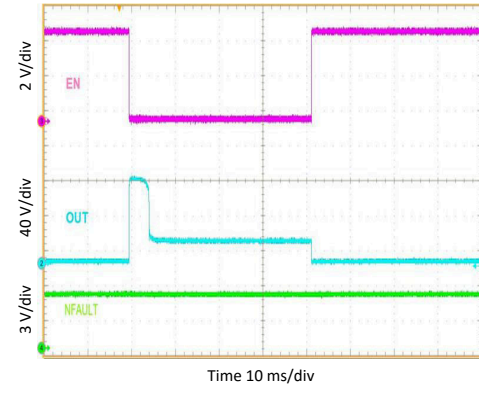
**图 9-8. OUT In Current Fault, High Side Mode**



**图 9-9. OUT In Current Fault Auto Recovery, Low Side Mode**

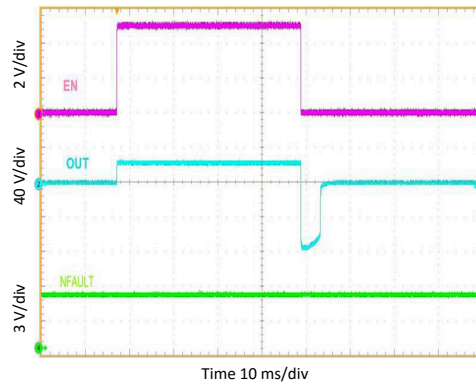


**图 9-10. OUT In Current Fault Auto Recovery, High Side Mode**



1.5-H Inductor With = 100 Ω R<sub>SET</sub> = OPEN

**图 9-11. OUT Driving, Low Side Mode**



1.5-H Inductor With = 100 Ω R<sub>SET</sub> = OPEN

**图 9-12. OUT Driving, High Side Mode**

## 10 Power Supply Recommendations

The TIOS101 and TIOS101x are designed to operate from a 24-V nominal supply at VCC, which can vary by +12 V and -17 V from the nominal value to remain within the device's recommended supply voltage range of 7 V to 36 V. This supply should be buffered with at least a 100-nF/100-V capacitor.

## 11 Layout

### 11.1 Layout Guidelines

- Use of a 4-layer board is recommended for good heat conduction. Use layer 1 (top layer) for control signals, layer 2 as GND, layer 3 for the 24-V supply plane (VCC), and layer 4 for the regulated output supply (VCC\_IN/OUT).
- Connect the thermal pad to GND with maximum amount of thermal vias for best thermal performance.
- Use entire planes for VCC, VCC\_IN/OUT and GND to assure minimum inductance.
- The VCC terminal must be decoupled to ground with a low-ESR ceramic decoupling capacitor with a minimum value of 100 nF. The capacitor must have a voltage rating of 50 V minimum (100 V depending on max sensor supply fault rating) and an X5R or X7R dielectric.
- • The optimum placement of the capacitor is closest to the VCC and GND terminals to reduce supply drops during large supply current loads. See [图 11-1](#) for a PCB layout example.
- Connect all open-drain control outputs via 10 k $\Omega$  pull-up resistors to the VCC\_IN/OUT plane to provide a defined voltage potential to the system controller inputs when the outputs are high-impedance.
- Connect the R<sub>SET</sub> resistor between ILIM\_ADJ and GND.
- Decouple the regulated output voltage at VCC\_IN/OUT to ground with a low-ESR, 1  $\mu$ F, ceramic decoupling capacitor. The capacitor should have a voltage rating of 10 V minimum and an X5R or X7R dielectric.

### 11.2 Layout Example

- VIA to Layer 2: Power Ground Plane (VCC)
- VIA to Layer 3: 24V Supply Plane (GND)
- VIA to Layer 4: Regulated Supply Plane (VCC\_IN/OUT)

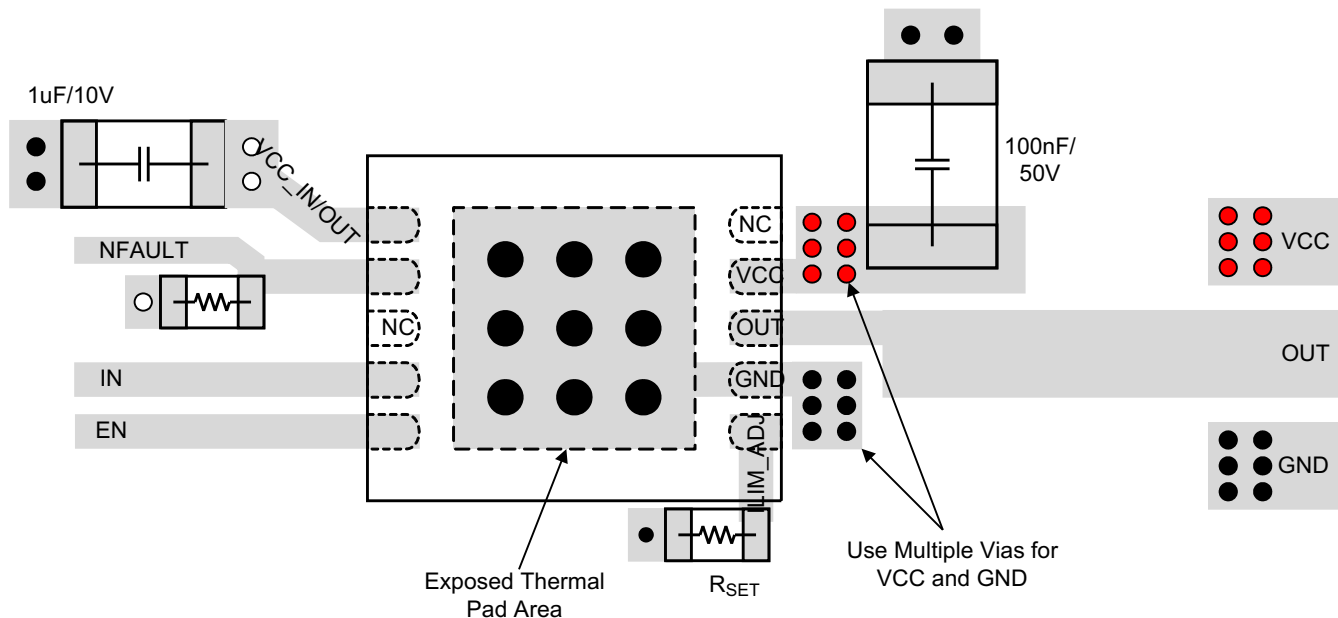


图 11-1. Layout Example

## 12 Device and Documentation Support

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIOS1013DMWR	ACTIVE	VSON	DMW	10	1500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS1013	<a href="#">Samples</a>
TIOS1013DMWT	ACTIVE	VSON	DMW	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS1013	<a href="#">Samples</a>
TIOS1015DMWR	ACTIVE	VSON	DMW	10	1500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS1015	<a href="#">Samples</a>
TIOS1015DMWT	ACTIVE	VSON	DMW	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS1015	<a href="#">Samples</a>
TIOS101DMWR	ACTIVE	VSON	DMW	10	1500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS101	<a href="#">Samples</a>
TIOS101DMWT	ACTIVE	VSON	DMW	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TS101	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

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**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

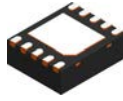
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TIOS1013DMWR	VSON	DMW	10	1500	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS1013DMWT	VSON	DMW	10	250	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS1015DMWR	VSON	DMW	10	1500	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS1015DMWT	VSON	DMW	10	250	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS101DMWR	VSON	DMW	10	1500	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2
TIOS101DMWT	VSON	DMW	10	250	178.0	13.5	2.75	3.35	1.05	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TIOS1013DMWR	VSON	DMW	10	1500	189.0	185.0	36.0
TIOS1013DMWT	VSON	DMW	10	250	189.0	185.0	36.0
TIOS1015DMWR	VSON	DMW	10	1500	189.0	185.0	36.0
TIOS1015DMWT	VSON	DMW	10	250	189.0	185.0	36.0
TIOS101DMWR	VSON	DMW	10	1500	189.0	185.0	36.0
TIOS101DMWT	VSON	DMW	10	250	189.0	185.0	36.0

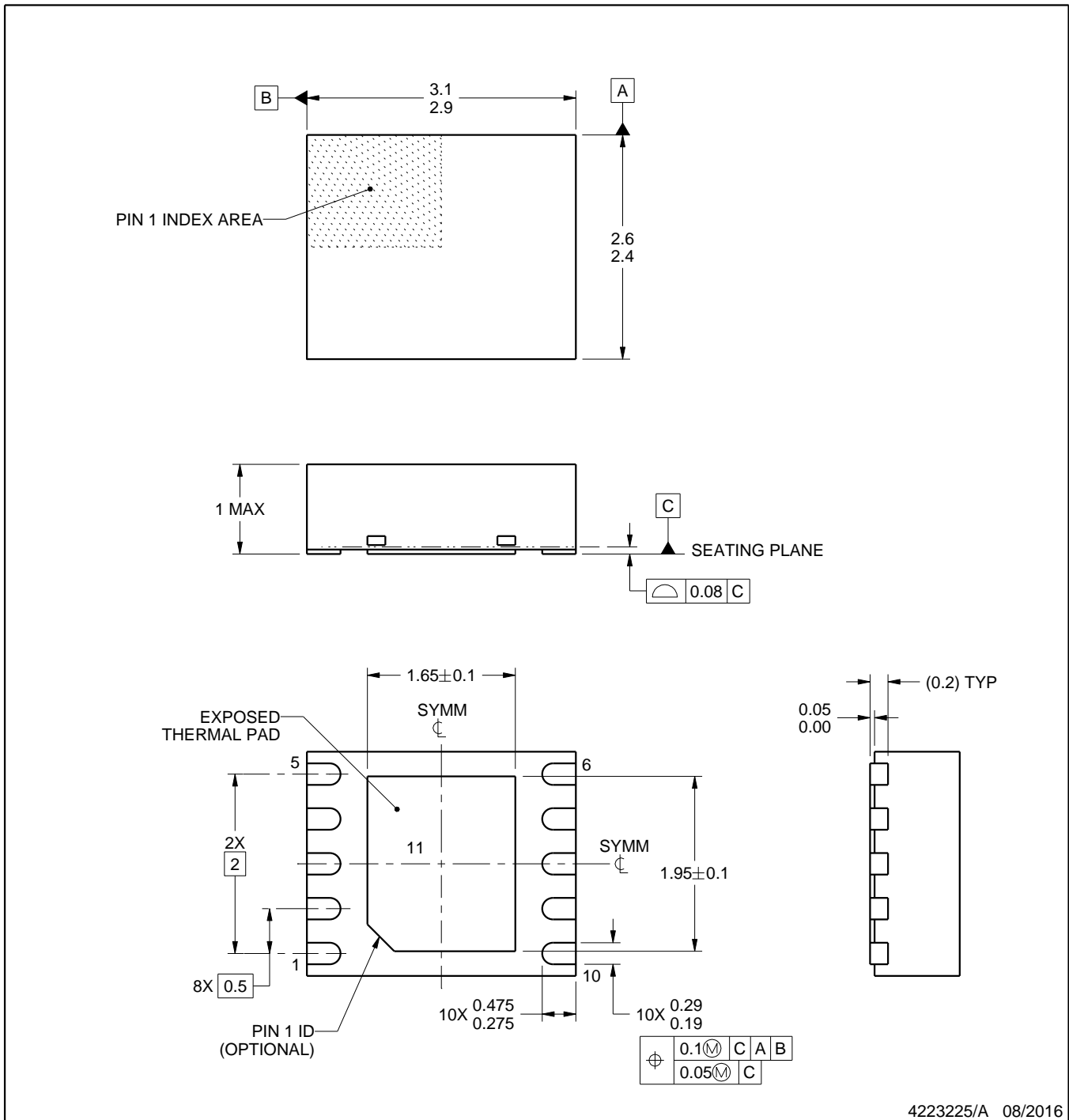
# DMW0010A



## PACKAGE OUTLINE

### VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4223225/A 08/2016

#### NOTES:

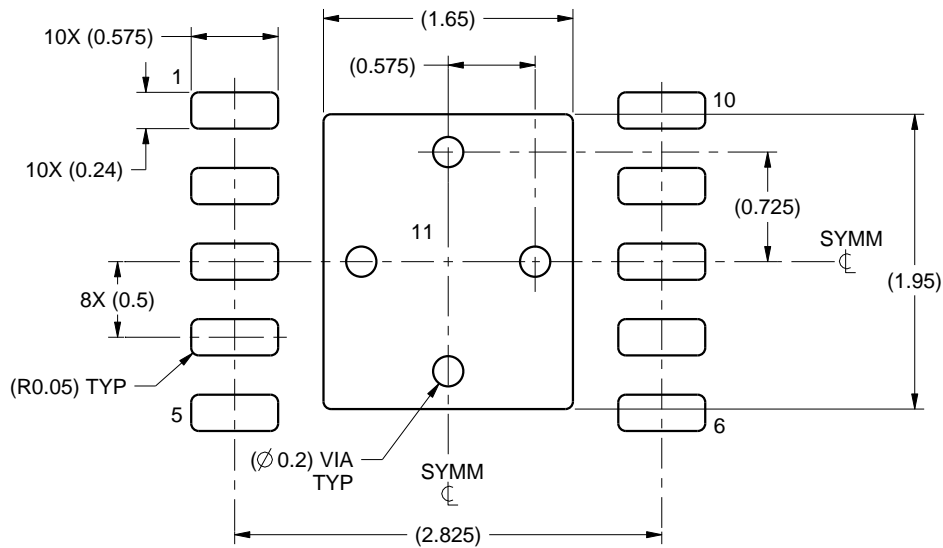
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

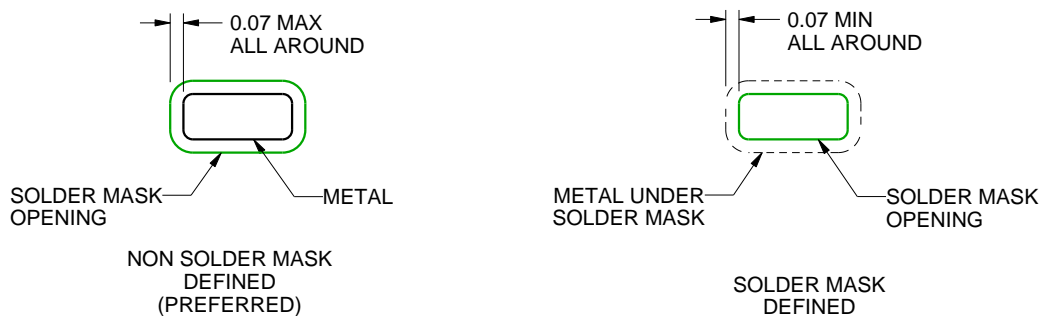
DMW0010A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

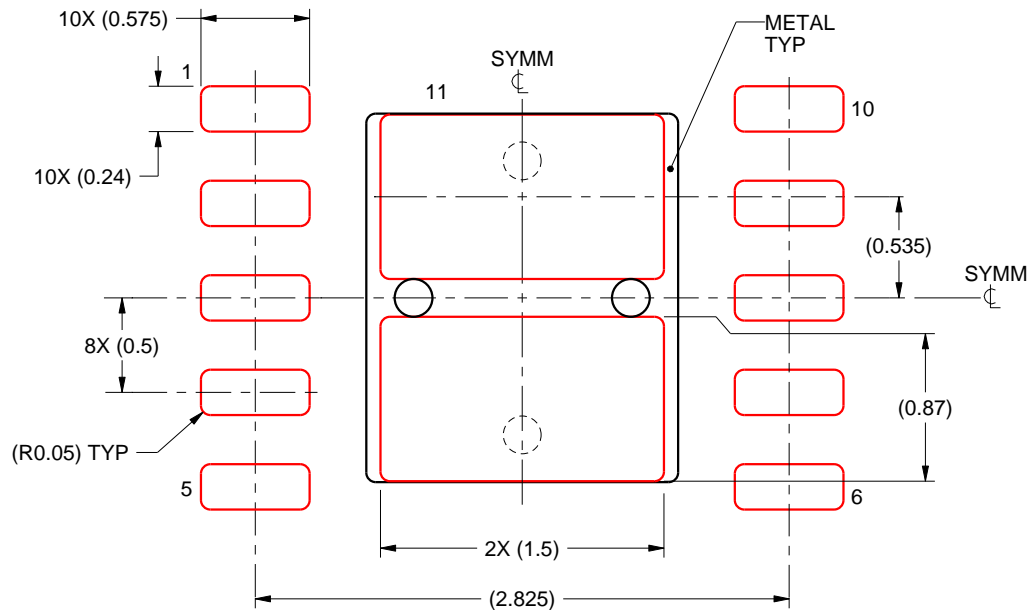
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DMW0010A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11  
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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[NCV1124DR2G](#) [ZSC31050FEG1-R](#) [ZSC31050FIG1-T](#) [ZSC31050FAG1-T](#) [ZSC31050FAG1-R](#) [ZSSC4151CE5R](#) [ZSSC3123AA2R](#)  
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