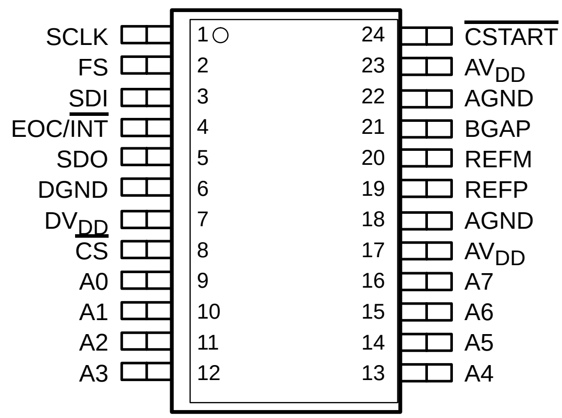
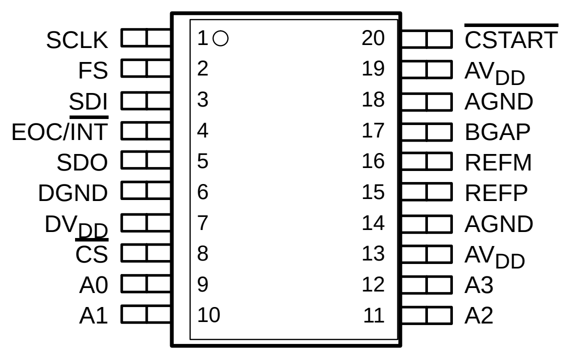
- **14-Bit Resolution**
- **Maximum Throughput 200 KSPS**
- **Analog Input Range 0-V to Reference Voltage**
- **Multiple Analog Inputs:**
  - **8 Channels for TLC3548**
  - **4 Channels for TLC3544**
- **Pseudodifferential Analog Inputs**
- **SPI/DSP-Compatible Serial Interfaces With SCLK up to 25 MHz**
- **Single 5-V Analog Supply; 3-/5-V Digital Supply**
- **Low Power:**
  - **4 mA (Internal Reference: 1.8 mA) for Normal Operation**
  - **20 μA in Autopower-Down**
- **Built-In 4-V Reference, Conversion Clock and 8x FIFO**
- **Hardware-Controlled and Programmable Sampling Period**
- **Programmable Autochannel Sweep and Repeat**
- **Hardware Default Configuration**
- **INL: ±1 LSB Max**
- **DNL: ±1 LSB Max**
- **SINAD: 80.8 dB**
- **THD: –95 dB**

TLC3548
DW OR PW PACKAGE
(TOP VIEW)



TLC3544
DW OR PW PACKAGE
(TOP VIEW)



description

The TLC3544 and TLC3548 are a family of 14-bit resolution high-performance, low-power, CMOS analog-to-digital converters (ADC). All devices operate from a single 5-V analog power supply and 3-V to 5-V digital supply. The serial interface consists of four digital inputs [chip select ($\overline{CS}$), frame sync (FS), serial input-output clock (SCLK), serial data input (SDI)], and a 3-state serial data output (SDO). $\overline{CS}$ (works as $\overline{SS}$, slave select), SDI, SDO, and SCLK form an SPI interface. FS, SDI, SDO, and SCLK form a DSP interface. The frame sync signal (FS) indicates the start of a serial data frame being transferred. When multiple converters connect to one serial port of a DSP, $\overline{CS}$ works as the chip select to allow the host DSP to access the individual converter. $\overline{CS}$ can be tied to ground if only one converter is used. FS must be tied to DV_{DD} if it is not used (such as in an SPI interface). When SDI is tied to DV_{DD}, the device is set in hardware default mode after power-on, and no software configuration is required. In the simplest case, only three wires (SDO, SCLK, and $\overline{CS}$ or FS) are needed to interface with the host.

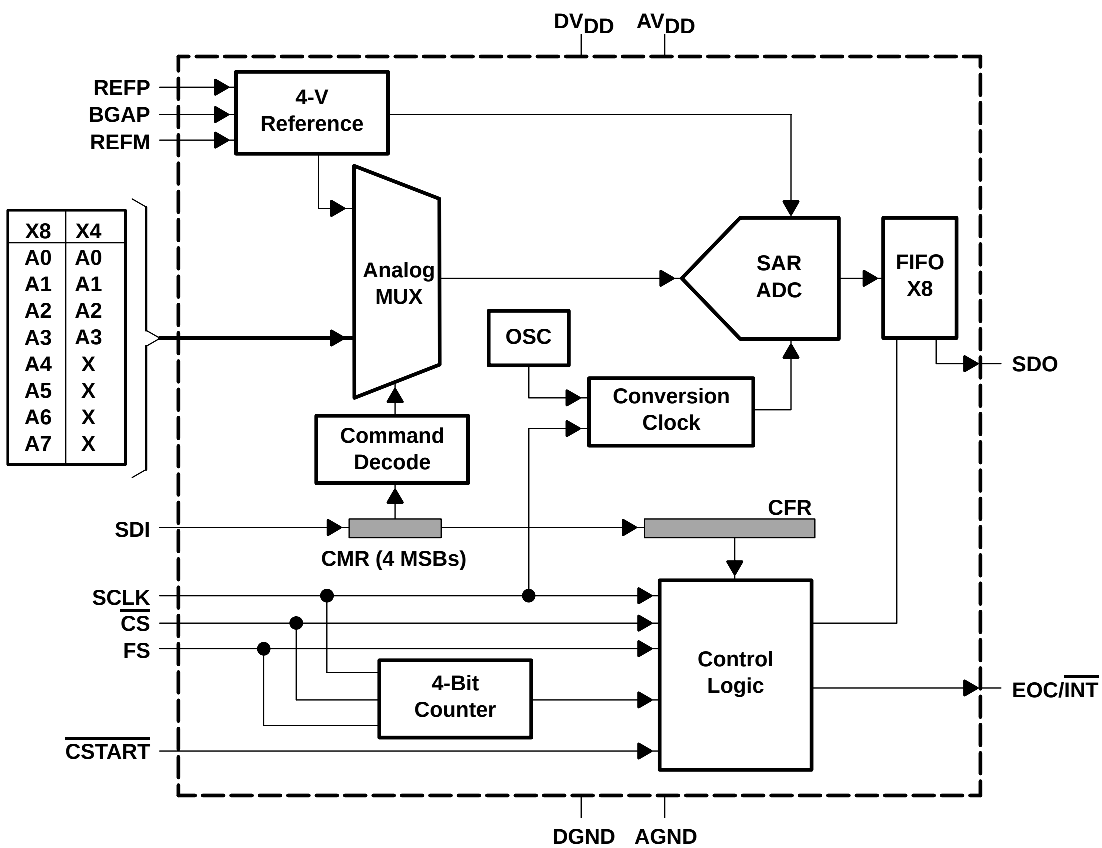
description (continued)

In addition to being a high-speed ADC with versatile control capability, these devices have an on-chip analog multiplexer (MUX) that can select any analog input or one of three self-test voltages. The sample-and-hold function is automatically started after the fourth SCLK (normal sampling) or can be controlled by $\overline{\text{CSTART}}$ to extend the sampling period (extended sampling). The normal sampling period can also be programmed as short sampling (12 SCLKs) or long sampling (44 SCLKs) to accommodate the faster SCLK operation popular among high-performance signal processors. The TLC3544 and TLC3548 are designed to operate with low power consumption. The power saving feature is further enhanced with software power-down/ autopower-down modes and programmable conversion speeds. The conversion clock (internal OSC) is built in. The converter can also use an external SCLK as the conversion clock for maximum flexibility. The TLC3544 and TLC3548 have a 4-V internal reference. The converters are specified with unipolar input range of 0-V to 5-V when a 5-V external reference is used.

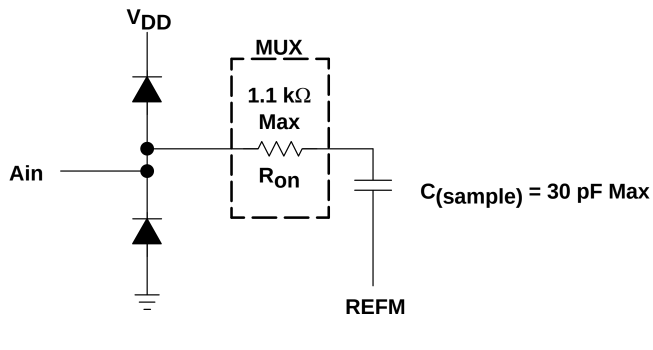
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	20-TSSOP (PW)	**20-SOIC (DW)**	**24-SOIC (DW)**	**24-TSSOP (PW)**
0°C to 70°C	TLC3544CPW	TLC3544CDW	TLC3548CDW	TLC3548CPW
–40°C to 85°C	TLC3544IPW	TLC3544IDW	TLC3548IDW	TLC3548IPW

functional block diagram

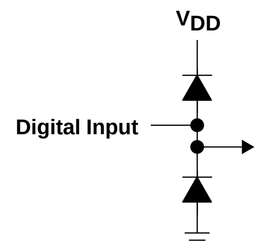


equivalent input circuit



Diode Turn on Voltage: 35 V

Equivalent Analog Input Circuit



Equivalent Digital Input Circuit

Terminal Functions

TERMINAL				I/O	DESCRIPTION
NAME		NO.			
		TLC3544	TLC3548		
A0 A1 A2 A3	A0 A1 A2 A3 A4 A5 A6 A7	9 10 11 12	9 10 11 12 13 14 15 16	I	Analog signal inputs. Analog input signals applied to these terminals are internally multiplexed. The driving source impedance should be less than or equal to 1 kΩ for normal sampling. For larger source impedance, use the external hardware conversion start signal $\overline{CSTART}$ (the low time of $\overline{CSTART}$ controls the sampling period) or reduce the frequency of SCLK to increase the sampling time.
AGND		14, 18	18, 22	I	Analog ground return for the internal circuitry. Unless otherwise noted, all analog voltage measurements are with respect to AGND.
AV_{DD}		13, 19	17, 23	I	Analog supply voltage
BGAP		17	21	I	Internal bandgap compensation pin. Install compensation capacitors between BGAP and AGND. 0.1 µF for external reference; 10 µF in parallel with 0.1 µF for internal reference.
$\overline{CS}$		8	8	I	Chip select. When $\overline{CS}$ is high, SDO is in high-impedance state, SDI is ignored, and SCLK is disabled to clock data but works as conversion clock source if programmed. The falling edge of $\overline{CS}$ input resets the internal 4-bit counter, enables SDI and SCLK, and removes SDO from high-impedance state. If FS is high at $\overline{CS}$ falling edge, $\overline{CS}$ falling edge initiates the operation cycle. $\overline{CS}$ works as slave select ($\overline{SS}$) to provide an SPI interface. If FS is low at $\overline{CS}$ falling edge, FS rising edge initiates the operation cycle. $\overline{CS}$ can be used as chip select to allow the host to access the individual converter.
$\overline{CSTART}$		20	24	I	External sampling trigger signal, which initiates the sampling from a selected analog input channel when the device works in extended sampling mode (asynchronous sampling). A high-to-low transition starts the sampling of the analog input signal. A low-to-high transition puts the S/H in hold mode and starts the conversion. The low time of the $\overline{CSTART}$ signal controls the sampling period. $\overline{CSTART}$ signal must be long enough for proper sampling. $\overline{CSTART}$ must stay high long enough after the low-to-high transition for the conversion to finish maturely. The activation of $\overline{CSTART}$ is independent of SCLK and the level of $\overline{CS}$ and FS. However, the first $\overline{CSTART}$ cannot be issued before the rising edge of the 11th SCLK. Tie this terminal to DV_{DD} if not used.
DGND		6	6	I	Digital ground return for the internal circuitry
DV_{DD}		7	7	I	Digital supply voltage

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO. TLC3544	NO. TLC3548		
EOC($\overline{INT}$)	4	4	O	End of conversion (EOC) or interrupt to host processor ($\overline{INT}$) EOC: used in conversion mode 00 only. EOC goes from high to low at the end of the sampling and remains low until the conversion is complete and data is ready. $\overline{INT}$: Interrupt to the host processor. The falling edge of $\overline{INT}$ indicates data is ready for output. $\overline{INT}$ is cleared by the following $\overline{CS}$↓, FS↑, or $\overline{CSTART}$↓.
FS	2	2	I	Frame sync input from DSP. The rising edge of FS indicates the start of a serial data frame being transferred (coming into or being sent out of the device). If FS is low at the falling edge of $\overline{CS}$, the rising edge of FS initiates the operation cycle, resets the internal 4-bit counter, and enables SDI, SDO, and SCLK. Tie this pin to DV_{DD} if FS is not used to initiate the operation cycle.
REFM	16	20	I	External low reference input. Connect REFM to AGND.
REFP	15	19	I	External positive reference input. When an external reference is used, the range of maximum input voltage is determined by the difference between the voltage applied to this terminal and to the REFM terminal. Always install decoupling capacitors (10 μF in parallel with 0.1 μF) between REFP and REFM.
SCLK	1	1	I	Serial clock input from the host processor to clock in the input from SDI and clock out the output via SDO. It can also be used as the conversion clock source when the external conversion clock is selected (see Table 2). When $\overline{CS}$ is low, SCLK is enabled. When $\overline{CS}$ is high, SCLK is disabled for the data transfer, but can still work as the conversion clock source.
SDI	3	3	I	Serial data input. The first 4 MSBs, ID[15:12], are decoded as one 4-bit command. All trailing bits, except for the CONFIGURE WRITE command, are filled with zeros. The CONFIGURE WRITE command requires additional 12-bit data. The MSB of input data, ID[15], is latched at the first falling edge of SCLK following FS falling edge, if FS starts the operation, or latched at the falling edge of first SCLK following $\overline{CS}$ falling edge when $\overline{CS}$ initiates the operation. The remaining input data (if any) is shifted in on the rising edge of SCLK and latched on the falling edge of SCLK. The input via SDI is ignored after the 4-bit counter counts to 16 (clock edges) or a low-to-high transition of $\overline{CS}$, whichever happens first. Refer to the timing specification for the timing requirements. Tie SDI to DV_{DD} if using hardware default mode (refer to device initialization).
SDO	5	5	O	The 3-state serial output for the A/D conversion result. All data bits are shifted out through SDO. SDO is in the high-impedance state when $\overline{CS}$ is high. SDO is released after a $\overline{CS}$ falling edge. The output format is MSB (OD[15]) first. When FS initiates the operation, the MSB of output via SDO, OD[15], is valid before the first falling edge of SCLK following the falling edge of FS. When $\overline{CS}$ initiates the operation, the MSB, OD[15], is valid before the first falling edge of SCLK following the $\overline{CS}$ falling edge. The remaining data bits are shifted out on the rising edge of SCLK and are valid before the falling edge of SCLK. Refer to the timing specification for the details. In a select/conversion operation, the first 14 bits are the results from the previous conversion (data). In READ FIFO operation, the data is from FIFO. In both cases, the last two bits are don’t care. In a WRITE operation, the output from SDO is ignored. SDO goes into high-impedance state at the sixteenth falling edge of SCLK after the operation cycle is initiated. SDO is in high-impedance state during conversions in modes 01, 10, and 11.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, GND to AV_{DD}, DV_{DD}	–0.3 V to 6.5 V
Analog input voltage range	–0.2 V to AV_{DD} +0.2 V
Analog input current	100 mA MAX
Reference input voltage	AV_{DD} + 0.3 V
Digital input voltage range	–0.3 V to DV_{DD} + 0.3 V
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating free-air industrial temperature range, T_A: I suffix	–40°C to 85°C
C suffix	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1.16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

general electrical characteristics over recommended operating free-air temperature range, single-ended input, normal long sampling, 200 KSPS, AV_{DD} = 5 V, external reference (V_{REFP} = 4 V, V_{REFM} = 0 V) or internal reference, SCLK frequency = 25 MHz, fixed channel at CONV mode 00, analog input signal source resistance = 25 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Digital Input							
V_{IH}	High-level control input voltage	DV_{DD} = 5 V		3.8			V
		DV_{DD} = 3 V		2.1			
V_{IL}	Low-level control input voltage	DV_{DD} = 5 V				0.8	V
		DV_{DD} = 3 V				0.6	
I_{IH}	High-level input current	$V_I = DV_{DD}$			0.005	2.5	µA
I_{IL}	Low-level input current	V_I = DGND		–2.5	0.005		µA
	Input capacitance				20	25	pF
Digital output							
V_{OH}	High-level digital output, V_{OH} at 30-pF load	I_O = –0.2 mA	DV_{DD} = 5 V	4.2			V
			DV_{DD} = 3 V	2.4			
V_{OL}	Low-level digital output, V_{OL} at 30-pF load	DV_{DD} = 5 V	I_O = 0.8 mA			0.4	V
			I_O = 50 µA			0.1	
		DV_{DD} = 3 V	I_O = 0.8 mA			0.4	
			I_O = 50 µA			0.1	
I_{OZ}	Off-state output current (high-impedance state)	$V_O = DV_{DD}$	$\overline{CS} = DV_{DD}$		0.02	1	µA
		V_O = DGND		–1	–0.02		
Power Supply							
AV_{DD}	Supply voltage			4.5	5	5.5	V
DV_{DD}				2.7	5	5.5	V
I_{CC}	Power supply current, AV_{DD} current-AI_{CC}	Conversion clock is internal OSC, EXT. reference, AV_{DD} = 5.5 V to 4.5 V, $\overline{CS}$ = DGND			2.8	3.6	mA
	Power supply current, DV_{DD} current-DI_{CC}				1.2	2	
$I_{CC(SW)}$	Software power-down power supply current	For all digital inputs DV_{DD} or DGND, $\overline{CS} = DV_{DD}$, AV_{DD} = 5.5 V	SCLK ON		175	240	µA
			SCLK OFF		20		
$I_{CC(Autodown)}$	Autopower-down power supply current	For all digital inputs DV_{DD} or DGND, AV_{DD} = 5.5 V, External reference	SCLK ON		175	230	µA
			SCLK OFF		20		
Operating temperature		C suffix		0		70	°C
		I suffix		–40		85	

† All typical values are at T_A = 25°C.

general electrical characteristics over recommended operating free-air temperature range, single-ended input, normal long sampling, 200 KSPS, AV_{DD} = 5 V, external reference (V_{REFP} = 4 V, V_{REFM} = 0 V) or internal reference, SCLK frequency = 25 MHz, fixed channel at CONV mode 00, analog input signal source resistance = 25 Ω (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Resolution			14			bits
Analog Input						
Voltage range			0		Reference	V
Leakage current				0.01	0.05	µA
Capacitance					30	pF
Reference						
	Internal reference voltage		3.85	4	4.07	V
	Internal reference temperature coefficient			100		ppm/°C
	Internal reference source current			1.8	2.5	mA
	Internal reference startup time			20		ms
V_{REFP}	External positive reference voltage		3		5	V
V_{REFM}	External negative reference voltage		0	AGND		V
	External reference input impedance	No conversion (AV_{DD} = 5 V, $\overline{CS}$ = DV_{DD}, SCLK = DGND)	100			MΩ
		Normal long sampling (AV_{DD} = 5 V, $\overline{CS}$ = DGND, SCLK = 25 MHz, External conversion clock)	8.3	12.5		kΩ
	External reference current	No conversion (V_{REFP} = AV_{DD} = 5 V, V_{REFM} = AGND, External reference, $\overline{CS}$ = DV_{DD})		1.5		µA
		Normal long sampling (AV_{DD} = 5 V, $\overline{CS}$ = DGND, SCLK = 25 MHz external conversion clock at V_{REF} = 5 V)		0.4	0.6	mA
Throughput Rate						
f	Internal oscillation frequency	DV_{DD} = 2.7 V to 5.5 V	6.5			MHz
$t_{(conv)}$	Conversion time	Internal OSC, 6.5 MHz minute			2.785	µs
		Conversion clock is external source, SCLK = 25 MHz (see Note 1)		2.895		µs
	Acquisition time	Normal short sampling		1.2		µs
	Throughput rate (see Note 2)	Normal long sampling, fixed channel in mode 00 or 01	200			KSPS
DC Accuracy—Normal Long Sampling						
E_L	Integral linearity error	See Note 3	–1	±0.5	1	LSB
E_D	Differential linearity error		–1	±0.5	1	LSB
E_O	Zero offset error	See Note 4	–3	±0.6	3	LSB
$E_{(g+)}$	Gain error	See Note 4	0	5	12	LSB

† All typical values are at T_A = 25°C.

NOTES: 1. Conversion time $t_{(conv)}$ = (18x4 / SCLK) + 15 ns.
2. This is for a fixed channel in conversion mode 00 or 01. When switching the channels, additional multiplexer setting time is required to overcome the memory effect of the charge redistribution DAC (refer to Figure 8).
3. Linear error is the maximum deviation from the best fit straight line through the A/D transfer characteristics.
4. Zero offset error is the difference between 00000000000000 and the converted output for zero input voltage; gain error is the difference between 11111111111111 and the converted output for full-scale input voltage. The full-scale input voltage is equal to the reference voltage being used.

general electrical characteristics over recommended operating free-air temperature range, single-ended input, normal long sampling, 200 KSPS, AV_{DD} = 5 V, external reference (V_{REFP} = 4 V, V_{REFM} = 0 V) or internal reference, SCLK frequency = 25 MHz, fixed channel at CONV mode 00, analog input signal source resistance = 25 Ω (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
DC Accuracy—Normal Short Sampling						
E_L	Integral linearity error	See Note 3		±0.8		LSB
E_D	Differential linearity error			±0.6		LSB
E_O	Zero offset error	See Note 4	–3	±0.6	3	LSB
$E_{(g+)}$	Gain error	See Note 4	0	5	12	LSB
AC Accuracy—Normal Long Sampling						
SINAD	Signal-to-noise ratio + distortion	f_i = 20 kHz	78.6	80.8		dB
		f_i = 100 kHz		77.6		
THD	Total harmonic distortion	f_i = 20 kHz		–95	–90	dB
		f_i = 100 kHz		–88		
SFDR	Spurious free dynamic range	f_i = 20 kHz	90	97		dB
		f_i = 100 kHz		89		
ENOB	Effective number of bits	f_i = 20 kHz	12.8	13.1		Bits
		f_i = 100 kHz		12.6		
SNR	Signal-to-noise ratio	f_i = 20 kHz	79	81		dB
		f_i = 100 kHz		78		
	Channel-to-channel isolation (see Notes 2 and 5)	Fixed channel in conversion mode 00, f_i = 35 kHz		100		dB
	Analog input bandwidth	Full power bandwidth, –1 dB		2		MHz
		Full power bandwidth, –3 dB		2.5		
AC Accuracy—Normal Short Sampling						
SINAD	Signal-to-noise ratio + distortion	f_i = 20 kHz		78.9		dB
		f_i = 100 kHz		77.6		
THD	Total harmonic distortion	f_i = 20 kHz		–95		dB
		f_i = 100 kHz		–88		
SNR	Signal-to-noise ratio	f_i = 20 kHz		79		dB
		f_i = 100 kHz		78		
ENOB	Effective number of bits	f_i = 20 kHz		12.8		Bits
		f_i = 100 kHz		12.6		
SFDR	Spurious free dynamic range	f_i = 20 kHz		97		dB
		f_i = 100 kHz		89		
	Channel-to-channel isolation (see Notes 2 and 5)	Fixed channel in conversion mode 00, f_i = 35 kHz		100		dB
	Analog input bandwidth	Full power bandwidth, –1 dB		2		MHz
		Full power bandwidth, –3 dB		2.5		

† All typical values are at T_A = 25°C.

NOTES:
2. This is for a fixed channel in conversion mode 00 or 01. When switching the channels, additional multiplexer setting time is required to overcome the memory effect of the charge redistribution DAC (refer to Figure 8).
3. Linear error is the maximum deviation from the best fit straight line through the A/D transfer characteristics.
4. Zero offset error is the difference between 00000000000000 and the converted output for zero input voltage; gain error is the difference between 11111111111111 and the converted output for full-scale input voltage. The full-scale input voltage is equal to the reference voltage being used.
5. It is measured by applying a full-scale of 35 kHz signal to other channels and determining how much the signal is attenuated in the channel of interest. The converter samples this examined channel continuously. The channel-to-channel isolation is degraded if the converter samples different channels alternately (refer to Figure 8).

timing requirements over recommended operating free-air temperature range, AV_{DD} = 5 V, DV_{DD} = 5 V, V_{REFP} = 5 V, V_{REFM} = 0 V, SCLK frequency = 25 MHz (unless otherwise noted)

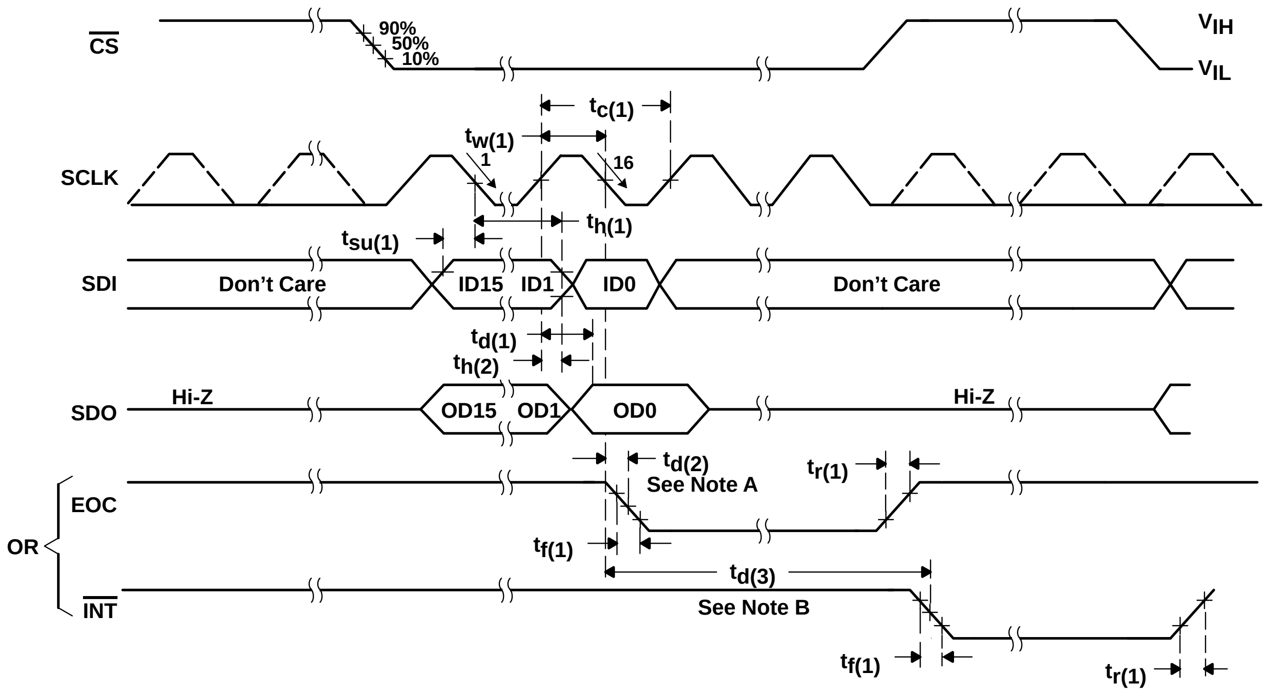
SCLK, SDI, SDO, EOC and $\overline{INT}$

PARAMETERS			MIN	TYP	MAX	UNIT
$t_{c(1)}$	Cycle time of SCLK at 25-pF load	DV_{DD} = 2.7 V	100			ns
		DV_{DD} = 5 V	40†			
$t_{w(1)}$	Pulse width, SCLK high time at 25-pF load		40%		60%	$t_{c(1)}$
$t_{r(1)}$	Rise time for $\overline{INT}$, EOC at 10-pF load	DV_{DD} = 5 V			6	ns
		DV_{DD} = 2.7 V			10	
$t_{f(1)}$	Fall time for $\overline{INT}$, EOC at 10-pF load	DV_{DD} = 5 V			6	ns
		DV_{DD} = 2.7 V			10	
$t_{su(1)}$	Setup time, new SDI valid (reaches 90% final level) before falling edge of SCLK, at 25-pF load		6		–	ns
$t_{h(1)}$	Hold time, old SDI hold (reaches 10% of old data level) after falling edge of SCLK, at 25-pF load		0		–	ns
$t_{d(1)}$	Delay time, new SDO valid (reaches 90% of final level) after SCLK rising edge, at 10-pF load	DV_{DD}= 5 V	0		10	ns
		DV_{DD} = 2.7 V	0		23‡	
$t_{h(2)}$	Hold time, old SDO hold (reaches 10% of old data level) after SCLK rising edge, at 10-pF load		0		–	ns
td(2)	Delay time, delay from sixteenth SCLK falling edge to EOC falling edge, normal sampling, at 10-pF load		0		6	ns
$t_{d(3)}$	Delay time, delay from the sixteenth falling edge of SCLK to $\overline{INT}$ falling edge, at 10-pF load [see the (‡) double dagger note and Note 6]		$t_{(conv)}$		$t_{(conv)}$ + 6	µs

† The minimum pulse width of SCLK high is 12.5 ns. The minimum pulse width of SCLK low is 12.5 ns.

‡ Specified by design

NOTE 6: For normal short sampling, $t_{d(3)}$ is the delay from 16th falling edge of SCLK to $\overline{INT}$ falling edge.
For normal long sampling, $t_{d(3)}$ is the delay from 48th falling edge of SCLK to the falling edge of $\overline{INT}$.
Conversion time, $t_{(conv)}$ is equal to $18 \times OSC + 15$ ns when using internal OSC as conversion clock, or $72 \times t_{c(1)} + 15$ ns when external SCLK is conversion clock source.



NOTES: A. For normal long sampling, $t_{d(2)}$ is the delay time of $\overline{EOC}$ low after the falling edge of 48th SCLK.

B. For normal long sampling, $t_{d(3)}$ is the delay time of $\overline{INT}$ low after the falling edge of 48th SCLK.

– – – – The dotted line means signal may or may not exist, depending on application. It must be ignored. Normal sampling mode, $\overline{CS}$ initiates the conversion, FS must be tied to high. When $\overline{CS}$ is high, SDO is in Hi-Z; all inputs (FS, SCLK, SDI) are inactive and are ignored.

Figure 1. Critical Timing for SCLK, SDI, SDO, EOC and $\overline{INT}$

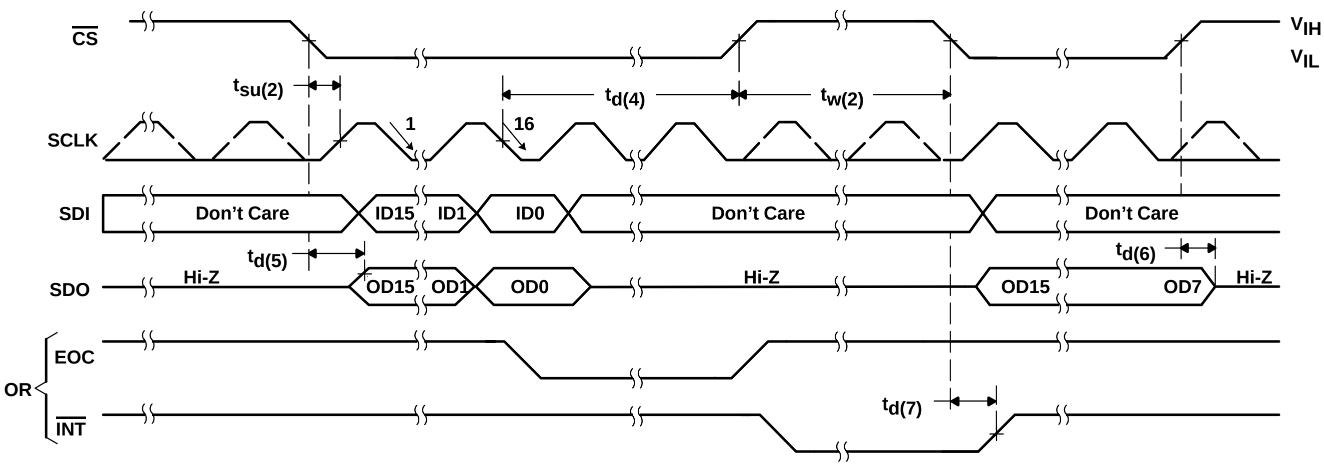
timing requirements over recommended operating free-air temperature range, AV_{DD} = 5 V, DV_{DD} = 5 V, V_{REFP} = 5 V, V_{REFM} = 0 V, SCLK frequency = 25 MHz (unless otherwise noted) (continued)

$\overline{CS}$ trigger

PARAMETERS			MIN	TYP	MAX	UNIT
$t_{su(2)}$	Setup time, $\overline{CS}$ falling edge before SCLK rising edge, at 25-pF load		12			ns
$t_{d(4)}$	Delay time, delay time from 16th SCLK falling edge to $\overline{CS}$ rising edge, at 25-pF load ‡		5			ns
$t_{w(2)}$	Pulse width, $\overline{CS}$ high time at 25-pF load		1			$t_{c(1)}$
$t_{d(5)}$	Delay time, delay from $\overline{CS}$ falling edge to MSB of SDO valid (reaches 90% final level), at 10-pF load	DV_{DD} = 5 V	0		12	ns
		DV_{DD} = 2.7 V	0		30†	
$t_{d(6)}$	Delay time, delay from $\overline{CS}$ rising edge to SDO 3-state, at 10-pF load		0		6	ns
$t_{d(7)}$	Delay time, delay from $\overline{CS}$ falling edge to $\overline{INT}$ rising edge, at 10-pF load	DV_{DD} = 5 V	0		6	ns
		DV_{DD} = 2.7 V	0		16†	

† Specified by design

‡ For normal short sampling, $t_d(4)$ is the delay time from 16th SCLK falling edge to $\overline{CS}$ rising edge.
For normal long sampling, $t_d(4)$ is the delay time from 48th SCLK falling edge to $\overline{CS}$ rising edge.



NOTE A: – – – – The dotted line means signal may or may not exist, depending on application. It must be ignored.
Normal sampling mode, $\overline{CS}$ initiates the conversion, FS must be tied to high. When $\overline{CS}$ is high, SDO is in Hi-Z, all inputs (FS, SCLK, SDI) are inactive and are ignored. Parts with date code earlier than 13XXXXX have these discrepancies:
(Date code is a 7 digit code next to the TI where the first digit indicates the year and the second digit is the month of production. 13, in this case, is 2001 and the month of March.)
FS is not ignored even if the device is in microcontroller mode ($\overline{CS}$ triggered).
FS must be tied to DV_{DD}.

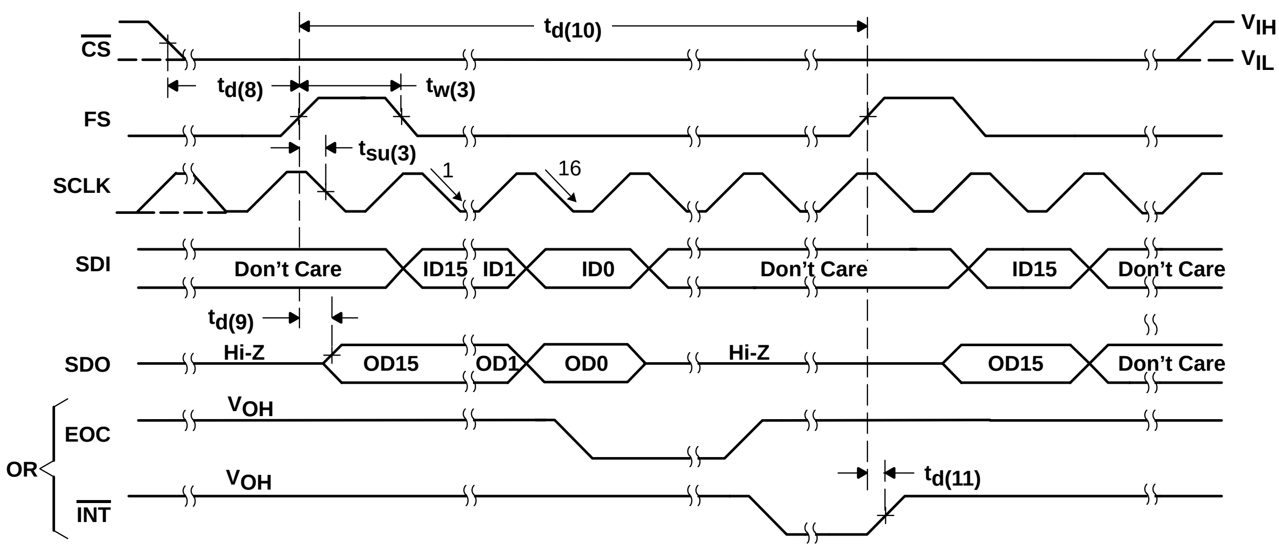
Figure 2. Critical Timing for $\overline{CS}$ Trigger

timing requirements over recommended operating free-air temperature range, AV_{DD} = 5 V, DV_{DD} = 5 V, V_{REFP} = 5 V, V_{REFM} = 0 V, SCLK frequency = 25 MHz (unless otherwise noted) (continued)

FS trigger

PARAMETERS			MIN	TYP	MAX	UNIT
$t_{d(8)}$	Delay time, delay from $\overline{CS}$ falling edge to FS rising edge, at 25-pF load		0.5			$t_{c(1)}$
$t_{su(3)}$	Setup time, FS rising edge before SCLK falling edge, at 25-pF load		$0.25 \times t_{c(1)}$		$0.5 \times t_{c(1)}+5$	ns
$t_{w(3)}$	Pulse width, FS high at 25-pF load		$0.75 \times t_{c(1)}$	$t_{c(1)}$	$1.25 \times t_{c(1)}$	ns
$t_{d(9)}$	Delay time, delay from FS rising edge to MSB of SDO valid (reaches 90% final level) at 10-pF load	DV_{DD} = 5 V			26†	ns
		DV_{DD} = 2.7 V			30†	
$t_{d(10)}$	Delay time, delay from FS rising edge to next FS rising edge at 25-pF load		Required sampling time + conversion time			µs
$t_{d(11)}$	Delay time, delay from FS rising edge to $\overline{INT}$ rising edge at 10-pF load	DV_{DD} = 5 V	0		6†	ns
		DV_{DD} = 2.7 V			16†	

† Specified by design



NOTE A: – – – – The dotted line means signal may or may not exist, depending on application. It must be ignored.
Normal sampling mode, FS initiates the conversion, $\overline{CS}$ can be tied to low. When $\overline{CS}$ is high, SDO is in Hi-Z, all inputs (FS, SCLK, SDI) are inactive and are ignored.
Parts with date code earlier than 13XXXXX have these discrepancies:
(Date code is a 7 digit code next to the TI where the first digit indicates the year and the second digit is the month of production. 13, in this case, is 2001 and the month of March.)
SDO MSB (OD[15]) comes out from the falling edge of $\overline{CS}$ instead of FS rising edge in DSP mode (FS triggered).

Figure 3. Critical Timing for FS Trigger

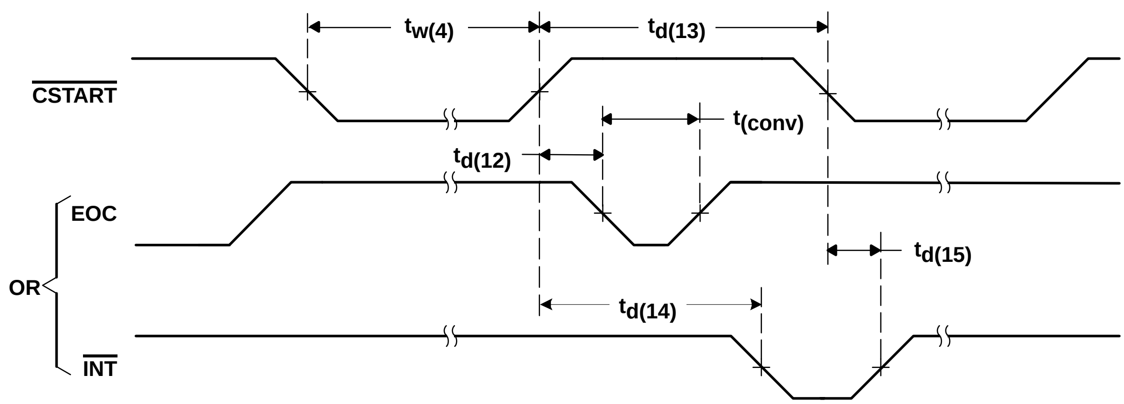
timing requirements over recommended operating free-air temperature range, AV_{DD} = 5 V, DV_{DD} = 5 V, V_{REFP} = 5 V, V_{REFM} = 0 V, SCLK frequency = 25 MHz (unless otherwise noted) (continued)

$\overline{\text{CSTART}}$ trigger

PARAMETERS		MIN	TYP	MAX	UNIT
$t_{d(12)}$	Delay time, delay from $\overline{\text{CSTART}}$ rising edge to EOC falling edge, at 10-pF load	0	15	21	ns
$t_{w(4)}$	Pulse width $\overline{\text{CSTART}}$ low time: $t_{W(L)}(\overline{\text{CSTART}})$, at 25-pF load	$t_{(sample – ref)}$+0.4	Note 7		µs
$t_{d(13)}$	Delay time, delay from $\overline{\text{CSTART}}$ rising edge to $\overline{\text{CSTART}}$ falling edge, at 25-pF load	$t_{(conv)}$ +15	Notes 7 and 8		ns
$t_{d(14)}$	Delay time, delay from $\overline{\text{CSTART}}$ rising edge to $\overline{\text{INT}}$ falling edge, at 10-pF load	$t_{(conv)}$ +15	Notes 7 and 8	$t_{(conv)}$+21	ns
$t_{d(15)}$	Delay time, delay from $\overline{\text{CSTART}}$ falling edge to $\overline{\text{INT}}$ rising edge, at 10-pF load	0		6	µs

NOTES: 7. The pulse width of $\overline{\text{CSTART}}$ must be not less than the required sampling time. The delay from $\overline{\text{CSTART}}$ rising edge to following $\overline{\text{CSTART}}$ falling edge must not be less than the required conversion time. The delay from $\overline{\text{CSTART}}$ rising edge to the $\overline{\text{INT}}$ falling edge is equal to the conversion time.

8. The maximum rate of SCLK is 25 MHz for normal long sampling and 10 MHz for normal short sampling.



Extended Sampling

Figure 4. Critical Timing for Extended Sampling ($\overline{\text{CSTART}}$ Trigger)

detailed description

converter

The converters are a successive-approximation ADC utilizing a charge redistribution DAC. Figure 5 shows a simplified block diagram of the ADC. The sampling capacitor acquires the signal on Ain during the sampling period. When the conversion process starts, the control logic directs the charge redistribution DAC to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator into a balanced condition. When balanced, the conversion is complete and the ADC output code is generated.

detailed description (continued)

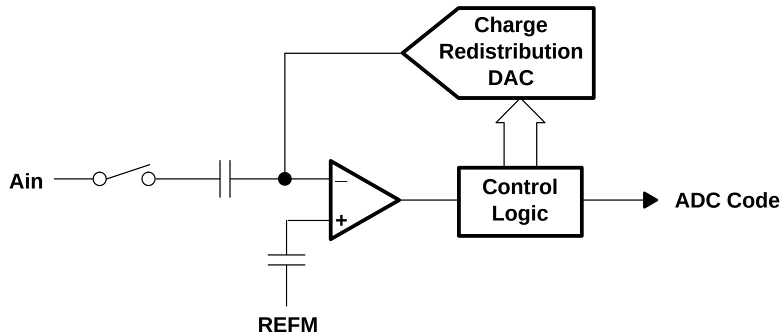


Figure 5. Simplified Block Diagram of the Successive-Approximation System

analog input range and internal test voltages

TLC3548 has eight analog inputs (TLC3544 has four) and three test voltages. The inputs are selected by the analog multiplexer according to the command entered (see Table 1). The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

The TLC3544 and TLC3548 are specified for a unipolar input range of 0-V to 4-V when the internal reference is selected, and 0-V to 5-V when an external 5-V reference is used.

analog input mode

Two input signal modes can be selected: single-ended input and pseudodifferential input.

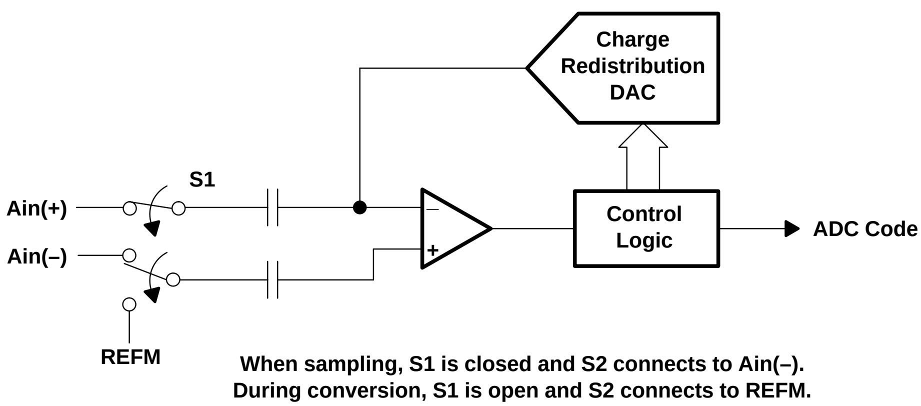
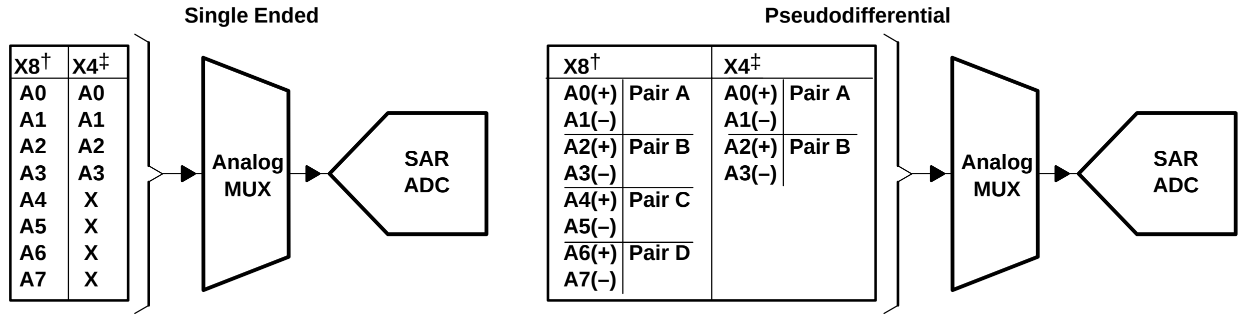


Figure 6. Simplified Pseudodifferential Input Circuit

Pseudodifferential input refers to the negative input, Ain(–); its voltage is limited in magnitude to ±0.2 V. The input frequency limit of Ain(–) is the same as the positive input Ain(+). This mode is normally used for ground noise rejection or dc bias offset.

When pseudodifferential mode is selected, only two analog input channel pairs are available for the TLC3544 and four channel pairs for the TLC3548, because half the inputs are used as the negative input (see Figure 7).

analog input mode (continued)



† TLC3548
‡ TLC3544

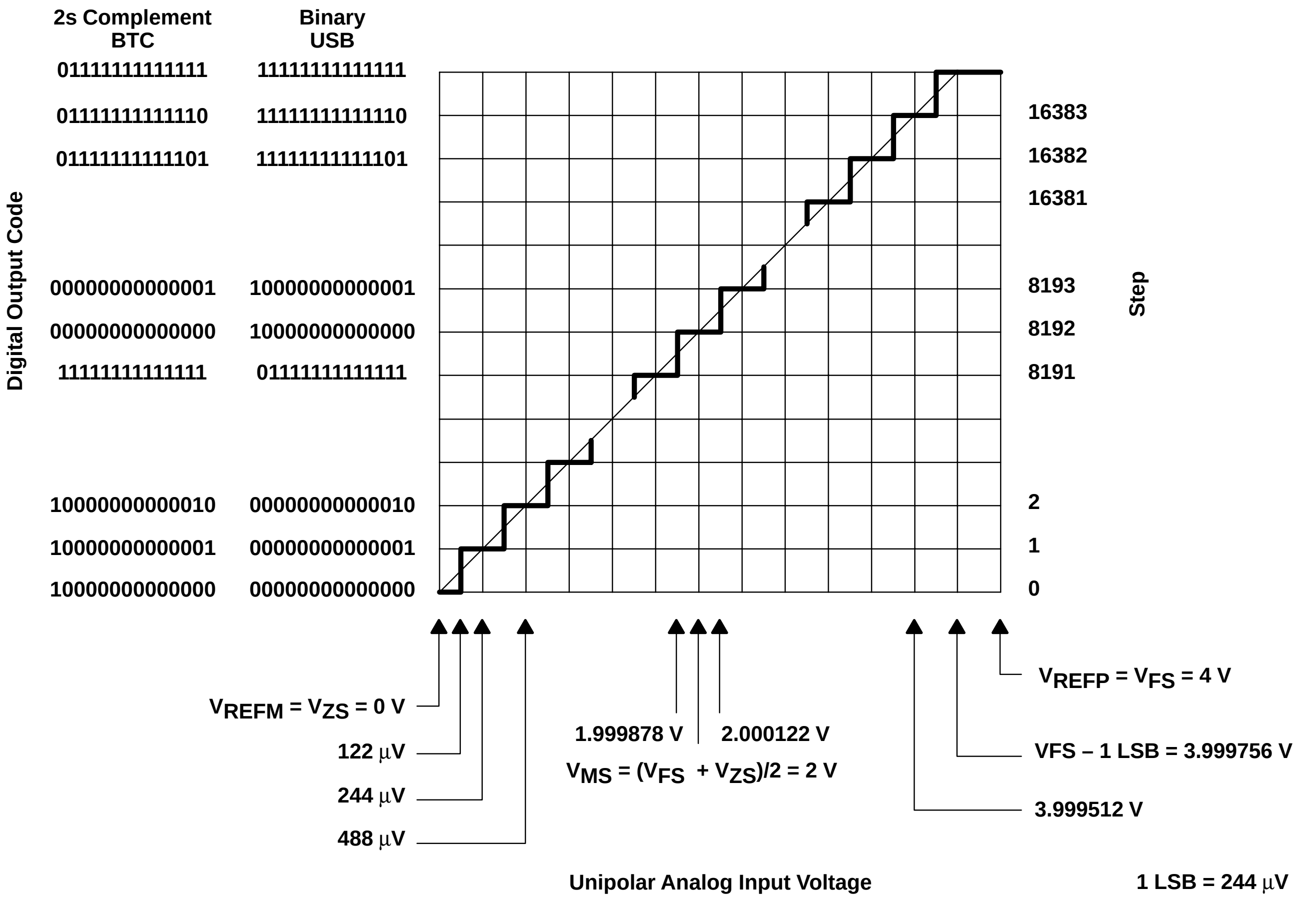
Figure 7. Pin Assignment of Single-Ended Input vs Pseudodifferential Input

reference voltage

There is a built-in 4-V reference. If the internal reference is used, REFP is internally set to 4-V and REFM is set to 0-V. The external reference can be applied to the reference-input pins (REFP and REFM) if programmed (see Table 2). The REFM pin should connect to analog ground. REFP can be 3-V to 5-V. Install decoupling capacitors (10 µF in parallel with 0.1 µF) between REFP and REFM. Install compensation capacitors (10 µF in parallel with 0.1 µF for internal reference, 0.1 µF only for external reference) between BGAP and AGND.

detailed description (continued)

ideal conversion characteristics



data format

INPUT DATA FORMAT (BINARY)		OUTPUT DATA FORMAT READ CONVERSION/FIFO	
MSB	**LSB**	**MSB**	**LSB**
ID[15:12]	ID[11:0]	OD[15:2]	OD[1:0]
Command	Configuration data field or filled with zeros	Conversion result	Don't Care

14-BIT
Unipolar Straight Binary Output: (USB) Zero-scale code = V_{ZS} = 0000h, V_{code} = V_{REFM} Mid-scale code = V_{MS} = 2000h, V_{code} = $V_{REFP}/2$ Full-scale code = V_{FS} = 3FFFh, V_{code} = V_{REFT} – 1 LSB **UnIpolar Input, Binary 2's Complement Output: (BTC)** Zero-scale code = V_{ZS} = 2000 h, V_{code} = V_{REFM} Mid-scale code = V_{MS} = 0000h, V_{code} = $(V_{REFP} – V_{REFM})/2$ Full-scale code = V_{FS} = 1FFFh, V_{code} = V_{REFP} – 1 LSB

detailed description (continued)

operation description

The converter samples the selected analog input signal, then converts the sample into digital output, according to the selected output format. The converter has four digital input pins (SDI, SCLK, $\overline{CS}$, and FS) and one digital output pin (SDO) to communicate with the host device. SDI is a serial data input pin, SDO is a serial data output pin, and SCLK is a serial clock from the host device. This clock is used to clock the serial data transfer. It can also be used as the conversion clock source (see Table 2). $\overline{CS}$ and FS are used to start the operation. The converter has a $\overline{CSTART}$ pin for an external hardware sampling and conversion trigger, and an $\overline{INT}$/EOC pin for interrupt purposes.

device initialization

After power on, the status of EOC/$\overline{INT}$ is initially high, and the input data register is set to all zeros. The device must be initialized before starting the conversion. The initialization procedure depends on the working mode. The first conversion result is ignored after power on.

Hardware Default Mode: Nonprogrammed Mode, Default. After power on, two consecutive active cycles initiated by $\overline{CS}$ or FS put the device into hardware default mode if SDI is tied to DV_{DD}. Each of these cycles must last 16 SCLKs at least. These cycles initialize the converter and load the CFR register with 800h (external reference, unipolar straight binary output code, normal long sampling, internal OSC, single-ended input, one-shot conversion mode, and EOC/$\overline{INT}$ pin as $\overline{INT}$). No additional software configuration is required.

Software Programmed Mode: Programmed. When the converter has to be configured, the host must write A000h into the converter first after power on, then perform the WRITE CFR operation to configure the device.

start of operation cycle

Each operation consists of several actions that the converter takes according to the command from the host. The operation cycle includes three periods: command period, sampling period, and conversion period. In the command period, the device decodes the command from the host. In the sampling period, the device samples the selected analog signal according to the command. In the conversion period, the sample of the analog signal is converted to digital format. The operation cycle starts from the command period, which is followed by one or several sampling and conversion periods (depending on the setting) and finishes at the end of the last conversion period.

The operation cycle is initiated by the falling edge of $\overline{CS}$ or the rising edge of FS.

$\overline{CS}$ Initiates The Operation: If FS is high at the falling edge of $\overline{CS}$, the falling edge of $\overline{CS}$ initiates the operation. When $\overline{CS}$ is high, SDO is in the high-impedance state, the signals on SDI, and SDO are ignored, and SCLK is disabled to clock the serial data. The falling edge of $\overline{CS}$ resets the internal 4-bit counter and enables SDO, SDI, and SCLK. The MSB of the input data via SDI, ID[15], is latched at the first falling edge of SCLK following the falling edge of $\overline{CS}$. The MSB of output data from SDO, OD[15], is valid before this SCLK falling edge. This mode works as an SPI interface when $\overline{CS}$ is used as the slave select ($\overline{SS}$). It also can be used as a normal DSP interface if $\overline{CS}$ connects to the frame sync output of the host DSP. *FS must be tied high in this mode*.

FS Initiates The Operation: If FS is low at the falling edge of $\overline{CS}$, the rising edge of FS initiates the operation, resets the internal 4-bit counter, and enables SDI, SDO, and SCLK. The ID[15] is latched at the first falling edge of SCLK following the falling edge of FS. OD[15] is valid before this falling edge of SCLK. This mode is used to interface the converter with a serial port of the host DSP. The FS of the device is connected to the frame sync of the host DSP. When several devices are connected to one DSP serial port, $\overline{CS}$ is used as chip select to allow the host DSP to access each device individually. If only one converter is used, $\overline{CS}$ can be tied low.

After the initiation, the remaining SDI data bits (if any) are shifted in and the remaining bits of SDO (if any) are shifted out at the rising edge of SCLK. The input data are latched at the falling edge of SCLK, and the output data are valid before this falling edge of SCLK. After the 4-bit counter reaches 16, the SDO goes to a high-impedance state. The output data from SDO is the previous conversion result in one shot conversion mode, or the contents in the top of the FIFO when the FIFO is used (refer to Figure 21).

detailed description (continued)

command period

After the rising edge of FS (FS triggers the operation) or the falling edge of $\overline{CS}$ ($\overline{CS}$ triggers the operation), SDI, SDO, and SCLK are enabled. The first four SCLK clocks form the command period. The four MSBs of input data, ID[15:12], are shifted in and decoded. These bits represent one of the 4-bit commands from the host, which defines the required operation (see Table 1, Command Set). The four MSBs of output, OD[15:12], are also shifted out via SDO during this period.

The commands are SELECT/CONVERSION, WRITE CFR, FIFO READ, SW POWER DOWN, and HARDWARE DEFAULT mode. The SELECT/CONVERSION command includes SELECT ANALOG INPUT and SELECT TEST commands. All cause a select/conversion operation. They select the analog signal being converted, and start the sampling/conversion process after the selection. WRITE CFR causes the configuration operation, which writes the device configuration information into the CFR register. FIFO READ reads the contents in the FIFO. SW POWER DOWN puts the device into software power-down mode to save power. Hardware default mode sets the device into the hardware default mode.

After the command period, the remaining 12 bits of SDI are written into the CFR register to configure the device if the command is *WRITE CFR*. Otherwise, these bits are ignored. The configuration is retained in the autopower-down and software power-down state. If SCLK stops (while $\overline{CS}$ remains low) after the first eight bits are entered, the next eight bits can be entered after SCLK resumes. The data on SDI are ignored after the 4-bit counter counts to 16 (falling edge of SCLK) or the low-to-high transition of $\overline{CS}$, whichever happens first.

The remaining 12 bits of output data are shifted out from SDO if the command is SELECT/CONVERSION or FIFO READ. Otherwise, the data on SDO are ignored. In any case, SDO goes into a high-impedance state after the 4-bit counter counts to 16 (falling edge of SCLK) or the low-to-high transition of $\overline{CS}$, whichever happens first.

Table 1. Command Set (CMR)

SDI Bit D[15:12]		TLC3548 COMMAND	TLC3544 COMMAND
BINARY	HEX		
0000b	0h	SELECT analog input channel 0	SELECT analog input channel 0
0001b	1h	SELECT analog input channel 1	SELECT analog input channel 1
0010b	2h	SELECT analog input channel 2	SELECT analog input channel 2
0011b	3h	SELECT analog input channel 3	SELECT analog input channel 3
0100b	4h	SELECT analog input channel 4	SELECT analog input channel 0
0101b	5h	SELECT analog input channel 5	SELECT analog input channel 1
0110b	6h	SELECT analog input channel 6	SELECT analog input channel 2
0111b	7h	SELECT analog input channel 7	SELECT analog input channel 3
1000b	8h	SW POWER DOWN	
1001b	9h	Reserved (test)	
1010b	Ah	WRITE CFR, the last 12 bits of SDI are written into CFR. This command resets FIFO.	
1011b	Bh	SELECT TEST, voltage = (REFP+REFM)/2 (see Notes 9 and 10)	
1100b	Ch	SELECT TEST, voltage = REFM (see Note 11)	
1101b	Dh	SELECT TEST, voltage = REFP (see Note 12)	
1110b	Eh	FIFO READ, FIFO contents is shown on SDO; OD[15:2] = result, OD[1:0] = xx	
1111b	Fh	Hardware default mode, CFR is loaded with 800h	

NOTES: 9. REFP is external reference if external reference is selected, or internal reference if internal reference is programmed.
10. The output code = mid-scale code + zero offset error + gain error.
11. The output code = zero scale code + zero offset error.
12. The output code = full-scale code + gain error.

detailed description (continued)

Table 2. Configuration Register (CFR) Bit Definition

<table>
<tr><th>SDI BIT</th><th>DEFINITION</th></tr>
<tr><td>D11</td><td>Reference select:
0: Internal (4 V) 1: External</td></tr>
<tr><td>D10</td><td>Conversion output code format select:
0: USB (unipolar straight binary) 1: Binary 2s complement</td></tr>
<tr><td>D9</td><td>Sample period select for normal sampling Don’t care in extended sampling.
0: Long sampling (4X) 44 SCLKs 1: Short sampling (1X) 12 SCLKs</td></tr>
<tr><td>D8</td><td>Conversion clock source select:
0: Conversion clock = Internal OSC 1: Conversion clock = SCLK/4</td></tr>
<tr><td>D7</td><td>Input mode select:
0: Single-ended 1: Pseudodifferential. Pin configuration shown below.
<table>
<tr><th colspan="3">Pin Configuration of TLC3548</th><th colspan="3">Pin Configuration of TLC3544</th></tr>
<tr><td>Pin No.</td><td>Single-ended</td><td>Pseudodifferential polarity</td><td>Pin No.</td><td>Single-ended</td><td>Pseudodifferential polarity</td></tr>
<tr><td>9
10</td><td>A0
A1</td><td>PLUS Pair A
MINUS</td><td>9
10</td><td>A0
A1</td><td>PLUS Pair A
MINUS</td></tr>
<tr><td>11
12</td><td>A2
A3</td><td>PLUS Pair B
MINUS</td><td>11
12</td><td>A2
A3</td><td>PLUS Pair B
MINUS</td></tr>
<tr><td>13
14</td><td>A4
A5</td><td>PLUS Pair C
MINUS</td><td colspan="3" rowspan="2"></td></tr>
<tr><td>15
16</td><td>A6
A7</td><td>PLUS Pair D
MINUS</td></tr>
</table></td></tr>
<tr><td>D[6:5]</td><td>Conversion mode select:
00: One shot mode
01: Repeat mode
10: Sweep mode
11: Repeat sweep mode</td></tr>
<tr><td>D[4:3]</td><td>Sweep auto sequence select (Note: These bits only take effect in conversion mode 10 and 11.)
<table>
<tr><th colspan="2">TLC3548</th><th colspan="2">TLC3544</th></tr>
<tr><td>Single ended(by ch)</td><td>Pseudodifferential (by pair)</td><td>Single ended (by ch)</td><td>Pseudodifferential (by pair)</td></tr>
<tr><td>00: 0–1–2–3–4–5–6–7
01: 0–2–4–6–0–2–4–6
10: 0–0–2–2–4–4–6–6
11: 0–2–0–2–0–2–0–2</td><td>00: N/A
01: A–B–C–D–A–B–C–D
10: A–A–B–B–C–C–D–D
11: A–B–A–B–A–B–A–B</td><td>00: 0–1–2–3–0–1–2–3
01: 0–2–0–2–0–2–0–2
10: 0–0–1–1–2–2–3–3
11: 0–0–0–0–2–2–2–2</td><td>00: N/A
01: A–B–A–B–A–B–A–B
10: N/A
11: A–A–A–A–B–B–B–B</td></tr>
</table></td></tr>
<tr><td>D2</td><td>EOC/$\overline{INT}$ pin function select:
0: Pin used as $\overline{INT}$ 1: Pin used as EOC (for mode 00 only)</td></tr>
<tr><td>D[1:0]</td><td>FIFO trigger level (sweep sequence length). Don’t care in one shot mode.
00: Full ($\overline{INT}$ generated after FIFO level 7 filled)
01: 3/4 ($\overline{INT}$ generated after FIFO level 5 filled)
10: 1/2 ($\overline{INT}$ generated after FIFO level 3 filled)
11: 1/4 ($\overline{INT}$ generated after FIFO level 1 filled)</td></tr>
</table>

sampling period

The sampling period follows the command period. The selected signal is sampled during this time. The device has three different sampling modes: normal short mode, normal long mode, and extended mode.

Normal Short Sampling Mode: Sampling time is controlled by SCLK. It takes 12 SCLK periods. At the end of sampling, the converter automatically starts the conversion period. After configuration, normal sampling, except FIFO READ and WRITE CFR commands, starts automatically after the fourth falling edge of SCLK that follows the falling edge of $\overline{CS}$ if $\overline{CS}$ triggers the operation, or follows the rising edge of FS if FS initiates the operation.

sampling period (continued)

Normal Long Sampling Mode: This mode is the same as normal short sampling, except that it lasts 44 SCLK periods.

Extended Sampling Mode: The external trigger signal, CSTART, triggers sampling and conversion. SCLK is not used for sampling. SCLK is also not needed for conversion if the internal conversion clock is selected. The falling edge of CSTART begins the sampling of the selected analog input. The sampling continues while CSTART is low. The rising edge of CSTART ends the sampling and starts the conversion (with about 15 ns internal delay). The occurrence of CSTART is independent of the SCLK clock, CS, and FS. However, the first CSTART cannot occur before the rising edge of the 11th SCLK. In other words, the falling edge of the first CSTART can happen at or after the rising edge of the 11th SCLK, but not before. The device enters the extended sampling mode at the falling edge of CSTART and exits this mode once CSTART goes to high followed by two consecutive falling edges of CS or two consecutive rising edges of FS (such as one read data operation followed by a write CFR). The first CS or FS does not cause conversion. Extended mode is used when a fast SCLK is not suitable for sampling, or when an extended sampling period is needed to accommodate different input signal source impedance.

conversion period

The conversion period is the third portion of the operation cycle. It begins after the falling edge of the 16th SCLK for normal short sampling mode, or after the falling edge of the 48th SCLK for normal long sampling, or on the rising edge of CSTART (with 15 ns internal delay) for extended sampling mode.

The conversion takes 18 conversion clocks plus 15 ns. The conversion clock source can be an internal oscillator, OSC, or an external clock, SCLK. The conversion clock is equal to the internal OSC if the internal clock is used, or equal to SCLK/4 when the external clock is programmed. To avoid premature termination of the conversion, enough time for the conversion must be allowed between consecutive triggers. EOC goes low at the beginning of the conversion period and goes high at the end of the conversion period. INT goes low at the end of this period.

conversion mode

Four different conversion modes (mode 00, 01, 10, 11) are available. The operation of each mode is slightly different, depending on how the converter samples and what host interface is used. Do not mix different types of triggers throughout the repeat or sweep operations.

One Shot Mode (Mode 00): Each operation cycle performs one sampling and one conversion for the selected channel. The FIFO is not used. When EOC is selected, it is generated while the conversion period is in progress. Otherwise, INT is generated after the conversion is done. The result is output through the SDO pin during the next select/conversion operation.

Repeat Mode (Mode 01): Each operation cycle performs multiple samplings and conversions for a fixed channel selected according to the 4-bit command. The results are stored in the FIFO. The number of samples to be taken is equal to the FIFO threshold programmed via D[1:0] in the CFR register. Once the threshold is reached, INT is generated, and the operation ends. If the FIFO is not read after the conversions, the data are replaced in the next operation. The operation of this mode starts with the WRITE CFR command to set conversion mode 01, then the SELECT/CONVERSION command, followed by a number of samplings and conversions of the fixed channel (triggered by CS, FS, or CSTART) until the FIFO threshold is hit. If CS or FS triggers the sampling, the data on SDI must be any one of the SELECT CHANNEL commands. This data is a dummy code for setting the converter in the conversion state. It does not change the existing channel selection set at the start of the operation until the FIFO is full. After the operation finishes, the host can read the FIFO, then reselect the channel and start the next REPEAT operation again; or immediately reselect the channel and start the next REPEAT operation (by issuing CS, FS, or CSTAR), or reconfigure the converter and then start a new operation according to the new setting. If CSTART triggers the sampling, the host can also immediately start the next REPEAT (on the current channel) after the FIFO is full. Besides, if FS initiates the operation and CSTART triggers the sampling and conversions, CS must not toggle during the conversion. This mode allows the host to set up the converter, continue monitoring a fixed input, and to get a set of samples as needed.

conversion mode (continued)

Sweep Mode (Mode 10): During each operation, all of the channels listed in the sweep sequence (D[4:3] of the CFR register) are sampled and converted at one time according to the programmed sequence. The results are stored in the FIFO. When the FIFO threshold is reached, an interrupt ($\overline{\text{INT}}$) is generated, and the operation ends. If the FIFO threshold is reached before all of the listed channels are visited, the remaining channels are ignored. This allows the host to change the sweep sequence length. The mode 10 operation starts with the WRITE CFR command to set the sweep sequence. The following triggers ($\overline{\text{CS}}$, FS, or $\overline{\text{CSTART}}$, depending on the interface) start the samplings and conversions of the listed channels in sequence until the FIFO threshold is hit. If $\overline{\text{CS}}$ or FS starts the sampling, the SDI data must be any one of the SELECT commands to set the converter in the conversion state. However, this command is a dummy code. It does not change the existing conversion sequence. After the FIFO is full, the converter waits for the FIFO READ. It does nothing before the FIFO READ or the WRITE CFR command is issued. The host must read the FIFO completely or write the CFR. If $\overline{\text{CSTART}}$ triggers the samplings, the host must issue an extra SELECT/CONVERSION command (select any channel) via $\overline{\text{CS}}$ or FS after the FIFO READ or WRITE CFR. This extra period is named the arm period and is used to set the converter into the conversion state, but does not affect the existing conversion sequence. Besides, if FS initiates the operation and $\overline{\text{CSTART}}$ triggers the sampling and conversions, $\overline{\text{CS}}$ must not toggle during the conversion.

Repeat Sweep Mode (Mode 11): This mode works in the same way as mode 10, except that it is not necessary to read the FIFO before the next operation after the FIFO threshold is hit. The next SWEEP can repeat immediately, but the contents in the FIFO are replaced by the new results. The host can read the FIFO completely, then issue the next SWEEP or repeat the SWEEP immediately (with the existing sweep sequence) by issuing sampling/conversion triggers ($\overline{\text{CS}}$, FS or $\overline{\text{CSTART}}$) or change the device setting with the WRITE CFR.

The memory effect of charge redistribution DAC exists when the mux switches from one channel to another. This degrades the channel-to-channel isolation if the channel changes after each conversion. For example, in mode 10 and 11, the isolation is about 70 dB for the sweep sequence 0-1-2-3-4 (refer to Figure 8). The memory effect can be reduced by increasing the sampling time or using the sweep sequence 0-0-2-2-4-4-6-6 and ignoring the first sample of each channel. Figure 8 shows the typical isolation vs throughput rate when applying a sine signal (35 kHz, 3.5 V_{p-p}) on CH0 and dc on CH1 converting both channels alternately and measuring the attenuation of the sine wave in CH1.

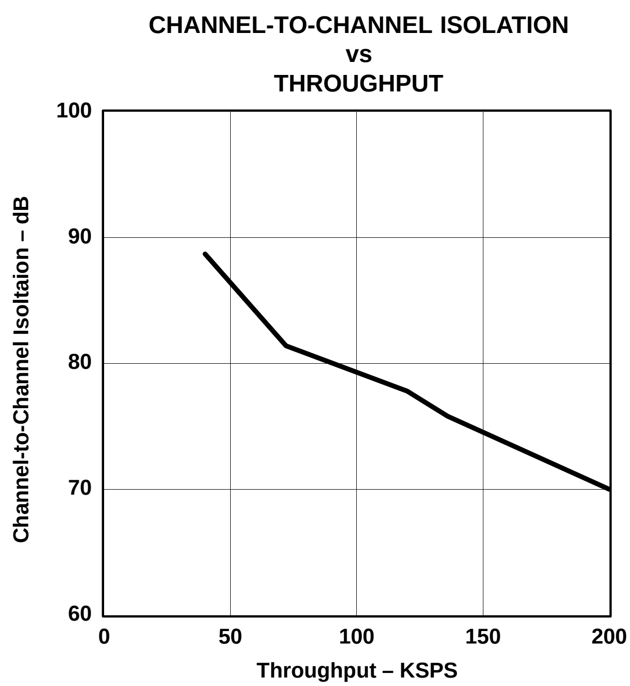
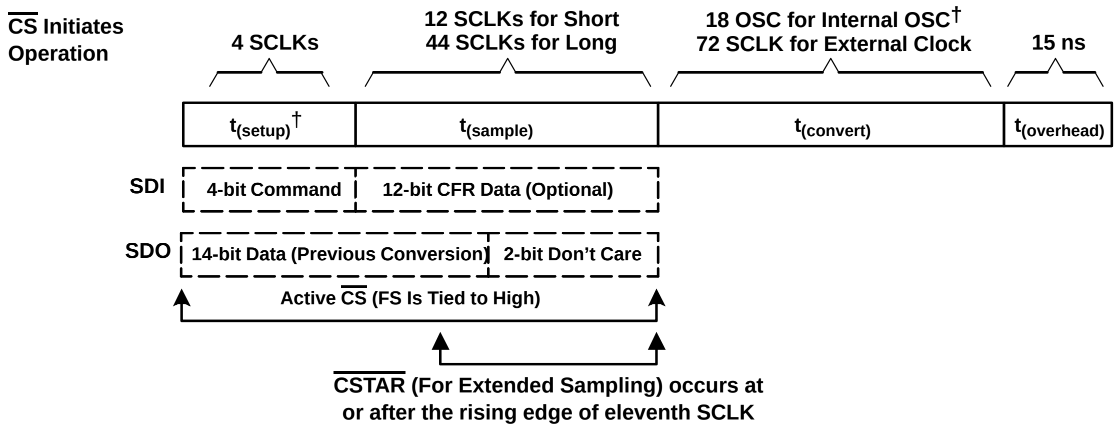
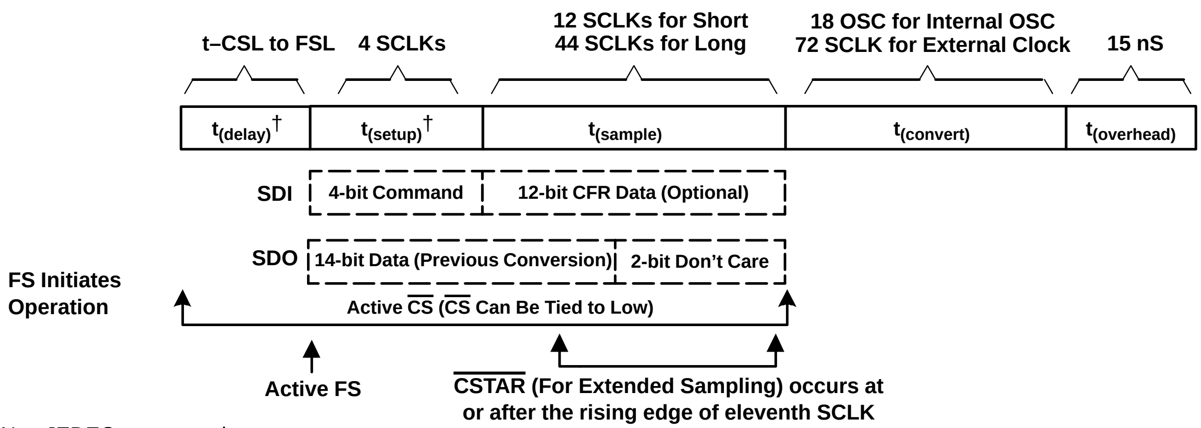


Figure 8

operation cycle timing





† Non JEDEC terms used.

After the operation is finished, the host has several choices. Table 3 summarizes operation options.

operation cycle timing (continued)

Table 3. Operation Options

MODE	CONVERSION IS INITIATED BY		
	$\overline{\text{CS}}$	FS	$\overline{\text{CSTART}}$
00	1. Issue new Select/Read operation to read data and start new conversion. 2. Reconfigure the device.	1. Issue new Select/Read operation to read data and start new conversion. 2. Reconfigure the device.	1. Issue new $\overline{\text{CSTART}}$ to start next conversion; old data lost. 2. Issue new Select/Read operation to read data—Issue new $\overline{\text{CSTART}}$ to start new conversion. 3. Reconfigure the device.
01	1. Read FIFO—Select Channel—Start new conversion. Channel must be selected after FIFO READ. 2. Select Channel—Start new conversion (old data lost) 3. Configure device again.	1. Read FIFO—Select Channel—Start new conversion. Channel must be selected after FIFO READ. 2. Select Channel—Start new conversion (old data lost) 3. Configure device again.	1. Read FIFO—Select channel—Start new conversion. Channel must be selected after FIFO READ. 2. Start new conversion (old data lost) with existing setting. 3. Configure device again.
10	1. Read FIFO—Start new conversion with existing setting. 2. Configure device—New conversion (old data lost)	1. Read FIFO—Start new conversion with existing setting. 2. Configure device—New conversion (old data lost)	1. Read FIFO—Arm Period—Start new conversion with existing setting 2. Configure device—Arm Period—New conversion (old data lost)
11	1. Read FIFO—Start new conversion with existing setting. 2. Start new conversion with the existing setting. 3. Configure device—Start new conversion with new setting.	1. Read FIFO—Start new conversion with existing setting 2. Start new conversion with the existing setting. 3. Configure Device—Start new conversion with new setting.	1. Read FIFO—Arm Period—Start new Conversion with existing setting 2. Start new conversion with existing setting. (old data lost) 3. Configure device—Arm Period—New conversion with new setting.

operation timing diagrams

The FIFO read and write CFR are nonconversion operations. The conversion operation performs one of four types of conversion: mode 00, 01, 10, and 11

Write Cycle (WRITE CFR Command): Write cycle does not generate EOC or $\overline{\text{INT}}$, nor does it carry out any conversion.

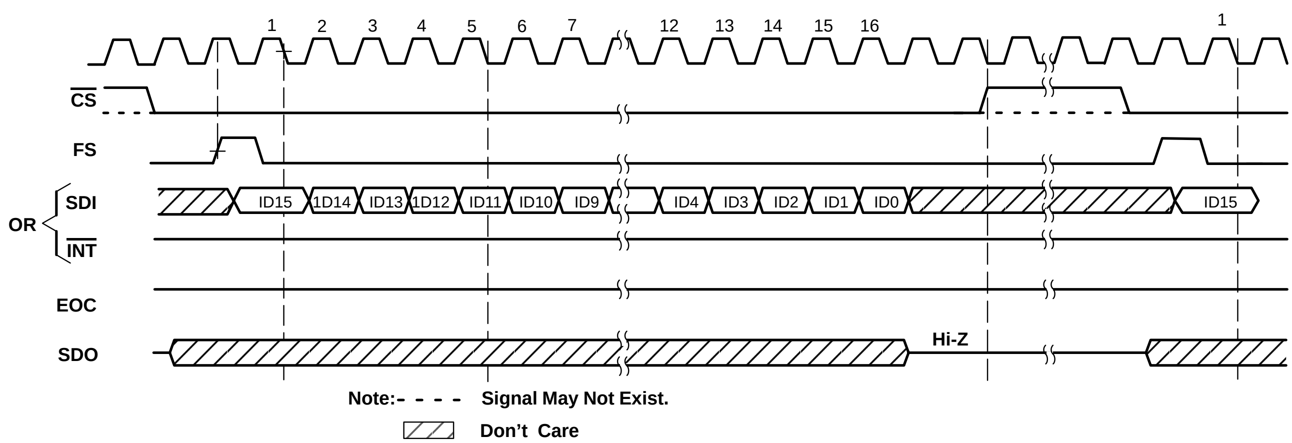


Figure 9. Write Cycle, FS Initiates Operation

operation timing diagrams (continued)

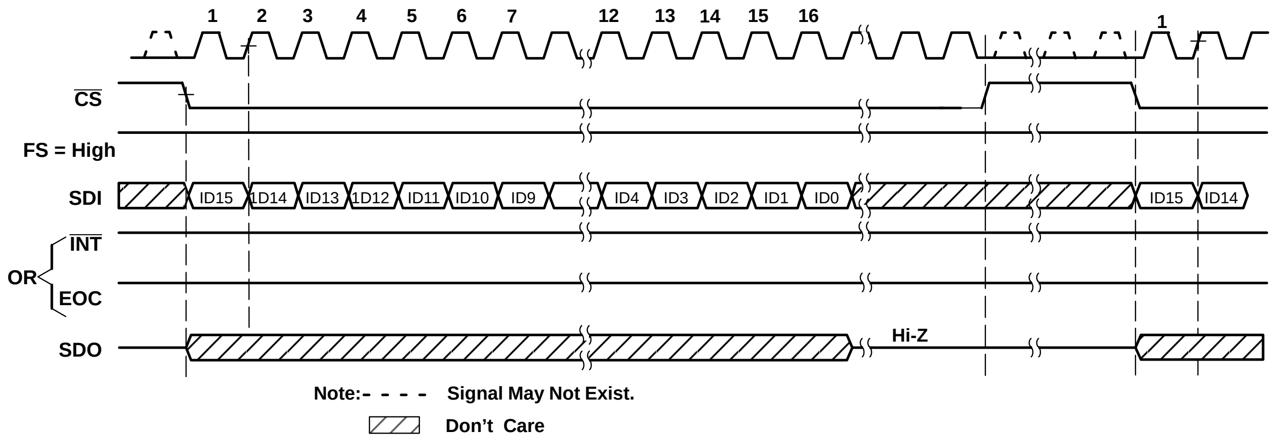


Figure 10. Write Cycle, $\overline{CS}$ Initiates Operation, FS = 1

FIFO Read Operation: When the FIFO is used, the first command after $\overline{INT}$ is generated is assumed to be the FIFO read. The first FIFO content is sent out immediately before the command is decoded. If this command is not a FIFO read, the output is terminated. Using more layers of the FIFO reduces the time taken to read multiple conversion results, because the read cycle does not generate an EOC or $\overline{INT}$, nor does it make a data conversion. Once the FIFO is read, the entire contents in the FIFO must be read out. Otherwise, the remaining data is lost.

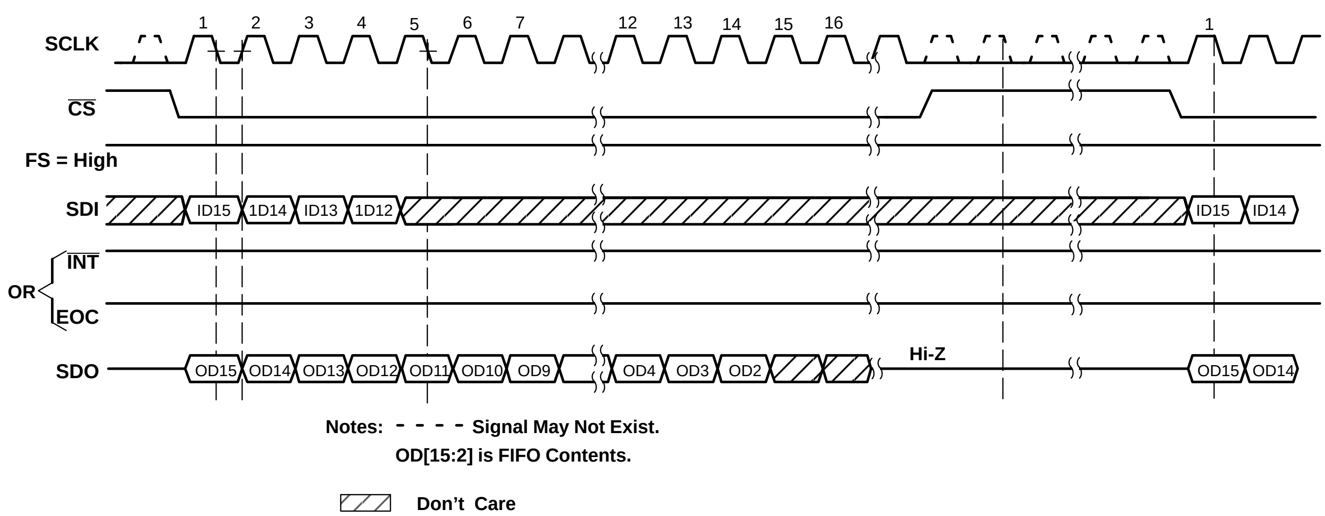


Figure 11. FIFO Read Cycle, $\overline{CS}$ Initiates Operation, FS = 1

conversion operation

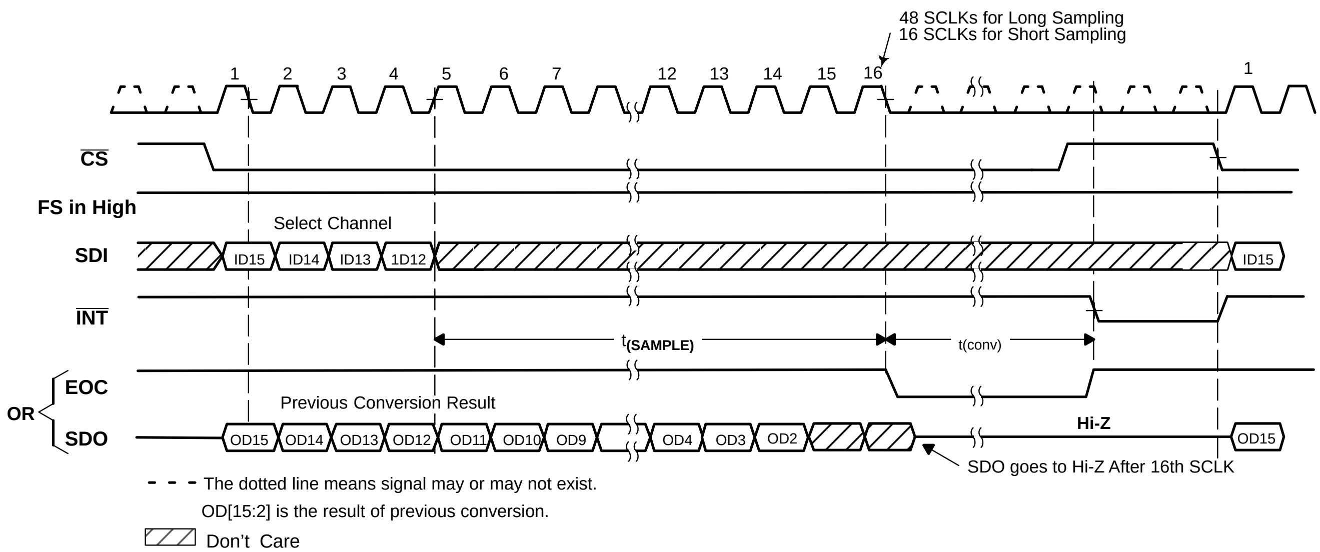


Figure 12. Mode 00, $\overline{CS}$ Initiates Operation

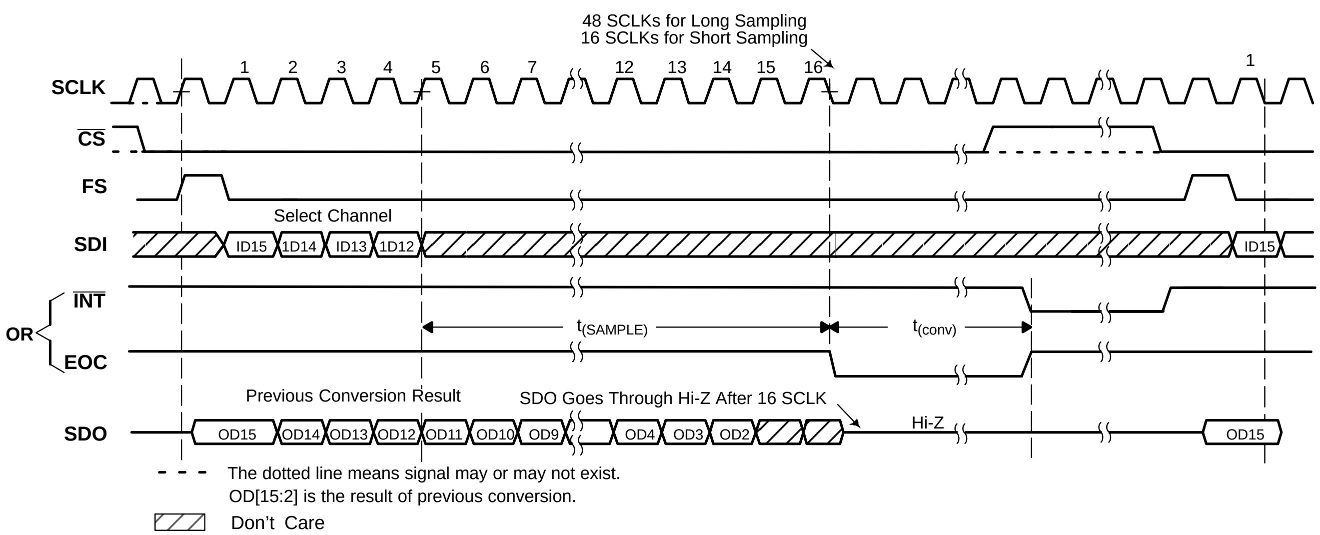


Figure 13. Mode 00, FS Initiates Operation

conversion operation (continued)

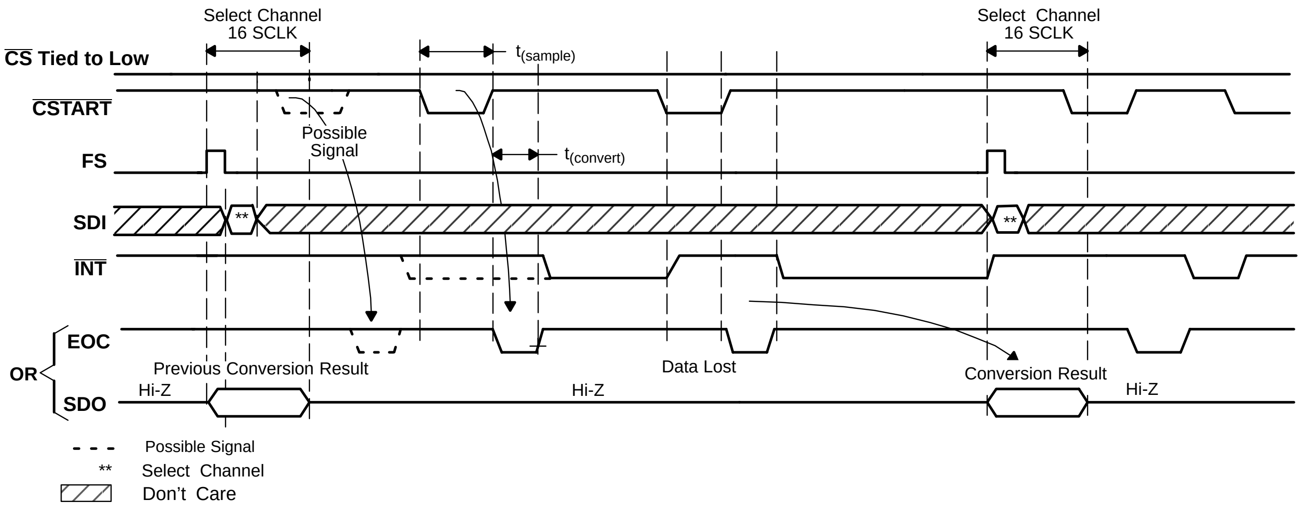


Figure 14. Mode 00, $\overline{\text{CSTART}}$ Triggers Sampling/Conversion, FS Initiates Select

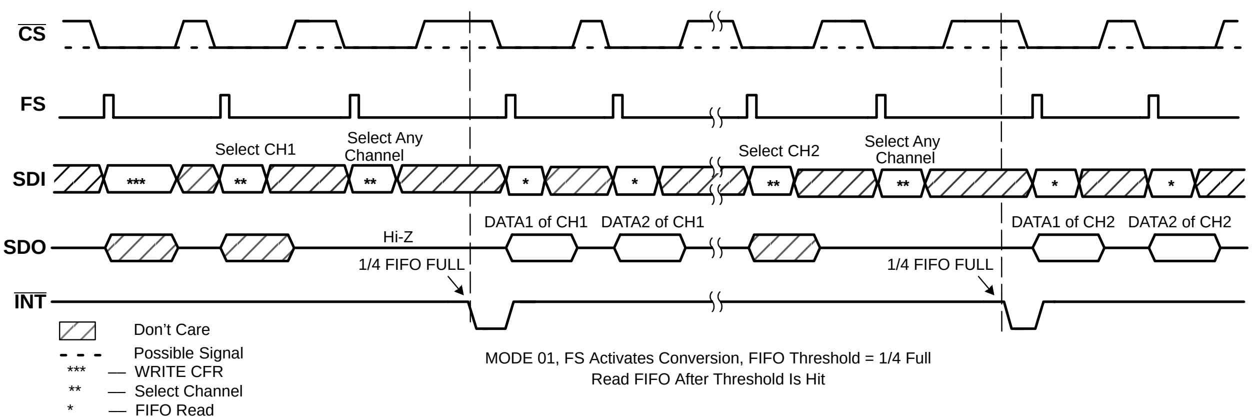


Figure 15. Mode 01, FS Initiates Operations

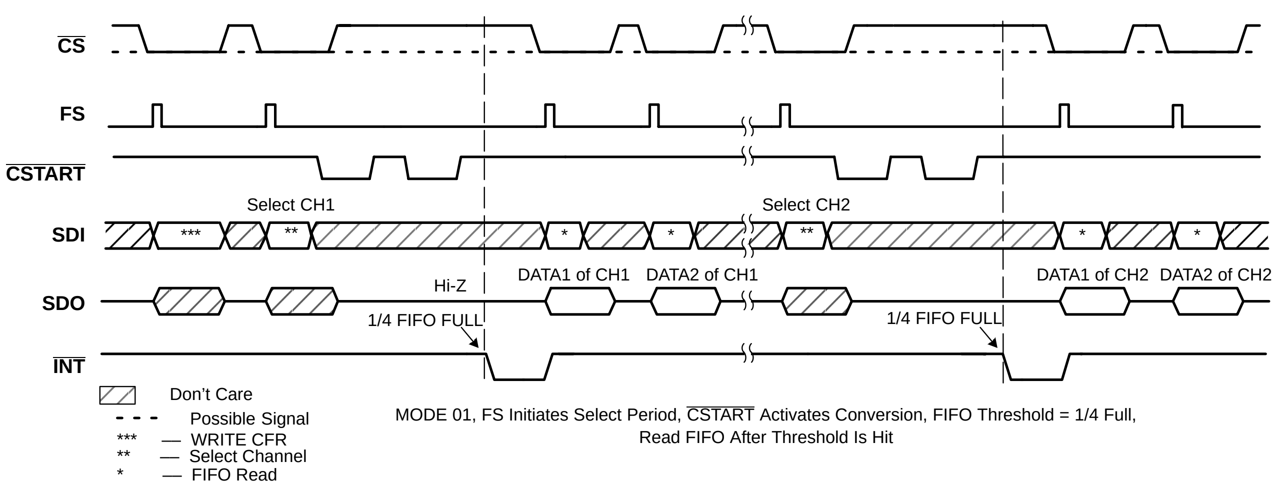


Figure 16. Mode 01, $\overline{\text{CSTART}}$ Triggers Samplings/Conversions

conversion operation (continued)

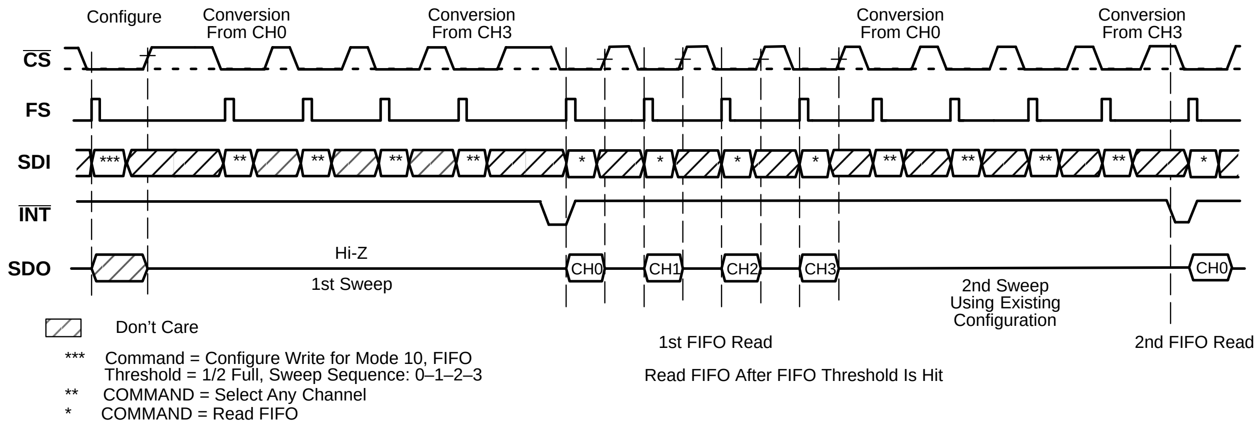


Figure 17. Mode 10, FS Initiates Operations

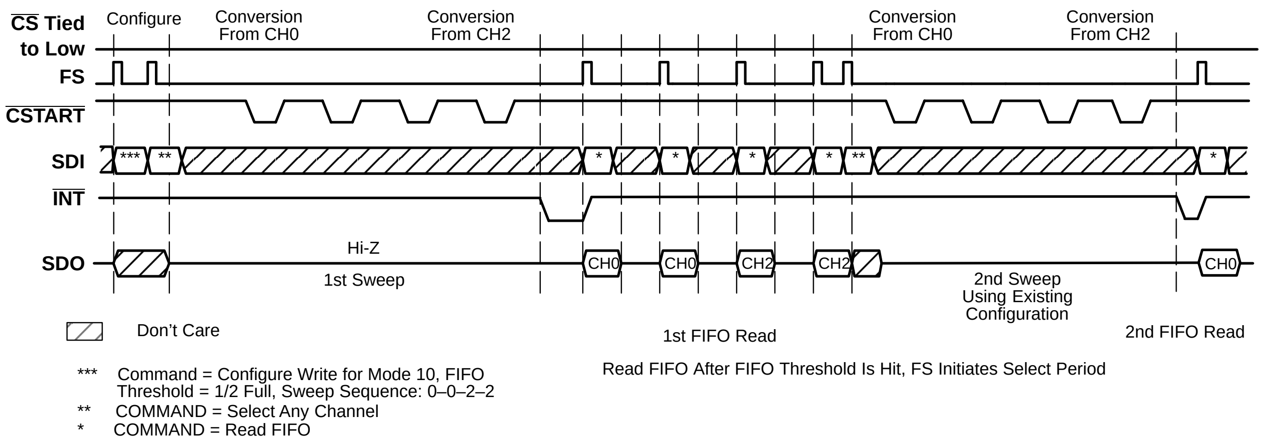


Figure 18. Mode 10, $\overline{\text{CSTART}}$ Initiates Operations

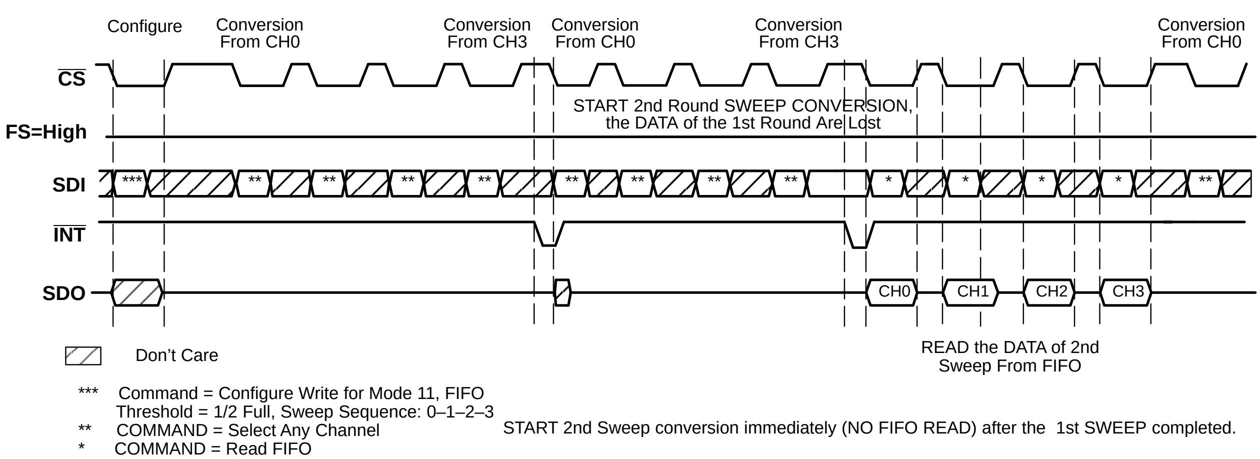


Figure 19. Mode 11, $\overline{\text{CS}}$ Initiates Operations

conversion operation (continued)

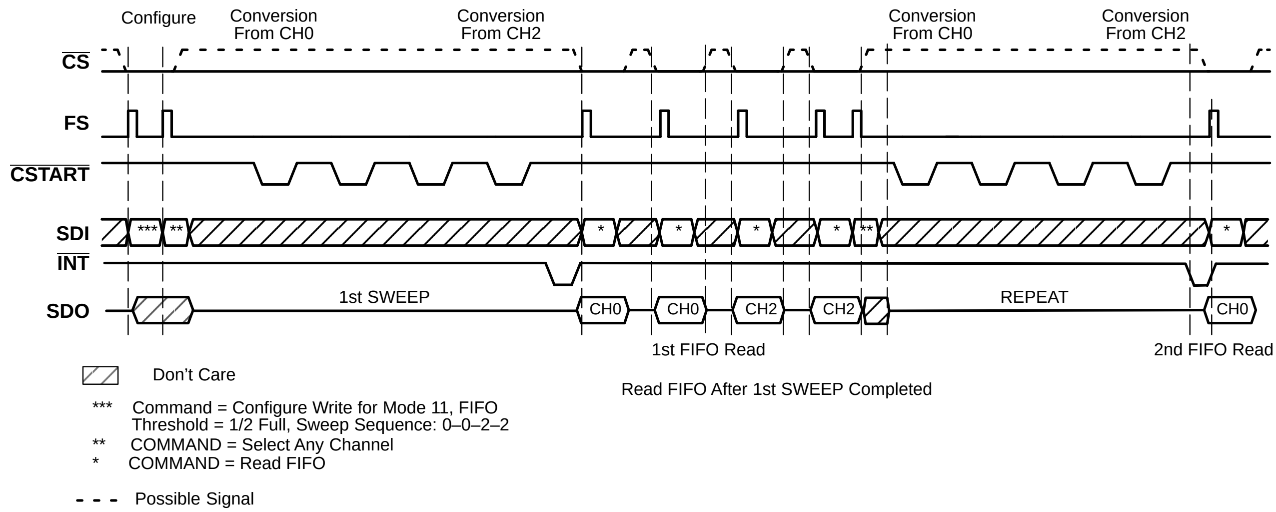


Figure 20. Mode 11, $\overline{\text{CSTART}}$ Triggers Samplings/Conversions

conversion clock and conversion speed

The conversion clock source can be the internal OSC, or the external clock SCLK. When the external clock is used, the conversion clock is equal to SCLK/4. It takes 18 conversion clocks plus 15 ns to finish the conversion. If the external clock is selected, the conversion time (not including sampling time) is $18X(4/f_{SCLK})$+15 ns. Table 4 shows the maximum conversion rate (including sampling time) when the analog input source resistor is 1 kΩ.

Table 4. Maximum Conversion Rate

DEVICE	SAMPLING MODE	CONVERSION CLK	MAX SCLK (MHz)	CONVERSION TIME (us)	RATE (KSPS)
TLC3544/48 (Rs = 1000)	Short (16 SCLK)	External SCLK/4	10	8.815	113.4
	Long (48 SCLK)	External SCLK/4	25	4.815	207.7
	Short (16 SCLK)	Internal 6.5 MHz	10	4.385	228
	Long (48 SCLK)	Internal 6.5 MHz	25	4.705	212.5

FIFO operation

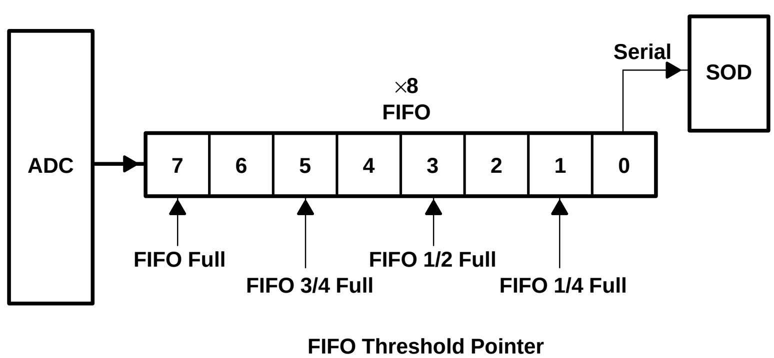


Figure 21. FIFO Structure

FIFO operation (continued)

The device has an 8-level FIFO that can be programmed for different thresholds. An interrupt is sent to the host after the preprogrammed threshold is reached. The FIFO is used to store conversion results in mode 01, 10, and 11, from either a fixed channel or a series of channels according to a preprogrammed sweep sequence. For example, an application may require eight measurements from channel 3. In this case, if the threshold is set to full, the FIFO is filled with 8 data conversions sequentially taken from channel 3. Another application may require data from channel 0, 2, 4, and 6 in that order. The threshold is set to 1/2 full and sweep sequence is selected as 0–2–4–6–0–2–4–6. An interrupt is sent to the host as soon as all four data conversions are in the FIFO. The FIFO is reset after a power on and a WRITE CFR operation. The contents of the FIFO are retained during autopower down and software power down.

Powerdown: The device has two power-down modes.

AutoPower-Down Mode: The device enters the autopower-down state at the end of a conversion.

In autopower-down, the power consumption reduces to about 1.8 mA when an internal reference is selected. The built-in reference is still on to allow the device to resume quickly. The resumption is fast enough for use between cycles. An active $\overline{CS}$, FS, or $\overline{CSTART}$ resumes the device from power-down state. The power current is 20 µA when an external reference is programmed and SCLK stops.

Software Power-Down Mode: Writing 8000h to the device puts the device into the software power-down state, and the entire chip (including the built-in reference) is powered down. The power current is reduced to about 20 µA if SCLK stops. Deselect $\overline{CS}$ to save power once the device is in the software power-down mode. An active $\overline{CS}$, FS, or $\overline{CSTART}$ restores the device. There is no time delay when an external reference is selected. However, if an internal reference is used, it takes about 20 ms to warm up.

The configuration register is not affected by any of the power-down modes but the sweep operation sequence must be started over again. All FIFO contents are retained in both power-down modes.

TYPICAL CHARACTERISTICS

**INTEGRAL NONLINEARITY
vs
DIGITAL OUTPUT CODE**

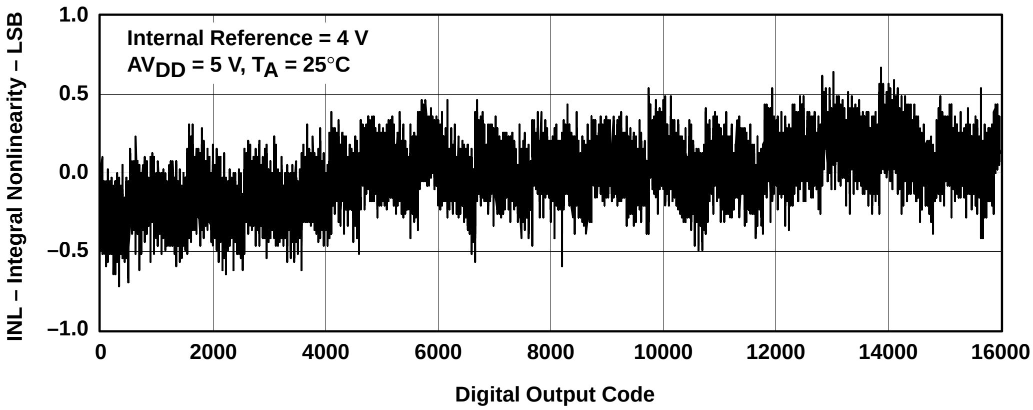


Figure 22

**DIFFERENTIAL NONLINEARITY
vs
DIGITAL OUTPUT CODE**

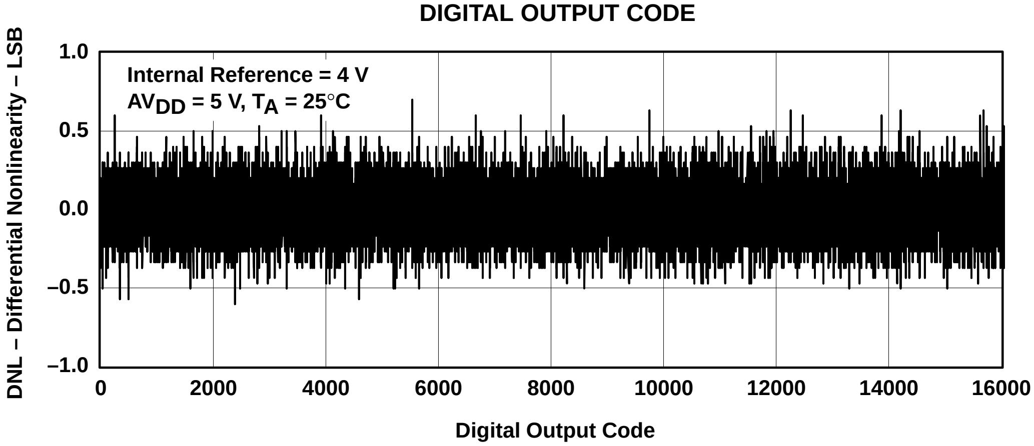


Figure 23

TYPICAL CHARACTERISTICS

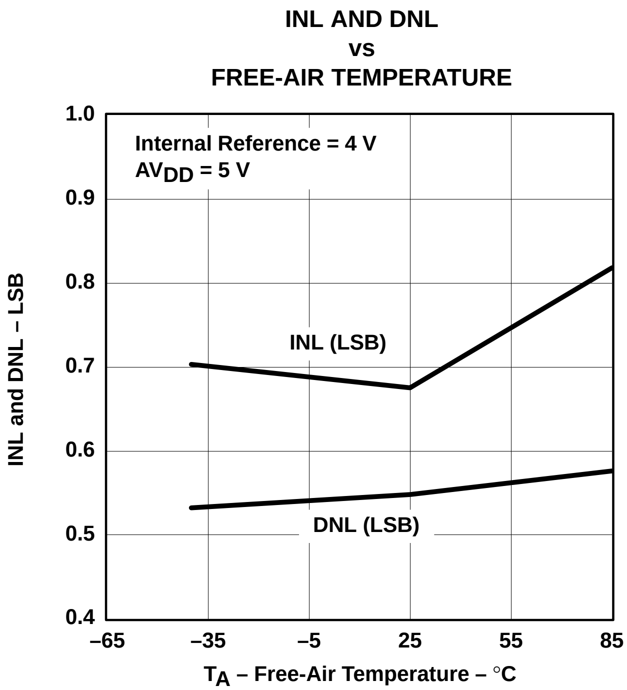


Figure 24

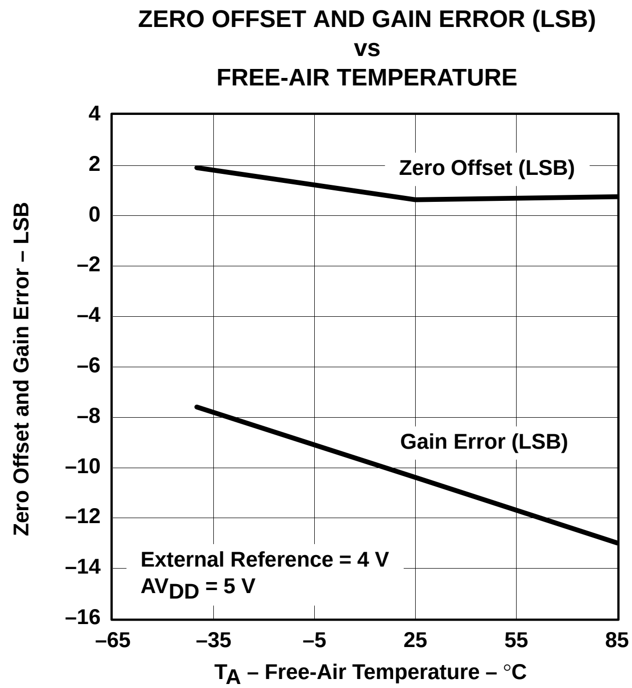


Figure 25

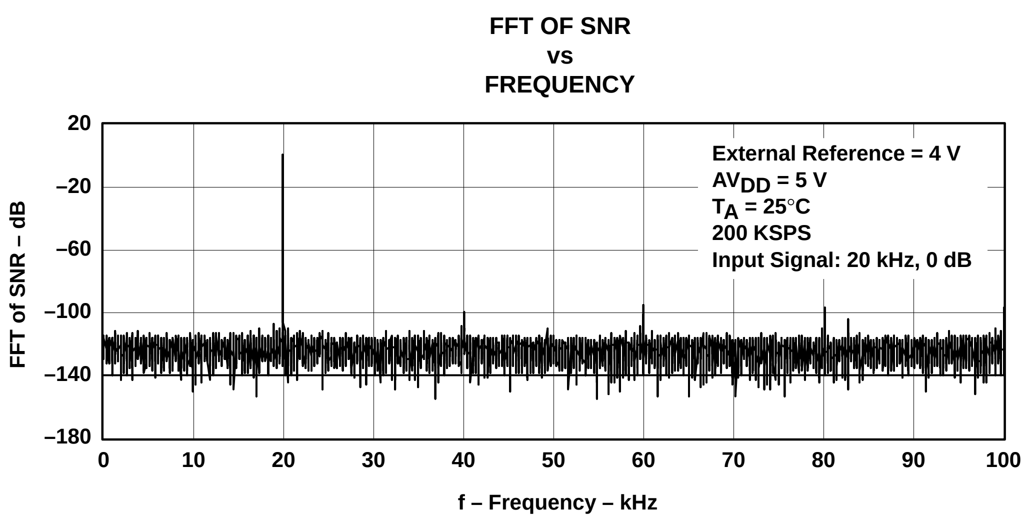


Figure 26

TYPICAL CHARACTERISTICS

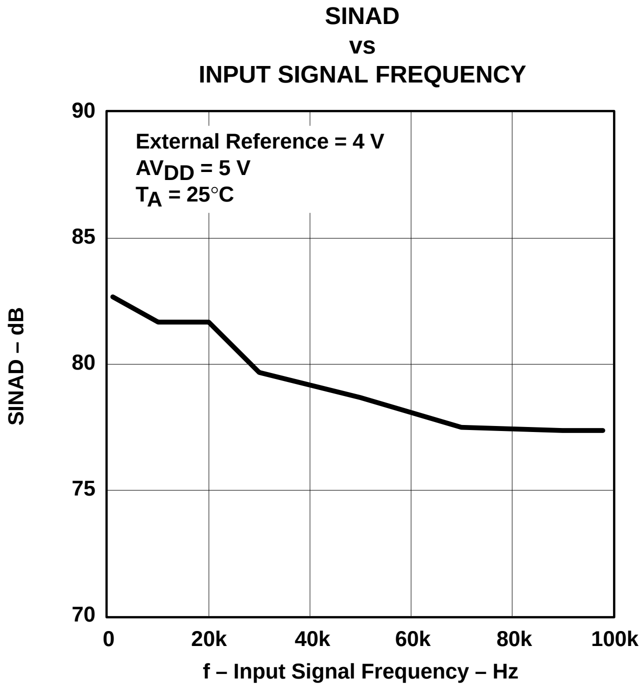


Figure 27

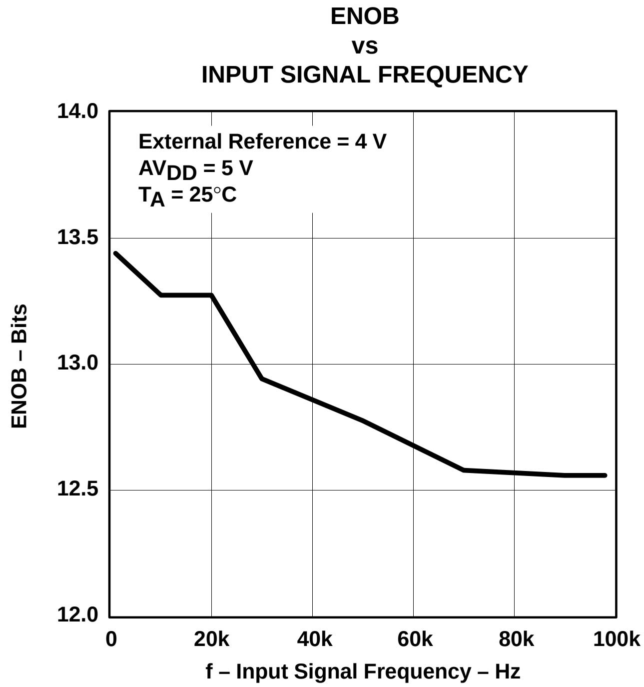


Figure 28

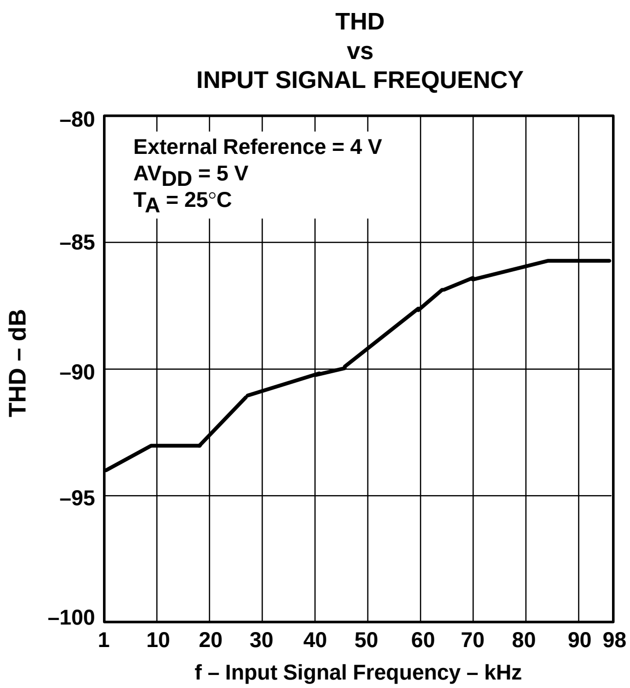


Figure 29

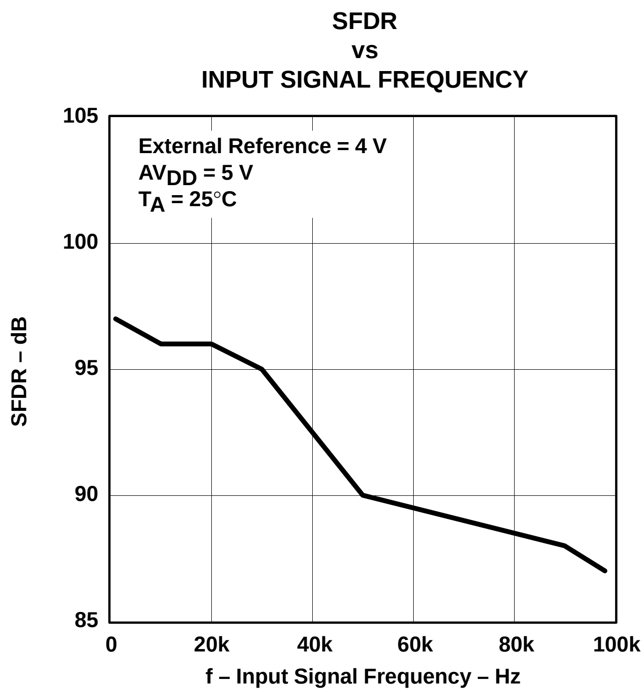


Figure 30

TYPICAL CHARACTERISTICS

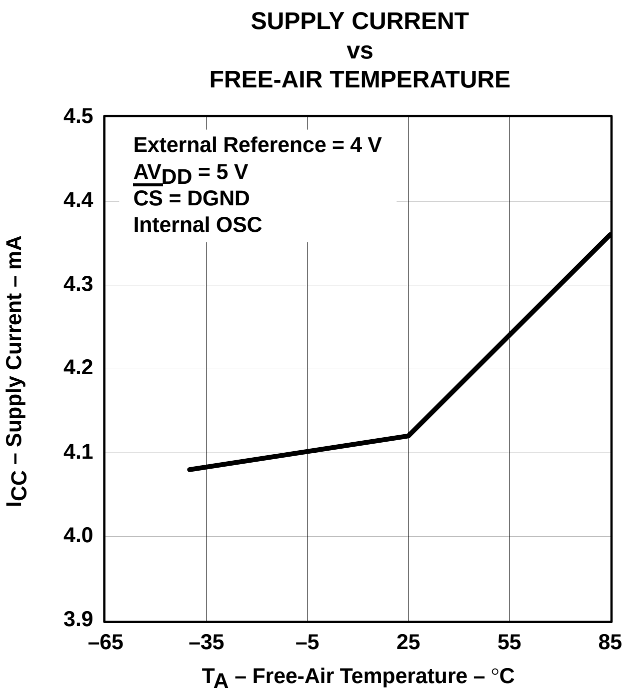


Figure 31

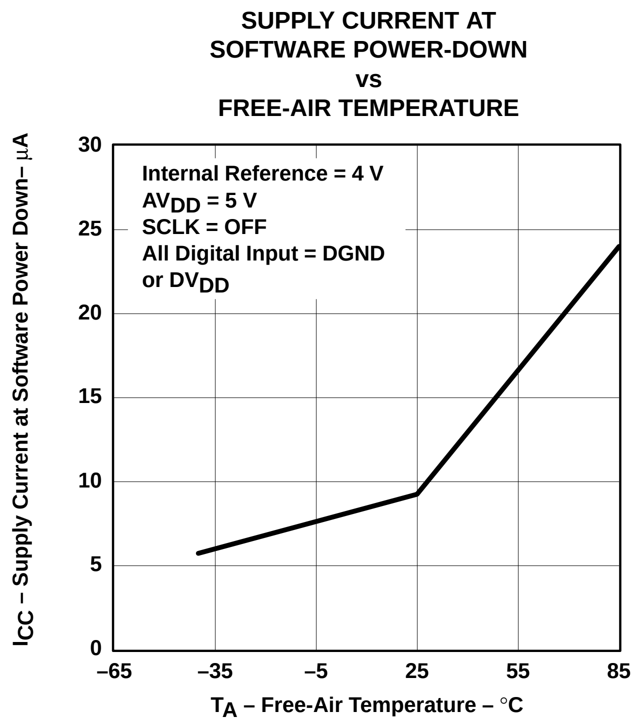


Figure 32

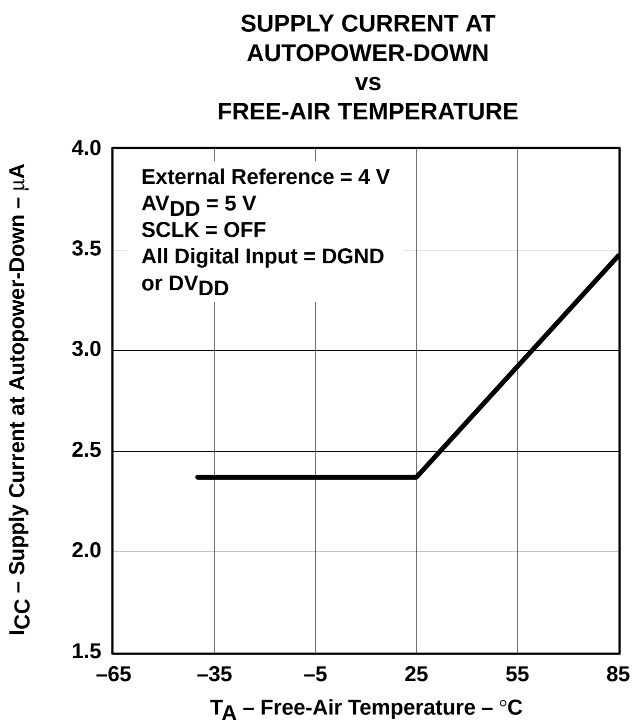


Figure 33

APPLICATION INFORMATION

interface with host

Figure 34 shows examples of the interface between a single converter and a host DSP (TMS320C54x™ DSP) or microprocessor. The C54x is set as FWID = 1 (active pulse width = 1CLK), (R/X) DATDLY = 1 (1 bit data delay), CLK(X/R)P = 0 (transmit data are clocked out at rising edge of CLK, receive data are sampled on falling edge of CLK), and FS(X/R)P = 1 (FS is active high). If multiple converters connect to the same C54x, use $\overline{CS}$ as the chip select.

The host microprocessor is set as the SPI master with CPOL = 0 (active high clock), and CPHA = 1 (transmit data is clock out at rising edge of CLK, receive data are sampled at falling edge of CLK). 16 bits (or more) per transfer is required.

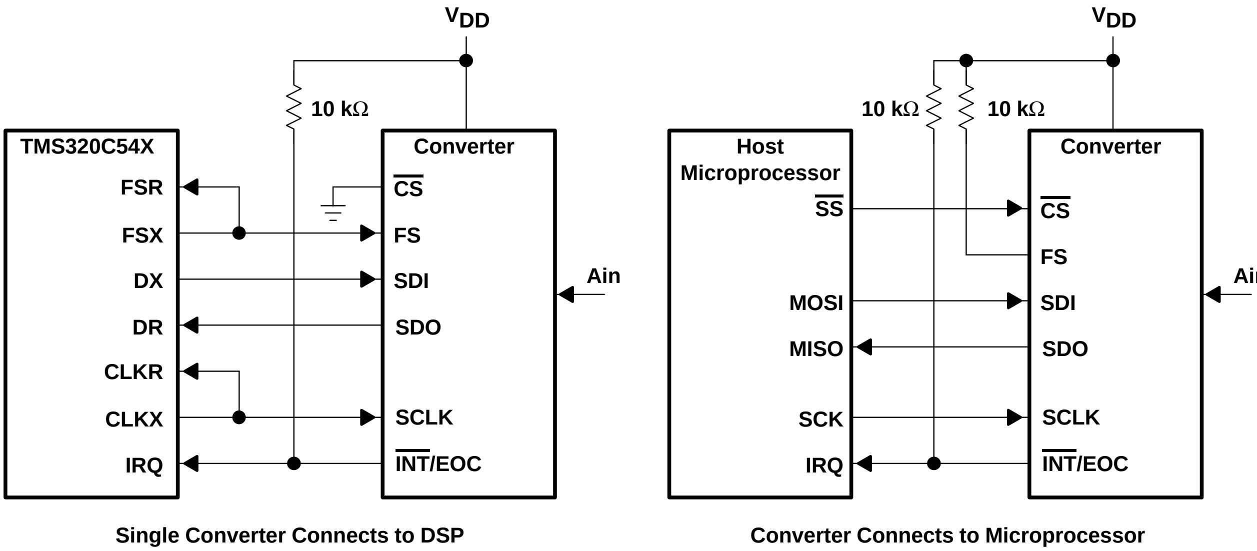


Figure 34. Typical Interface to Host DSP and Microprocessor

sampling time analysis

Figure 35 shows the equivalent analog input circuit of the converter. During the sampling, the input capacitor, C_i, has to be charged to V_C, ($V_C = V_S \pm$ voltage of 1/4 LSB = $V_S \pm [V_S/65532]$ for 14 bit converter).

$t_{(s)} = R_t \times C_i \times \ln(65532)$ where $R_t = R_S + r_i$, $t_{(s)}$ = Sampling time

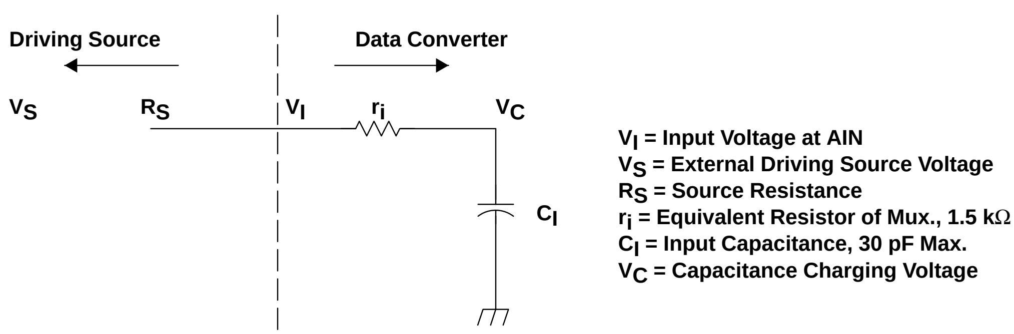


Figure 35. Equivalent Input Circuit Including the Driving Source

TMS320C54x is a trademark of Texas Instruments.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC3544CDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC3544	Samples
TLC3544CPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC3544	Samples
TLC3544CPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC3544	Samples
TLC3544IDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC3544I	Samples
TLC3544IPW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y3544	Samples
TLC3548CDW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC3548	Samples
TLC3548CDWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC3548	Samples
TLC3548CPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLC3548	Samples
TLC3548CPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLC3548	Samples
TLC3548IDW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC3548I	Samples
TLC3548IDWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC3548I	Samples
TLC3548IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	Y3548	Samples
TLC3548IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	Y3548	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

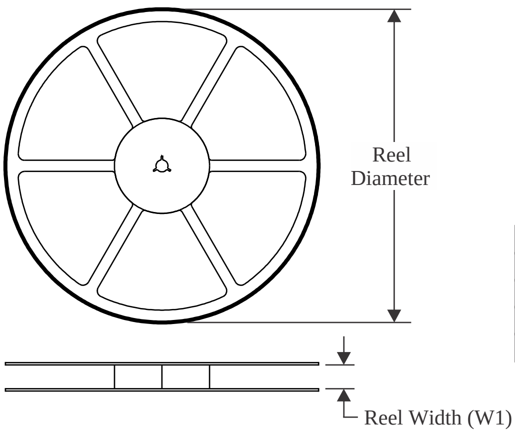
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

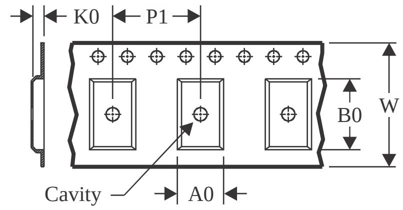
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

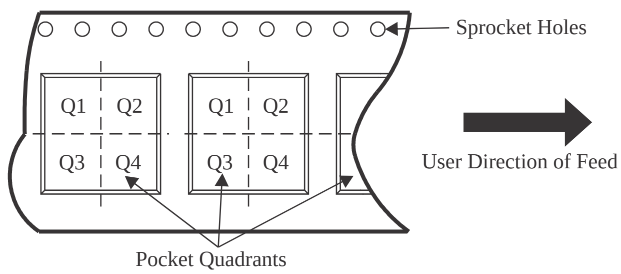


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

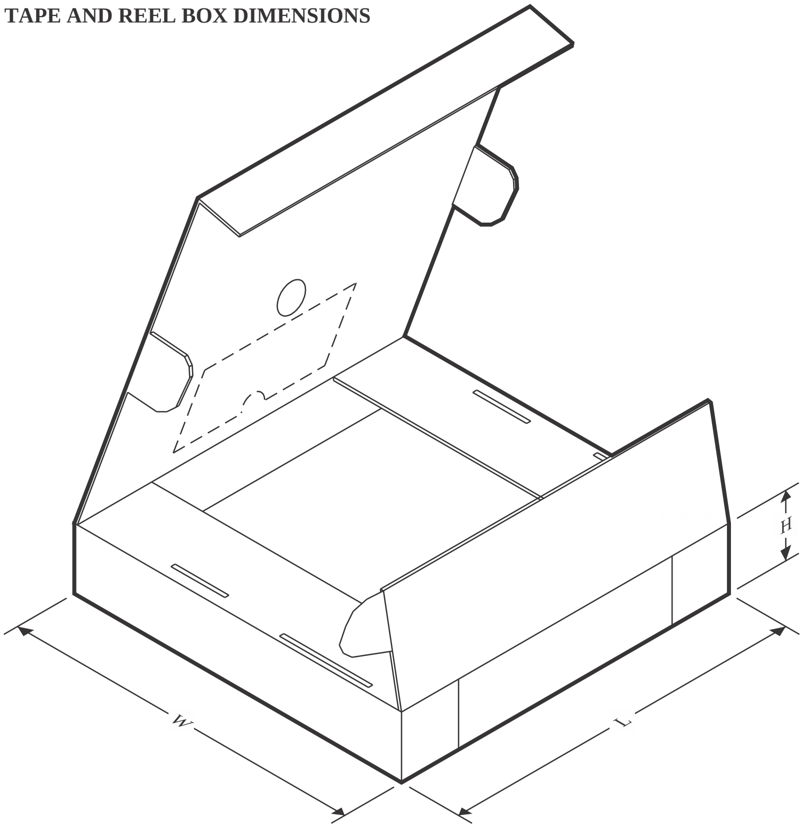
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC3544CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC3548CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TLC3548CPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TLC3548IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TLC3548IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

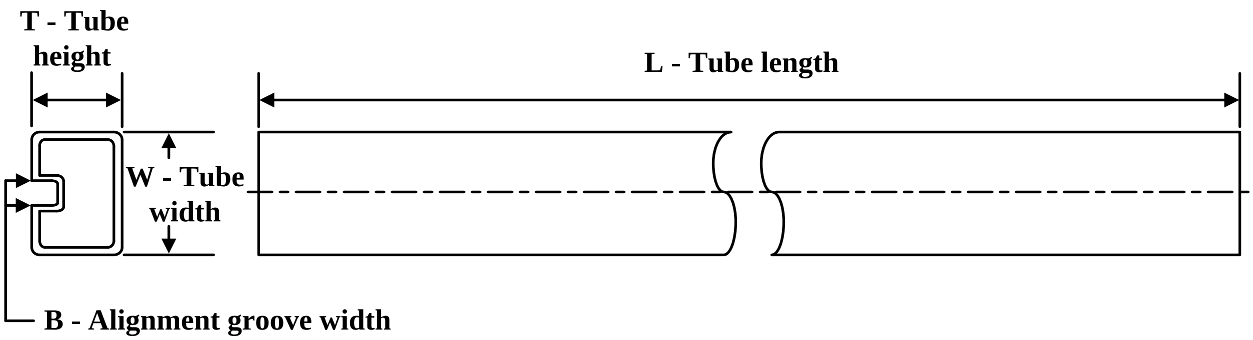
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

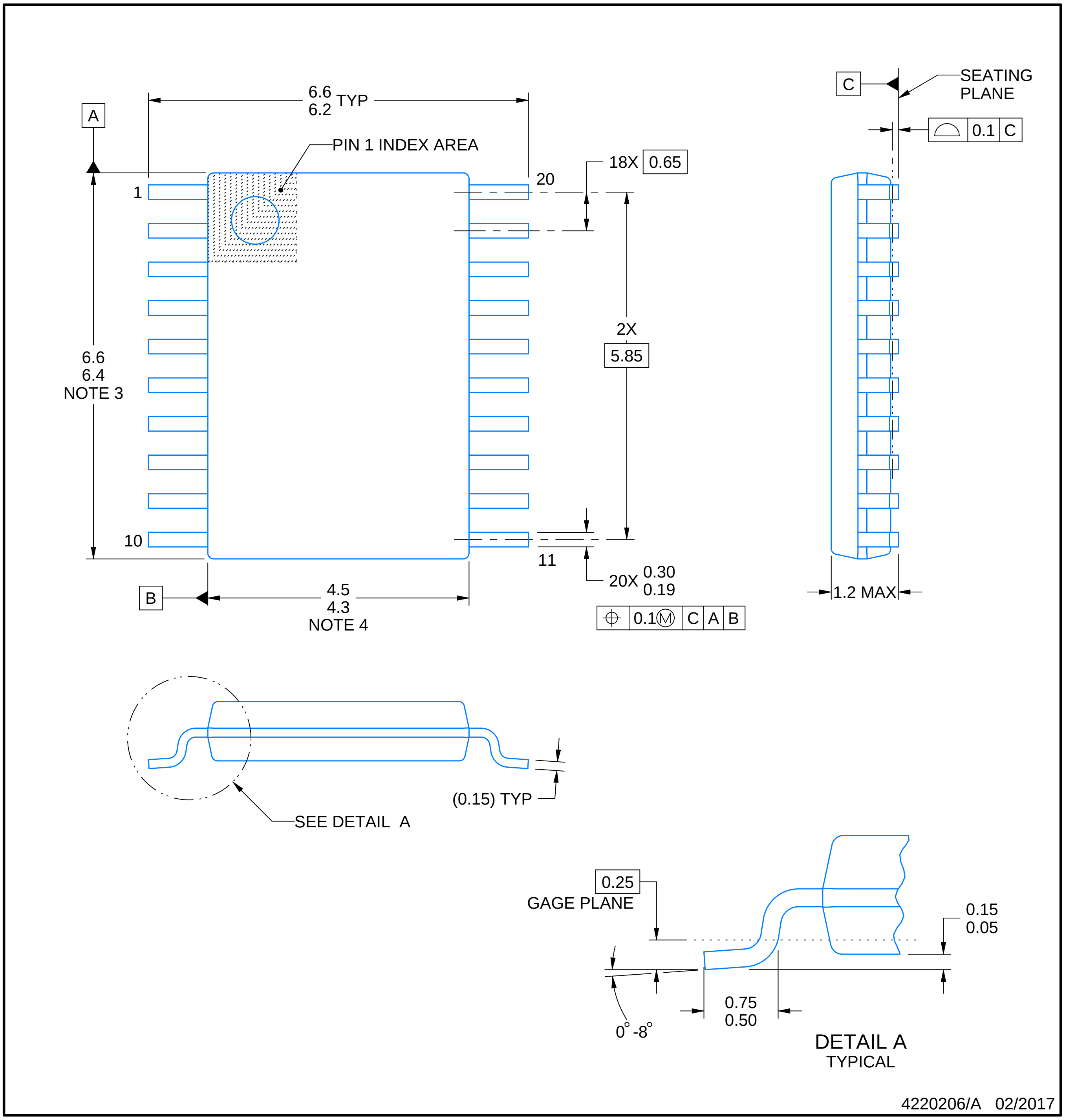
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC3544CPWR	TSSOP	PW	20	2000	350.0	350.0	43.0
TLC3548CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TLC3548CPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
TLC3548IDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TLC3548IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0

TUBE



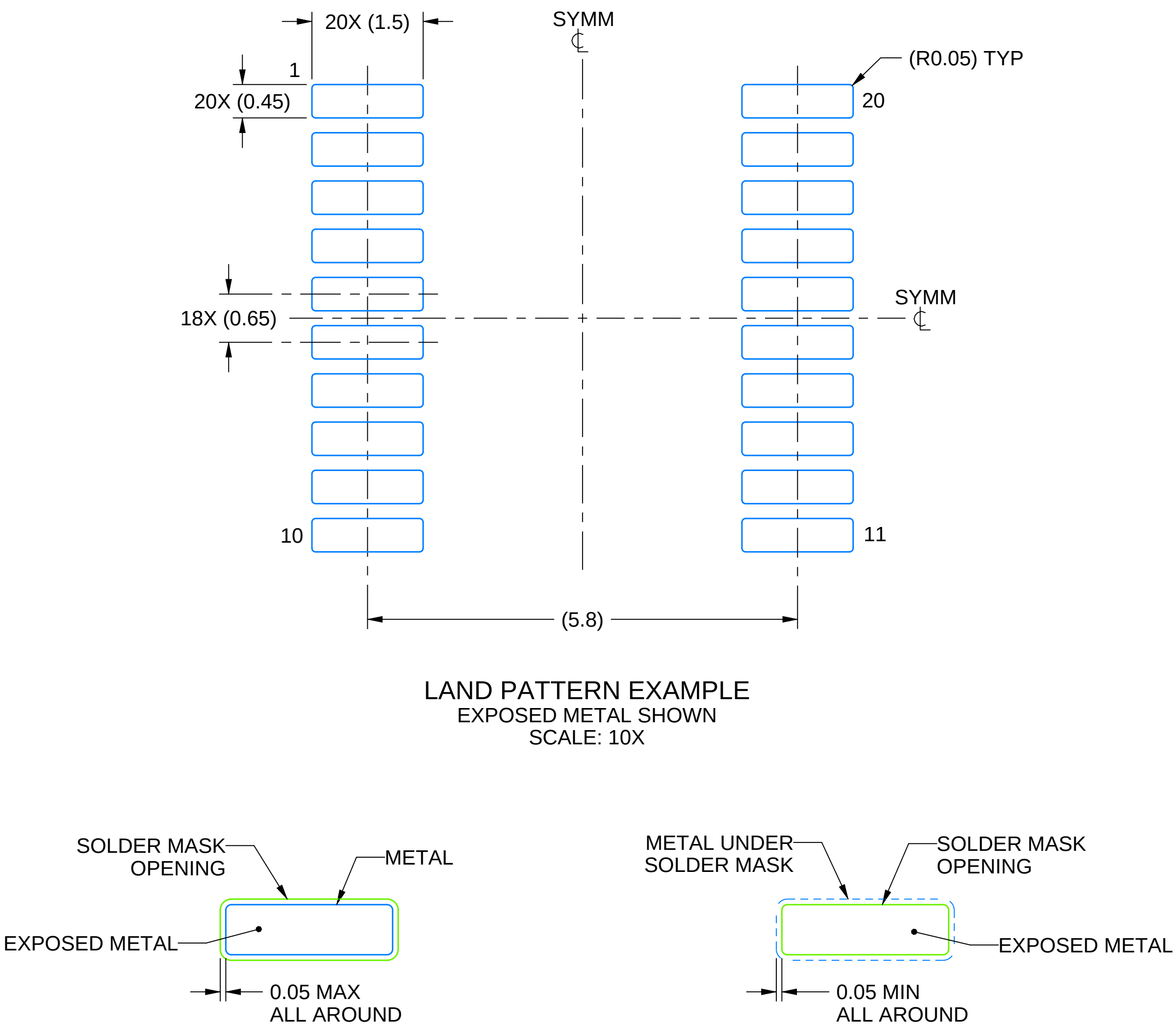
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC3544CDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC3544CPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLC3544IDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC3544IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLC3548CDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
TLC3548CPW	PW	TSSOP	24	60	530	10.2	3600	3.5
TLC3548IDW	DW	SOIC	24	25	506.98	12.7	4826	6.6
TLC3548IPW	PW	TSSOP	24	60	530	10.2	3600	3.5



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

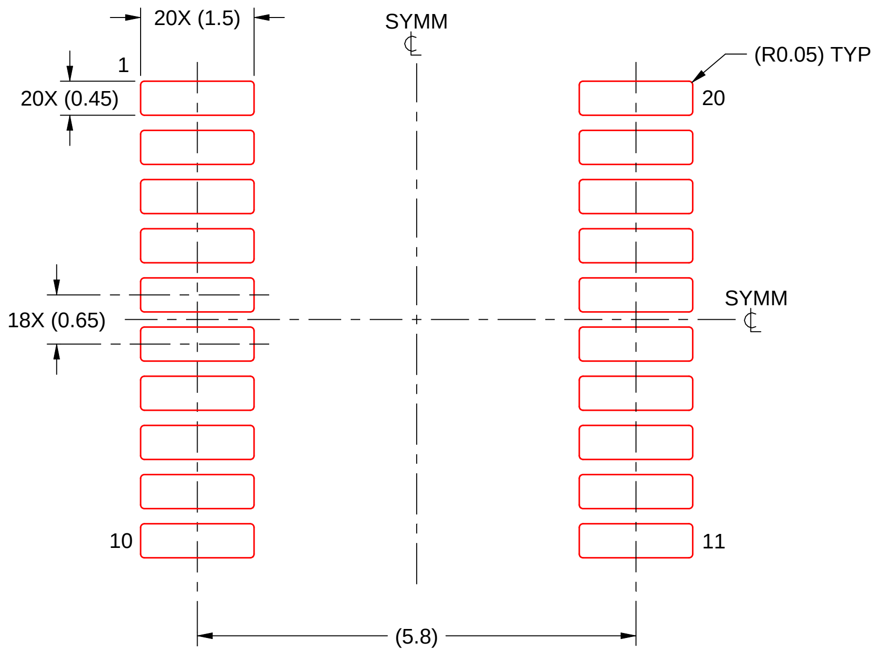
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



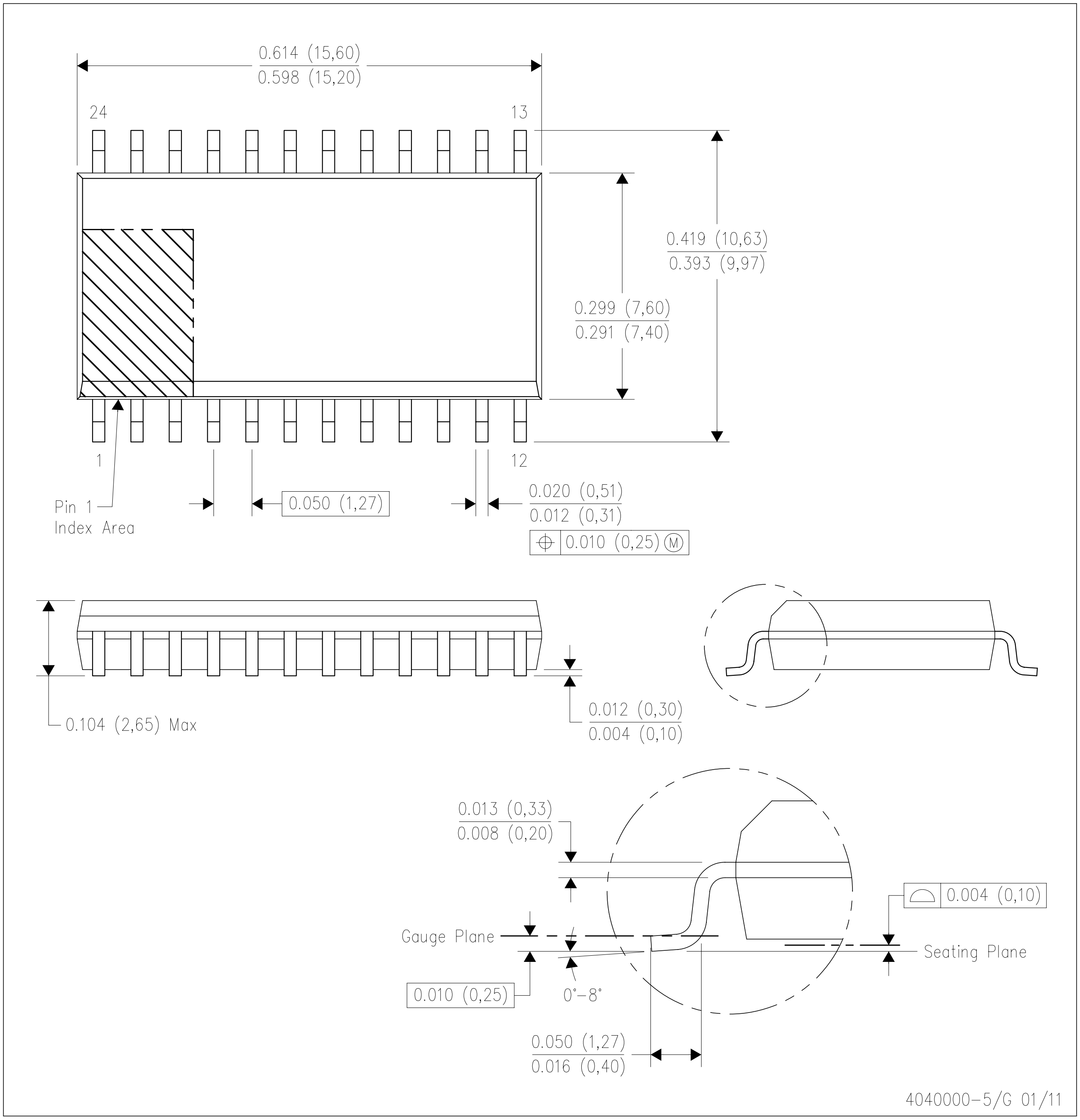
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

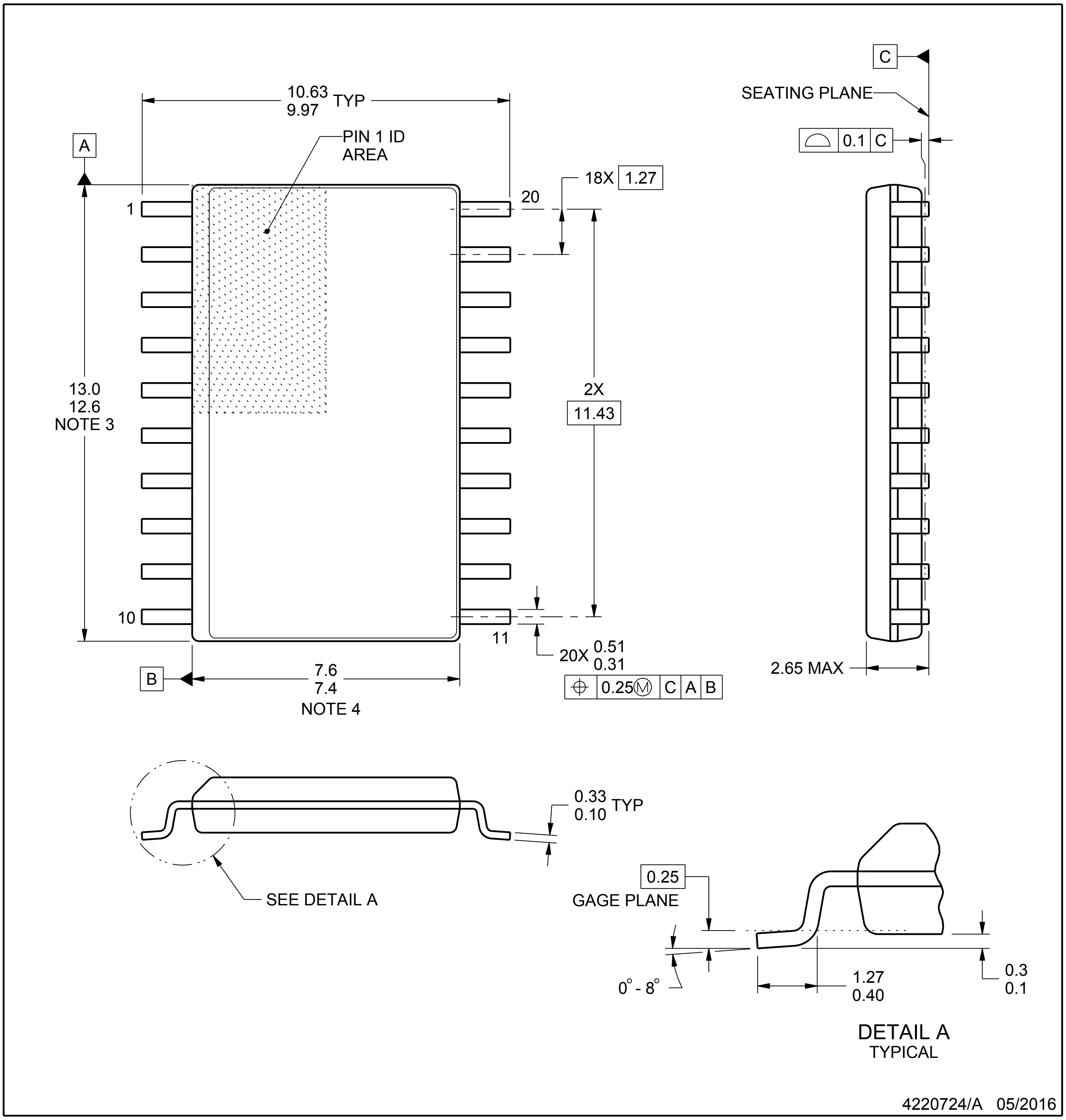
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24) PLASTIC SMALL OUTLINE

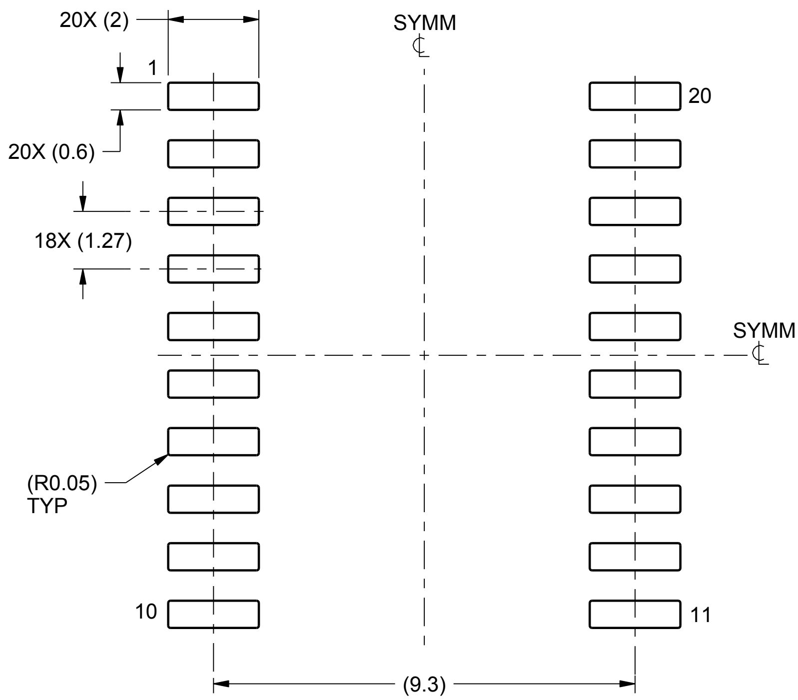


NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.

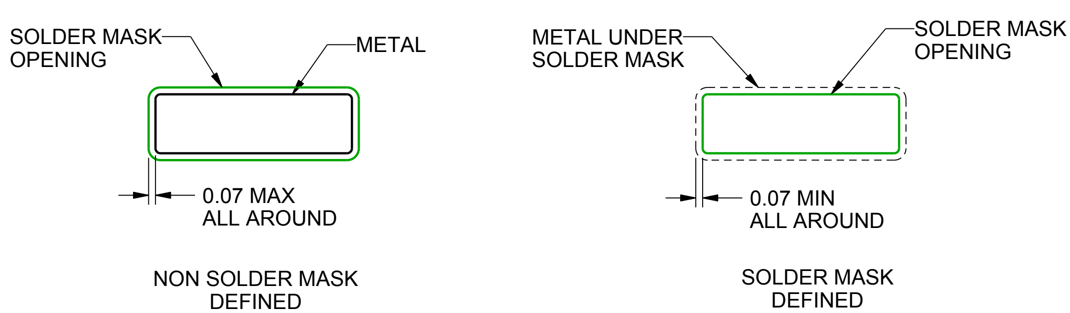


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

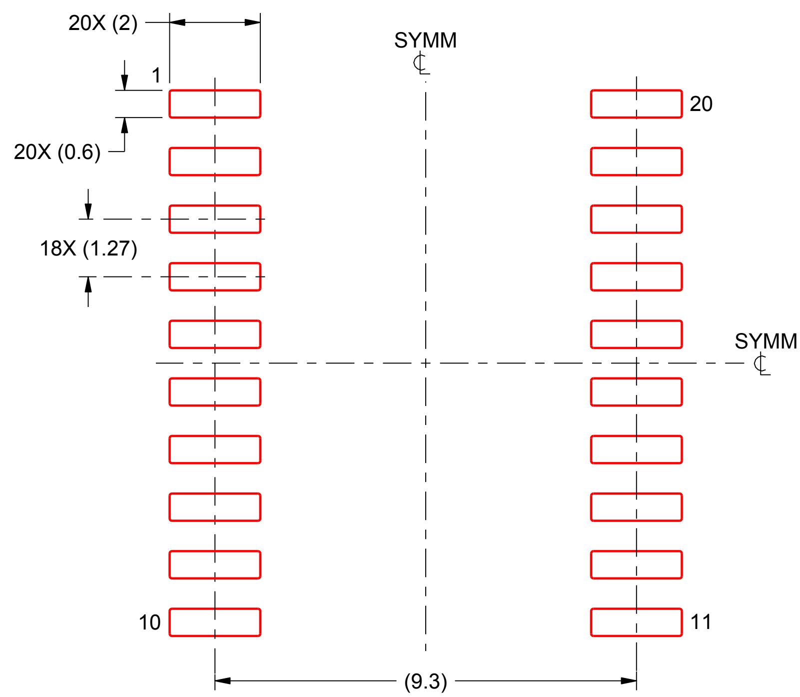


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

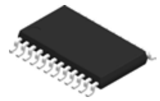


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

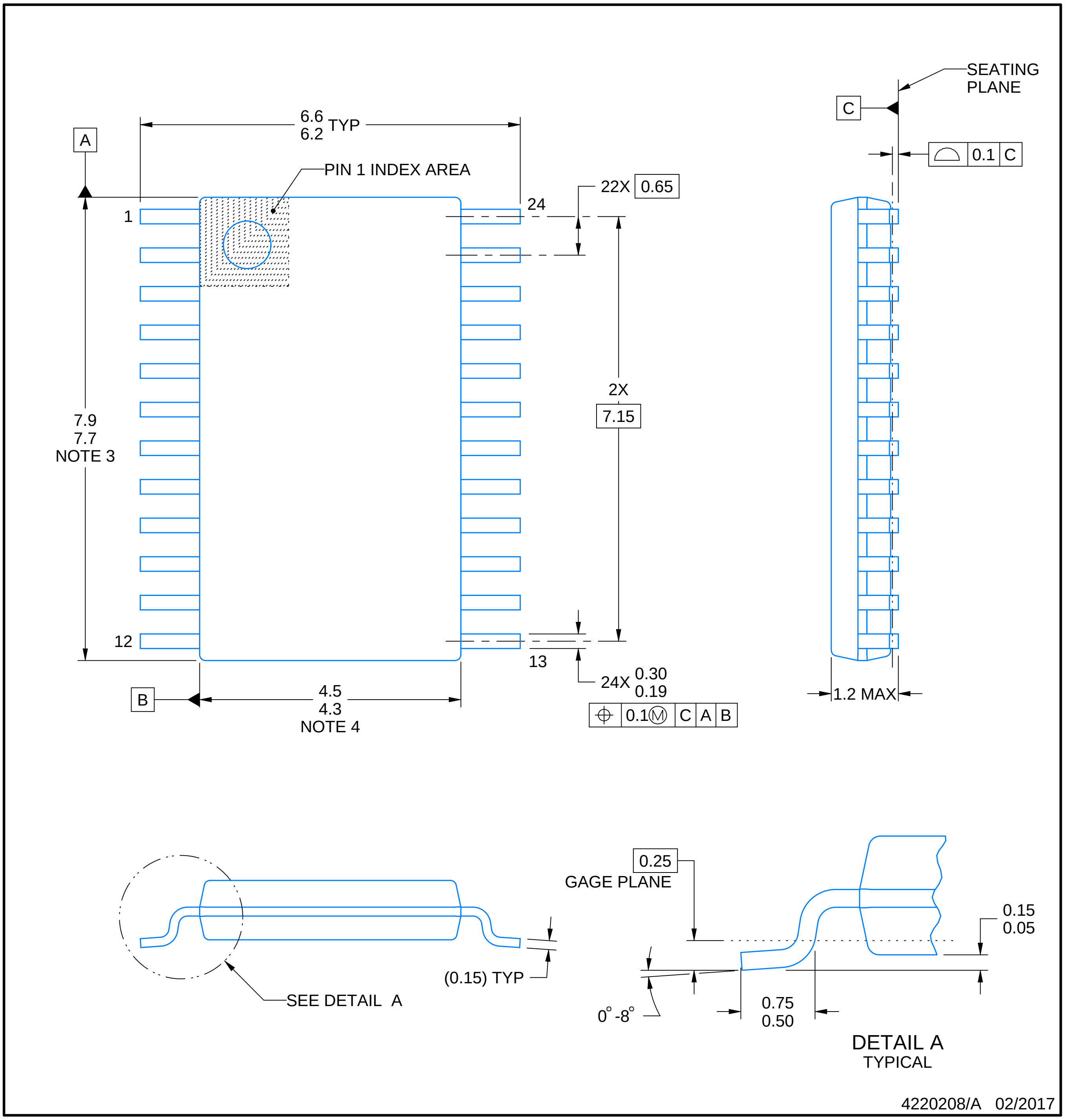
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

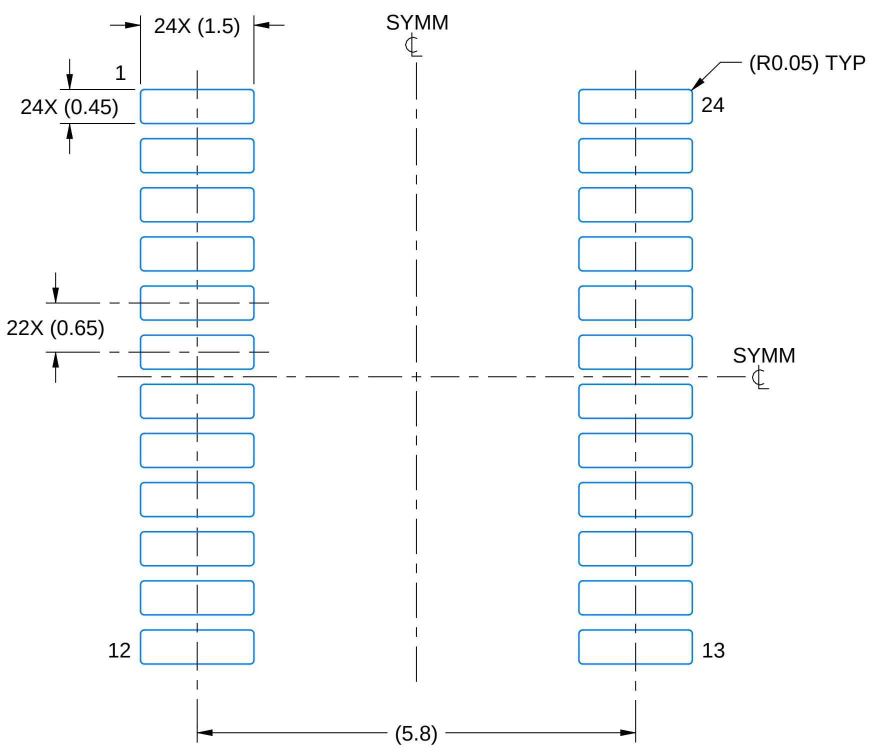
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

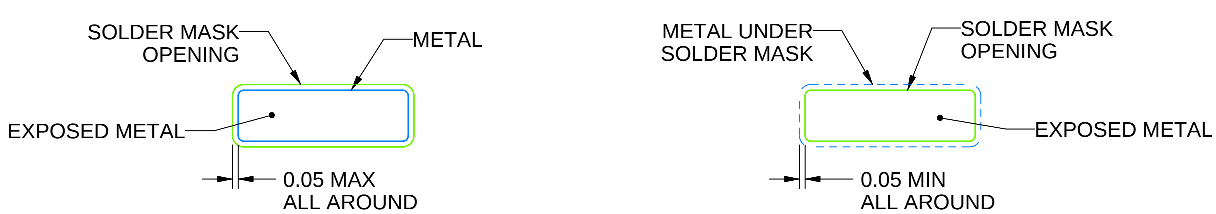


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

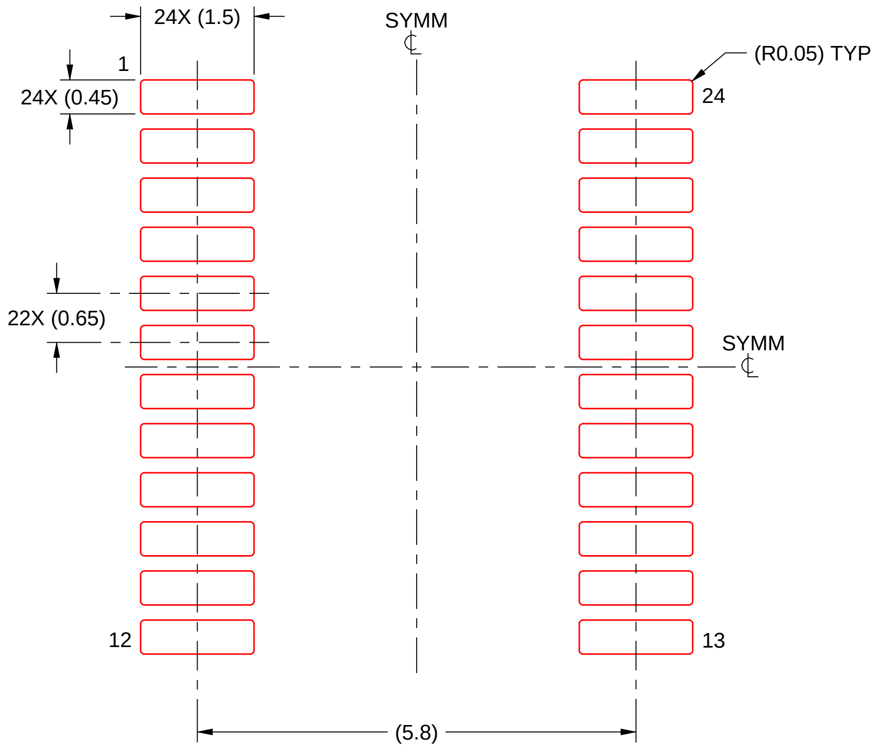


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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