16 通道恒定电流 LED 驱动器支持 7 位全局亮度控制、节电模式以及针对 LED 灯的全面自我诊断功能

查询样品: TLC5929

特性

- **16** 个支持开关控制的恒定电流汇极输出通道
- 电流性能:
  - **40 mA (V_{CC} ≤ 3.6 V)**
  - **50 mA (V_{CC} > 3.6 V)**
- 全局亮度控制: **7** 位（**128** 步）
- 电源电压范围: **3.0 V** 至 **5.5 V**
- **LED** 电源电压: 高达 **10 V**
- 恒定电流准确性:
  - 通道间 **= ±1%** （典型值），**±3% (**最大值**)**
  - 设备间 **= ±2% (**典型值**), ±4% (**最大值**)**
- 数据传输速率: **33 MHz**
- **BLANK** 脉宽: **40 ns** （最小值）
- 支持无形检测模式的 **LED** 开路检测 **(LOD)/LED** 短路检测
- 输出漏电检测 **(OLD)** 可检测 **3 µA** 漏电
- 预热报警 **(PTW)**
- 热关断 **(TSD)**
- 电流参考端接短路标记 **(ISF)**
- **10-µA** 流耗节电模式
- 欠压锁定可设置默认数据
- 每通道间 **2-ns** 延迟开关可最大限度减少浪涌电流
- 工作温度范围: **–40°C** 至 **+85°C**

应用范围

- 可变消息标志 **(VMS)**
- 照明

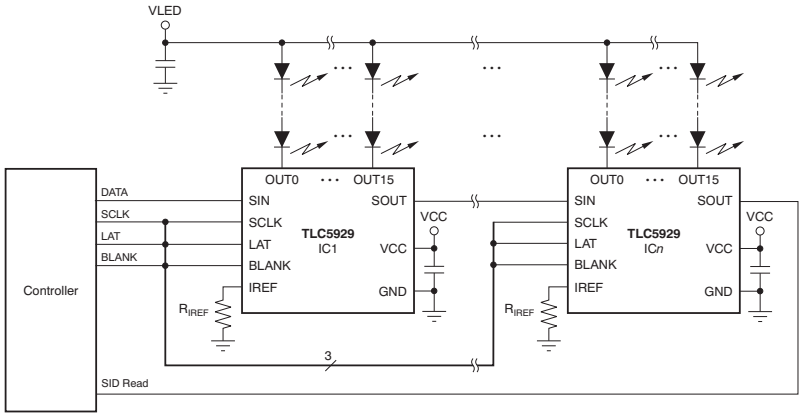
说明

TLC5929 是 16 通道恒定电流汇极 LED 驱动器。 可通过向内部寄存器写入数据对每一通道进行开关操作。 所有 16 个通道的恒定电流值都由单个外部电阻器设置，此电阻器支持 128 步全局亮度控制 (BC)。

TLC5929 具有六个错误标记：LED 开路检测 (LOD)、LED 短路检测(LSD)、输出漏电检测 (OLD)、参考电流端接短路检测 (ISF)、预热报警 (PTW) 以及散热故障标记 (TEF)。 此外，LOD 和 LSD 功能还提供无形检测模式 (IDM)，可在输出关闭时检测这些故障。 故障检测结果可通过串行接口端口读取。

TLC5929 还具有省电模式，可在全部输出关闭后将总电流消耗设为 10 µA（典型值）。

典型应用电路（多菊花链 **TLC5929**）



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5929	SSOP/QSOP-24	DBQ	TLC5929DBQR	Tape and Reel, 2500
			TLC5929DBQ	Tube, 50
	HTSSOP-24 PowerPAD™	PWP	TLC5929PWPR	Tape and Reel, 2000
			TLC5929PWP	Tube, 60
	QFN-24	RGE	TLC5929RGER	Tape and Reel, 3000
			TLC5929RGE	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	VCC	–0.3	+6.0	V
	SIN, SCLK, LAT, BLANK, IREF, SOUT	–0.3	V_{CC} + 0.3	V
	OUT0 to OUT15	–0.3	+11	V
Current	OUT0 to OUT15	0	+65	mA
Temperature	Operating junction, T_J (max)	–40	+150	°C
	Storage, T_{STG}	–55	+150	°C
Electrostatic Discharge Ratings	Human body model (HBM)		4000	V
	Charged device model (CDM)		2000	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under R*ecommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to device ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC5929			UNITS
		DBQ	PWP	RGE	
		24 PINS	24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	85.3	37.6	38.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	48.8	24.5	45.3	
θ_{JB}	Junction-to-board thermal resistance	38.6	11.5	16.9	
ψ_{JT}	Junction-to-top characterization parameter	11.9	0.5	0.9	
ψ_{JB}	Junction-to-board characterization parameter	38.3	11.3	16.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	5.7	6.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

At T_A= –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5929			UNIT
			MIN	NOM	MAX	
DC Characteristics: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0	3.3	5.5	V
V_O	Voltage applied to output	OUT0 to OUT15			10	V
V_{IH}	High-level input voltage	SIN, SCLK, LAT, BLANK	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	SIN, SCLK, LAT, BLANK	GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–2	mA
I_{OL}	Low-level output current	SOUT			2	mA
I_{OLC}	Constant output sink current	OUT0 to OUT15, 3 V ≤ V_{CC} < 3.6 V			40	mA
		OUT0 to OUT15, 3.6 V ≤ V_{CC} < 5.5 V			50	mA
T_A	Operating free-air temperature range		–40		+85	°C
T_J	Operating junction temperature range		–40		+125	°C
AC Characteristics: V_{CC} = 3 V to 5.5 V						
$f_{CLK\ (SCLK)}$	Data shift clock frequency	SCLK			33	MHz
t_{WH0}	Pulse duration (see Figure 4 and Figure 6)	SCLK	10			ns
t_{WL0}		SCLK	10			ns
t_{WH1}		LAT	20			ns
t_{WH2}		BLANK	40			ns
t_{WL2}		BLANK	40			ns
t_{SU0}	Setup time (see Figure 4 and Figure 6)	SIN to SCLK↑	5			ns
t_{SU1}		LAT↑ to SCLK↑	200			ns
t_{H0}	Hold time (see Figure 4 and Figure 6)	SIN to SCLK↑	3			ns
t_{H1}		LAT↑ to SCLK↑	10			ns

ELECTRICAL CHARACTERISTICS

At V_{CC} = 3 V to 5.5 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TLC5929 MIN	TLC5929 TYP	TLC5929 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA at SOUT		V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA at SOUT				0.4	V
V_{LOD}	LED open detection threshold	All OUT*n* = on		0.25	0.30	0.35	V
V_{LSD0}	LED short detection threshold	All OUT*n* = on, detection voltage code = 0h		0.32 × V_{CC}	0.35 × V_{CC}	0.38 × V_{CC}	V
V_{LSD1}		All OUT*n* = on, detection voltage code = 1h		0.42 × V_{CC}	0.45 × V_{CC}	0.48 × V_{CC}	V
V_{LSD2}		All OUT*n* = on, detection voltage code = 2h		0.52 × V_{CC}	0.55 × V_{CC}	0.58 × V_{CC}	V
V_{LSD3}		All OUT*n* = on, detection voltage code = 3h		0.62 × V_{CC}	0.65 × V_{CC}	0.68 × V_{CC}	V
V_{IREF}	Reference voltage output	R_{IREF} = 1.3 kΩ		1.175	1.205	1.235	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND at SIN, SCLK, LAT, and BLANK		–1		1	µA
I_{CC0}	Supply current (V_{CC})	SIN/SCLK/LAT = low, BLANK = high, all OUT*n* = off, V_{OUTn} = 0.8 V, BC = 7Fh, R_{IREF} = open			2	3	mA
I_{CC1}		SIN/SCLK/LAT = low, BLANK = high, all OUT*n* = off, V_{OUTn} = 0.8 V, BC = 7Fh, R_{IREF} = 3.6 kΩ (I_{OUT} = 18.3 mA target)			5	7	mA
I_{CC2}		SIN/SCLK/LAT/BLANK = low, All OUT*n* = on, V_{OUTn} = 0.8 V, BC = 7Fh, R_{IREF} = 3.6 kΩ (I_{OUT} = 18.3 mA target)			5	7	mA
I_{CC3}		SIN/SCLK/LAT/BLANK = low, All OUT*n* = on, V_{OUTn} = 0.8 V, BC = 7Fh, R_{IREF} = 1.6 kΩ (I_{OUT} = 41.3 mA target)			9	11	mA
I_{CC4}		V_{CC} = 5.0 V, SIN/SCLK/LAT/BLANK = low, All OUT*n* = on, V_{OUTn} = 0.8 V, BC = 7Fh, R_{IREF} = 1.3 kΩ (I_{OUT} = 50.8 mA target)			11	14	mA
I_{CC5}		V_{CC} = 5.0 V, SIN/SCLK/LAT/BLANK = low, All OUT*n* = on, V_{OUTn} = 0.8 V, BC = 7Fh, R_{IREF} = 1.3 kΩ (I_{OUT} = 50.8 mA target), all output data off with power-save mode enabled			10	40	µA
I_{OLC0}	Constant output sink current (OUT0 to OUT15, see Figure 3)	All OUT*n* = on, V_{OUTn} = V_{OUTfix} = 0.8 V, BC = 7Fh, R_{IREF} = 1.6 kΩ		38.5	41.3	44.1	mA
I_{OLC1}		V_{CC} = 5.0 V, All OUT*n* = on, V_{OUTn} = V_{OUTfix} = 1 V, BC = 7Fh, R_{IREF} = 1.3 kΩ		47.3	50.8	54.3	mA
I_{OLKG0}	Output leakage current (OUT0 to OUT15, see Figure 3)	BLANK = high, V_{OUTn} = V_{OUTfix} = 10 V, R_{IREF} = 1.6 kΩ	T_J = +25°C			0.1	µA
I_{OLKG1}			T_J = +85°C(1)			0.2	µA
I_{OLKG2}			T_J = +125°C(1)		0.3	0.8	µA
ΔI_{OLC0}	Constant-current error (channel-to-channel, OUT0 to OUT15)(2)	All OUT*n* = on, V_{OUTn} = V_{OUTfix} = 0.8 V, BC = 7Fh, R_{IREF} = 1.6 kΩ, T_A = +25°C			±1	±3	%
ΔI_{OLC1}	Constant-current error (device-to-devicel, OUT0 to OUT15)(3)	All OUT*n* = on, V_{OUTn} = V_{OUTfix} = 0.8 V, BC = 7Fh, R_{IREF} = 1.6 kΩ, T_A = +25°C			±2	±4	%

(1) Not tested; specified by design.

(2) The deviation of each output from the average of OUT0 to OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta\ (\%) = 100 \times \left(\frac{I_{OLC(n)}}{\left(\frac{(I_{OLC(0)} + I_{OLC(1)} + \ldots + I_{OLC(14)} + I_{OLC(15)})}{16} \right)} - 1 \right)$$

(3) The deviation of the OUT0 to OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the formula:

$$\Delta\ (\%) = 100 \times \left(\frac{\left(\frac{(I_{OLC(0)} + I_{OLC(1)} + \ldots I_{OLC(14)} + I_{OLC(15)})}{16} \right) - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right)$$

Ideal current is calculated by the formula:

$$I_{OLC(IDEAL)} = 54.8 \times \left(\frac{1.205}{R_{IREF}} \right)$$

ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 3 V to 5.5 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5929			UNIT
			MIN	TYP	MAX	
ΔI_{OLC2}	Line regulation(4)	All OUT*n* = on, V_{OUTn} = V_{OUTfix} = 0.8 V, BC = 7Fh, R_{IREF} = 1.6 kΩ		±0.1	±1	%/V
ΔI_{OLC3}	Load regulation(5)	All OUT*n* = on, V_{OUTn} = 0.8 V to 3 V, V_{OUTfix} = 0.8 V, BC = 7Fh, R_{IREF} = 1.6 kΩ		±0.5	±3	%/V
T_{TEF}	Thermal error flag threshold	Junction temperature(6)	150	165	180	°C
T_{HYS}	Thermal error flag hysteresis	Junction temperature(6)	5	10	20	°C
T_{PTW}	Pre-thermal warning threshold	Junction temperature(6)	125	138	150	°C

(4) Line regulation is calculated by the formula:

$$\Delta\ (\%) = 100 \times \left(\frac{(I_{OLC(n)} \text{ at } V_{CC} = 5.5\ V) - (I_{OLC(n)} \text{ at } V_{CC} = 3.0\ V)}{2.5 \times (I_{OLC(n)} \text{ at } V_{CC} = 3.0\ V)} \right)$$

Where 2.5 is the difference between the maximum and minimum V_{CC} voltage.

(5) Load regulation is calculated by the equation:

$$\Delta\ (\%) = 100 \times \left(\frac{(I_{OLC(n)} \text{ at } V_{OUTn} = 3\ V) - (I_{OLC(n)} \text{ at } V_{OUTn} = 0.8\ V)}{2.2 \times (I_{OLC(n)} \text{ at } V_{OUTn} = 0.8\ V)} \right)$$

Where 2.2 is the difference between the maximum and minimum V_{CC} voltage.

(6) Not tested; specified by design.

SWITCHING CHARACTERISTICS (See Figure 1, Figure 2, and Figure 5 through Figure 7)

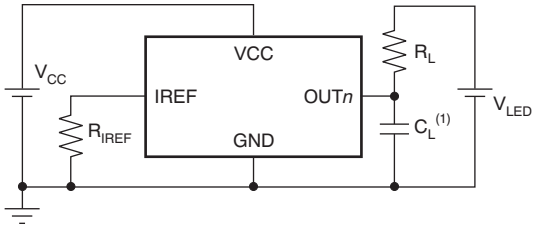
At V_{CC} = 3 V to 5.5 V, T_A = –40°C to +85°C, C_L = 15 pF, R_L = 82 Ω, R_{IREF} = 1.3 kΩ, and V_{LED} = 5.0 V.
Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5929			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	SOUT		3	10	ns
t_{R1}		OUT*n*, BC = 7Fh, T_A = +25°C		23	60	ns
t_{F0}	Fall time	SOUT		3	10	ns
t_{F1}		OUT*n*, BC = 7Fh, T_A = +25°C		31	60	ns
t_{D0}	Propagation delay	SCLK↑ to SOUT↑↓		15	25	ns
t_{D1}		LAT↑ or BLANK↑↓ to OUT0 sink current on/off, BC = 7Fh		35	65	ns
t_{D2}		OUT*n* on/off to OUT*n* + 1 on/off, BC = 7Fh		3	11	ns
t_{D3}		LAT↑ to power-save mode by data writing for all output off			300	ns
t_{D4}		SCLK↑ to normal mode operation			20	µs
t_{ON_ERR}	Output on-time error(1)	Output on/off data = all '1', BLANK low pulse = 40 ns, BC = 7Fh	–30		20	ns
f_{OSC}	Internal oscillator frequency		12	20	28	MHz

(1) Output on-time error (t_{ON_ERR}) is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – 40 ns. t_{OUTON} is the actual on-time of OUT*n*.

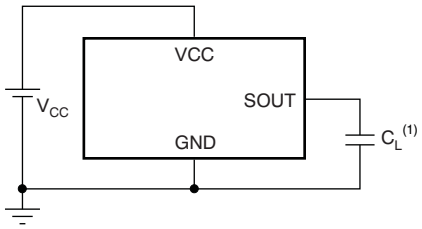
PARAMETER MEASUREMENT INFORMATION

TEST CIRCUITS



(1) C_L includes measurement probe and jig capacitance.

Figure 1. Rise Time and Fall Time Test Circuit for OUT*n*



(1) C_L includes measurement probe and jig capacitance.

Figure 2. Rise Time and Fall Time Test Circuit for SOUT

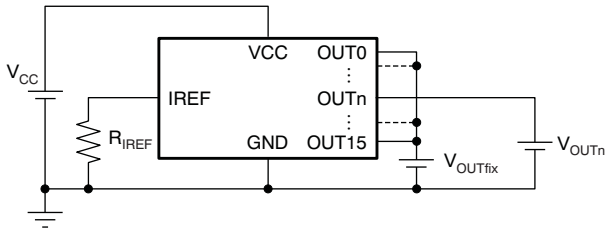
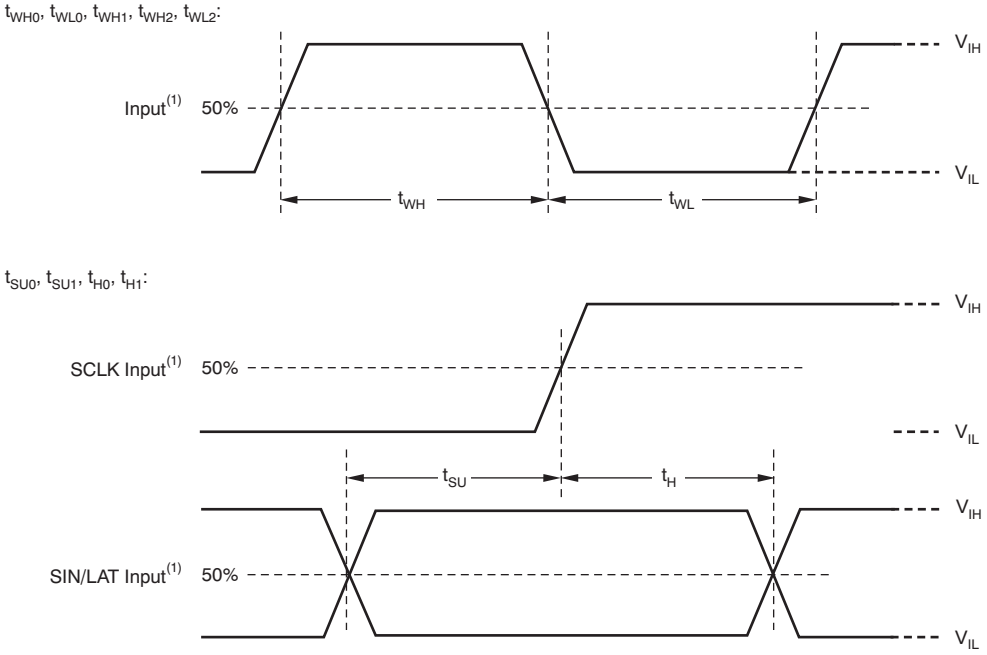


Figure 3. Constant-Current Test Circuit for OUT*n*

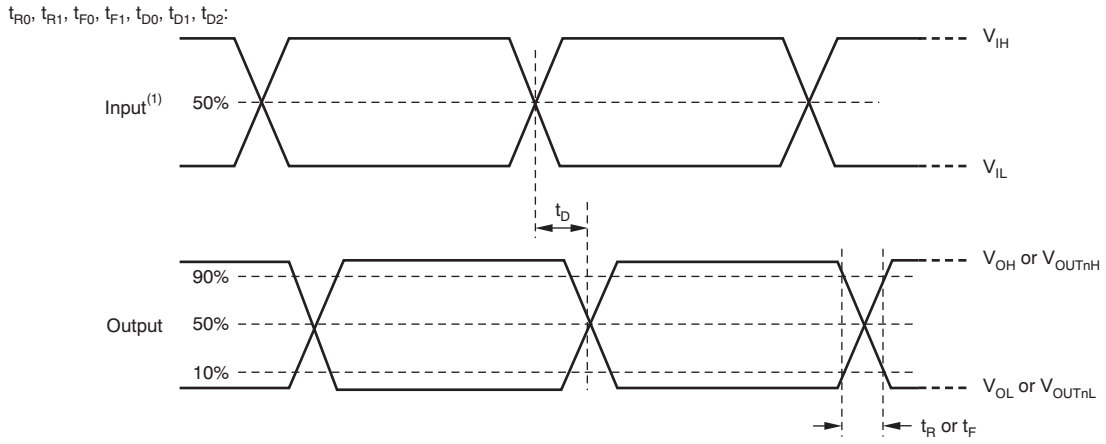
PARAMETER MEASUREMENT INFORMATION (continued)

TIMING DIAGRAMS



(1) Input pulse rise and fall time is 1 ns to 3 ns.

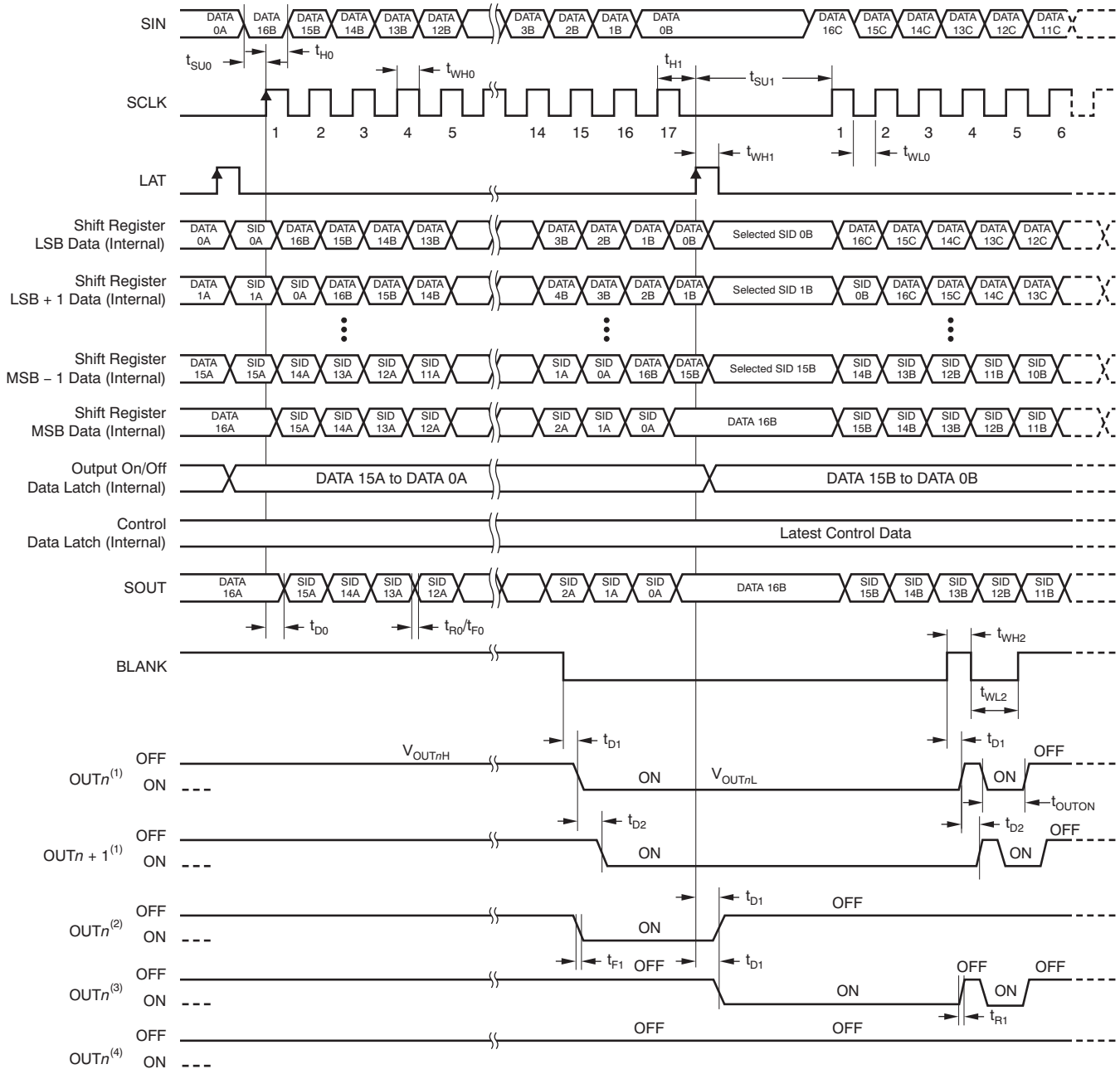
Figure 4. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 5. Output Timing

PARAMETER MEASUREMENT INFORMATION (continued)



(1) On/off latched data is '1'.

(2) On/off latched data change from '1' to '0' at second LAT signal.

(3) On/off latched data change from '0' to '1' at second LAT signal.

(4) On/off latched data is '0'.

Figure 6. Write for On/Off Data and Output Timing

PARAMETER MEASUREMENT INFORMATION (continued)

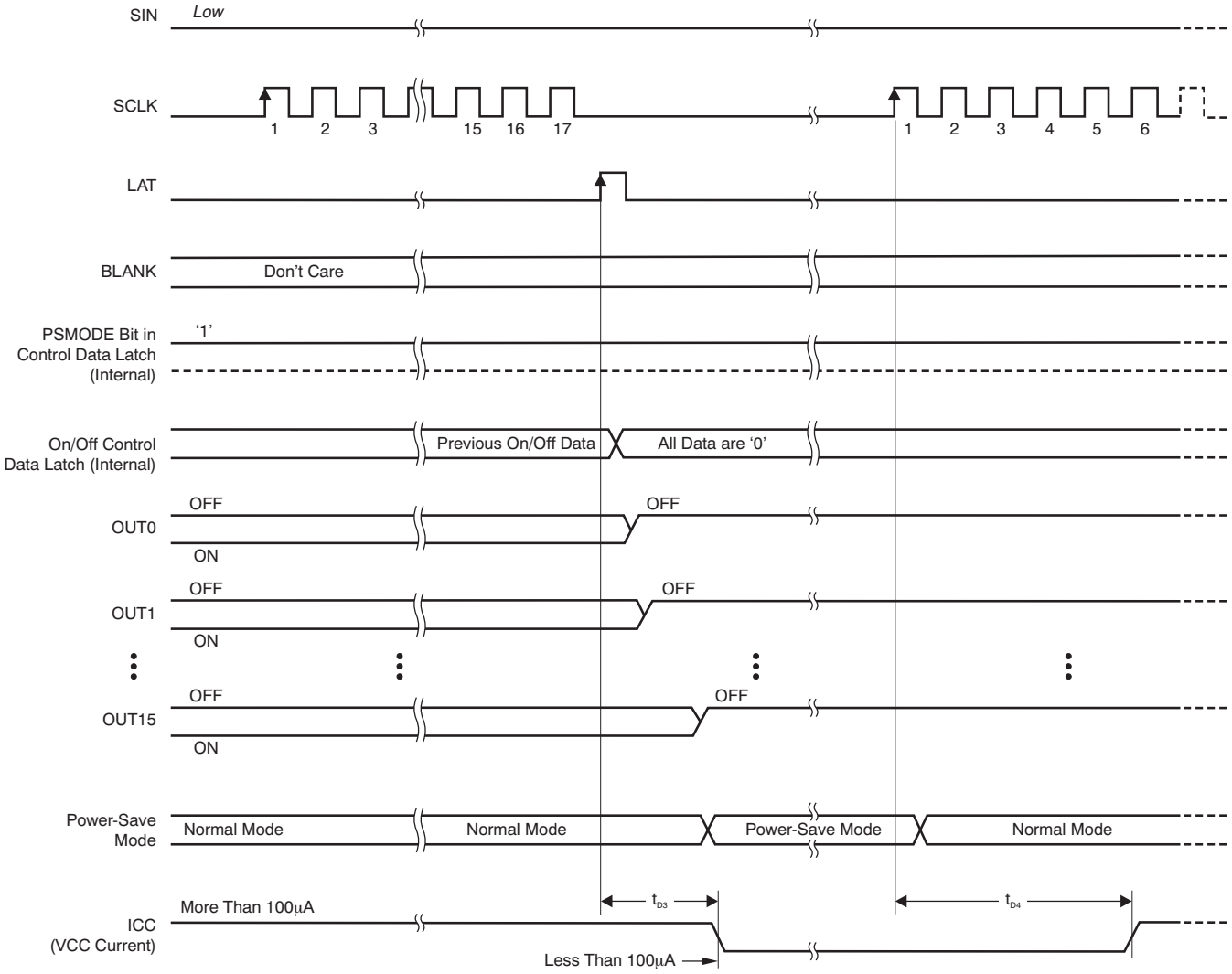
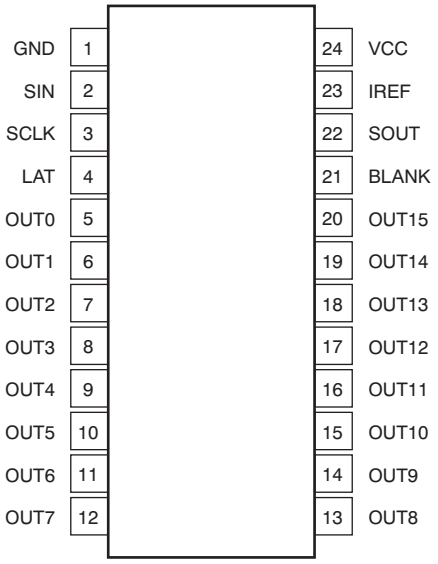


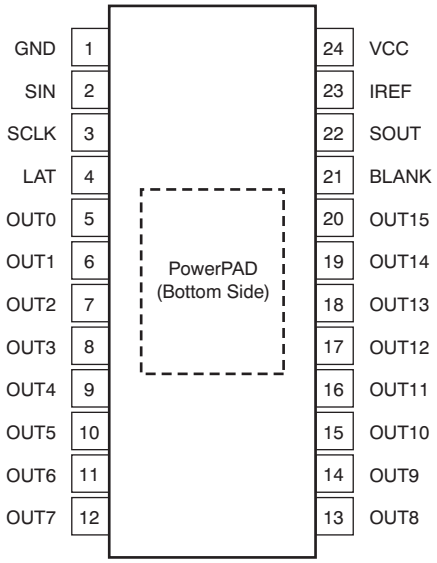
Figure 7. Power-Save Mode Timing

PIN CONFIGURATIONS

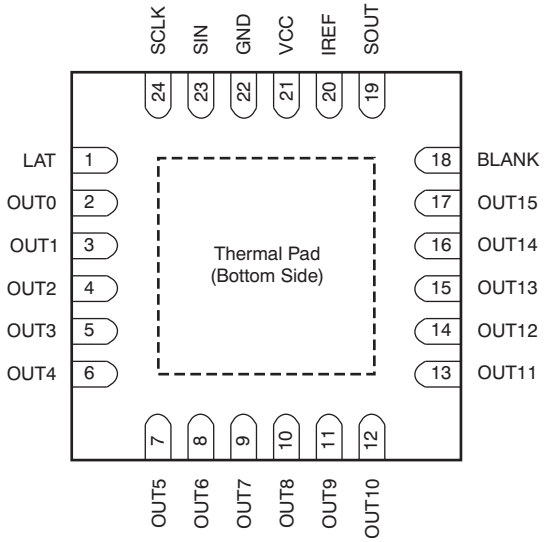
SSOP/QSOP-24
DBQ PACKAGE
(TOP VIEW)



HTSSOP-24
PWP PACKAGE
(TOP VIEW)



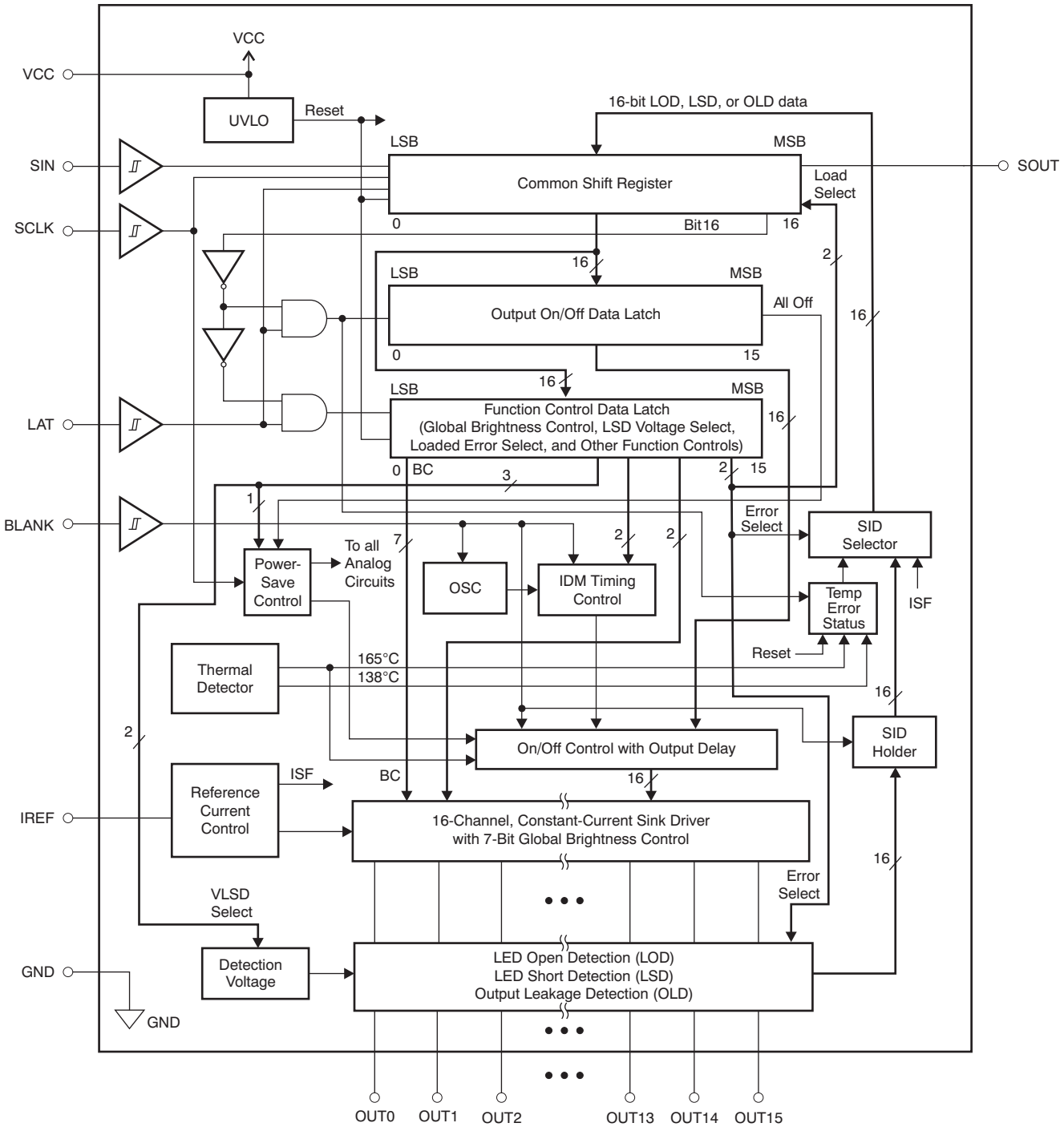
QFN-24
RGE PACKAGE
(TOP VIEW)



PIN DESCRIPTIONS

PIN			I/O	DESCRIPTION
NAME	DBQ/PWP	RGE		
BLANK	21	18	I	Blank all outputs. When BLANK is high, all constant-current outputs (OUT0 to OUT15) are forced off. When BLANK is low, all constant-current outputs are controlled by the on/off control data in the data latch.
GND	1	22	—	Ground
IREF	23	20	I/O	Maximum current programming terminal. A resistor connected between IREF and GND sets the maximum current for every constant-current output. When this terminal is directly connected to GND, all outputs are forced off. The external resistor should be placed close to the device and must be in the range of 1.32 kΩ to 66.0 kΩ.
LAT	4	1	I	Data latch. The rising edge of LAT latches the data from the common shift register into the output on/off data latch. At the same time, the data in the common shift register are replaced with SID, which is selected by SIDLD. See the *Output On/Off Data Latch* section and *Status Information Data (SID)* section for more details.
OUT0	5	2	O	Constant-current sink outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUT1	6	3	O	
OUT2	7	4	O	
OUT3	8	5	O	
OUT4	9	6	O	
OUT5	10	7	O	
OUT6	11	8	O	
OUT7	12	9	O	
OUT8	13	10	O	
OUT9	14	11	O	
OUT10	15	12	O	
OUT11	16	13	O	
OUT12	17	14	O	
OUT13	18	15	O	
OUT14	19	16	O	
OUT15	20	17	O	
SCLK	3	24	I	Serial data shift clock. Data present on SIN are shifted to the LSB of the 17-bit shift register with the SCLK rising edge. Data in the shift register are shifted toward the MSB at each SCLK rising edge. The MSB data of the common shift register appear on SOUT.
SIN	2	23	I	Serial data input for the 17-bit common shift register. When SIN is high, a '1' is written to the LSB of the common shift register at the rising edge of SCLK.
SOUT	22	19	O	Serial data output of the 17-bit common shift register. SOUT is connected to the MSB of the 17-bit shift register. Data are clocked out at the rising edge of SCLK.
VCC	24	21	—	Power-supply voltage

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

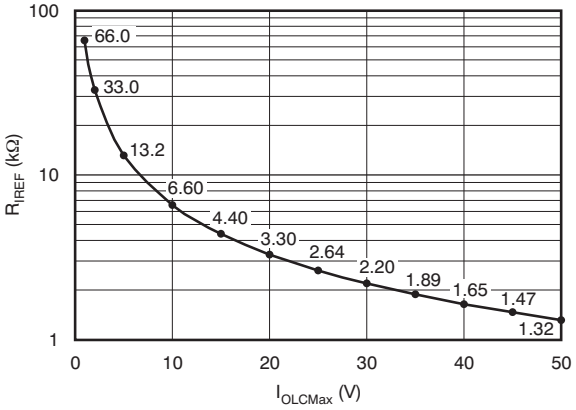


Figure 8.

OUT*n* CURRENT vs OUTPUT VOLTAGE (+3.3 V)

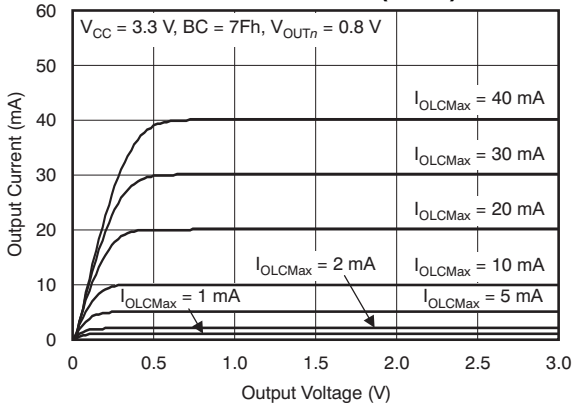


Figure 9.

OUT*n* CURRENT vs OUTPUT VOLTAGE (+3.3 V)

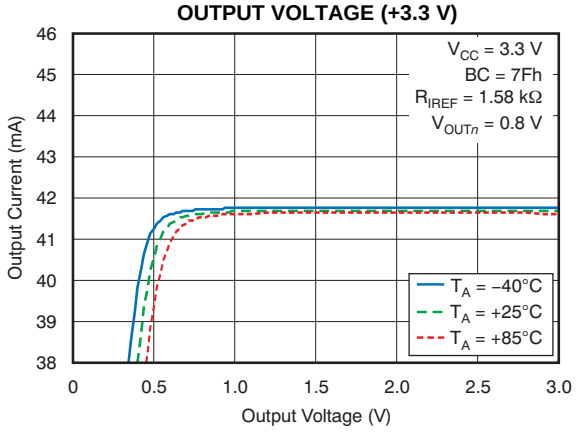


Figure 10.

OUT*n* CURRENT vs OUTPUT VOLTAGE (+5 V)

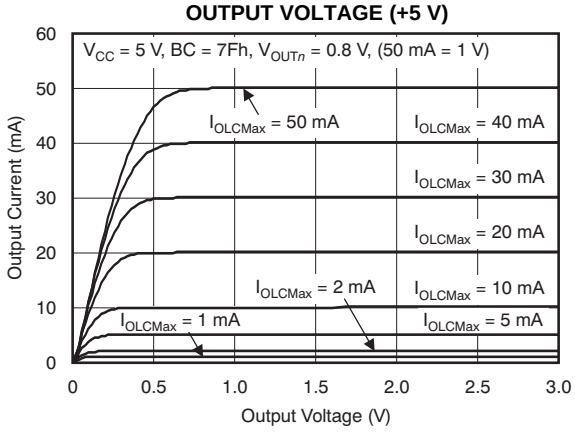


Figure 11.

OUT*n* CURRENT vs OUTPUT VOLTAGE (+5 V)

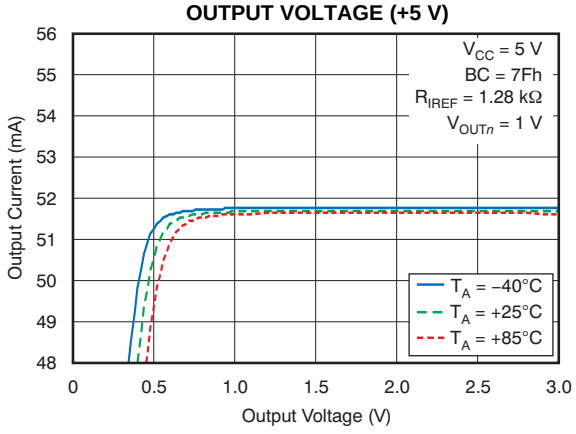


Figure 12.

CONSTANT-CURRENT ERROR vs OUTPUT CURRENT SET BY R_{IREF} or BC DATA (Channel-to-Channel)

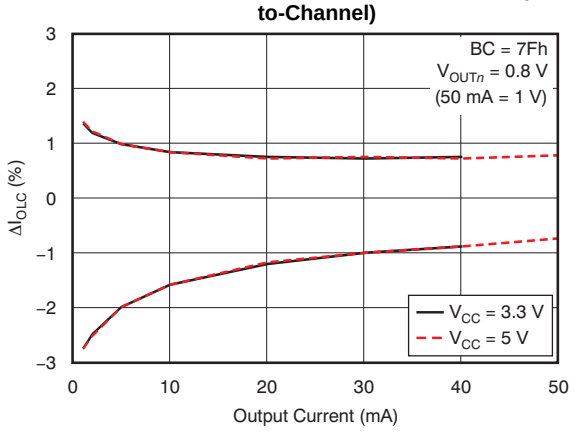


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

CONSTANT-CURRENT ERROR vs AMBIENT TEMPERATURE (Channel-to-Channel)

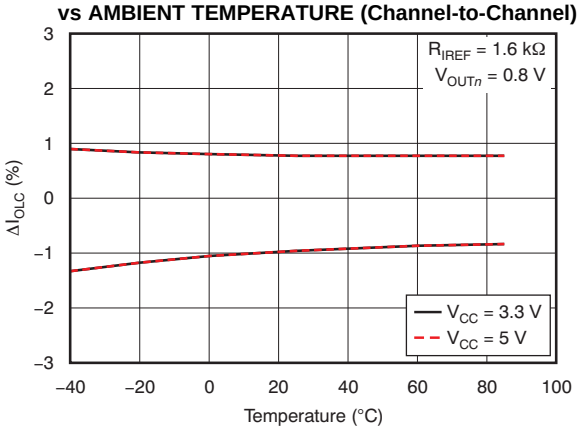


Figure 14.

GLOBAL BRIGHTNESS CONTROL LINEARITY

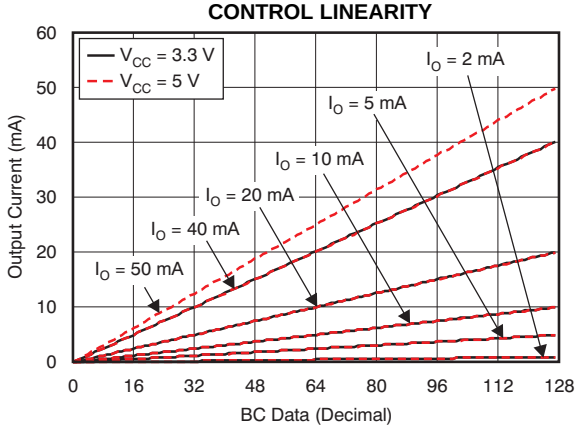


Figure 15.

SUPPLY CURRENT vs OUTPUT CURRENT SET BY R_{IREF}

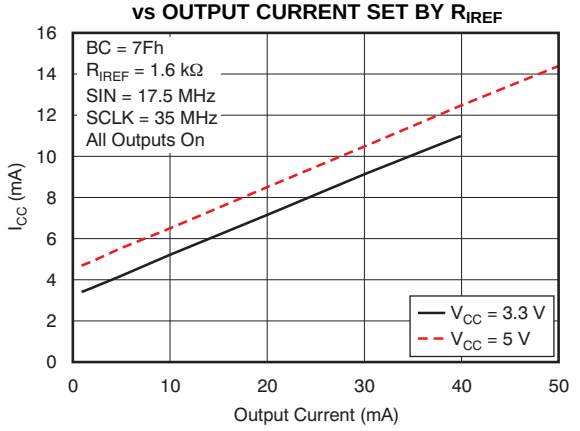


Figure 16.

SUPPLY CURRENT vs AMBIENT TEMPERATURE

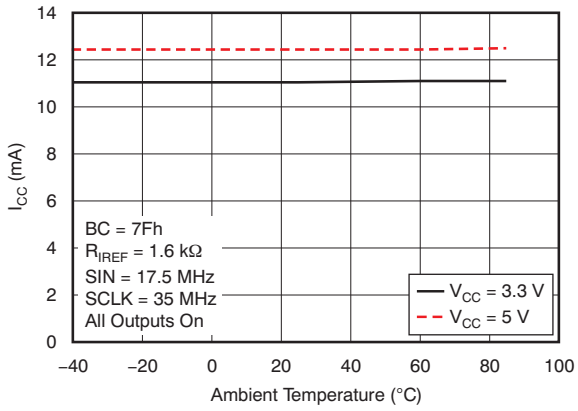


Figure 17.

SUPPLY CURRENT IN POWER-SAVE MODE vs AMBIENT TEMPERATURE

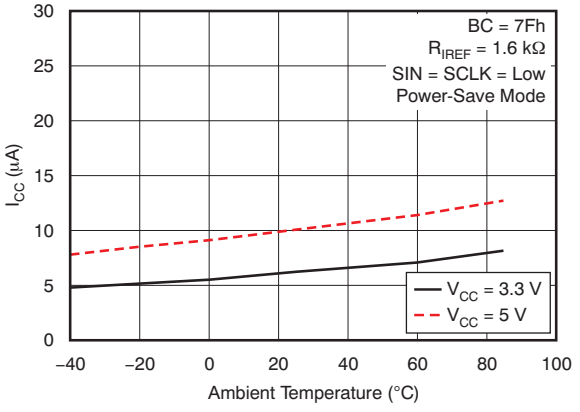


Figure 18.

CONSTANT-CURRENT OUTPUT VOLTAGE WAVEFORM

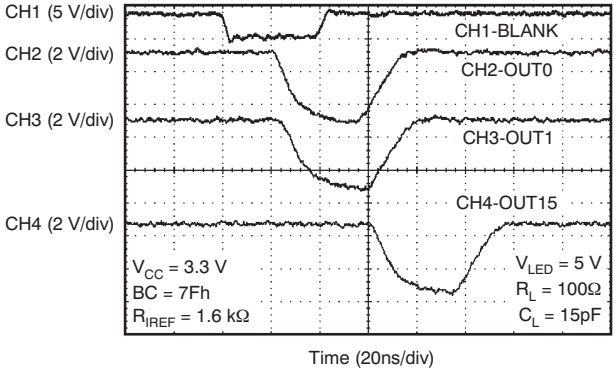


Figure 19.

DETAILED DESCRIPTION

MAXIMUM CONSTANT SINK CURRENT

The maximum output current of each channel (I_{OLCMax}) is programmed by a single resistor (R_{IREF}) that is placed between the IREF and GND pins. The current value can be calculated by Equation 1:

$$R_{IREF} = \frac{V_{IREF}}{I_{OLCMax}} \times 54.8 \quad (1)$$

Where:

V_{IREF} = the internal reference voltage on IREF (typically 1.205 V when the global brightness control data are at maximum.

I_{OLCMax} = 1 mA to 40 mA for $V_{CC} \leq 3.6$ V, or 1 mA to 50 mA for $V_{CC} > 3.6$ V at OUT0 to OUT15 with BC = 7Fh

I_{OLCMax} is the highest current for each output. Each output sinks I_{OLCMax} current when it is turned on with the maximum global brightness control (BC) data. Each output sink current can be reduced by lowering the global brightness control value. R_{IREF} must be between 1.32 kΩ and 66.0 kΩ in order to hold I_{OLCMax} between 50 mA (typ) and 1 mA (typ). Otherwise, the output may be unstable. Output currents lower than 1 mA can be achieved by setting I_{OLCMax} to 1 mA or higher and then using the global brightness control to lower the output current.

Figure 8 and Table 1 show the characteristics of the constant-current sink versus the external resistor, R_{IREF}.

Table 1. Maximum Constant Current Output versus External Resistor Value

I_{OLCMax} (mA)	R_{IREF} (kΩ, typ)
50 (V_{CC} > 3.6 V only)	1.32
45 (V_{CC} > 3.6 V only)	1.47
40	1.65
35	1.89
30	2.20
25	2.64
20	3.30
15	4.40
10	6.60
5	13.2
2	33.0
1	66.0

GLOBAL BRIGHTNESS CONTROL (BC) FUNCTION

The TLC5929 has the ability to adjust the output current of all constant current outputs simultaneously. This function is called *global brightness control* (BC). The global BC for all outputs (OUT0 to OUT15) can be set with a 7-bit word. The global BC adjusts all output currents in 128 steps from 0% to 100%. where 100% corresponds to the maximum output current set by R_{IREF}. Equation 2 calculates the actual output current. BC data can be set via the serial interface.

$$I_{OLCn}\,(mA) = \frac{I_{OLCMax}\,(mA) \times BC}{127} \quad (2)$$

Where:

I_{OLCMax} = the maximum constant-current value for each output determined by R_{IREF}.

BC = the global brightness control value in the control data latch (0h to 7Fh)

Table 2 shows the BC data versus the constant-current ratio against I_{OLCMAx}.

Table 2. BC Data versus Constant-Current Ratio Against I_{OLCMAx}

BC DATA			RATIO OF OUTPUT CURRENT TO I_{OLCMax} (%)	I_{OLC} (mA, I_{OLCMax}= 40mA, typ)	I_{OLC} (mA, I_{OLCMax}= 1mA, typ)
BINARY	DECIMAL	HEX			
000 0000	0	00	0	0	0
000 0001	1	01	0.8	0.31	0.01
000 0010	2	02	1.6	0.63	0.02
. . .	. . .	. . .	. . .	. . .	. . .
111 1101	125	7D	98.4	39.4	0.98
111 1110	126	7E	99.2	39.7	0.99
111 1111	127	7F	100.0	40.0	1.00

REGISTER AND DATA LATCH CONFIGURATION

The TLC5929 has one common shift register and two control data latches. The common shift register is 17-bits long and the two control data latches are 16-bits long. When the MSB of the common shift register is '0' and LAT shows a rising edge, the lower 16 bits of the common shift register are copied into the output on/off data latch. When the MSB is '1' and LAT shows a rising edge, the lower 16 bits are copied into the control data latch. Figure 20 shows the configuration of the common shift register and the two control data latches.

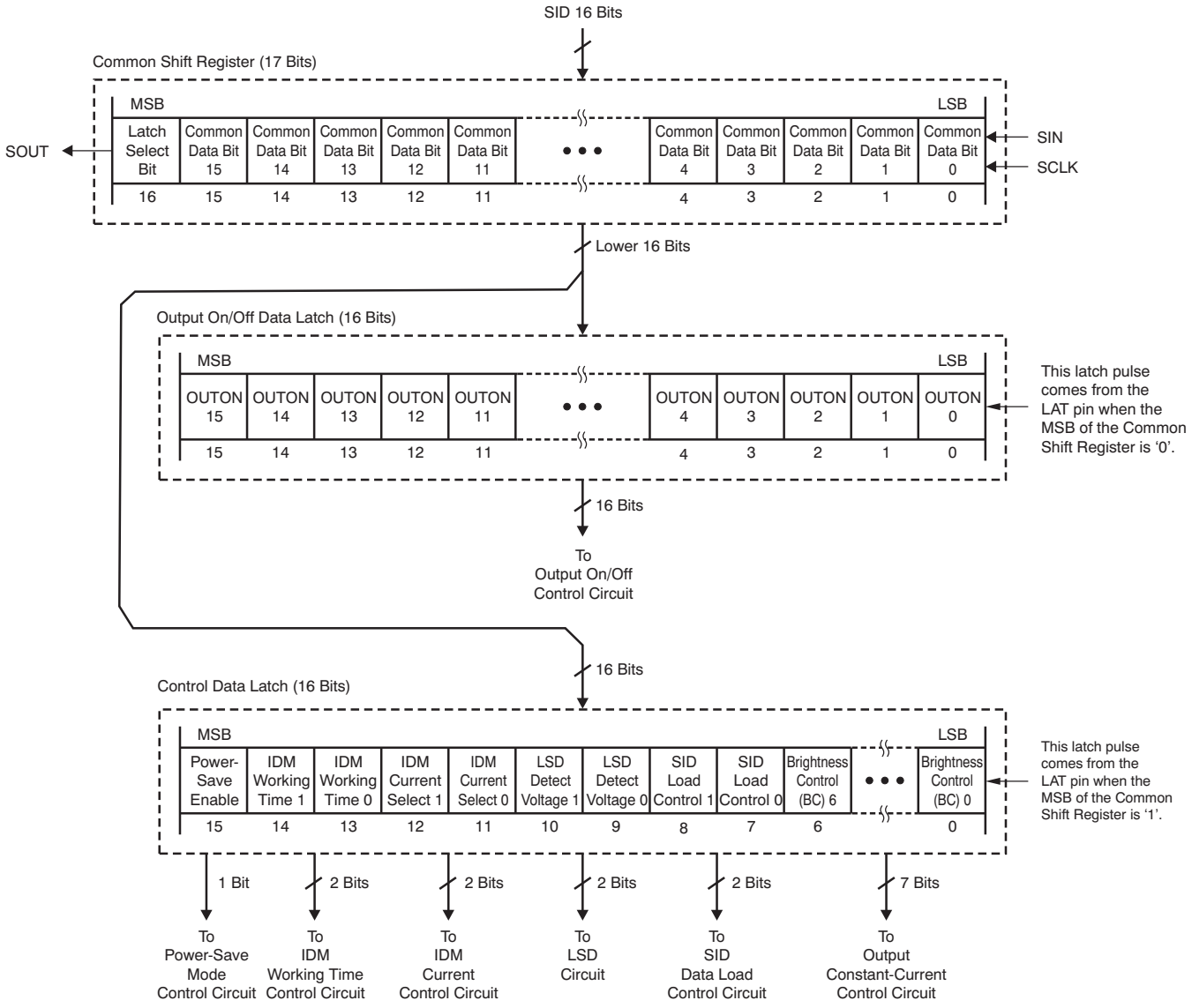


Figure 20. Common Shift Register and Control Data Latches Configuration

Common Shift Register

The 17-bit common shift register is used to shift data from the SIN pin into the TLC5929. The data shifted into the register are used for the output on/off control, global BC, and the control functions. The LSB of the common shift register is connected to SIN and the MSB is connected to SOUT. On each rising edge of SCLK, the data on SIN are shifted into the LSB and all 17 bits are shifted towards the MSB. The register MSB is always connected to SOUT.

In addition, the status information data (SID) selected by the load select data in the control data latch are loaded to the lower 16 bits of the common shift register when a rising edge is input on LAT and the MSB of the shift register is '0'.

When the device is powered on, all 17 bits of the common shift register are set to '0'.

Output On/Off Data Latch

The output on/off data latch is 16 bits long and sets the on or off status for each constant-current output.

When BLANK is low, the output corresponding to the specific bit in the output on/off data latch is turned on if the data is '1' and remains off if the data is '0'. When BLANK is high, all outputs are forced off, but the data in the latch do not change as long as LAT does not latch in new data.

When the device is powered on, all bits in the data latch are set to '0'.

The output on/off data latch configuration is shown in Figure 21 and the data bit assignment is shown in Table 3.

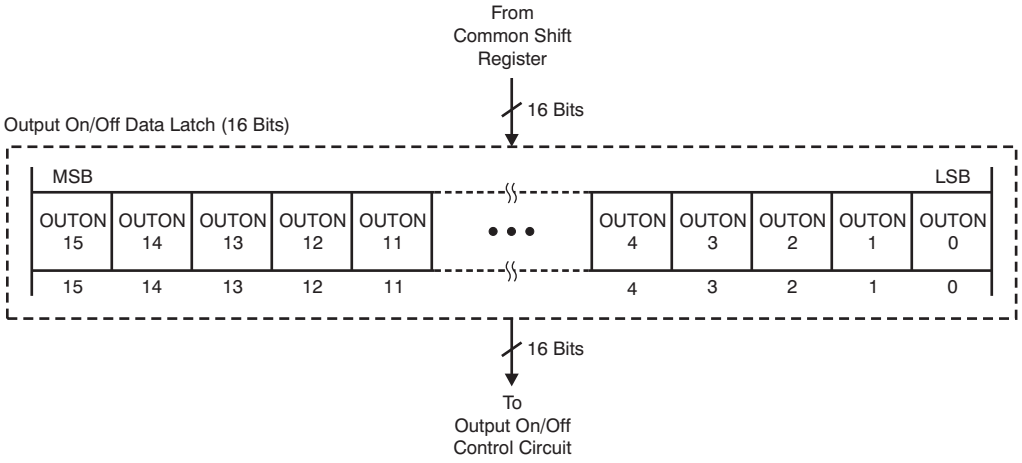


Figure 21. Output On/Off Data Latch Configuration

Table 3. On/Off Control Data Latch Bit Assignment

BIT NUMBER	BIT NAME	CONTROLLED CHANNEL	DESCRIPTION
0	OUTON0	OUT0	'0' = Output off '1' = Output on with BLANK low. When the device is powered on, all bits are set to '0'.
1	OUTON1	OUT1	
2	OUTON2	OUT2	
· · ·	· · ·	· · ·	
13	OUTON13	OUT13	
14	OUTON14	OUT14	
15	OUTON15	OUT15	

Function Control Data Latch

The function control data latch is 16 bits long and contains the global brightness control (BC) data, status information data (SID) load control data, LED short detection (LSD) voltage level data, the current value of the invisible detection mode (IDM), IDM working time, and power-save mode enable control data.

When the device is powered up, the data in this data latch are set to the default values shown in Table 4. This table contains the bit names, numbers and descriptions.

The function control data latch configuration is shown in Figure 22. Table 4 lists the bit descriptions.

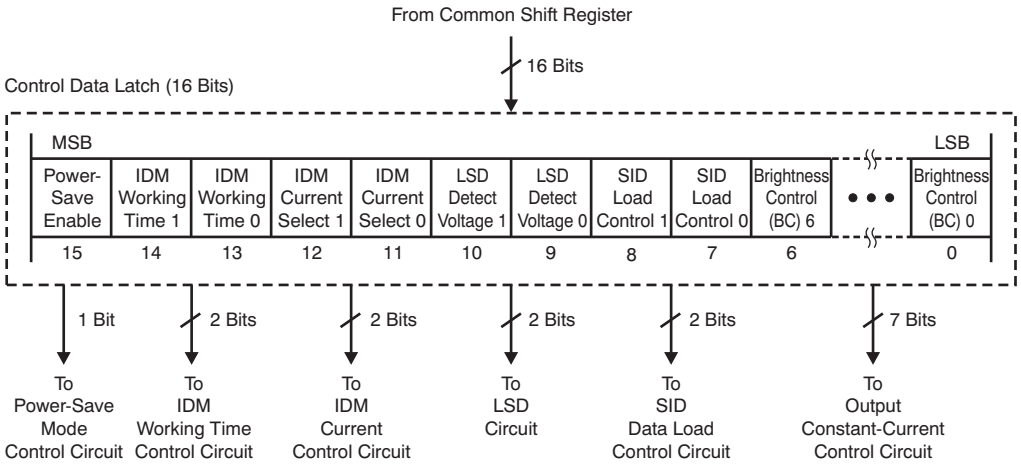


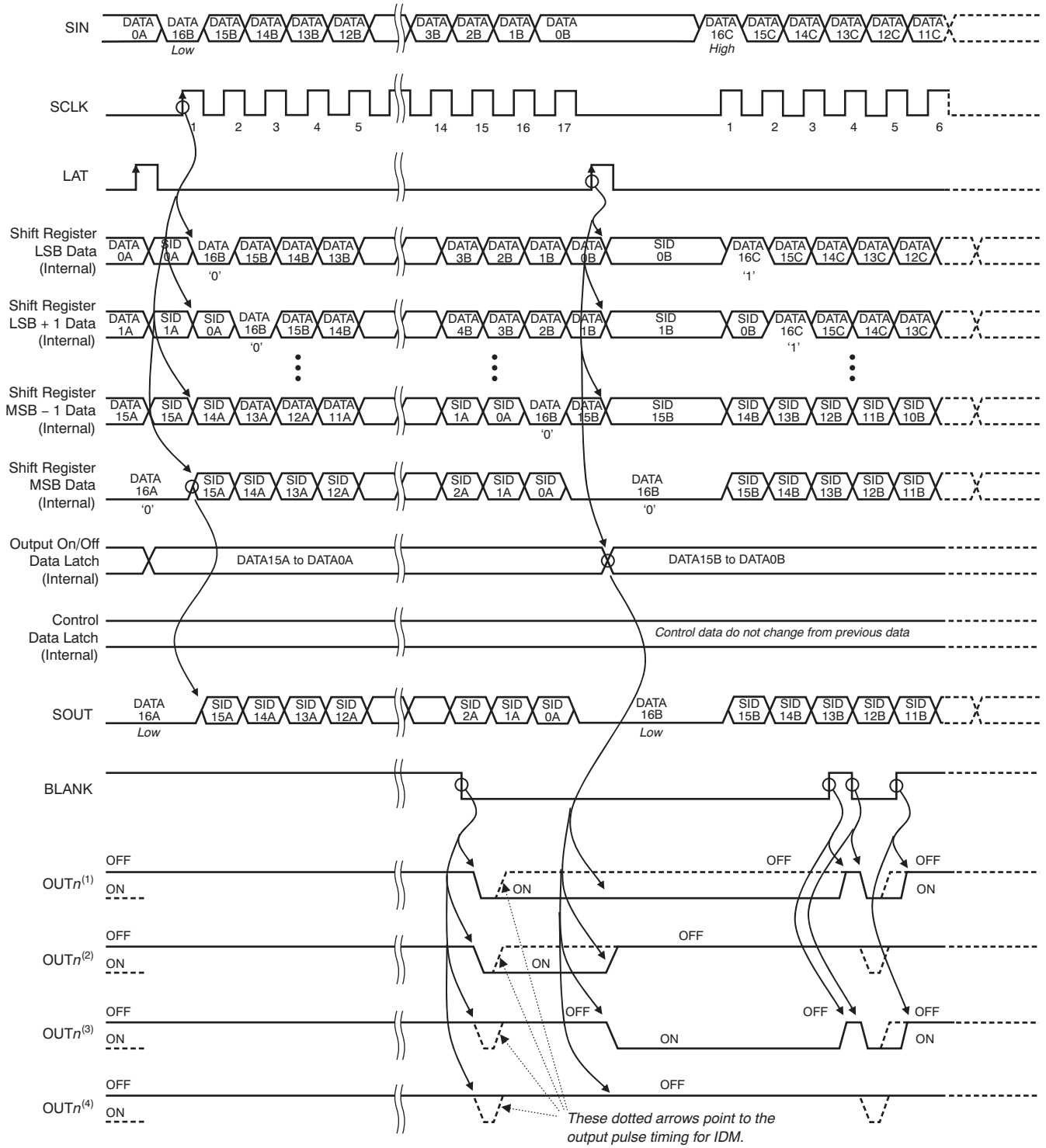
Figure 22. Function Control Data Latch Configuration

Table 4. Function Control Data Latch Bit Description

BIT NUMBER	BIT NAME	DEFAULT VALUE (BINARY)	DESCRIPTION
[6:0]	BCALL	1111111	Global brightness control. These seven bits control the current of all outputs with 128 steps between 0% to 100% of the maximum current value set by the external resistor. Table 2 shows the current value truth table.
[8:7]	SIDLD	00	SID load control. These two bits select the SID loaded to the common register when the LAT pulse is input for on/off data writing (MSB of the common shift register must be '0'). Table 6 shows the selected data truth table.
[10:9]	LSDVLT	11	LSD detection voltage select. These two bits select the detection threshold voltage for the LED short detection (LSD). Table 7 shows the detect voltage truth table.
[12:11]	IDMCUR	00	IDM current select. These two bits select the sink current at OUT*n* for the IDM to detect the LED open detection (LOD) or the LED short detection (LSD) without visible lighting. Table 8 shows the current value truth table. Figure 27 and Figure 28 show the IDM operation timing.
[14:13]	IDMTIM	11	IDM working time select. These two bits select the time of the IDMCUR output sink current at OUT*n* to detect the LED open detection (LOD) or LED short detection (LSD) without visible light. Table 9 shows the work-time truth table. Figure 27 and Figure 28 show the IDM operation timing.
[15]	PSMODE	1	Power save mode enable. This bit enables or disables the power-save mode. When the mode is enabled (PSMODE = '1'), the device goes into power-save mode if all data in the on/off data latch are '0'. Table 10 shows the power-save mode truth table. Figure 25 shows the power-save mode operation timing.

Output On/Off Data Write Timing and Output Control

When the 17-bit shift register MSB is '0', the output on/off data latch can be updated with the lower 16 bits of data in the shift register at the rising edge of the LAT signal, after the data are stored in the shift register using the SIN and SCLK signals. When the output on/off data latch is updated, SID (selected by the SIDLD bit) is loaded into the shift register, except when SIDLD = '00' (see Table 6). The output on/off data write timing is shown in Figure 23.



(1) On/off latch data is '1'.

(2) On/off latch data change from '1' to '0' at second LAT signal.

(3) On/off latch data is change from '0' to '1' at second LAT signal.

(4) On/off latch data is '0'.

Figure 23. On/Off Data Write Timing

Function Control Data Writing

When the MSB is 1' in the 17-bit shift register, the control data latch can be updated with the lower 16 bits of data in the shift register at the rising edge of the LAT signal after the data are stored to the shift register using the SIN and SCLK signals. When the control data latch is updated, SID is not loaded into the shift register. The function control data write timing is shown in Figure 24.

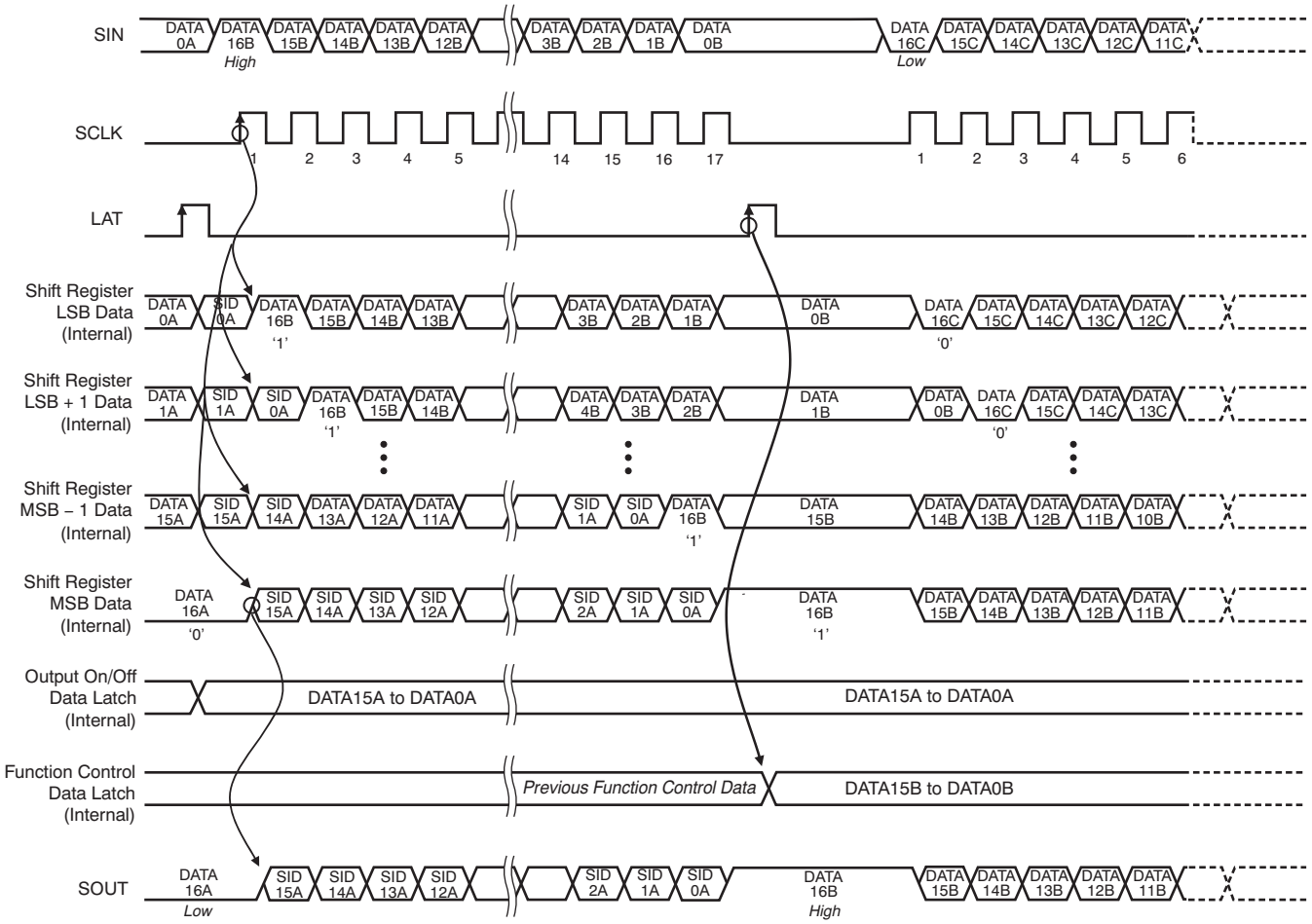


Figure 24. Function Control Data Write Timing

Function Control Data Bit Assignment

The function control data latch is 16 bits long and is used to adjust the output current values for LED brightness, SID selection, LSD voltage level, output current for IDM, output on-time for IDM, and power-save mode enable/disable. When the device powers on, the function control data latch is set to the default value (E67Fh). The function control data latch truth tables are shown in Table 5 through Table 10.

Table 5. Global Brightness Control (BC) Truth Table

BCALL BITS[6:0]	DESCRIPTION
0000000	Output current of OUT*n* is set to I_{OLCMax} × 0%
0000001	I_{OLCMax} × 0.8%
. . .	. . .
1111110	I_{OLCMax} × 99.2%
1111111	I_{OLCMax} × 100% (default value)

Table 6. SID Load Control Truth Table (see Table 11 for more details)

SIDLD		
BIT 8	BIT 7	STATUS INFORMATION DATA (SID) LOADED TO THE COMMON SHIFT REGISTER
0	0	No data is loaded (default value)
0	1	LED open detection (LOD) or thermal error flag (TEF) data are loaded
1	0	LED short detection (LSD) or pre-thermal warning (PTW) data are loaded
1	1	Output leakage detection (OLD) or IREF pin short flag (ISF) data are loaded

Table 7. LSD Threshold Voltage Truth Table

LSDVLT		
BIT 10	BIT 9	LED SHORT DETECTION (LSD) THRESHOLD VOLTAGE
0	0	V_{LSD0} (0.35 × V_{CC} typ)
0	1	V_{LSD1} (0.45 × V_{CC} typ)
1	0	V_{LSD2} (0.55 × V_{CC} typ)
1	1	V_{LSD3} (0.65 × V_{CC} typ, default value)

Table 8. Current Select for IDM

IDMCUR		
BIT 12	BIT 11	SINK CURRENT AT OUT*n* FOR INVISIBLE DETECTION MODE (IDM)
0	0	IDM is disabled (default value)
0	1	2 µA (typ)
1	0	10 µA (typ)
1	1	20 µA (typ)

Table 9. IDM Work-Time Truth Table

IDMTIM		
BIT 14	BIT 13	INVISIBLE DETECTION MODE (IDM) WORKING TIME
0	0	All outputs are turned on for 17 OSC clocks (0.85 µs typ)
0	1	All outputs are turned on for 33 OSC clocks (1.65 µs typ)
1	0	All outputs are turned on for 65 OSC clocks (3.25 µs typ)
1	1	All outputs are turned on for 129 OSC clocks (6.45 µs typ, default value)

Table 10. Power-Save Mode Truth Table

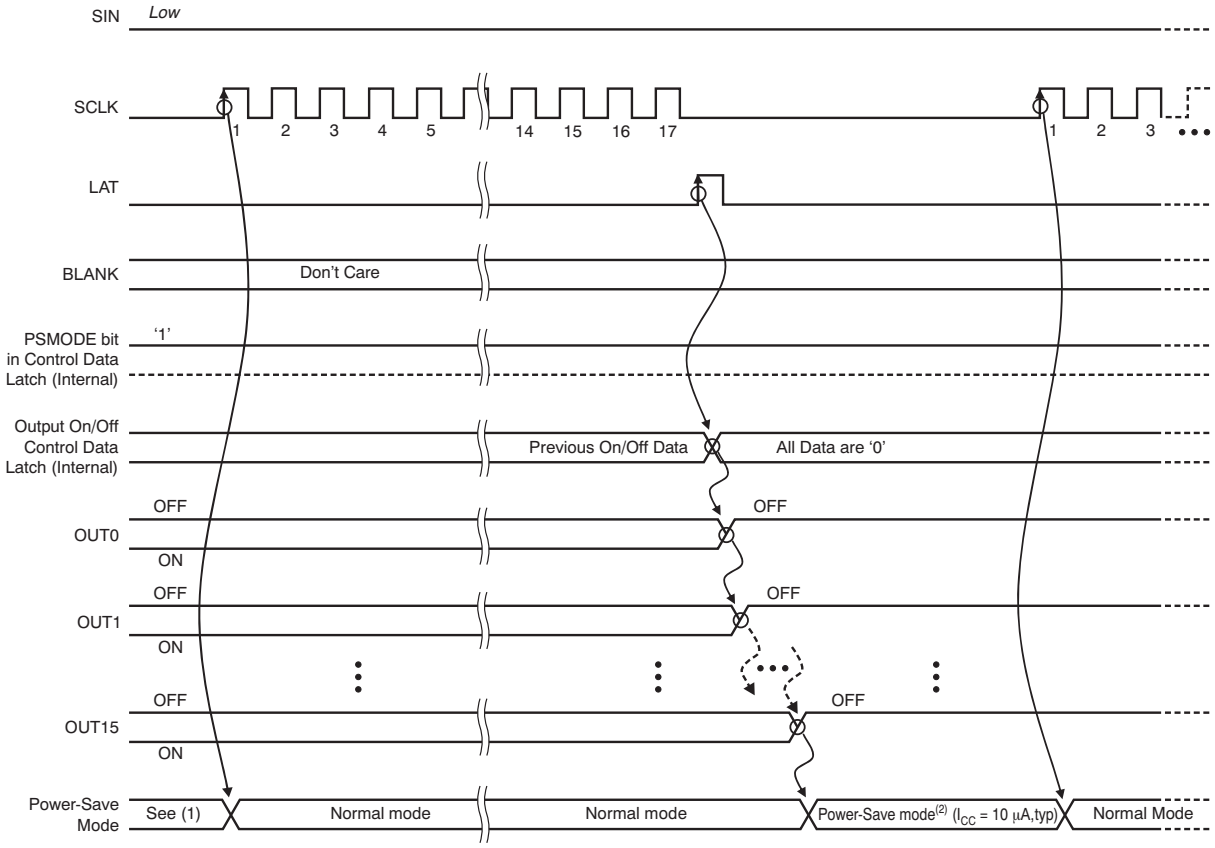
PSMODE	POWER-SAVE MODE FUNCTION
BIT 15	
0	Power-save mode is disabled. The device does not go into power-save mode even if the bits in the output on/off data latch are all '0'.
1	Power save mode is enabled (default value). The device goes into power-save mode when the bits in the output on/off data latch are all '0'.

Table 11. SID Load Assignment

SIDLD BIT (BINARY)	SELECTED DETECTOR	CHECKED OUT*n*	BIT NUMBER LOADED INTO COMMON SHIFT REGISTER	DESCRIPTION
00	No detector selected	—	No data loaded	The data in the common shift register are not changed.
01	LED open detection (LOD)	OUT0	0	The data in the common shift register are updated with LOD or TEF data.
		OUT1	1	All bits '1' = device junction temperature (T_J) is very high ($T_J > T_{TEF}$) and all outputs are forced off by the thermal shutdown function.
		· · ·	· · ·	
		OUT14	14	'1' = OUT*n* shows lower voltage than the LED open detection threshold (V_{LOD}).
		OUT15	15	'0' = normal operation.
10	LED short detection (LSD)	OUT0	0	The data in the common shift register are updated with LSD or PTW data.
		OUT1	1	All bits '1' = device junction temperature (T_J) is high ($T_J > T_{PTW}$).
		· · ·	· · ·	
		OUT14	14	'1' = OUT*n* shows higher voltage than the LED short detection threshold (V_{LSD}) selected by LSDVLT.
		OUT15	15	'0' = normal operation.
11	Output leakage detection (OLD)	OUT0	0	The data in the common shift register are updated with OLD or ISF data.
		OUT1	1	All bits '1' = IREF pin is shorted to GND with low impedance.
		· · ·	· · ·	'1' = OUT*n* is leaking to GND with greater than 3μA.
		OUT14	14	'0' = normal operation.
		OUT15	15	

POWER-SAVE MODE

In power-save mode, the TLC5929 input current becomes 10 µA (typ). When the PSMODE bit in the control data latch is '1', power-save mode is enabled. If the rising edge of LAT writes '0' into all bits of the output on/off data latch or any data into the control data latch with all bits of the on/off data latch being '0', the TLC5929 goes into power-save mode. The device stays in power-save mode until the next rising edge on SCLK is received. The power-save mode timing is shown in Figure 25.



(1) Contents depend on output on/off data.

(2) When PSMODE bit is '0', the device does not go into power-save mode even if the output on/off data is all '0'.

(3) Because it takes 20 µs (max) to return to normal mode, the first SCLK rising edge should be input at least 20 µs before OUT*n* is enabled.

Figure 25. Power-Save Mode Timing

LED OPEN DETECTION (LOD)

LOD detects a fault caused by an open circuit in the *n*th LED string, or a short from OUT*n* to ground, by comparing the OUT*n* voltage to the LOD detection threshold voltage level (V_{LOD} = 0.3 V, typ). If the OUT*n* voltage is lower than V_{LOD}, that output LOD bit is set to '1' to indicate an open LED string. Otherwise, the LOD bit is set to '0'. LOD data are only valid for outputs that are programmed to be enabled. LOD data for outputs that are programmed to be disabled are always '0' (see Table 11), except when IDM is enabled.

The LOD data are stored in a 16-bit register called SID holder (see the *Functional Block Diagram*) at the rising edge of BLANK when the SIDLD bits are set to '01' (see Table 6). However, when the IDM is enabled, the LOD bits are stored in the SID holder at the end of the IDM working time selected by IDMTIM (see Table 9).

The stored LOD data can be read out through the common shift register as SID at the SOUT pin. LOD/LSD data are not valid for 0.5 µs after the output is turned on.

When the device resumes operation from power-save mode, the LOD cannot be executed before the propagation delay (t_{D4}) has elapsed because LOD does not work during power-save mode.

LED SHORT DETECTION (LSD)

The LSD data are stored into a 16-bit register called SID holder at the rising edge of BLANK when the SIDLD bits are set to '10' (see Table 6) or when IDM is enabled. The LSD bits are stored in the SID holder at the end of the IDM working time (IDMTIM). The stored LSD data can be read out through the common shift register as SID at the SOUT pin. Note that the LOD/LSD bits are not stable during the first 0.5 µs after the falling edge of BLANK.

LSD data detect a fault caused by a shorted LED by comparing the OUT*n* voltage to the LSD detection threshold voltage level set by LSDVLT in the control data latch (see Table 4 and Table 7). If the OUT*n* voltage is higher than the programmed voltage, the corresponding output LSD bit is set to '1' to indicate a shorted LED. Otherwise, the LSD bit is set to '0'. LSD data are only valid for outputs that are programmed to be enabled. LSD data for outputs that are programmed to be disabled are always '0' (see Table 11), except when IDM is enabled. When the device resumes operation from the power-save mode, LSD cannot be executed before the propagation delay (t_{D4}) has elapsed because LSD does not work during power-save mode.

INVISIBLE DETECTION MODE (IDM)

Invisible detection mode (IDM) can detect LOD and LSD even when the output on/off data are set to the off state. When the IDMCUR bits in the control data latch are set to any value except '00', all outputs start sinking the current set by the IDMCUR bits at the falling edge of BLANK and stop sinking the current at the rising edge of BLANK, or the time set by IDMTIM has elapsed. When OUT*n* stops, the selected SID data by SIDLD bits are latched into the SID holder.

When the IDMCUR bits in the control data latch are set to '00', IDM is disabled.

Figure 26 shows the LOD/LSD/OLD/IDM circuits. Figure 27 and Figure 28 illustrate the IDM operation timing and Table 12 shows a truth table for LOD/LSD/OLD.

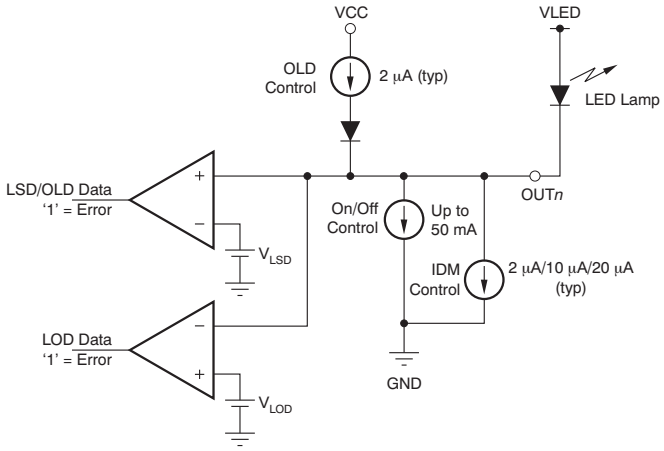


Figure 26. LOD/LSD/OLD/IDM Circuit

Table 12. LOD/LSD/OLD Truth Table

LOD	LSD	OLD	CORRESPONDING BIT IN SID
LED is not opened ($V_{OUTn} > V_{LOD}$)	LED is not shorted ($V_{OUTn} \le V_{LSD}$)	OUT*n* does not leak to GND ($V_{OUTn} > V_{LSD}$ when constant-current output off and OUT*n* source current on)	0
LED is open or shorted to GND ($V_{OUTn} \le V_{LOD}$)	LED is shorted between anode and cathode, or shorted to higher voltage side ($V_{OUTn} > V_{LSD}$)	Current leaks from OUT*n* to internal GND, or OUT*n* is shorted to external GND with high impedance ($V_{OUTn} \le V_{LSD}$ when constant-current output off and OUT*n* source current on)	1

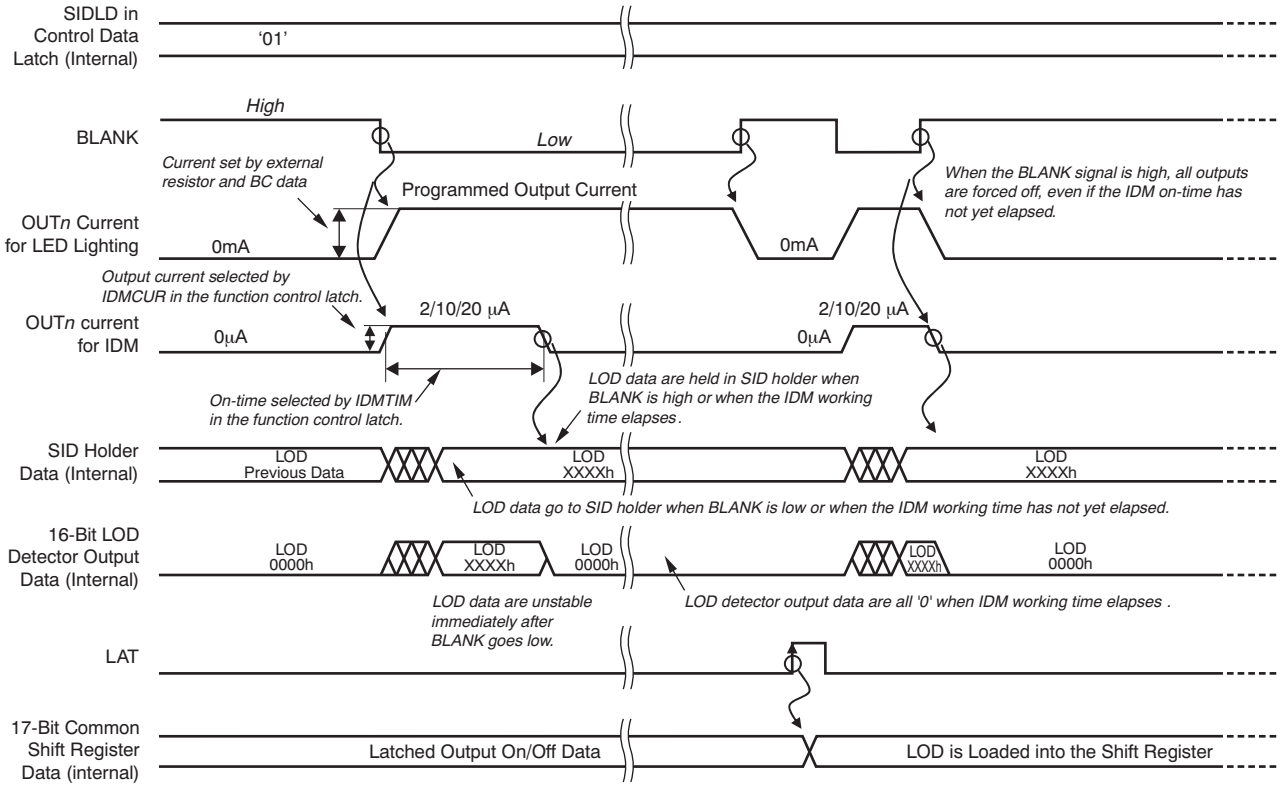


Figure 27. IDM Operation Timing with LOD Selected and IDM Enabled

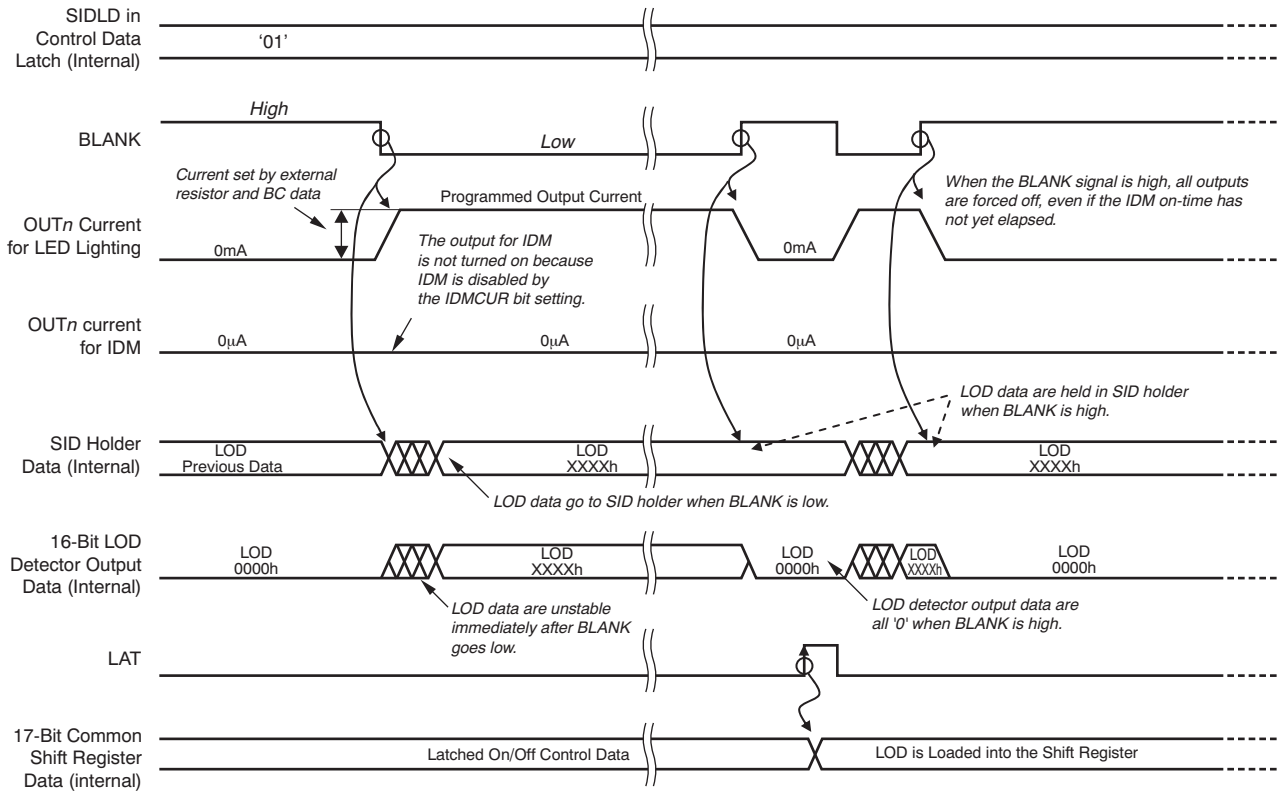


Figure 28. IDM Operation Timing with LOD Selected and IDM Disabled

OUTPUT LEAKAGE DETECTION (OLD)

When IDM mode is enabled, OLD is always disabled.

Output leakage detection (OLD) detects a fault caused by a short with high resistance from OUT*n* to GND by comparing the OUT*n* voltage to the LSD detection threshold voltage when the output on/off data are set to the off state. OLD can also detect a short between adjacent pins. A very small current is sourced from the turned-off OUT*n* to detect leaking when the SIDLD bits are '11' and BLANK is low. OLD operation is disabled when the SIDLD bits are set to any value except '11', and then the current source is stopped. If the OUT*n* voltage is lower than the programmed LSD threshold voltage, the corresponding OLD bit is set to '1' to indicate a leaking LED. Otherwise, the OLD bit is set to '0'. The OLD result is valid for disabled outputs only. The OLD data are latched into the SID holder when BLANK goes high. The OLD bits of the enabled outputs are always '0'. When the device resumes operation from power-save mode, OLD cannot be executed until after the propagation delay (t_{D4}) has elapsed because OLD does not work during power-save mode.

STATUS INFORMATION DATA (SID)

The status information data (SID) contains the status of the LED open detection (LOD), LED short detection (LSD), output leakage detection (OLD), pre-thermal warning (PTW), thermal error flag (TEF), and IREF short flag (ISF), depending on the SIDLD bits in the control data latch. When the MSB of the common shift register is set to '0', the selected SID overwrite the lower 16 bits in the common shift register at the rising edge of LAT after the data in the common shift register are copied to the output on/off data latch. If the MSB of the common shift register is '1', the data in the common shift register do not change.

After being copied into the common shift register, new SID data are not available until new data are written into the common shift register. If new data are not written, the LAT signal is ignored. To recheck SID without changing the on/off control data, reprogram the common shift register with the same data currently programmed into the on/off data latch. When LAT goes high, the output on/off data do not change, but new SID data are loaded into the common shift register. LOD, LSD, OLD, PTW, TEF, and ISF are shifted out of SOUT with each rising edge of SCLK.

The SID reading must be delayed for a duration of t_{D4} or more after the device resumes operation from the power-save mode because SID does not indicate correct data during the power-save mode. The SID load configuration and SID read timing are shown in Figure 29 and Figure 30, respectively.

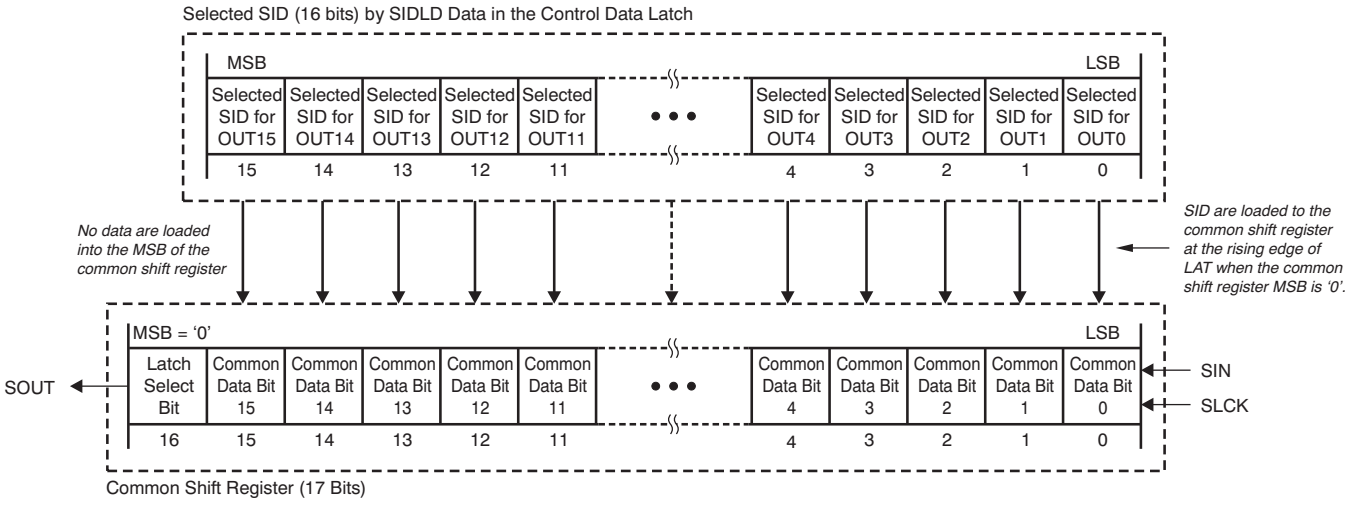


Figure 29. SID Load Configuration

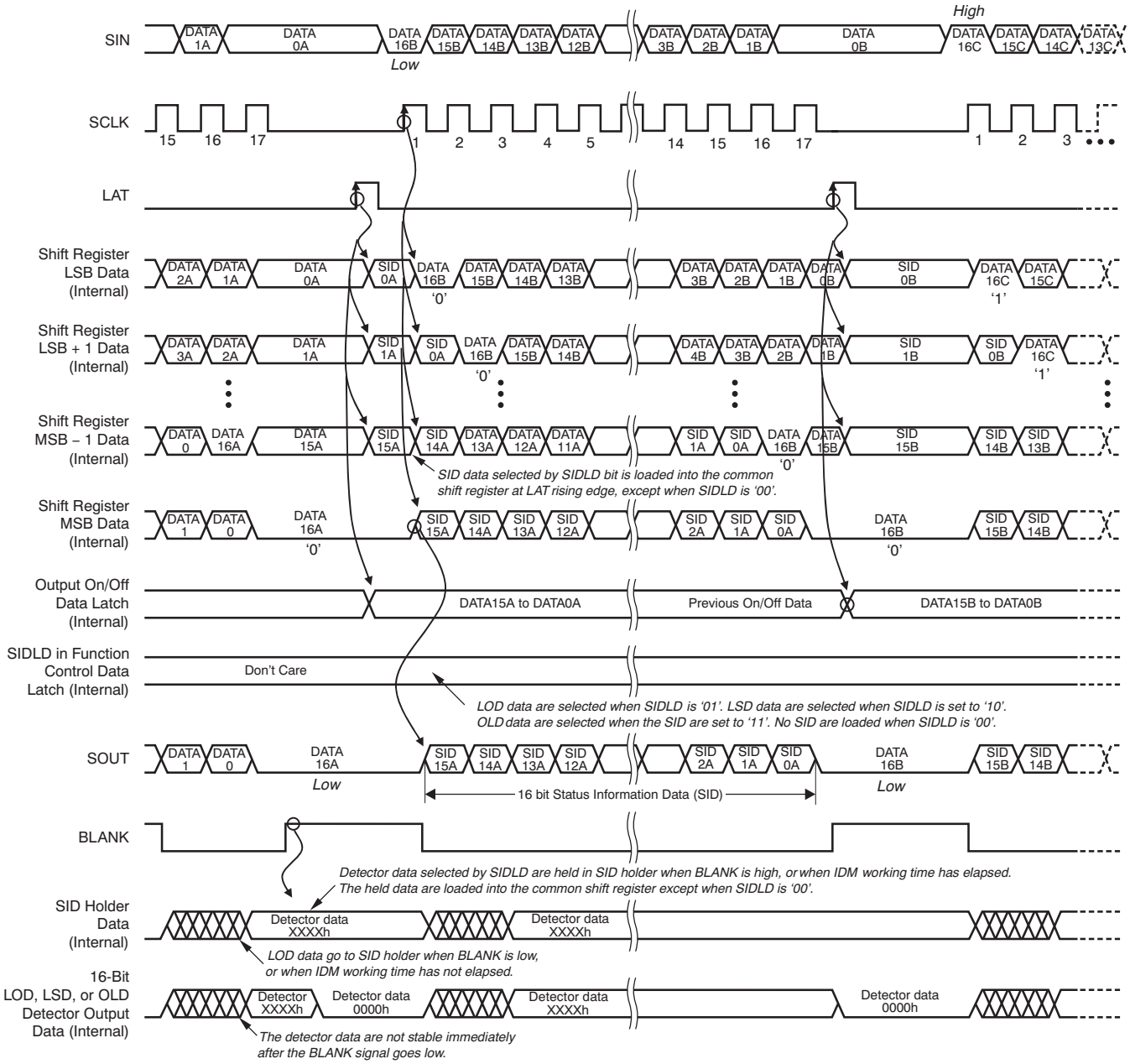


Figure 30. SID Read Timing

THERMAL SHUTDOWN (TSD) AND THERMAL ERROR FLAG (TEF)

The thermal shutdown (TSD) function turns off all constant-current outputs when the junction temperature (T_J) exceeds the threshold (T_{TEF} = +165°C, typ) and sets all LOD data bits to '1'. When the junction temperature drops below (T_{TEF} – T_{HYST}), the output control starts normally. The TEF remains '1' until the next rising edge on LAT even if the temperature drops below the low level. Figure 31 shows the timing diagram and Table 13 shows the truth table for TEF.

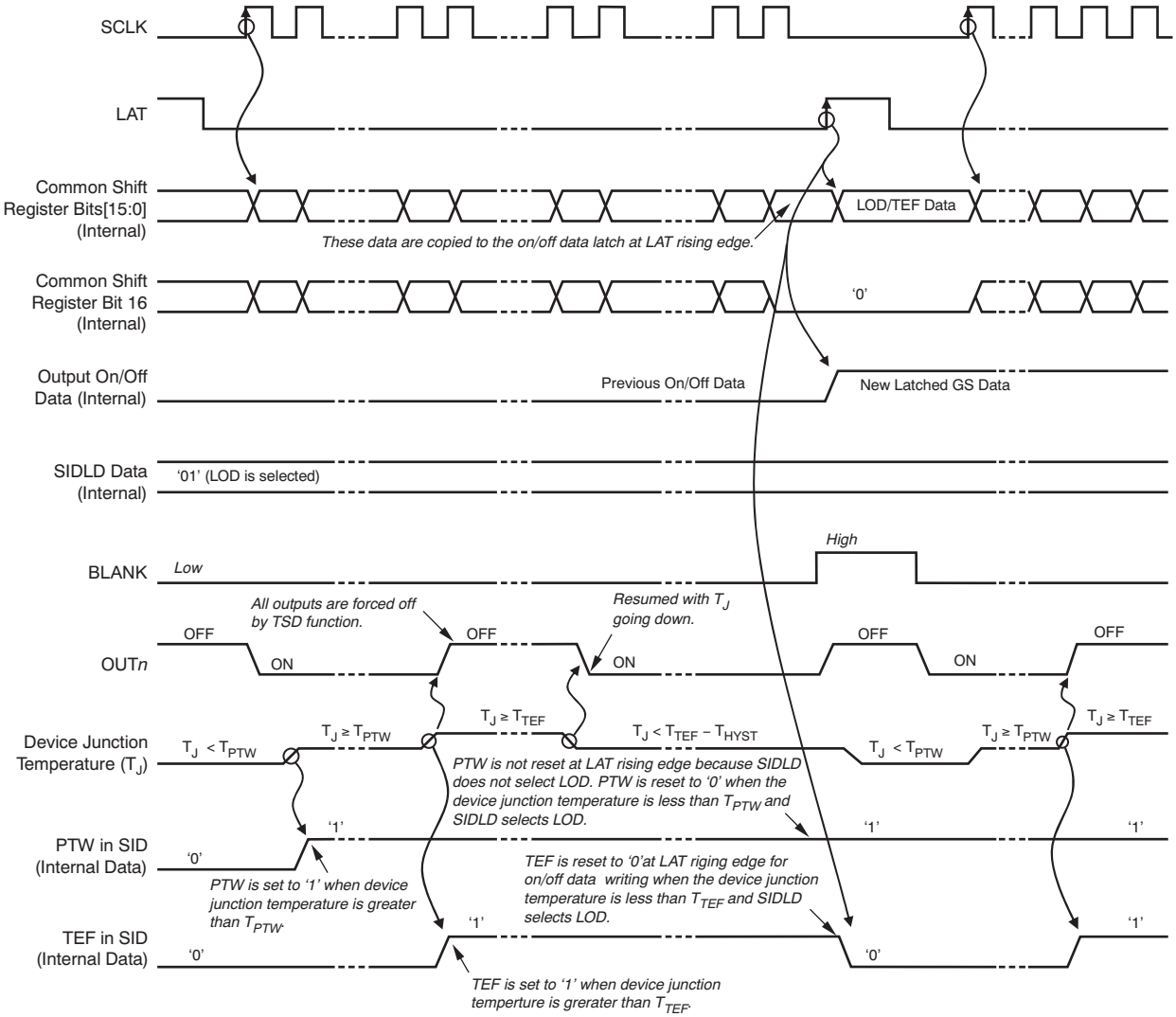


Figure 31. TEF/PTW/ISF Timing (LOD selected)

Table 13. TEF/PTW/ISF Truth Table

TEF	PTW	ISF	CORRESPONDING DATA BITS IN SID
Device temperature is lower than high-side detect temperature (temperature ≤ T_{TEF})	Device temperature is lower than pre-thermal warning temperature (temperature ≤ T_{PTW})	IREF terminal is not shorted	Depends on LOD/LSD/OLD
Device temperature is higher than high-side detect temperature and all outputs are forced off (temperature >T_{TEF})	Device temperature is higher than pre-thermal warning temperature (temperature > T_{PTW})	IREF terminal is shorted to GND with low impedance and all outputs (OUT0 to OUT15) are forced off	SID is all 1s for TEF when SIDLD bit = '01'. SID is all 1s for PTW when SIDLD = '10'. SID is all 1s for ISF when SIDLD = '11'.

PRE-THERMAL WARNING (PTW)

The PTW function indicates that the device junction temperature is high. The PTW is set and all LSD data bits are set to '1' while the device junction temperature exceeds the temperature threshold (T_{PTW} = +138°C, typ); however, the outputs are not forced off. When the PTW indicates a high temperature, the device temperature should be reduced by lowering the power dissipated in the driver to avoid a forced shutdown by the thermal shutdown circuit. This reduction can be accomplished by lowering the values of the BC data or the LED supply voltage. The PTW remains '1' until the next rising edge on LAT, even if the temperature drops below T_{PTW}. Figure 31 shows a timing diagram and Table 13 shows the truth table for PTW.

CURRENT REFERENCE (IREF PIN) SHORT FLAG (ISF)

The ISF function indicates that the IREF pin is shorted with low impedance to GND. When ISF is set, all OLD data bits are set to '1'. Then all outputs (OUT*n*) are forced off and remain off until the short is removed. Table 13 shows the truth table for ISF.

NOISE REDUCTION

Large surge currents may flow through the device and the board on which the device is mounted if all 16 outputs turn on simultaneously when BLANK goes low or on/off data change at the LAT rising edge with BLANK low. These large current surges could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5929 turns the outputs on with a 2-ns series delay for each output in order to provide a circuit soft-start feature.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2011) to Revision B **Page**

- Deleted application bullet 1
- Updated text in Table 6 (typo) 22

Changes from Original (April 2011) to Revision A **Page**

- 为恒定电流准确特性添加的最大值 1
- Added new RGE (QFN-24) package to Package/Ordering Information table 2
- Added new RGE (QFN-24) package to Thermal Information table 2
- Added new RGE (QFN-24) pinout 10
- Added new RGE (QFN-24) package to Pin Descriptions table 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5929DBQ	ACTIVE	SSOP	DBQ	24	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5929	Samples
TLC5929DBQR	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5929	Samples
TLC5929PWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PJ5929	Samples
TLC5929PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PJ5929	Samples
TLC5929RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5929	Samples
TLC5929RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5929	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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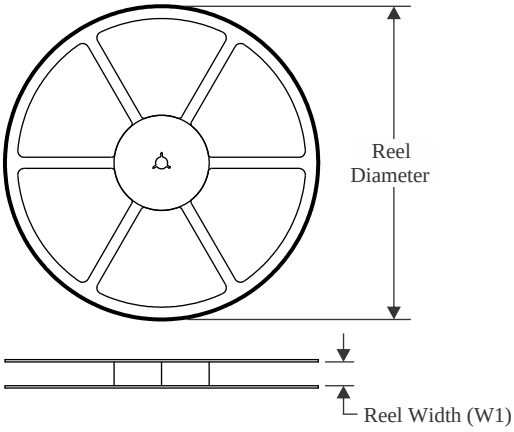
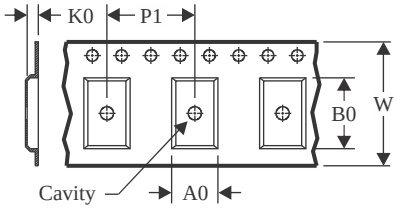
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

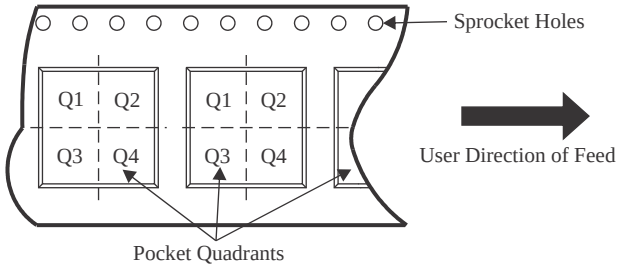


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

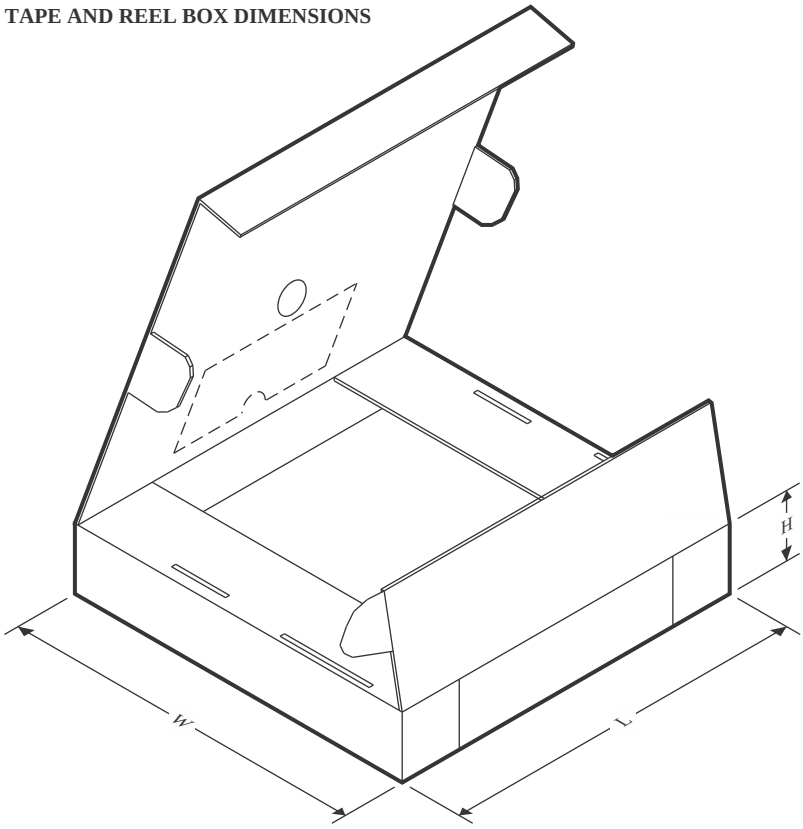
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5929DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5929PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TLC5929RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC5929RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

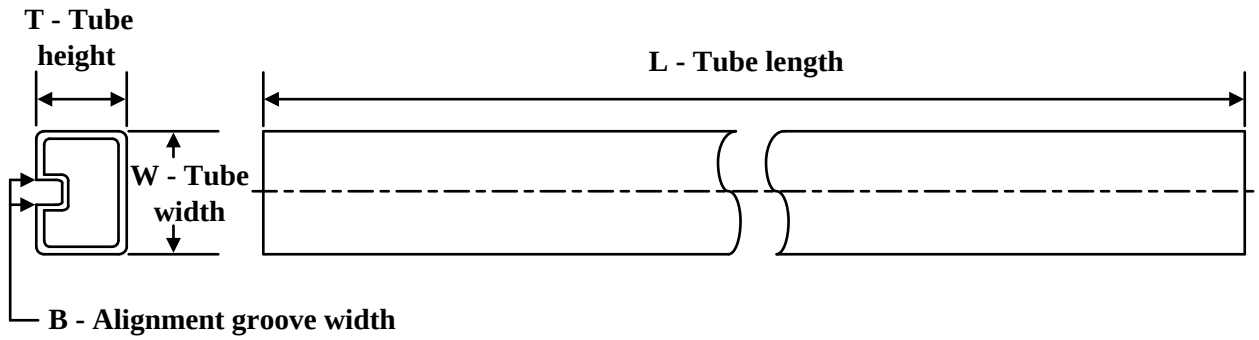
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5929DBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
TLC5929PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
TLC5929RGER	VQFN	RGE	24	3000	356.0	356.0	35.0
TLC5929RGET	VQFN	RGE	24	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5929DBQ	DBQ	SSOP	24	50	506.6	8	3940	4.32
TLC5929PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

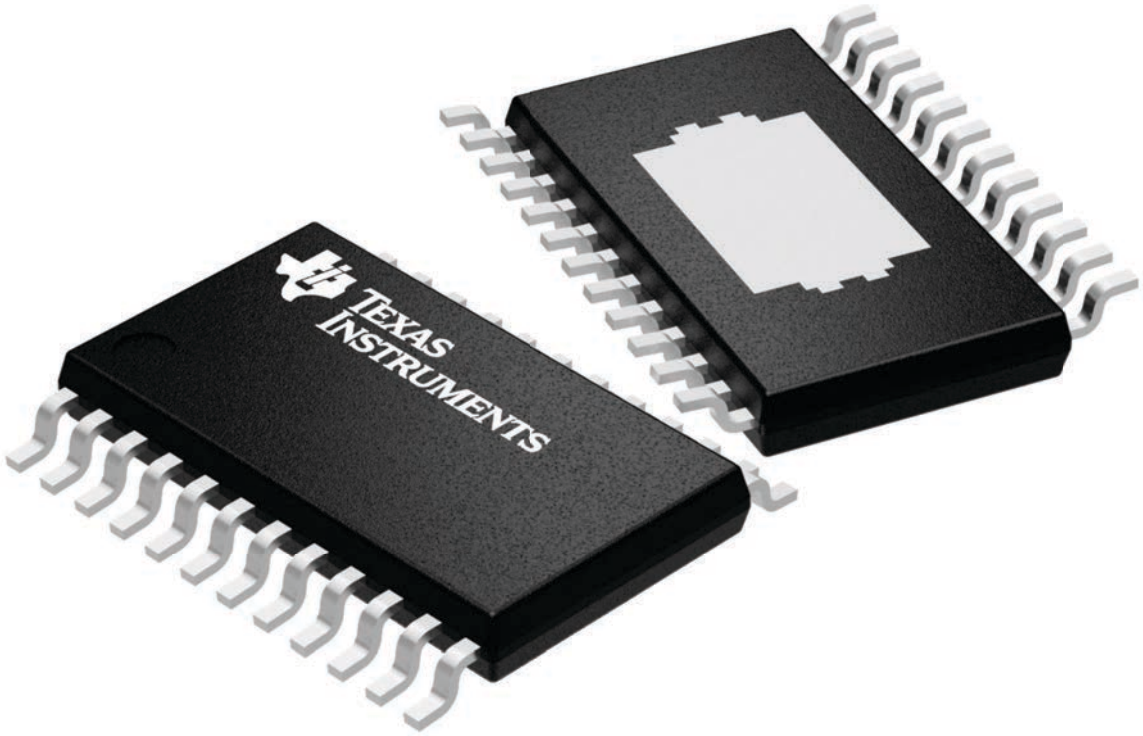
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



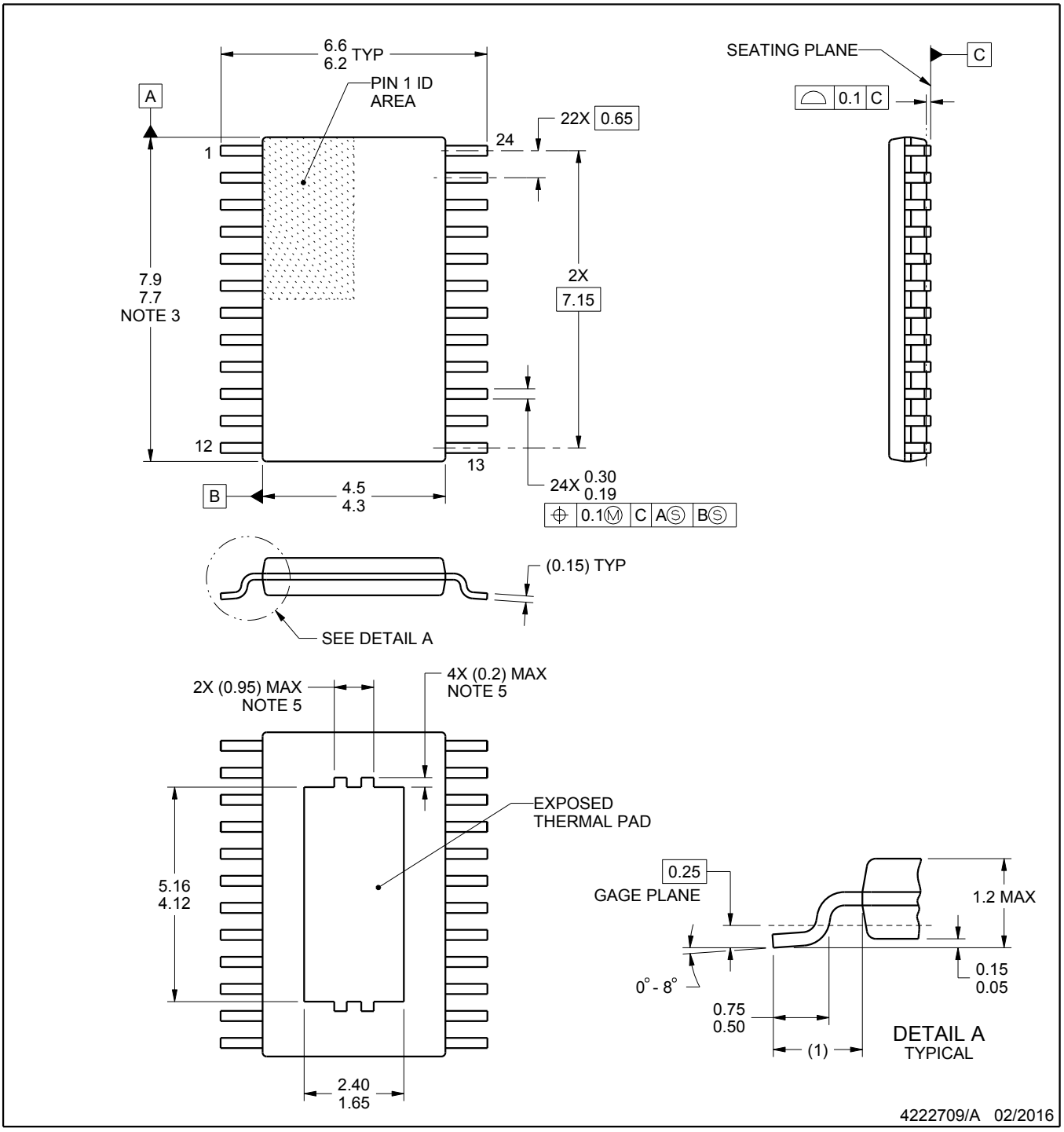
4224742/B

PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

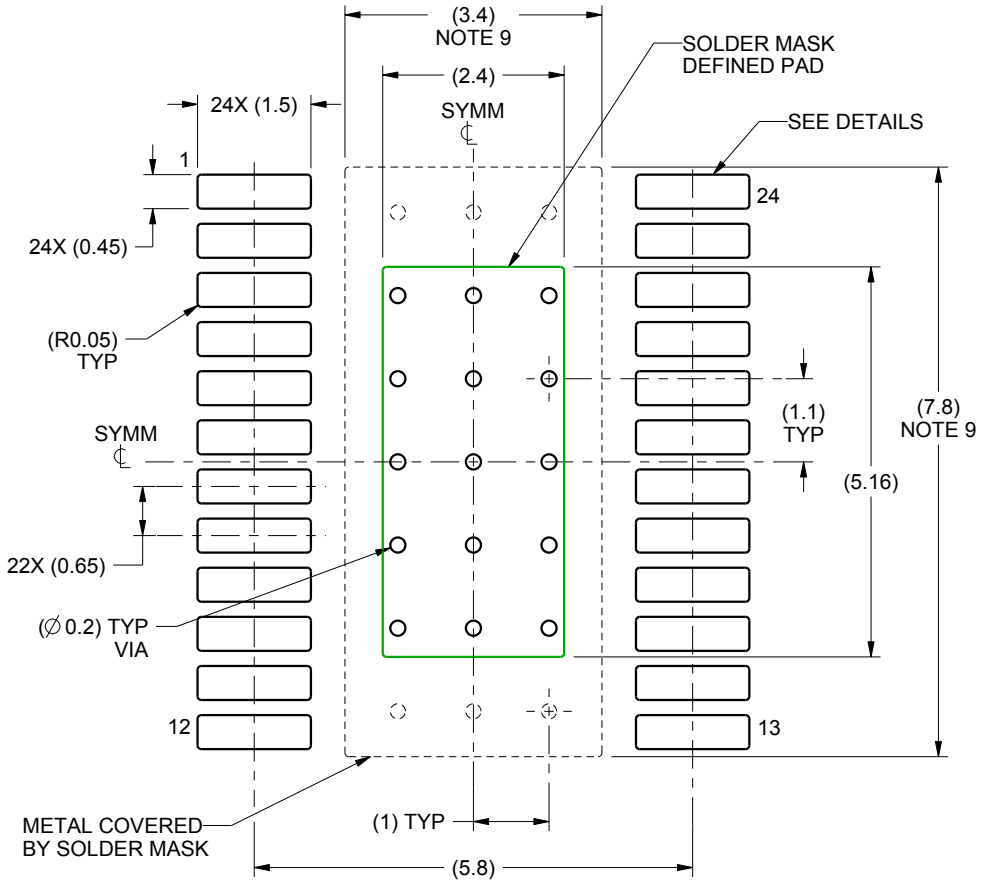
PLASTIC SMALL OUTLINE



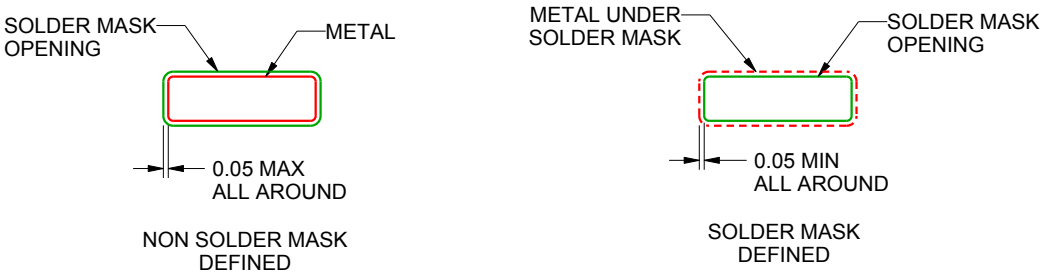
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

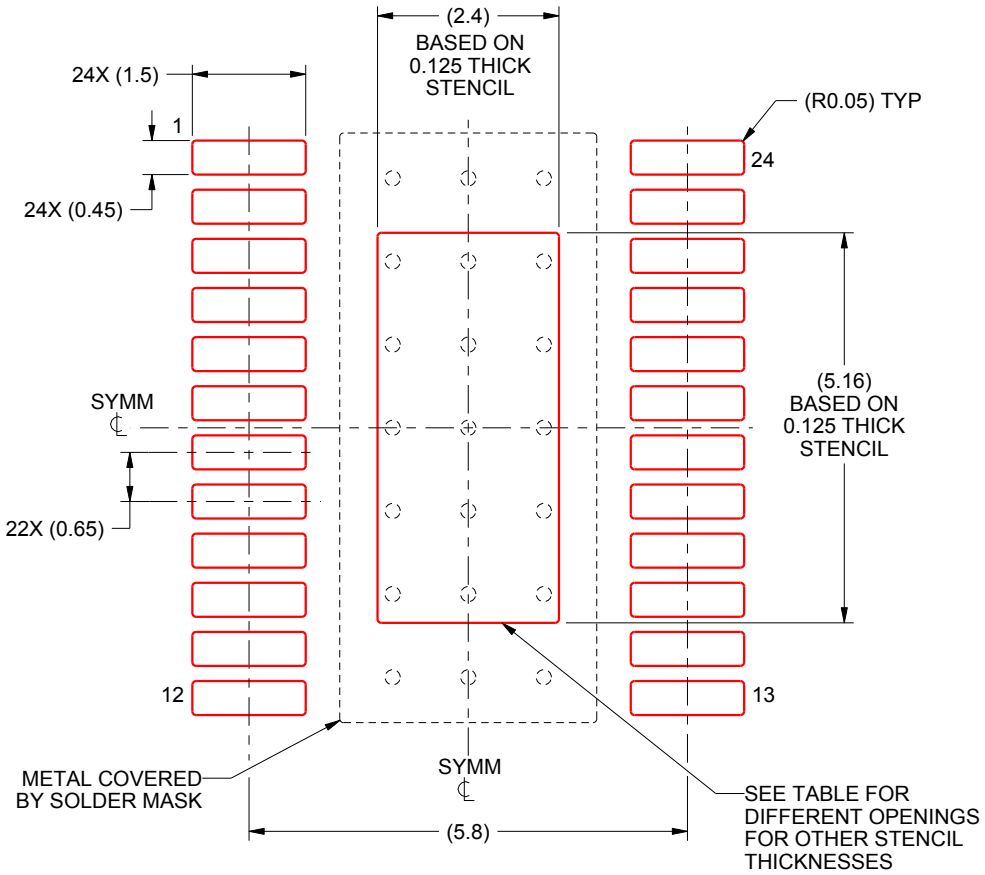


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

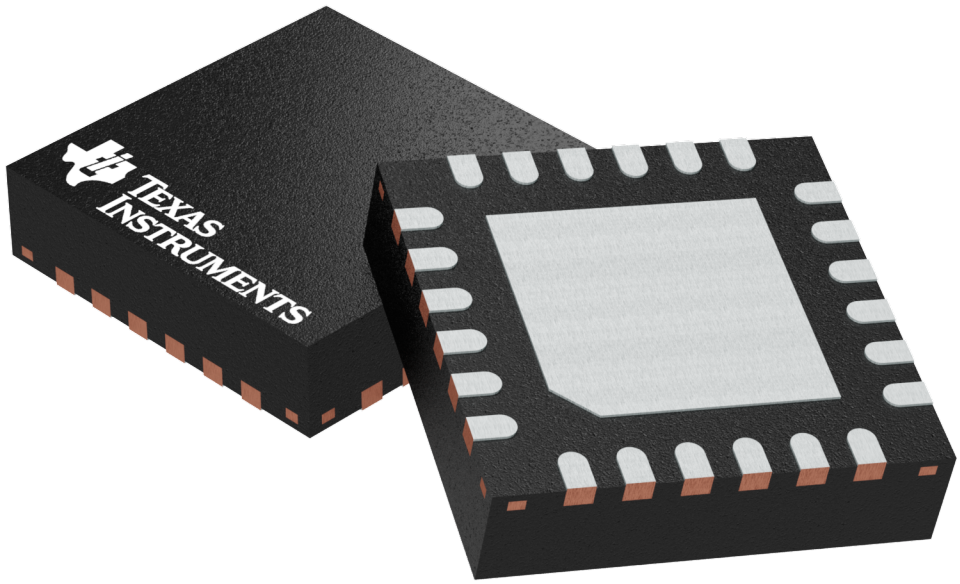
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

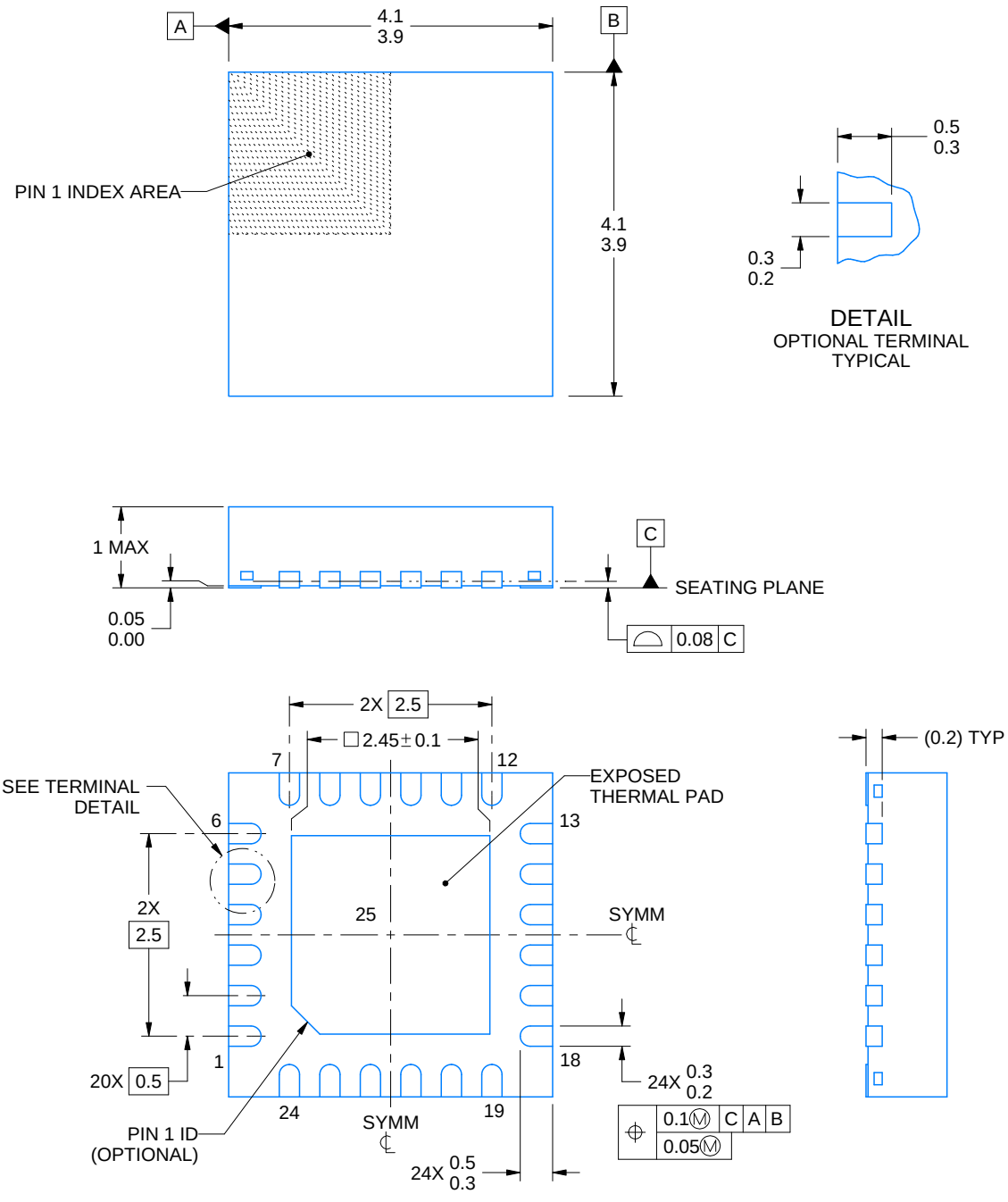
4204104/H

PACKAGE OUTLINE

RGE0024B

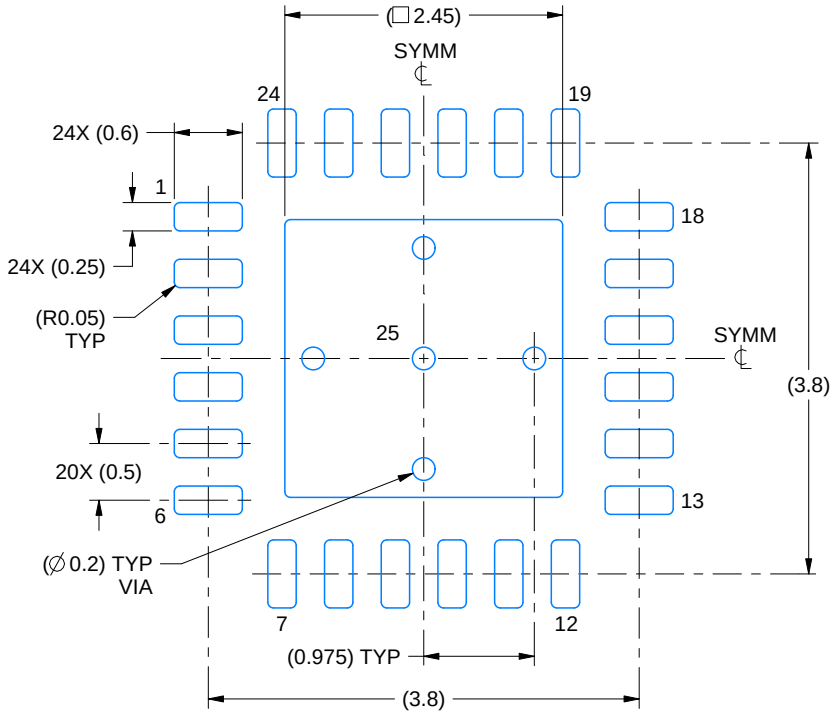
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

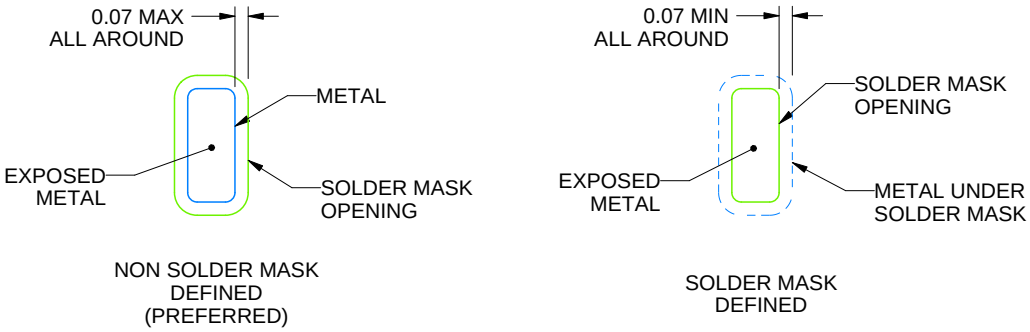


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

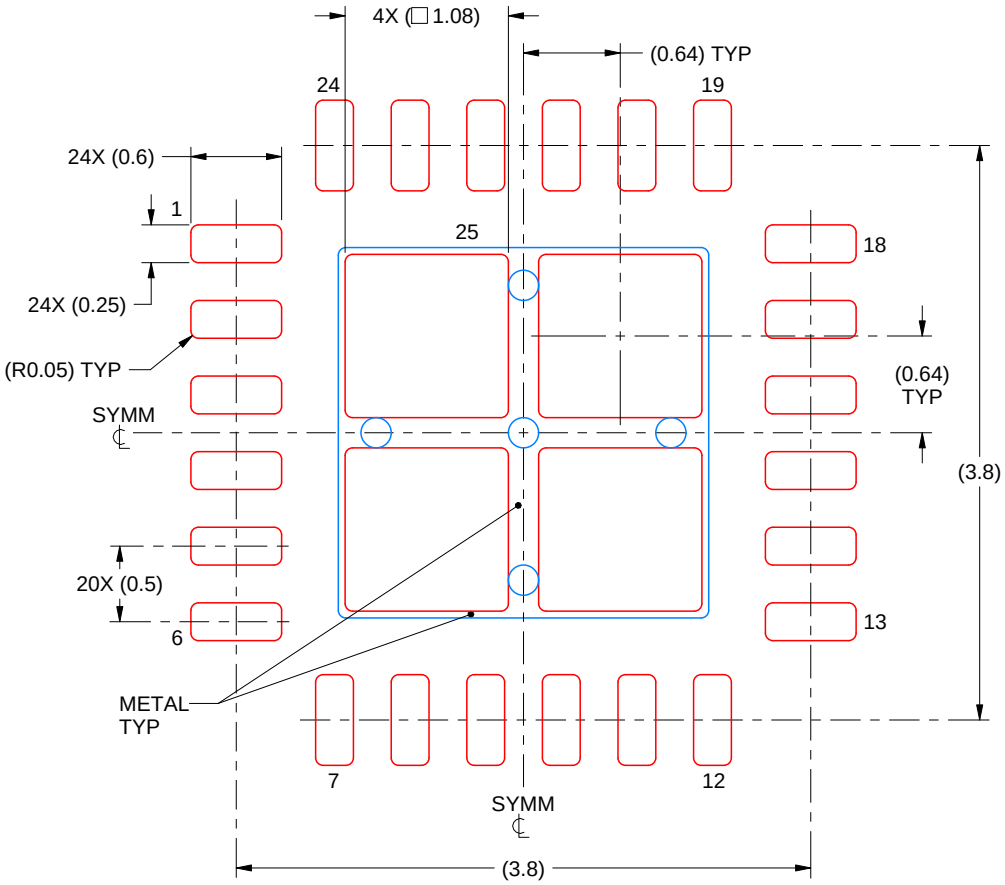


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

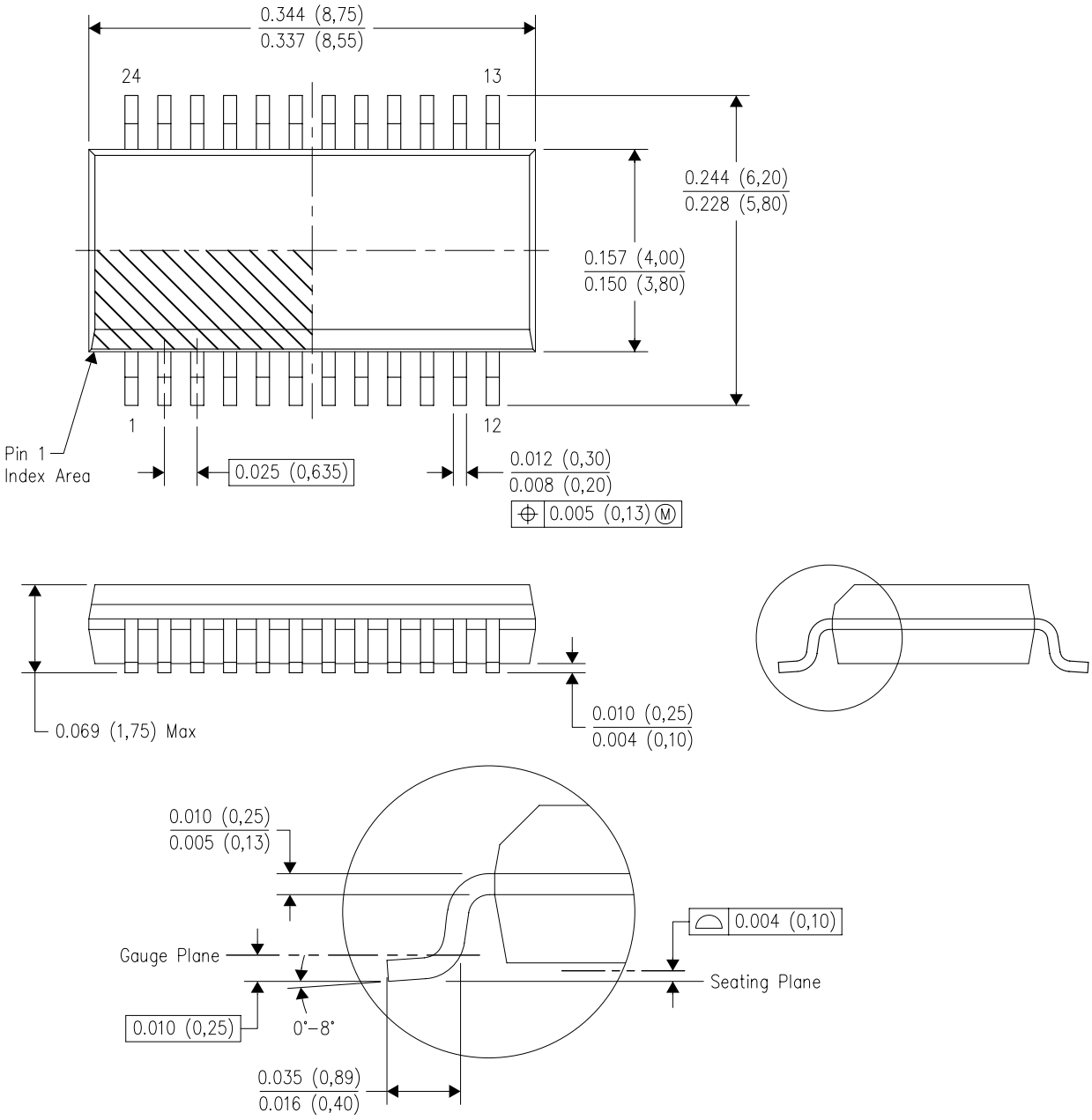
EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

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