具有交叉点的双通道 XAUI/10GBASE-KR 收发器

查询样品: TLK10232

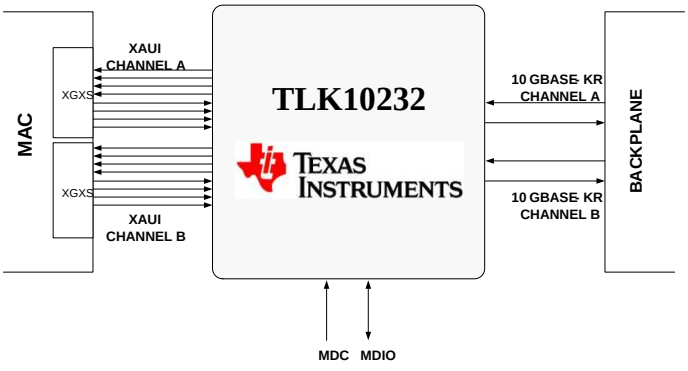
1 介绍

1.1 特性

- 双通道多速率收发器
- 支持 **10GBASE-KR**，**XAUI**，和 **1GBASE-KX** 以太网标准
- 支持所有数据速率高达 **10Gbps** 通用公共无线接口 **(CPRI)** 和开放基站架构协议 **(OBSAI)**
- 在高速端支持数据速率高达 **10.3125Gbps** 的多速率串行解串器 **(SERDES)** 运行，在低速端支持的数据速率高达 **5Gbps**
- 高速端和低速端上的差分电流模式逻辑 **(CML) I/O** 接口
- 到背板、无源和有源铜线缆、或者小尺寸可插拔 **(SFP)+** 光模块的接口
- 可选基准时钟每通道（带有多输出时钟选项）
- 集成交叉点开关可实现灵活的信号路由和冗余输出
- 支持数据重定时操作
- 支持伪随机二进制序列 **(PRBS)**，随机测试兼容模板 **(CRPAT)**，长连续抖动测试图案 **(CJPAT)**，高/低/混频模式，和 **KR** 伪随机模式生成以及验证，方波生成
- 两个电源：**1.0V**（内核），以及 **1.5** 或 **1.8V (I/O)**
- 无需电源排序
- 发送去加重功能和接收自适应均衡可允许扩展背板/线缆达到高速端和低速端
- 信号损失 **(LOS)** 检测
- 支持 **10G-KR** 链路协商、前向纠错、自动协商
- 超大数据包支持
- **JTAG**；**IEEE 1149.1** 测试接口
- 工业标准管理数据输入输出 **(MDIO)** 控制接口
- **65nm** 高级 **CMOS** 技术
- 工业用环境运行温度（**-40°C** 至 **85°C**）
- 功耗：每通道 **800mW**（标称值）
- 器件封装：**13mm x 13mm**，**144** 引脚塑料球状引脚栅格阵列封装 **(PBGA)**，**1mm** 焊球间距

1.2 应用范围

- **10GBASE-KR** 兼容背板连接
- **10** 兆位以太网交换机、路由器、和网络接口卡
- 私有线缆/背板连接
- 高速点到点传输系统



1.3 说明

TLK10232 是一款双通道多速率收发器，此收发器用于高速双向点到点数据传输系统中。 这个器件支持三个主模式。 它可被用作一个 XAUI 到 10GBASE-KR 的收发器、一个通用 8b/10b 多速率 4:1，2:1，1:1 串行器/解串行器，或者被用在 1G-KX 模式中。

运行在 10GBASE-KR 模式中时，TLK10232 将出现在其低速 (LS) 端数据输入上的 8B/10B 经编码 XAUI 数据流串行化。 经串行化的 8B/10B 经编码数据以 64B/66B 编码格式出现在高速 (HS) 端输出上。 相似的，TLK10232 对出现在其高速端数据输入上的 64B/66B 经编码数据流进行解串操作。 格式为 XAUI 8B/10B 的经解串行化 64B/66B 数据出现在低侧端输出上。 这个模式支持链路协商以及针对扩展长度应用的前向纠错 (FEC)。

当运行在通用 SERDES 模式时，TLK10232 将出现在其低速 (LS) 端数据输入上的 8B/10B 经编码数据流进行 2:1 和 4:1 串化。 经串化的 8B/10B 编码数据出现在高速 (HS) 输出上。 相似的，TLK10232 将出现在其高速端数据输入上的 8B/10B 编码数据流进行 1:2 和 1:4 解串化。 经解串化的 8B/10B 编码数据出现在低速端输出上。 根据串化/解串化比率，低速端数据传输速率范围介于 0.5Gbps 至 5Gbps 之间，而高速端数据传输速率介于 1Gbps 至 10Gbps 之间。还支持 1:1 重定时模式，但是速率限制在 1Gbps 至 5Gbps。

TLK10232 还支持具有 PCS (CTC) 功能的 1G-KX (1.25Gbps) 模式。 通过软件服务开通或者自动协商可启用这个模式。 如果使用了软件服务开通，那么支持的数据传输速率可高达 3.125Gbps。

TLK10232 特有一个内置的交叉点开关，此开关可实现冗余输出和简便的数据重路由。 每个输出端口（高速或低速）能够被配置成输出来自任一器件输入端口的数据。 此切换可通过一个硬件引脚或软件控制来启动，并可被配置成立即切换，或配置成在当前数据包的末尾后出现。 这可在不破坏数据包的情况下实现数据源之间的切换。

低速端和高速端数据输入和输出是具有集成端接电阻器的差分电流模式逻辑 (CML) 类型。

为了支持不同操作，TLK10232 提供了灵活的计时机制。 这些机制包括对使用一个从高速端恢复的外部抖动清除时钟进行计时的支持。 此器件还能够在 10GBASE-KR 和 1GBASE-KX 模式下执行时钟容限补偿 (CTC)，从而实现异步计时。

TLK10232 为自检和系统诊断用途提供低速端和高速端回路模式。

TLK10232 具有内置模式生成器和验证器以帮助进行系统测试。 此器件支持不同 PRBS，高/低/混合频率，CRPAT 长/短，CJPAT，和 KR 伪随机测试模式的生成和验证以及方波生成。 低速端和高速端上支持的模式类型取决于所选择的操作模式。

TLK10232 在高速端和低速端都具有一个集成信号损失 (LOS) 检测功能。 在输入差分电压摆幅少于 LOS 置位阀值的条件下，LOS 被置为有效。

TLK10232 的两个通道是完全独立的。 它们可以在不同的基准时钟、不同的数据速率、和不同的串化/解串化比率下运行。

TLK10232 的低速端非常适合与现场可编程栅极阵列 (FPGA)，特定用途集成电路 (ASIC)，媒体访问控制器 (MAC) 或能够处理较低速率串行数据流的网络处理器对接。 高速端非常适合通过光纤、电缆、或者背板接口与远程系统对接。 TLK10232 支持 SFP 和 SFP+ 光模块，以及 10GBASE-KR 兼容背板系统的运行。

2 Physical Characteristics

2.1 Block Diagram

Various interfaces of the TLK10232 device are shown in Figure 2-1 for Channel A. The implementation is the same for Channel B. A simplified one-channel block diagram of both the transmit and recive data path is shown in Figure 2-2. This low-power transceiver consists of two serializer/deserializer (SERDES) blocks, one on the low speed side and the other on the high speed side. The core logic block that lies between the two SERDES blocks carries out all the logic functions including channel synchronization, lane alignment, 8B/10B and 64B/66B encoding/decoding, as well as test pattern generation and verification.

The TLK10232 provides a management data input/output (MDIO Clause 22/45) interface as well as a JTAG interface for device configuration, control, and monitoring. Detailed description of the TLK10232 pin functions is provided in Table 2-1.

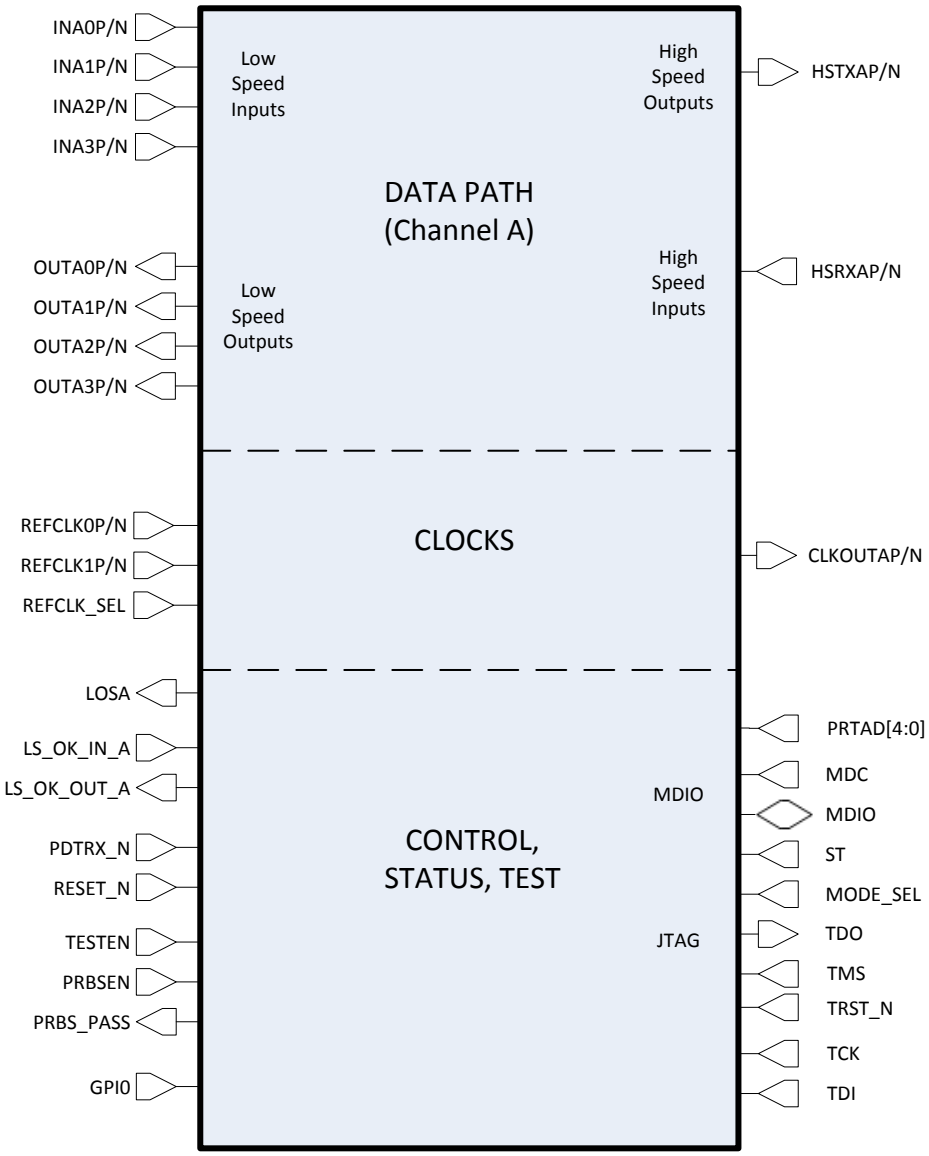


Figure 2-1. TLK10232 Interfaces

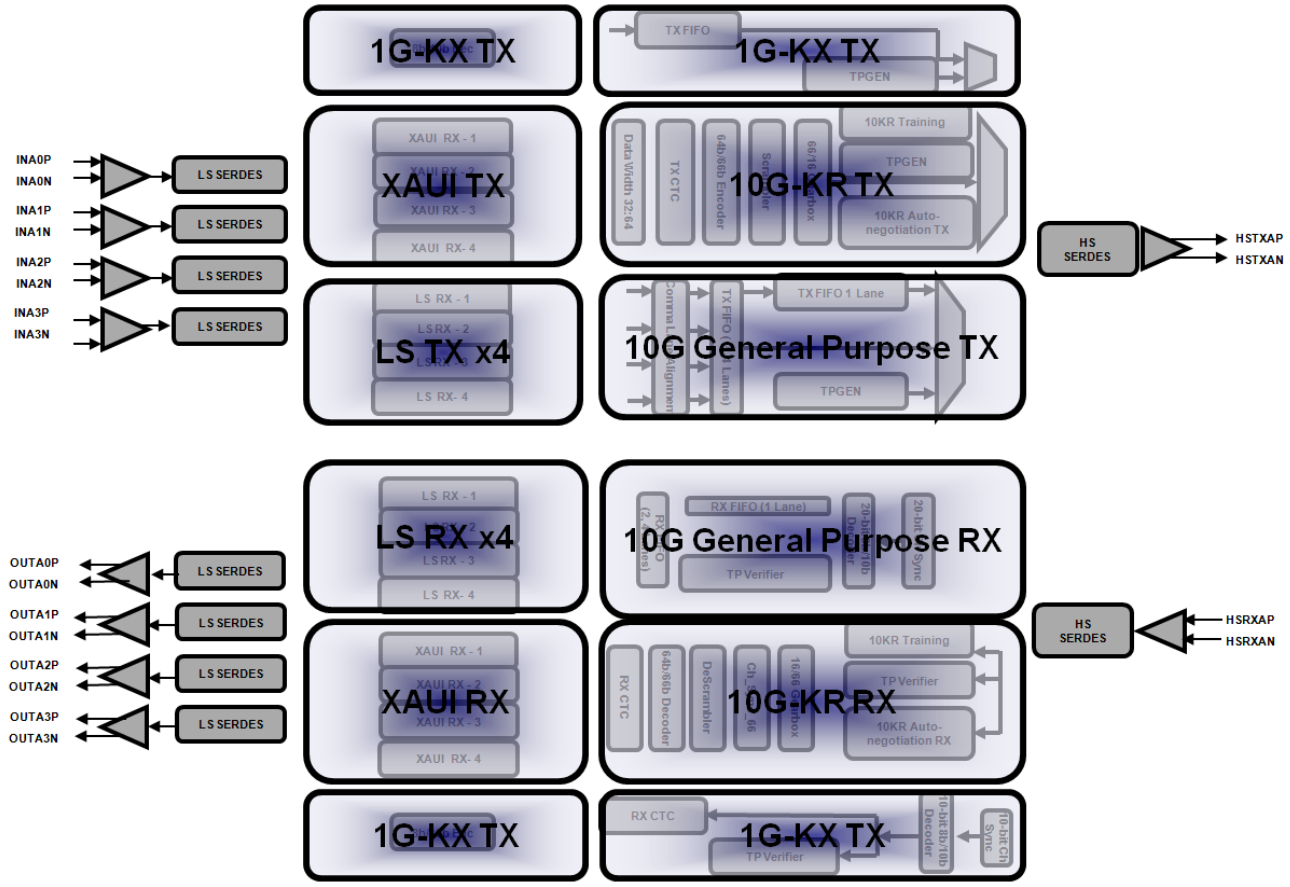


Figure 2-2. A Simplified One Channel Block Diagram of the TLK10232 Data Paths

2.2 Package

A 13-mm x 13-mm, 144-pin PBGA package with a ball pitch of 1 mm is used. The device pin-out is as shown in Figure 2-3 and is described in detail in Table 2-1 and Table 2-2.

	1	2	3	4	5	6	7	8	9	10	11	12
A	INA1P	VSS	INA0N	INA0P	VSS	OUTA0P	OUTA0N	PDTRXA_N	CLKOUTBP	CLKOUTBN	VSS	HSRXAN
B	INA1N	INA2P	VSS	VSS	OUTA1P	OUTA1N	VSS	TMS	PRBSEN	LS_OK_IN_A	VSS	HSRXAP
C	VSS	INA2N	VDDRA_LS	OUTA2P	OUTA2N	VSS	VDDO0	TDI	CLKOUTAP	CLKOUTAN	AMUXA	VSS
D	INA3P	VDDA_LS	VSS	AMUXB	VSS	TDO	VPP	TCK	LS_OK_OUT_A	VSS	VSS	HSTXAP
E	INA3N	VSS	OUTA3N	VSS	TRST_N	VDDD	DVDD	VDDD	LOSA	PRTAD0	VDDRA_HS	HSTXAN
F	VSS	VDDA_LS	OUTA3P	VDDT_LS	VSS	VDDD	DVDD	VSS	VDDT_HS	VSS	VDDA_HS	VSS
G	VSS	VDDA_LS	VSS	VDDT_LS	VSS	DVDD	VSS	DVDD	PRTAD1	VDDA_HS	VSS	HSRXBN
H	INB0P	VSS	OUTB0N	VSS	RESET_N	VDDD	DVDD	VDDD	LS_OK_OUT_B	MODE_SEL	VSS	HSRXBP
J	INB0N	VDDA_LS	OUTB0P	PDTRXB_N	VSS	PRTAD3	MDIO	MDC	PRBS_PASS	GPI0	VDDRB_HS	VSS
K	VSS	INB1P	VDDRB_LS	OUTB1N	OUTB1P	VSS	VDDO1	LOSB	REFCLK1P	REFCLK1N	VSS	HSTXBP
L	INB2P	INB1N	VSS	VSS	OUTB2N	OUTB2P	VSS	LS_OK_IN_B	PRTAD2	TESTEN	VSS	HSTXBN
M	INB2N	VSS	INB3P	INB3N	VSS	OUTB3N	OUTB3P	PRTAD4	ST	REFCLK0P	REFCLK0N	VSS

Figure 2-3. The Pin-Out of the TLK10232

2.3 Terminal Functions

The details of the terminal functions of the TLK10232 are provided in Table 2-1 and Table 2-2.

Table 2-1. Pin Description - Signal Pins

TERMINAL		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
CHANNEL A			
HSTXAP HSTXAN	D12 E12	Output CML VDDA_HS	**High Speed Transmit Channel A Output.** HSTXAP and HSTXAN comprise the high speed side transmit direction Channel A differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.
HSRXAP HSRXAN	B12 A12	Input CML VDDA_HS	**High Speed Receive Channel A Input.** HSRXAP and HSRXAN comprise the high speed side receive direction Channel A differential serial input signal. These CML input signals must be AC coupled.
INA[3:0]P/N	D1/E1 B2/C2 A1/B1 A4/A3	Input CML VDDA_LS	**Low Speed Channel A Inputs.** INAP and INAN comprise the low speed side transmit direction Channel A differential input signals. These signals must be AC coupled.
OUTA[3:0]P/N	F3/E3 C4/C5 B5/B6 A6/A7	Output CML VDDA_LS	**Low Speed Channel A Outputs.** OUTAP and OUTAN comprise the low speed side receive direction Channel A differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. These signals must be AC coupled.
LOSA	E9	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	C**hannel A Receive Loss Of Signal (LOS) Indicator.** LOSA=0: Signal detected. LOSA=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXAP/N has a differential input signal swing of ≤75 mV_{pp}, LOSA will be asserted (if enabled). If the input signal is greater than 150 mV_{p-p}, LOS will be deasserted. Outside of these ranges, the LOS indication is undefined. Other functions can be observed on LOSA real-time, configured via MDIO During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXA_N asserted low), this pin is floating. During register based power down, this pin is floating. It is highly recommended that LOSA be brought to an easily accessible point on the application board (header) in the event that debug is required.
LS_OK_IN_A	B10	Input LVCMOS 1.5V/1.8V VDDO0	**Channel A Receive Lane Alignment Status Indicator.** Lane alignment status signal received from a Lane Alignment Slave on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_IN_A=0: Channel A link partner receive lanes not aligned. LS_OK_IN_A=1: Channel A link partner receive lanes aligned
LS_OK_OUT_A	D9	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	**Channel A Transmit Lane Alignment Status Indicator.** Lane alignment status signal sent to a Lane Alignment Master on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_OUT_A=0: Channel A link partner transmit lanes not aligned. LS_OK_OUT_A=1: Channel A link partner transmit lanes aligned.
PDTRXA_N	A8	Input LVCMOS 1.5V/1.8V VDDO0	**Transceiver Power Down.** When this pin is held low (asserted), Channel A is placed in power down mode. When deasserted, Channel A operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.
CHANNEL B			
HSTXBP HSTXBN	K12 L12	Output CML VDDA_HS	**High Speed Transmit Channel B Output.** HSTXBP and HSTXBN comprise the high speed side transmit direction Channel B differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.
HSRXBP HSRXBN	H12 G12	Input CML VDDA_HS	**High Speed Receive Channel B Input.** HSRXBP and HSRXBN comprise the high speed side receive direction Channel B differential serial input signal. These CML input signals must be AC coupled.
INB[3:0]P/N	M3/M4 L1/M1 K2/L2 H1/J1	Input CML VDDA_LS	**Low Speed Channel B Inputs.** INBP and INBN comprise the low speed side transmit direction Channel B differential input signals. These signals must be AC coupled.
OUTB[3:0]P/N	M7/M6 L6/L5 K5/K4 J3/H3	Output CML VDDA_LS	**Low Speed Channel B Outputs.** OUTBP and OUTBN comprise the low speed side receive direction Channel B differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. These signals must be AC coupled.

Table 2-1. Pin Description - Signal Pins (continued)

TERMINAL		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
LOSB	K8	Output LVCMOS 1.5V/1.8V VDDO1 40Ω Driver	**Channel B Receive Loss Of Signal (LOS) Indicator.** LOSB=0: Signal detected. LOSB=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXBP/N has a differential input signal swing of ≤75 mV_{pp}, LOSB will be asserted (if enabled). If the input signal is greater than 150 mV_{p-p}, LOS will be deasserted. Outside of these ranges, the LOS indication is undefined. Other functions can be observed on LOSB real-time, configured via MDIO During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXB_N asserted low), this pin is floating. During register based power down, this pin is floating. It is highly recommended that LOSB be brought to easily accessible point on the application board (header), in the event that debug is required.
LS_OK_IN_B	L8	Input LVCMOS 1.5V/1.8V VDDO0	**Channel B Receive Lane Alignment Status Indicator.** Lane alignment status signal received from a Lane Alignment Slave on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_IN_B=0: Channel B Receive lanes not aligned. LS_OK_IN_B=1: Channel B Receive lanes aligned
LS_OK_OUT_B	H9	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	**Channel B Transmit Lane Alignment Status Indicator.** Lane alignment status signal sent to a Lane Alignment Master on the link partner device. Valid in 10G General Purpose Serdes Mode. LS_OK_OUT_B=0: Channel B Transmit lanes not aligned. LS_OK_OUT_B=1: Channel B Transmit lanes aligned.
PDTRXB_N	J4	Input LVCMOS 1.5V/1.8V VDDO1	**Transceiver Power Down.** When this pin is held low (asserted), Channel B is placed in power down mode. When deasserted, Channel B operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.
REFERENCE CLOCKS, OUTPUT CLOCKS, AND CONTROL AND MONITORING SIGNALS			
REFCLK0P/N	M10 M11	Input LVDS/ LVPECL DVDD	**Reference Clock Input Zero.** This differential input is a clock signal used as a reference to channels A or B. The reference clock selection is done through MDIO. This input signal **must** be AC coupled. If unused, REFCLK0P/N should be pulled down to GND through a shared 100 Ω resistor.
REFCLK1P/N	K9 K10	Input LVDS/ LVPECL DVDD	**Reference Clock Input One.** This differential input is a clock signal used as a reference to channels A or B. The reference clock selection is done through MDIO. This input signal **must** be AC coupled. If unused, REFCLK1P/N should be pulled down to GND through a shared 100 Ω resistor.
CLKOUTAP/N CLKOUTBP/N	C9/C10 A9/A10	Output CML DVDD	**Channel A/B Output Clock.** By default, these outputs are enabled and output the high speed side Channel A recovered byte clock (high speed line rate divided by 16 or 20). Optionally, they can be configured to output the VCO clock divided by 2. (Note: for full rates, VCO/2 pre-divided clocks will be equivalent to the line rate divided by 8; for sub-rates, VCO/2 pre-divided clocks will be equivalent to the line rate divided by 4). These CML outputs must be AC coupled. During device reset (RESET_N asserted low), pin-based power down (PDTRXA_N and PDTRXB_N asserted low), or register-based power down, these pins are floating.
PRBSEN	B9	Input LVCMOS 1.5V/1.8V VDDO0	**Enable PRBS:** When this pin is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high speed and low speed sides of both channels. The PRBS 2^7-1 pattern is selected by default, and can be changed through MDIO.
PRBS_PASS	J9	Output LVCMOS 1.5V/1.8V VDDO1 40Ω Driver	**Receive PRBS Error Free (Pass) Indicator.** When PRBS test is enabled (PRBSEN=1): PRBS_PASS=1 indicates that PRBS pattern reception is error free. PRBS_PASS=0 indicates that a PRBS error is detected. The channel, high speed or low speed side, and lane (for low speed side) that this signal refers to is chosen through MDIO. During device reset (RESET_N asserted low) this pin is driven high. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is floating. During register based power down, this pin is floating. It is highly recommended that PRBS_PASS be brought to easily accessible point on the application board (header), in the event that debug is required.
ST	M9	Input LVCMOS 1.5V/1.8V VDDO[1:0]	**MDIO Select**. Used to select Clause 22 (=1) or Clause 45 (=0) operation. Note that selecting clause 22 will impact mode availability. See MODE_SEL. A hard or soft reset must be applied after a change of state occurs on this input signal.
MODE_SEL	H10	Input LVCMOS 1.5V/1.8V VDDO[1:0]	**Device Operating Mode Select.** Used together with ST pin to select device operating mode. See Table 2-3 for details.

Table 2-1. Pin Description - Signal Pins (continued)

TERMINAL		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
PRTAD[4:0]	M8 J6 L9 G9 E10	Input LVCMOS 1.5V/1.8V VDDO[1:0]	**MDIO Port Address.** Used to select the MDIO port address. PRTAD[4:1] selects the MDIO port address. The TLK10232 has two different MDIO port addresses. Selecting a unique PRTAD[4:1] per TLK10232 device allows 16 TLK10232 devices per MDIO bus. Each channel can be accessed by setting the appropriate port address field within the serial interface protocol transaction. The TLK10232 will respond if the 4 MSB's of the port address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1]. If PA[0] = 1'b0, TLK10232 Channel A will respond. If PA[0] = 1'b1, TLK10232 Channel B will respond. PRTAD0 is not needed for port addressing, but can be used as a general purpose input pin to control the switching function or the stopwatch latency measurement. If these functions are not needed, PRTAD0 should be grounded on the application board.
RESET_N	H5	Input LVCMOS 1.5V/1.8V VDDO01	**Low True Device Reset.** RESET_N must be held asserted (low logic level) for at least 10us after device power stabilization.
MDC	J8	Input LVCMOS with Hysteresis 1.5V/1.8V VDDO1	**MDIO Clock Input.** Clock input for the MDIO interface. Note that an external pullup is generally not required on MDC except if driven by an open-drain/open-collector clock source.
MDIO	J7	Input/ Output LVCMOS 1.5V/1.8V VDDO1 25Ω Driver	**MDIO Data I/O.** MDIO interface data input/output signal for the MDIO interface. **This signal must be externally pulled up to VDDO using a 2kΩ resistor.** During device reset (RESET_N asserted low) this pin is floating. During software initiated power down the management interface remains active for control register writes and reads. Certain status bits will not be deterministic as their generating clock source may be disabled as a result of asserting either power down input signal. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is floating. During register based power down, this pin is driven normally.
TDI	C8	Input LVCMOS 1.5V/1.8V VDDO0 (Internal Pullup)	**JTAG Input Data.** TDI is used to serially shift test data and test instructions into the device during the operation of the test port. In system applications where JTAG is not implemented, this input signal may be left floating. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is not pulled up. During register based power down, this pin is pulled up normally.
TDO	D6	Output LVCMOS 1.5V/1.8V VDDO0 50Ω Driver	**JTAG Output Data.** TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state. During device reset (RESET_N asserted low) this pin is floating. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is not pulled up. During register based power down, this pin is pulled up normally.
TMS	B8	Input LVCMOS 1.5V/1.8V VDDO0 (Internal Pullup)	**JTAG Mode Select.** TMS is used to control the state of the internal test-port controller. In system applications where JTAG is not implemented, this input signal can be left unconnected. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is not pulled up. During register based power down, this pin is pulled up normally.
TCK	D8	Input LVCMOS with Hysteresis 1.5V/1.8V VDDO0	**JTAG Clock.** TCK is used to clock state information and test data into and out of the device during boundary scan operation. In system applications where JTAG is not implemented, this input signal should be grounded.
TRST_N	E5	Input LVCMOS 1.5V/1.8V VDDO0 (Internal Pulldown)	**JTAG Test Reset.** TRST_N is used to reset the JTAG logic into system operational mode. This input can be left unconnected in the application and is pulled down internally, disabling the JTAG circuitry. If JTAG is implemented on the application board, this signal should be deasserted (high) during JTAG system testing, and otherwise asserted (low) during normal operation mode. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is not pulled up. During register based power down, this pin is pulled up normally.
TESTEN	L10	Input LVCMOS 1.5V/1.8V VDDO1	**Test Enable.** This signal is used during the device manufacturing process. It should be grounded through a resistor in the device application board. The application board should allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO).
GPI0	J10	Input LVCMOS 1.5V/1.8V VDDO1	G**eneral Purpose Input.** This signal is used during the device manufacturing process. It should be grounded through a resistor on the device application board. The application board should also allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO).
AMUXA	C11	Analog I/O	**SERDES Channel A Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.
AMUXB	D4	Analog I/O	**SERDES Channel B Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.

Table 2-2. Pin Description - Power Pins

TERMINAL		TYPE	DESCRIPTION
SIGNAL	BGA		
VDDA_LS/HS	D2, F2, G2, J2, G10, F11	Power	**SERDES Analog Power.** VDDA_LS and VDDA_HS provide supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1.0V nominal. Can be tied together on the application board.
VDDT_LS/HS	F4, G4, F9	Power	**SERDES Analog Power.** VDDT_LS and VDDT_HS provide termination and supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1.0V nominal. Can be tied together on the application board.
VDDD	E6, F6, H6, E8, H8	Power	**SERDES Digital Power.** VDDD provides supply voltage for the digital circuits internal to the SERDES. 1.0V nominal.
DVDD	G6, E7, F7, H7, G8	Power	**Digital Core Power.** DVDD provides supply voltage to the digital core. 1.0V nominal.
VDDRA_LS/HS	C3 E11	Power	**SERDES Analog Regulator Power.** VDDRA_LS and VDDRA_HS provide supply voltage for the internal PLL regulator for Channel A low speed and high speed sides respectively. 1.5V or 1.8V nominal.
VDDRB_LS/HS	K3 J11	Power	**SERDES Analog Regulator Power** VDDRB_LS and VDDRB_HS provide supply voltage for the internal PLL regulator for Channel B low speed and high speed sides respectively. 1.5V or 1.8V nominal.
VDDO[1:0]	K7 C7	Power	**LVCMOS I/O Power.** VDDO0 and VDDO1 provide supply voltage for the LVCMOS inputs and outputs. 1.5V or 1.8V nominal. Can be tied together on the application board.
VPP	D7	Power	**Factory Program Voltage.** Used during device manufacturing. The application must connect this power supply directly to DVDD.
VSS	A2, A5, A11, B3, B4, B7, B11, C1, C6, C12, D3, D5, D10, D11, E2, E4, F1, F5, F8, F10, F12, G1, G3, G5, G7, G11, H2, H4, H11, J5, J12, K1, K6, K11, L3, L4, L7, L11, M2, M5, M12	Ground	**Ground.** Common analog and digital ground.

2.4 Operating Modes

The TLK10232 is a versatile high-speed transceiver device that is designed to perform various physical layer functions in three operating modes: 10GBASE-KR Mode, 1G-KX Mode, and General Purpose (10G) SERDES Mode. The three modes are described in three separate sections. The device operating mode is determined by the MODE_SEL and ST pin settings, as well as MDIO register 1E.0001 bit 10.

Table 2-3. TLK10232 Operating Mode Selection

	ST = 0 (Clause 45)	ST = 1 (Clause 22)
{MODE_SEL pin, Register 1E.0001 bit 10}		
1x	10G	10G
01	10G	10G
00	10G-KR/1G-KX (Determined by Auto Neg)	1G-KX (No Auto Neg)

3 10GBASE-KR MODE FUNCTIONAL DESCRIPTION

A simplified block diagram of the transmit and receive data paths in 10GBASE-KR mode is shown in Figure 3-1. This section gives a high-level overview of how data moves through these paths, then gives a more detailed description of each block's functionality.

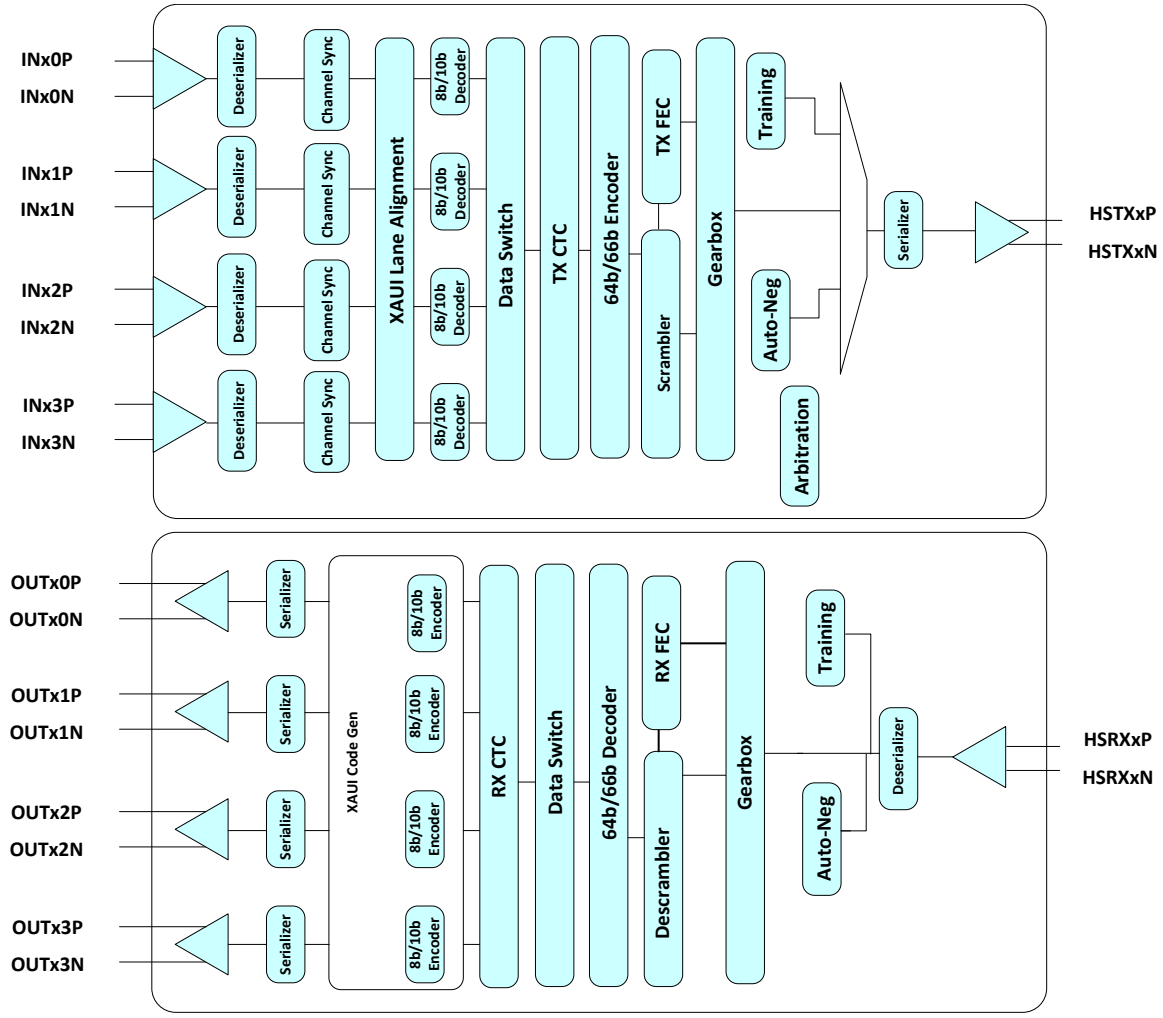


Figure 3-1. A Simplified One Channel KR Data Path Block Diagram

3.1 10GBASE-KR Transmit Data Path Overview

In 10GBASE-KR Mode, the TLK10232 takes in XAUI data on the four low speed input lanes. The serial data in each lane is deserialized into 10-bit parallel data, then byte aligned (channel synchronized) based on comma detection. The four XAUI lanes are then aligned with one another, and the aligned data is input to four 8B/10B decoders. The decoded data is then input to the transmit clock tolerance compensation (CTC) block which compensates for any frequency offsets between the incoming XAUI data and the local reference clock. The CTC block then delivers the data to a 64B/66B encoder and a scrambler. The resulting scrambled 10GBASE-KR data is then input to a transmit gearbox which in turn delivers it to the high speed side SERDES for serialization and output through the HSTX*P/N pins.

3.2 10GBASE-KR Receive Data Path Overview

In the receive direction, the TLK10232 will take in 64B/66B-encoded serial 10GBASE-KR data on the HSRX*P/N pins. This data is deserialized by a high speed SERDES, then input to a receive gearbox. After the gearbox, the data is aligned to 66-bit frames, descrambled, 64B/66B decoded, and then input to the receive CTC block. After CTC, the data is encoded by four 8B/10B encoders, and the resulting four 10-bit parallel words are serialized by the low speed SERDES blocks. The four serial XAUI output lanes are transmitted out the OUT*P/N pins.

3.3 Channel Synchronization Block

When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to be able to recognize the byte boundary again. Generally, this is accomplished through the use of a synchronization pattern. This is a unique pattern of 1's and 0's that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8B/10B encoding contains a character called the comma (b'0011111' or b'1100000') which is used by the comma detect circuit to align the received serial data back to its original byte boundary. The TLK10232 channel synchronization block detects the comma pattern found in the K28.5 character, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It is important to note that the comma can be either a (b'0011111') or the inverse (b'1100000') depending on the running disparity. The TLK10232 decoder will detect both patterns.

The TLK10232 performs channel synchronization per lane as shown in the flowchart of Figure 3-2.

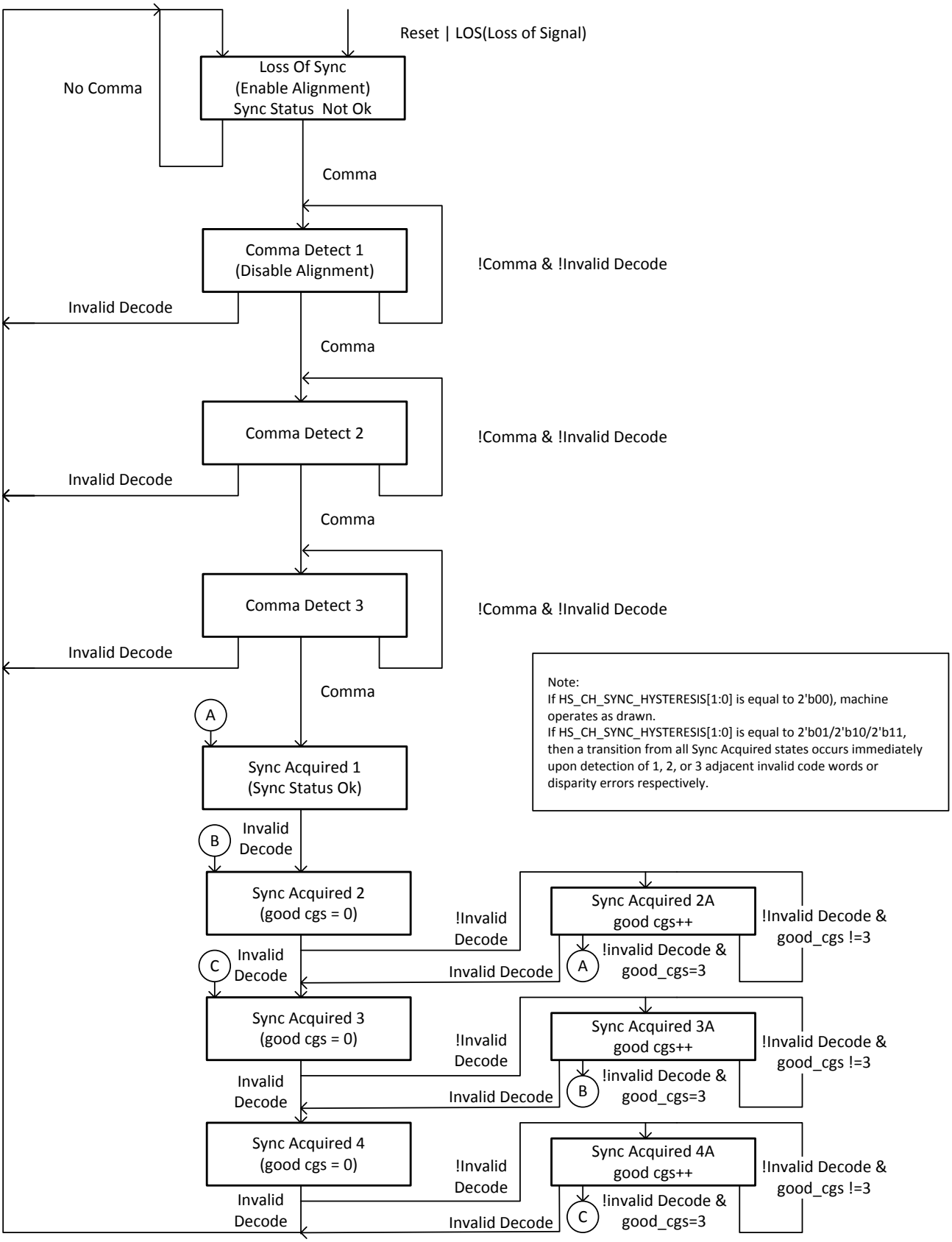


Figure 3-2. Channel Synchronization Flowchart

3.4 8B/10B Encoder

Embedded-clock serial interfaces require a method of encoding to ensure sufficient transition density for the receiving CDR to acquire and maintain lock. The encoding scheme also maintains the signal DC balance by keeping the number of ones and zeros balanced which allows for AC coupled data transmission. The TLK10232 uses the 8B/10B encoding algorithm that is used by the 10 Gbps and 1 Gbps Ethernet and Fibre Channel standards. This provides good transition density for clock recovery and improves error checking.

The 8B/10B encoder converts each 8-bit wide data to a 10-bit wide encoded data character to improve its transition density. This transmission code includes /D/ characters, used for transmitting data, and /K/ characters, used for transmitting protocol information. Each /K/ or /D/ character code word can also have both a positive and a negative disparity version. The disparity of a code word is selected by the encoder to balance the running disparity of the serialized data stream.

3.5 8B/10B Decoder

Once the Channel Synchronization block has identified the byte boundaries from the received serial data stream, the 8B/10B decoder converts 10-bit 8B/10B-encoded characters into their respective 8-bit formats. When a code word error or running disparity error is detected in the decoded data, the error is reported in the status register (1E.000F) and the LOS pin is asserted (depending on the LOS overlay selection).

3.6 64B/66B Encoder/Scrambler

To facilitate the transmission of data received from the media access control (MAC) layer, the TLK10232 encodes data received from the MAC using the 64B/66B encoding algorithm defined in the IEEE802.3-2008 standard. The TLK10232 takes two consecutive transfers from the XAUI interface and encodes them into a 66-bit code word. The information from the two XAUI transfers includes 64 bits of data and 8 bits of control information after 8B/10B decoding.

If the 64B/66B encoder detects an invalid packet format from the XAUI interface, it replaces erroneous information with appropriately-encoded error information. The resulting 66-bit code word is then sent on to the transmit gearbox.

The encoding process implemented in the TLK10232 includes two steps:

1. an encoding step, which converts the 72 bits of data (8 data bytes plus 8 control-code indicators) received from the transmit CTC FIFO into a 66-bit code word
2. a scrambling step, which scrambles 64 bits of encoded data using the scrambler polynomial $x^{58}+x^{39}+1$. The 66 bits created by the encoder consists of 64 bits of data and a 2-bit synchronization field consisting of either 01 or 10. Only the 64 bits of data are scrambled, leaving the two synchronization bits unmodified. The two synchronization bits allow the receive gearbox to obtain frame alignment and, in addition, ensure an edge transition of at least once in 66 bits of data. The encoding process allows a limited amount of control information to be sent in-line with the data.

3.7 Forward Error Correction

Optionally enabled, Forward Error Correction (FEC) follows the IEEE 802.3-2008 standard, and is able to correct a burst errors up to 11 bits. In the TX data path, the FEC logic resides between the scrambler and gearbox. In the RX datapath, FEC resides between the gearbox and descrambler. Frame alignment is handled inside the RX FEC block during FEC operation, and the RX gearbox sync header alignment is bypassed. Because latency is increased in both the TX and RX data paths with FEC enabled, it is disabled by default and must be enabled through MDIO programming. Note that FEC by nature will add latency due to frame storage.

3.8 64B/66B Decoder/Descrambler

The data received from the serial 10GBASE-KR is 64B/66B-encoded data. The TLK10232 decodes the data received using the 64B/66B decoding algorithm defined in the IEEE 802.3-2008 standard. The TLK10232 creates consecutive 72-bit data words from the encoded 66-bit code words for transfer over the XAUI interface to the MAC. The information for the two XAUI transfers includes 64 bits of data and 8 bits of control information before 8B/10B encoding.

Not all 64B/66B block payloads are valid. Invalid block payloads are handled by the 64B/66B decoder block and appropriate error handling is provided, as defined in the IEEE 802.3-2008 standard. The decoding algorithm includes two steps: a descrambling step which descrambles 64 bits of the 66-bit code word with the scrambling polynomial $x^{58}+x^{39}+1$, and a decoding step which converts the 66 bits of data received into 64 bits of data and 8 bits of control information. These words are sent to the receive CTC FIFO.

3.9 Transmit Gearbox

The function of the transmit gearbox is to convert the 66-bit encoded, scrambled data stream into a 16-bit-wide data stream to be sent out to the serializer and ultimately to the physical medium attachment (PMA) device. The gearbox is needed because while the effective bit rate of the 66-bit data stream is equal to the effective bit rate of the 16-bit data, the clock rates of the two buses are of different frequencies.

3.10 Receive Gearbox

While the transmit gearbox only performs the task of converting 66-bit data to be transported on to the 16-bit serializer, the receive gearbox has more to do than just the reverse of this function. The receive gearbox must also determine where within the incoming data stream the boundaries of the 66-bit code words are.

The receive gearbox has the responsibility of initially synchronizing the header field of the code words and continuously monitoring the ongoing synchronization. After obtaining synchronization to the incoming data stream, the gearbox assembles 66-bit code words and presents these to the 64B/66B decoder.

Note that in FEC mode, the Receive Gearbox blindly converts 16-bit data to 66-bit data and depends on the RX FEC logic to frame align the data.

3.11 XAUI Lane Alignment / Code Gen (XAUI PCS)

The XAUI interface standard is defined to allow for 21 UI of skew between lanes. This block is implemented to handle up to 30 UI (XAUI UI) of skew between lanes using /A/ characters. The state machine follows the standard 802.3-2008 defined state machine.

3.12 Inter-Packet Gap (IPG) Characters

The XAUI interface transports information that consists of packets and inter-packet gap (IPG) characters. The IEEE 802.3-2008 standard defines that the IPG, when transferred over the XAUI interface, consists of alignment characters (/A/), control characters (/K/) and replacement characters (/R/).

TLK10232 converts all AKR characters to IDLE characters, performs insertions or deletions on the IDLE characters, and transmits only encoded IDLE characters out to the 10GBASE-KR interface. The receive channel expects encoded IDLE characters to enter the 10GBASE-KR interface, and performs insertions and deletions on IDLE characters and then converts IDLE characters back to AKR characters. Any AKR characters received on the high speed interface are by default converted to IDLE characters for reconversion to AKR columns.

Both the transmit and receive FIFOs rely upon a valid IDLE stream to perform clock tolerance compensation (CTC).

3.13 Clock Tolerance Compensation (CTC)

The XAUI interface is defined to allow for separate clock domains on each side of the link. Though the reference clocks for two devices on a XAUI link have the same specified frequencies, there can be slight differences that, if not compensated for, will lead to over or under run of the FIFO's on the receive/transmit data path. The TLK10232 provides compensation for these differences in clock frequencies via the insertion or the removal of idle (/I/) characters on all lanes, as shown in Figure 3-3 and Figure 3-4.

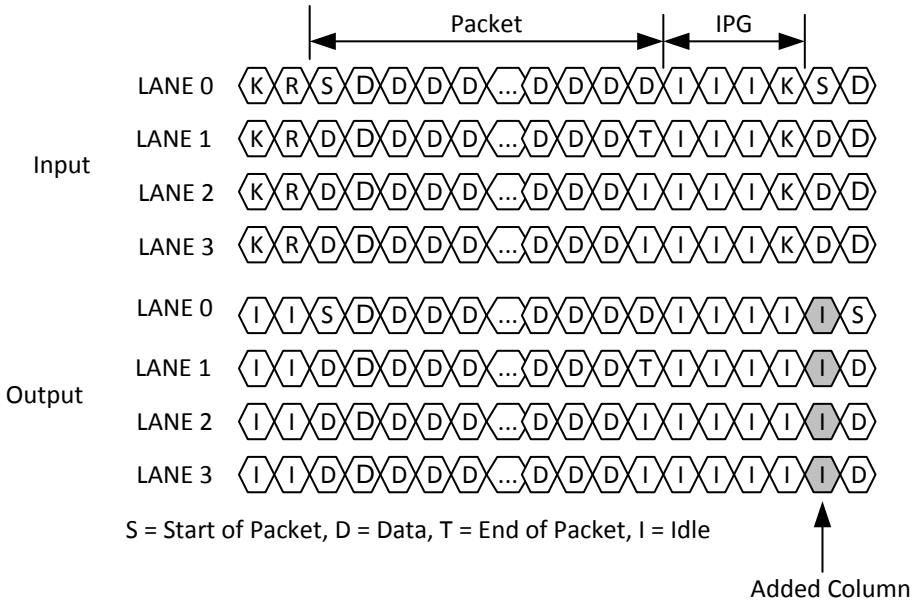


Figure 3-3. Clock Tolerance Compensation: Add

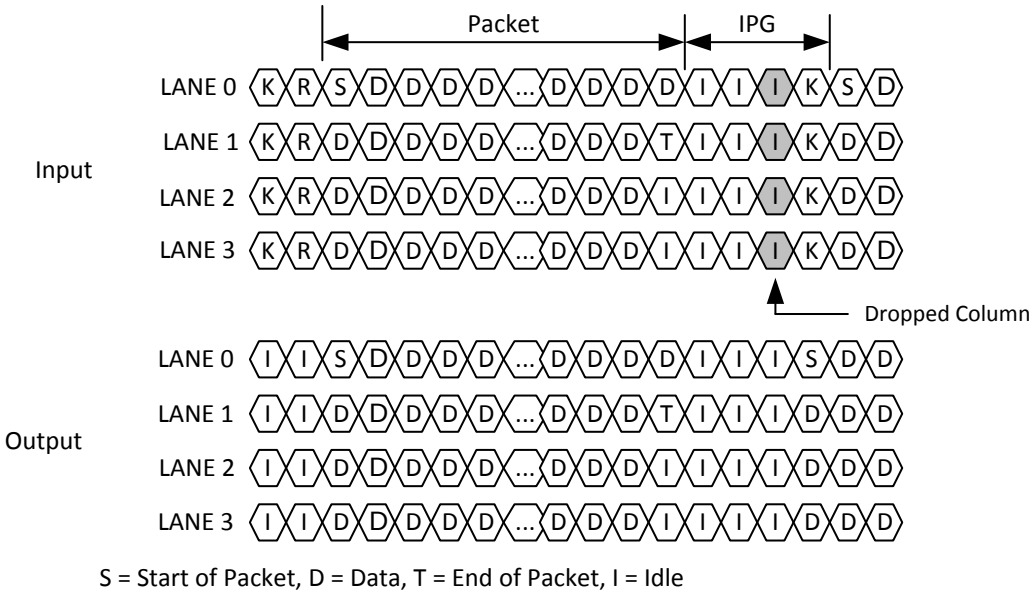


Figure 3-4. Clock Tolerance Compensation: Drop

The TLK10232 allows for provisioning of both the CTC FIFO depth and the low/high watermark thresholds that trigger idle insertion/deletion beyond the standard requirements. This allows for optimization between maximum clock tolerance and packet length. For more information on the TLK10232 CTC provisioning, see Appendix A.

3.14 10GBASE-KR Auto-Negotiation

When TLK10232 is selected to operate in 10GKR/1G-KX mode (MODE_SEL pin held low), Clause 73 Auto-Negotiation will commence after power up or hardware or software reset. The data path chosen from the result of Auto-Negotiation will be the highest speed of 10G-KR or 1G-KX as advertised in the MDIO ability fields (set to 10G-KR by default). If 10G-KR is chosen, link training will commence immediately following the completion of Auto-Negotiation. Legacy devices that operate in 1G-KX mode and do not support Clause 73 Auto Negotiation will be recognized through the Clause 73 parallel detection mechanism.

3.15 10GBASE-KR Link Training

Link training for 10G-KR mode is performed after auto-negotiation, and follows the procedure described in IEEE 802.3-2008. The high speed TX SERDES side will update pre-emphasis tap coefficients as requested through the Coefficient update field. Received training patterns are monitored for bit errors (MDIO configurable), and requests are made to update partner channel TX coefficients until optimal settings are achieved.

The RX link training algorithm consists of sending a series of requests to move the link partner's transmitter tap coefficients to the center point of an error free region. Once link training has completed, the 10G-KR data path is enabled. If link is lost, the entire process repeats with auto-negotiation, link training, and 10G-KR mode.

TLK10232 also offers a manual mode whereby coefficient update requests are handled through external software management.

3.16 10GBASE-KR Line Rate, PLL Settings, and Reference Clock Selection

The TLK10232 includes internal low-jitter high quality oscillators that are used as frequency multipliers for the low speed and high speed SERDES and other internal circuits of the device. Specific MDIO registers are available for SERDES rate and PLL multiplier selection to match line rates and reference clock (REFCLK0/1) frequencies for various applications.

The external differential reference clock has a large operating frequency range allowing support for many different applications. A low-jitter reference clock should be used, and its frequency accuracy should be within ±200 PPM of the incoming serial data rate (±100 PPM of nominal data rate).

When the TLK10232 device is set to operate in the 10GBASE-KR mode with a low speed side line rate of 3.125 Gbps and a high speed side line rate of 10.3125 Gbps, the reference clock choices are as shown in Table 3-1. In general, using a higher reference clock frequency results in improved jitter performance.

Table 3-1. Specific Line Rate and Reference Clock Selection for the 10GBASE-KR Mode:

LOW SPEED SIDE					HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)		Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
3125	10	Full	156.25		10312.5	16.5	Full	156.25
3125	5	Full	312.5		10312.5	8.25	Full	312.5

3.17 10GBASE-KR Test Pattern Support

The TLK10232 has the capability to generate and verify various test patterns for self-test and system diagnostic measurements. The following test patterns are supported:

- High Speed (HS) Side: PRBS 2^7 – 1, PRBS 2^{23} – 1, PRBS 2^{31} – 1, Square Wave with Provisionable Length, and KR Pseudo-Random Pattern
- Low Speed (LS) Side: PRBS 2^7 – 1, PRBS 2^{23} – 1, PRBS 2^{31} – 1, High Frequency, Low Frequency, Mixed Frequency, CRPAT, CJPAT.

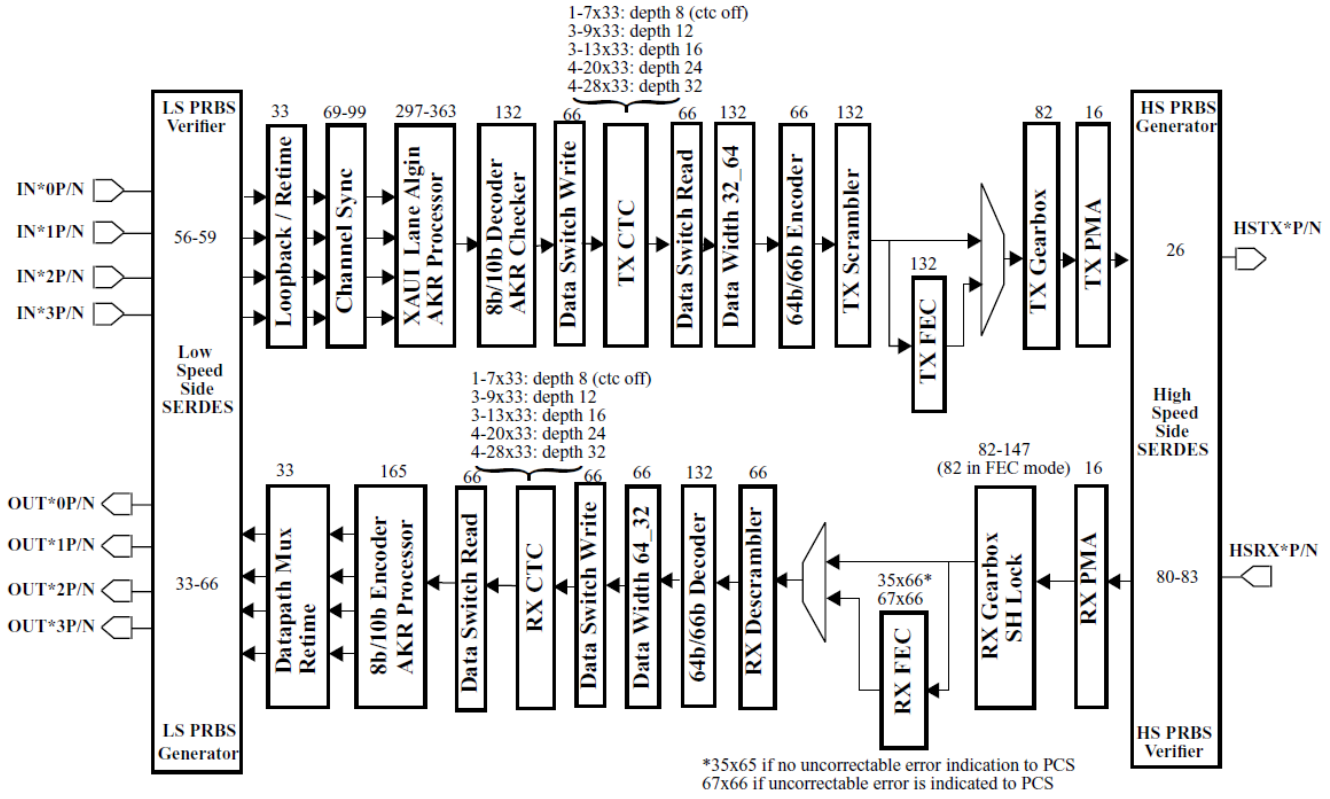
The TLK10232 provides two pins: PRBSEN and PRBS_PASS, for additional control and monitoring of PRBS pattern generation and verification. When PRBSEN is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high speed and low speed sides of all channels. PRBS 2^7-1 is selected by default, and can be changed through MDIO.

When PRBS test is enabled (PRBSEN=1):

- PRBS_PASS = 1 indicates that PRBS pattern reception is error free.
- PRBS_PASS = 0 indicates that a PRBS error is detected. The channel, the side (high speed or low speed), and the lane (for low speed side) that this signal refers to is chosen through MDIO.

3.18 10GBASE-KR Latency

The latency through the TLK10232 in 10GBASE-KR mode is as shown in Figure 3-5. Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.



TX, FEC bypassed, CTC depth 12: 1269-1569 UI (123ns - 152ns)
NOTE: TX Latency numbers represent no external skew between lanes. External lane skew will increase overall latency

RX, FEC bypassed, CTC depth 12: 838-1203 UI (81ns - 117ns)

Figure 3-5. 10GBASE-KR Mode Latency Per Block

4 1GBASE-KX MODE FUNCTIONAL DESCRIPTION

A simplified block diagram of the 1GBASE-KX data path is shown in Figure 4-1.

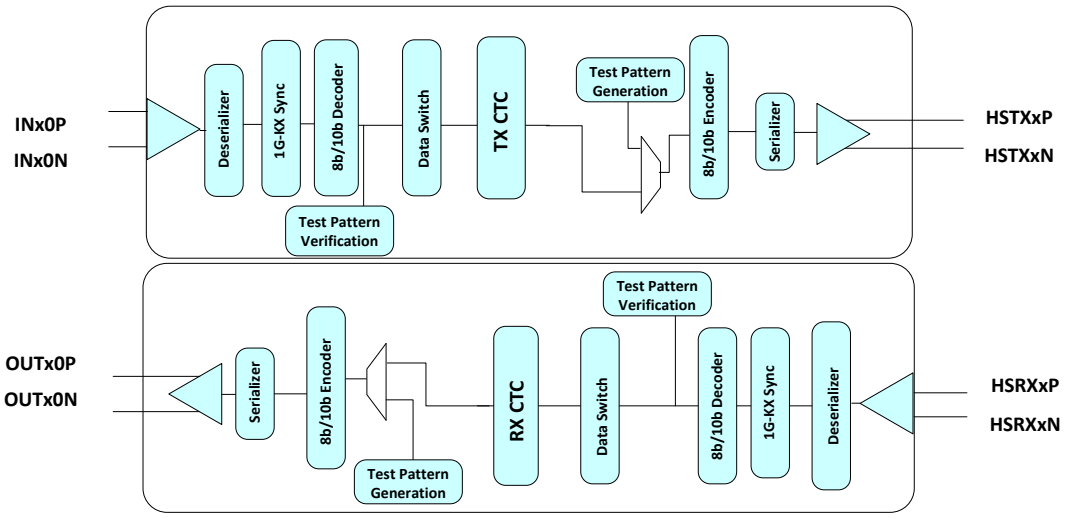


Figure 4-1. A Simplified One Channel Block Diagram of the 1GKX Data Path

4.1 Channel Sync Block

This block is used to align the deserialized signals to the proper 10-bit word boundaries. The Channel Sync block generates a synchronization flag indicating incoming data is synchronized to the correct word boundary. This module implements the synchronization state machine found in Figure 36-9 of the IEEE 802.3-2008 Standard. A synchronization status signal, latched low, is available to indicate synchronization errors.

4.2 8b/10b Encoder and Decoder Blocks

As in the 10GBASE-KR operating mode, these blocks are used to convert between 10-bit (encoded) data and 8-bit data words. They can be optionally bypassed. A code invalid signal, latched low, is available to indicate 8b/10b encode and decode errors.

4.3 TX CTC

The transmit clock tolerance compensation (CTC) block acts as a FIFO with add and delete capabilities, adding and deleting 2 cycles each time to support ±200ppm during IFG (no errors) between the read and write clocks. This block implements a 12 deep asynchronous FIFO with a usable space 8 deep. It has two separate pointer tracking systems. One determines when to delete or insert and another determines when to reset. Inserts and deletes are only allowed during non-errored inter-frame gaps and occurs 2 cycles at a time. It has an auto reset feature once collision occurs. If a collision occurs, the indication is latched high until read by MDIO.

4.4 1GBASE-KX Line Rate, PLL Settings, and Reference Clock Selection

When the TLK10232 is configured to operate in the 1GBASE-KX mode, the available line rates, reference clock frequencies, and corresponding PLL multipliers are summarized in Table 4-1.

Table 4-1. Specific Line Rate and Reference Clock Selection for the 1GBASE-KX Mode

LOW SPEED SIDE					HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)		Line Rate (Mbps[1])	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
3125[2]	10	Full	156.25		3125[2]	10	Full	156.25
3125[2]	5	Full	312.5		3125[2]	5	Full	312.5
1250	10	Half	125[2]		1250	20	Quarter	125[2]
1250	8	Half	156.25		1250	16	Quarter	156.25
1250	8	Quarter	312.5		1250	8	Quarter	312.5

(1) High Speed Side SERDES runs at 2x effective data rate.
(2) Manual mode only, as auto negotiation does not support 125Mhz REFCLK or line rate of 3125Mbps. To disable automatic setting of PLL and rate modes, write 1'b1 to bit 13 of register 0x1E.001D.

4.5 Test Pattern Generator

In 1G-KX mode, this block can be used to generate test patterns allowing the 1G-KX channel to be tested for compliance while in a system environment or for diagnostic purposes. Test patterns generated are high/low/mixed frequency and CRPAT long or short.

4.6 Test Pattern Verifier

The 1G-KX test pattern verifier performs the verification and error reporting for the CRPAT Long and Short test patterns specified in Annex 36A of the IEEE 802.3-2008 standard. Errors are reported to MDIO registers.

4.7 1GBASE-KX Mode Latency

The latency through the TLK10232 in 1G-KX mode is as shown in Figure 4-2. Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.

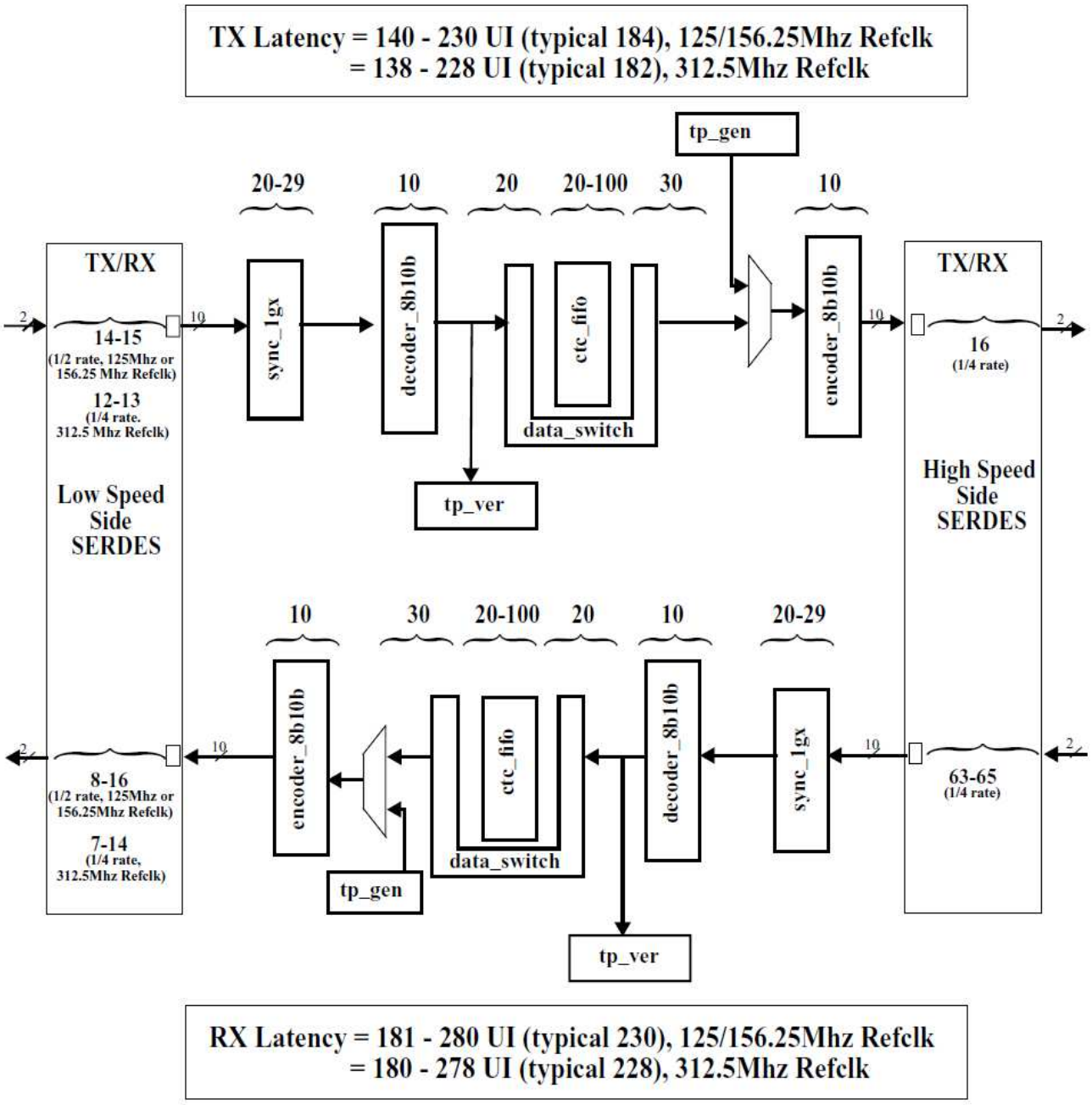


Figure 4-2. 1G-KX Mode Latency

5 GENERAL PURPOSE (10G) SERDES MODE FUNCTIONAL DESCRIPTION

A block diagram showing the transmit and receive data paths of the TLK10232 operating in General Purpose (10G) SerDes mode is shown in Figure 5-1.

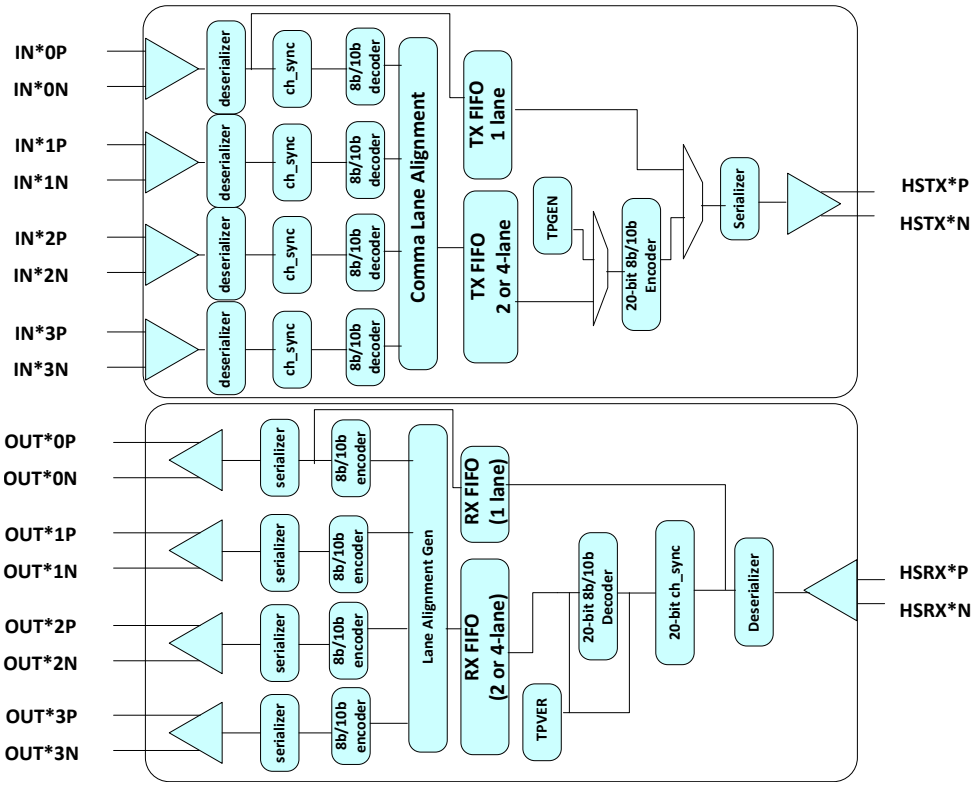


Figure 5-1. Block Diagram Showing General Purpose SerDes Mode

5.1 General Purpose SERDES Transmit Data Path

The TLK10232 General Purpose SERDES low speed to high speed (transmit) data path with the device configured to operate in the normal transceiver (mission) mode is shown in the upper half of Figure 5-1. In this mode, 8B/10B encoded serial data (IN*P/N) in 2 or 4 lanes is received by the low speed side SERDES and deserialized into 10-bit parallel data for each lane. The data in each individual lane is then byte aligned (channel synchronized) and then 8B/10B decoded into 8-bit parallel data for each lane. The lane data is then lane aligned by the Lane Alignment Slave. 32 bits of lane aligned parallel data is input to a transmit FIFO which delivers it to an 8B/10B encoder, 16 data bits at a time. The resulting 20-bit 8B/10B encoded parallel data is sent to the high speed side SERDES for serialization and output through the HSTX*P/N pins.

5.2 General Purpose SERDES Receive Data Path

With the device configured to operate in the normal transceiver (mission) mode, the high speed to low speed (receive) data path is shown in the lower half of Figure 5-1. 8B/10B encoded serial data (HSRX*P/N) is received by the high speed side SERDES and deserialized into 20-bit parallel data. The data is then byte aligned, 8B/10B decoded into 16-bit parallel data, and then delivered to a receive FIFO. The receive FIFO in turn delivers 32-bit parallel data to the Lane Alignment Master which splits the data into the same number of lanes as configured on the transmit data path. The lane data is then 8B/10B encoded and the resulting 10-bit parallel data for each lane is input to the low speed side SERDES for serialization and output through the OUT*P/N pins.

5.3 Channel Synchronization

As in the 10GBASE-KR mode, the channel synchronization block is used in the 10G General Purpose SERDES mode to align received serial data to a defined byte boundary. The channel synchronization block detects the comma pattern found in the K28.5 character, and follows the synchronization flowchart shown in Figure 3-2.

5.4 8B/10B Encoder and Decoder

As in the 10GBASE-KR and 1GBASE-KX modes, the 8B/10B encoder and decoder blocks are used to convert between 10-bit (encoded) and 8-bit (unencoded) data words.

5.5 Lane Alignment Scheme for 8b/10b General Purpose Serdes Mode

Lower rate multi-lane serial signals per channel must be byte aligned and lane aligned such that high speed multiplexing (proper reconstruction of higher rate signal) is possible. For that reason, the TLK10232 implements a special lane alignment scheme on the low speed (LS) side for 8b/10b data that does not contain XAUI alignment characters.

During lane alignment, a proprietary pattern (or a custom comma compliant data stream) is sent by the LS transmitter to the LS receiver on each active lane. This pattern allows the LS receiver to both delineate byte boundaries within a lower speed lane and align bytes across the lanes (2 or 4) such that the original higher rate data ordering is restored.

Lane alignment completes successfully when the LS receiver asserts a “Link Status OK” signal monitored by the LS transmitter on the link partner device such as an FPGA. The TLK10232 sends out the “Link Status OK” signals through the LS_OK_OUT_A/B output pins, and monitors the “Link Status OK” signals from the link partner device through the LS_OK_IN_A/B input pins. If the link partner device does not need the TLK10232 Lane Alignment Master (LAM) to send proprietary lane alignment pattern, LS_OK_IN_A/B can be tied high on the application board or set through MDIO register bits.

The lane alignment scheme is activated under any of the following conditions:

- Device/System power up (after configuration/provisioning)
- Loss of channel synchronization assertion on any enabled LS lane
- Loss of signal assertion on any enabled LS lane
- LS SERDES PLL Lock indication deassertion
- After device configuration change
- After software determined LS 8B/10B decoder error rate threshold exceeded
- After device reset is deasserted
- Any time the LS receiver deasserts “Link Status OK”.
- Presence of reoccurring higher level / protocol framing errors

All the above conditions are selectable through MDIO register provisioning.

The block diagram of the lane alignment scheme is shown in Figure 5-2.

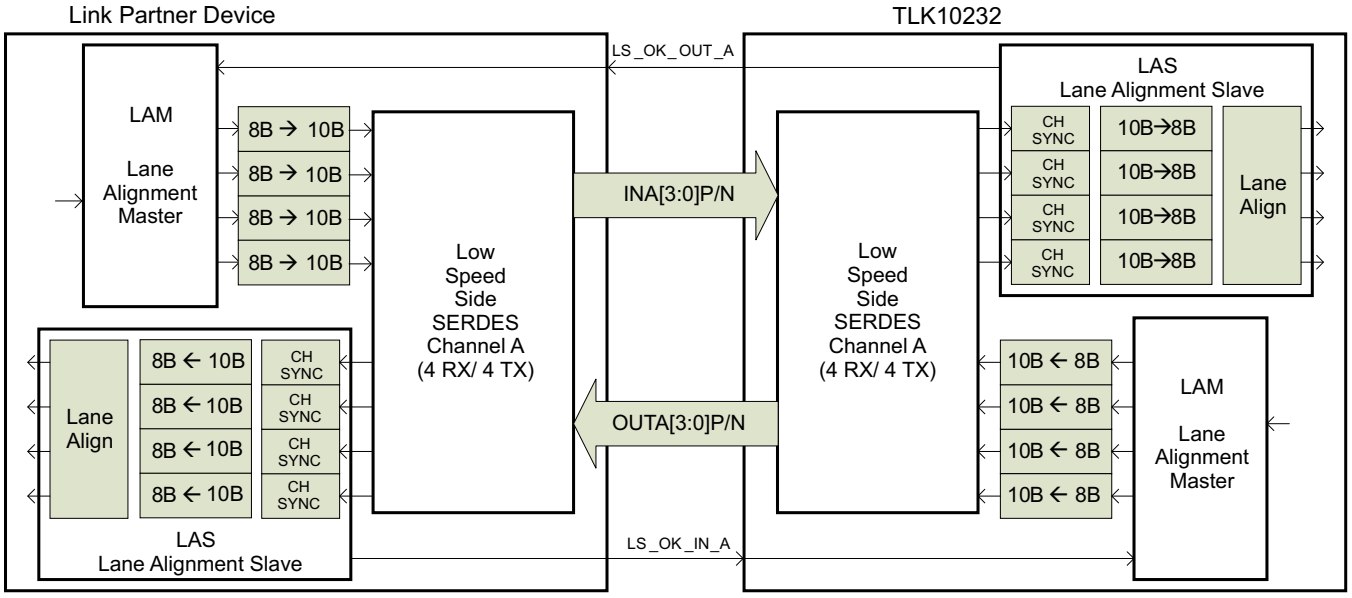


Figure 5-2. Block Diagram of the Lane Alignment Scheme

5.6 Lane Alignment Components

- Lane Alignment Master (LAM)
  - Responsible for generating proprietary LS lane alignment initialization pattern
  - Resides in the TLK10232 receive path (one instance per channel)
    - Responsible for bringing up LS receive link for the data sent from the TLK10232 to a link partner device
    - Monitors the LS_OK_IN pins for “Link Status OK” signals sent from the Lane Alignment Slave (LAS) of the link partner device
  - Resides in the link partner device (one instance per channel)
    - Responsible for bringing up LS transmit link for the data sent from the link partner device to the TLK10232
    - Monitors the “Link Status OK” signals sent from the LS_OK_OUT pins of the Lane Alignment Slave (LAS) of the TLK10232
- Lane Alignment Slave (LAS)
  - Responsible for monitoring the LS lane alignment initialization pattern
  - Performs channel synchronization per lane (2 or 4 lanes) through byte rotation
  - Performs lane alignment and realignment of bytes across lanes
  - Resides in the TLK10232 transmit path (one instance per channel)
    - Generates the “Link Status OK” signal for the LAM on the link partner device
  - Resides in the link partner device (one instance per channel)
    - Generates the “Link Status OK” signal for the LAM on the TLK10232 device.

Reference code from Texas Instruments is available for the LAM and LAS modules for easy integration into FPGAs.

5.7 Lane Alignment Operation

During lane alignment, the LAM sends a repeating pattern of 49 characters (control + data) simultaneously across all enabled LS lanes. These simultaneous streams are then encoded by 8B/10B encoders in parallel. The proprietary lane alignment pattern consists of the following characters:

/K28.5/ (CTL=1, Data=0xBC)

Repeat the following sequence of 12 characters four times:

/D30.5/ (CTL=0, Data=0xBE)
/D23.6/ (CTL=0, Data=0xD7)
/D3.1/ (CTL=0, Data=0x23)
/D7.2/ (CTL=0, Data=0x47)
/D11.3/ (CTL=0, Data=0x6B)
/D15.4/ (CTL=0, Data=0x8F)
/D19.5/ (CTL=0, Data=0xB3)
/D20.0/ (CTL=0, Data=0x14)
/D30.2/ (CTL=0, Data=0x5E)
/D27.7/ (CTL=0, Data=0xFB)
/D21.1/ (CTL=0, Data=0x35)
/D25.2/ (CTL=0, Data=0x59)

The above 49-character sequence is repeated until LS_OK_IN is asserted. Once LS_OK_IN is asserted, the LAM resumes transmitting traffic received from the high speed side SERDES immediately.

The TLK10232 performs lane alignment across the lanes similar in fashion to the IEEE 802.3-2008 (XAUI) specification. XAUI only operates across 4 lanes while LAS operates with 2 or 4 lanes. The lane alignment state machine is shown in Figure 5-3. The TLK10232 uses the comma (K28.5) character for lane to lane alignment by default, but can be provisioned to use XAUI's /A/ character as well.

Lane alignment checking is not performed by the LAS after lane alignment is achieved. After LAM detects that the LS_OK_IN signal is asserted, normal system traffic is carried instead of the proprietary lane alignment pattern.

Channel synchronization is performed during lane alignment and normal system operation.

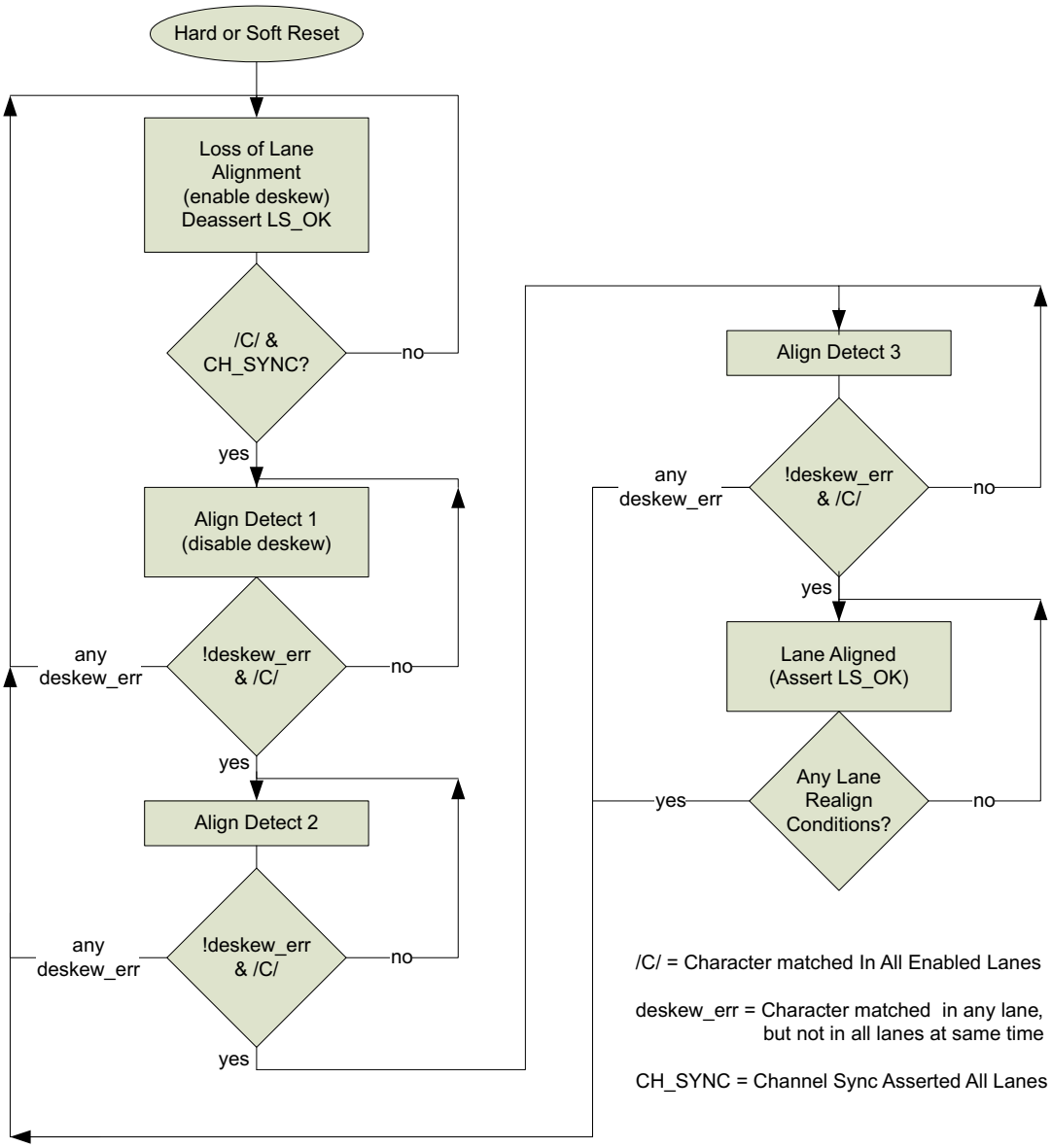


Figure 5-3. Lane Alignment State Machine

5.8 Line Rate, SERDES PLL Settings, and Reference Clock Selection for the General Purpose SERDES Mode

When the TLK10232 is set to operate in the General Purpose SERDES mode, the following tables show a summary of line rates and reference clock frequencies used for CPRI/OBSAI for 1:1, 2:1 and 4:1 operation modes.

Table 5-1. Specific Line Rate Selection for the 1:1 General Purpose Operation Mode

LOW SPEED SIDE				HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)	Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
4915.2	20	Full	122.88	4915.2	20	Half	122.88
3840	12.5	Full	153.6	3840	12.5	Half	153.6
3125	10	Full	156.25	3125	10	Half	156.25
3125	5	Full	312.5	3125	5	Half	312.5
3072	10	Full	153.6	3072	10	Half	153.6
2457.6	8/10	Full	153.6/122.88	2457.6	16/20	Quarter	153.6/122.88
1920	12.5	Half	153.6	1920	12.5	Quarter	153.6
1536	10	Half	153.6	1536	10	Quarter	153.6
1228.8	8/10	Half	153.6/122.88	1228.8	16/20	Eighth	153.6/122.88

Table 5-2. Specific Line Rate and Reference Clock Selection for the 2:1 General Purpose Operation Mode

LOW SPEED SIDE				HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)	Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
4915.2	20	Full	122.88	9830.4	20	Full	122.88
3840	12.5	Full	153.6	7680	12.5	Full	153.6
3072	10	Full	153.6	6144	10	Full	153.6
2457.6	8/10	Full	153.6/122.88	4915.2	16/20	Half	153.6/122.88
1920	12.5	Half	153.6	3840	12.5	Half	153.6
1536	10	Half	153.6	3072	10	Half	153.6
1228.8	8/10	Half	153.6/122.88	2457.6	16/20	Quarter	153.6/122.88
768	10	Quarter	153.6	1536	10	Quarter	153.6
614.4	8/10	Quarter	153.6/122.88	1228.8	16/20	Eighth	153.6/122.88

Table 5-3. Specific Line Rate and Reference Clock Selection for the 4:1 General Purpose Operation Mode

LOW SPEED SIDE				HIGH SPEED SIDE			
Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)	Line Rate (Mbps)	SERDES PLL Multiplier	Rate	REFCLKP/N (MHz)
2457.6	8/10	Full	153.6/122.88	9830.4	16/20	Full	153.6/122.88
1536	10	Half	153.6	6144	10	Full	153.6
1228.8	8/10	Half	153.6/122.88	4915.2	16/20	Half	153.6/122.88
768	10	Quarter	153.6	3072	10	Half	153.6
614.4	8/10	Quarter	153.6/122.88	2457.6	16/20	Quarter	153.6/122.88

Table 5-1, Table 5-2, and Table 5-3 indicate two possible reference clock frequencies for CPRI/OBSAI applications: 153.6MHz and 122.88MHz, which can be used based on the application preference. The SERDES PLL Multiplier (MPY) has been given for each reference clock frequency respectively. For each channel, the low speed side and the high speed side SERDES use the same reference clock frequency. Note that Channel A and B are independent and their application rates and references clocks are separate.

For other line rates not shown in Table 5-1, Table 5-2, or Table 5-3, valid reference clock frequencies can be selected with the help of the information provided in Table 5-4 and Table 5-5 for the low speed and high speed side SERDES. The reference clock frequency has to be the same for the two SERDES and must be within the specified valid ranges for different PLL multipliers.

Table 5-4. Line Rate and Reference Clock Frequency Ranges for the Low Speed Side SERDES (General Purpose Mode)

SERDES PLL Multiplier (MPY)	Reference Clock (MHz)		Full Rate (Gbps)		Half Rate (Gbps)		Quarter Rate (Gbps)	
	Min	Max	Min	Max	Min	Max	Min	Max
4	250	425	2	3.4	1	1.7	0.5	0.85
5	200	425	2	4.25	1	2.125	0.5	1.0625
6	166.667	416.667	2	5	1	2.5	0.5	1.25
8	125	312.5	2	5	1	2.5	0.5	1.25
10	122.88	250	2.4576	5	1.2288	2.5	0.6144	1.25
12	122.88	208.333	2.94912	5	1.47456	2.5	0.73728	1.25
12.5	122.88	200	3.072	5	1.536	2.5	0.768	1.25
15	122.88	166.667	3.6864	5	1.8432	2.5	0.9216	1.25
20	122.88	125	4.9152	5	2.4576	2.5	1.2288	1.25
RateScale: Full Rate = 0.5, Half Rate = 1, Quarter Rate = 2								

Table 5-5. Line Rate and Reference Clock Frequency Ranges for the High Speed Side SERDES (General Purpose Mode)

SERDES PLL Multiplier (MPY)	Reference Clock (MHz)		Full Rate (Gbps)		Half Rate (Gbps)		Quarter Rate (Gbps)		Eighth Rate (Gbps)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
4	375	425	6	6.8	3	3.4	1.5	1.7		
5	300	425	6	8.5	3	4.25	1.5	2.125	1.0	1.0625
6	250	416.667	6	10	3	5	1.5	2.5	1.0	1.25
8	187.5	312.5	6	10	3	5	1.5	2.5	1.0	1.25
10	150	250	6	10	3	5	1.5	2.5	1.0	1.25
12	125	208.333	6	10	3	5	1.5	2.5	1.0	1.25
12.5	153.6	200	7.68	10	3.84	5	1.92	2.5	1.0	1.25
15	122.88	166.667	7.3728	10	3.6864	5	1.8432	2.5	1.0	1.25
16	122.88	156.25	7.86432	10	3.932	5	1.966	2.5	1.0	1.25
20	122.88	125	9.8304	10	4.9152	5	2.4576	2.5	1.2288	1.25
RateScale: Full Rate = 0.25, Half Rate = 0.5, Quarter Rate = 1, Eighth Rate = 2										

For example, in the 2:1 operation mode, if the low speed side line rate is 1.987Gbps, the high-speed side line rate will be 3.974Gbps. The following steps can be taken to make a reference clock frequency selection:

1. Determine the appropriate SERDES rate modes that support the required line rates. Table 5-4 shows that the 1.987Gbps line rate on the low speed side is only supported in the half rate mode (RateScale = 1). Table 5-5 shows that the 3.974Gbps line rate on the high speed side is only supported in the half rate mode (RateScale = 1).
2. For each SERDES side, and for all available PLL multipliers (MPY), compute the corresponding reference clock frequencies using the formula:

   Reference Clock Frequency = (LineRate x RateScale)/MPY

The computed reference clock frequencies are shown in Table 5-6 along with the valid minimum and maximum frequency values.

3. Mark all the common frequencies that appear on both SERDES sides. Note and discard all those that fall outside the allowed range. In this example, the common frequencies are highlighted in Table 5-6. The highest and lowest computed reference clock frequencies must be discarded because they exceed the recommended range.
4. Select any of the remaining marked common reference clock frequencies. Higher reference clock frequencies are generally preferred. In this example, any of the following reference clock frequencies can be selected: 397.4MHz, 331.167MHz, 248.375MHz, 198.7MHz, 165.583MHz, 158.96MHz, and 132.467MHz

Table 5-6. Reference Clock Frequency Selection Example

LOW SPEED SIDE SERDES					HIGH SPEED SIDE SERDES			
SERDES PLL MULTIPLIER	REFERENCE CLOCK FREQUENCY (MHz)				SERDES PLL MULTIPLIER	REFERENCE CLOCK FREQUENCY (MHz)		
	COMPUTED	MIN	MAX			COMPUTED	MIN	MAX
4	~~496.750~~	250	425		4	~~496.750~~	375	425
5	397.400	200	425		5	397.400	300	425
6	331.167	166.667	416.667		6	331.167	250	416.667
8	248.375	125	312.5		8	248.375	187.5	312.5
10	198.700	122.88	250		10	198.700	150	250
12	165.583	122.88	208.333		12	165.583	125	208.333
12.5	158.960	122.88	200		12.5	158.960	153.6	200
15	132.467	122.88	166.667		15	132.467	122.88	166.667
20	~~99.350~~	122.88	125		20	~~99.350~~	122.88	125

5.9 General Purpose SERDES Mode Test Pattern Support

The TLK10232 has the capability to generate and verify various test patterns for self-test and system diagnostic measurements. Most of the same test pattern support is available for 10G General Purpose Mode as for 10G-KR. (See Register 1E.000B for details).

5.10 General Purpose SERDES Mode Latency

The latency through the TLK10232 in General Purpose SERDES mode is as shown in Figure 5-4. Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.

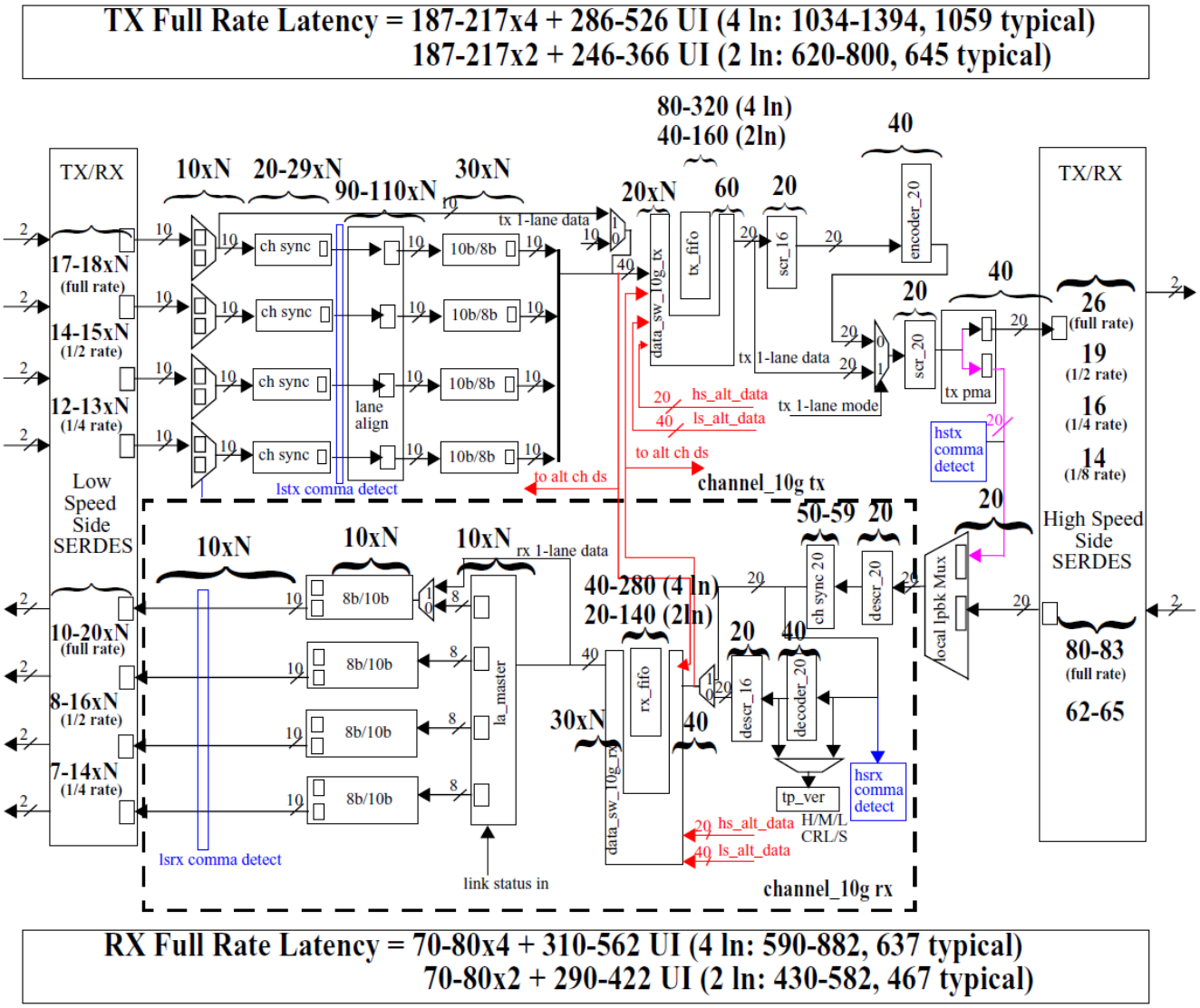


Figure 5-4. General Purpose SERDES Mode Latency

6 CLOCKING ARCHITECTURE (All Modes)

A simplified clocking architecture for the TLK10232 is captured in Figure 6-1. Each channel has an option of operating with a differential reference clock provided either on pins REFCLK0P/N or REFCLK1P/N. The choice is made either through MDIO or through REFCLK_SEL pins. The reference clock frequencies for each channel can be chosen independently. For each channel, the low speed side SERDES, high speed side SERDES and the associated part of the digital core can operate from the same reference clock.

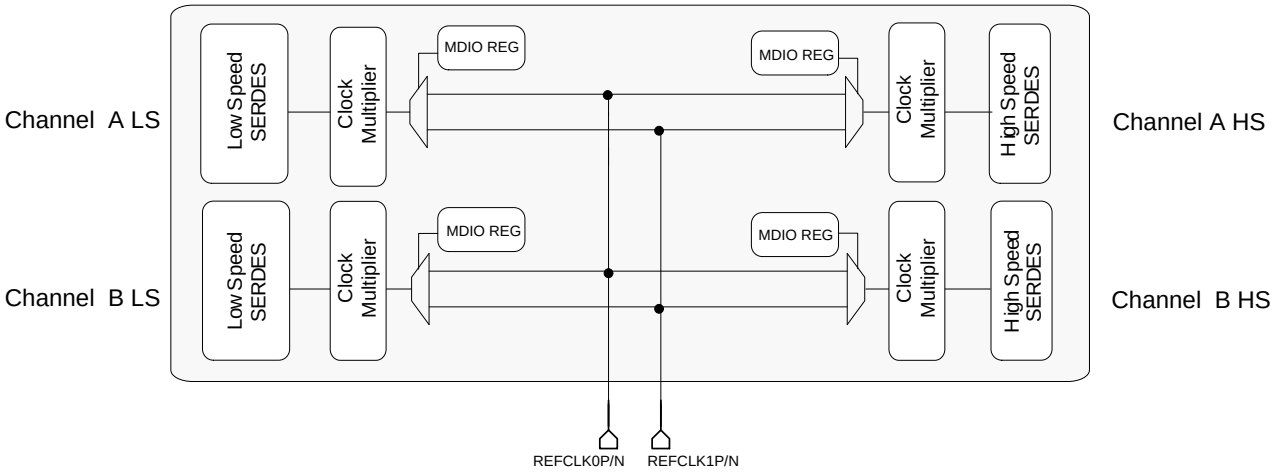


Figure 6-1. Reference Clock Architecture

The TLK10232 has two output clock ports - CLKOUTAP/N and CLKOUTBP/N. Both of these output ports can be configured to output the recovered byte clock of either channel's low speed or high speed sides. Output clocks can also be chosen to be synchronous with the transmit clock rate. Various divider values can be chosen using the MDIO interface. The maximum CLKOUT frequency is 500 MHz.

7 ADDITIONAL FEATURES

7.1 Integrated Smart Switch

The TLK10232 allows for adjustable routing of data within the device. Each output port may be configured to output data corresponding to any input port.

Figure 7-1 illustrates the different possible data path routings.

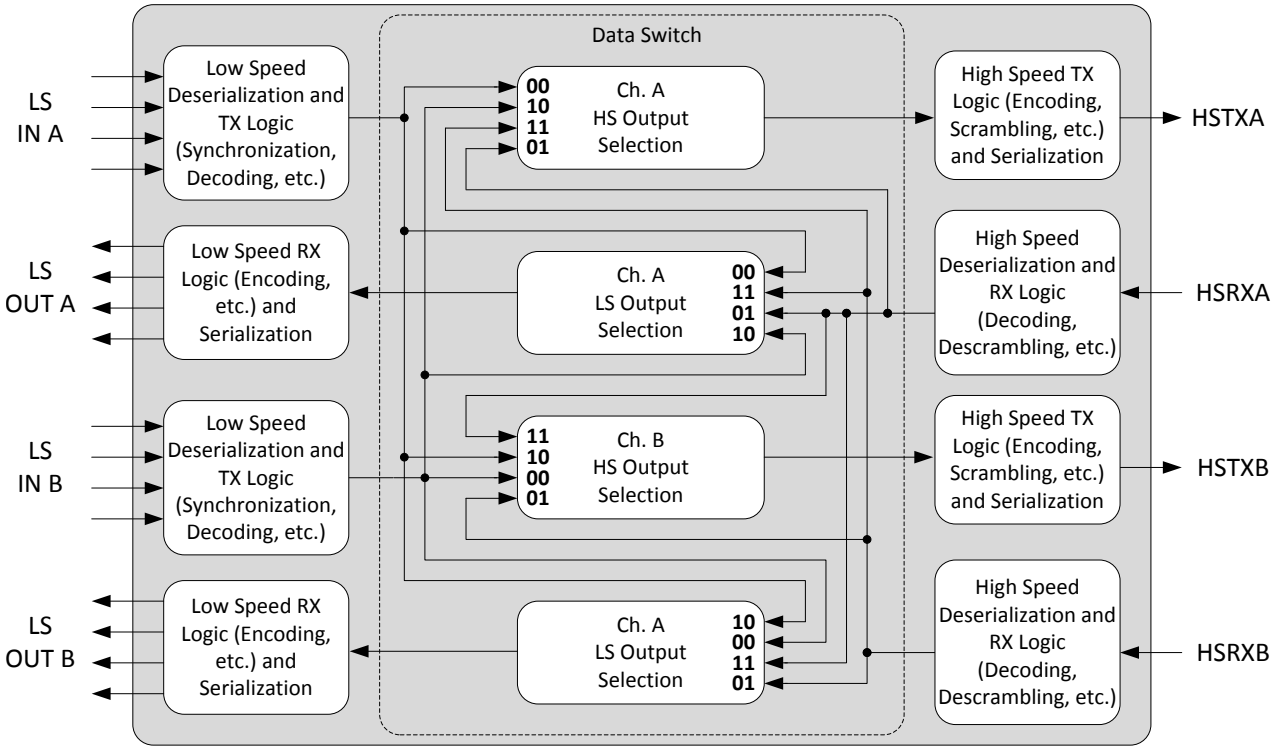


Figure 7-1. Signal Routings for Integrated Smart Switch

7.2 Intelligent Switching Modes

The TLK10232 supports various switching modes that allow for the user to choose when changes in data routing take effect. There are three options:

1. Wait for the end of the current packet, insert IDLEs, then switch to the new channel at the start of its next packet. This option allows the current packet to complete so that data is not lost.
2. Drop current packet and insert a programmable character (such as Local Fault), then switch to the new channel at the start of its next packet. This can provide a more immediate switch-over at the expense of the current packet's data.
3. Immediately switch lanes without packet monitoring.

For more information on selecting different intelligent switching modes, see MDIO register bits 0x1E.0017 through 0x1E.001B.

7.3 Serial Loopback Modes

The TLK10232 supports internal loopback of the serial output signals for self-test and system diagnostic purposes. Loopback mode can be enabled independently for each SERDES via MDIO register bits. When loopback mode is enabled for a particular SERDES, the serial output data will be internally routed to the SERDES's serial input port. The output data will remain available for monitoring on the output pins.

7.4 Latency Measurement Function (General Purpose SerDes Mode)

The TLK10232 includes a latency measurement function to support CPRI and OBSAI type applications. There are two start and two stop locations for the latency counter as shown in Figure 7-2 for Channel A. The start and stop locations are selectable through MDIO register bits. The elapsed time from a comma detected at an assigned counter start location of a particular channel to a comma detected at an assigned counter stop location of the same channel is measured and reported through the MDIO interface. The function operates on one channel at a time. The following three control characters (containing commas) are monitored:

1. K28.1 (control = 1, data = 0x3C)
2. K28.5 (control = 1, data = 0xBC)
3. K28.7 (control = 1, data = 0xFC).

The first comma found at the assigned counter start location will start up the latency counter. The first comma detected at the assigned counter stop location will stop the latency counter. The 20-bit latency counter result of this measurement is readable through the MDIO interface. The accuracy of the measurement is a function of the serial bit rate at which the channel being measured is operating. The register will return a value of 0xFFFFF if the duration between transmit and receive comma detection exceeds the depth of the counter. Only one measurement value is stored internally until the 20-bit results counter is read. The counter will return zero in cases where a transmit comma was never detected (indicating the results counter never began counting). In addition, the stopwatch counter can be configured to be started or stopped manually based on the state of the PRTAD0 pin (see MDIO register map for details).

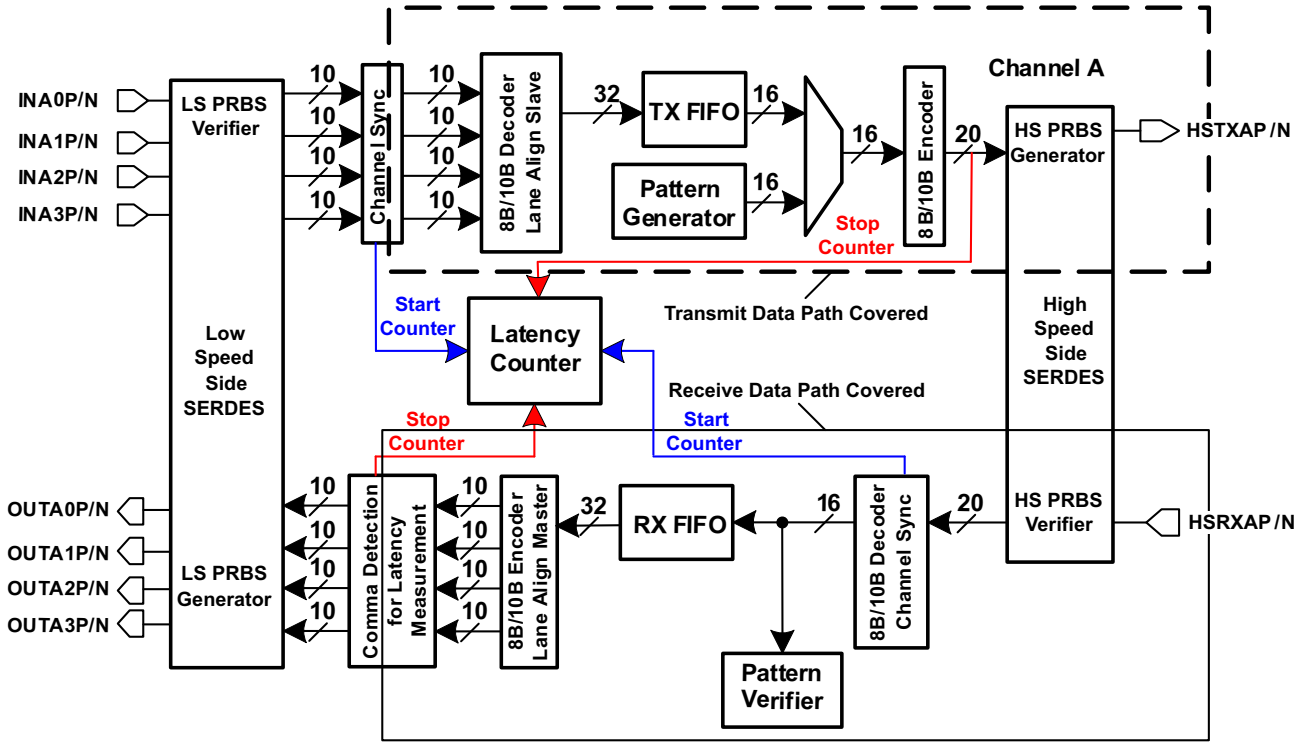


Figure 7-2. Location of TX and RX Comma Character Detection (Only Channel A Shown)

In high speed side SERDES full rate mode, the latency measurement function runs off of an internal clock which is equal to the frequency of the transmit serial bit rate divided by 8. In half rate mode, the latency measurement function runs off of an internal clock which is equal to the serial bit rate divided by 4. In quarter rate mode, the latency measurement function runs off of an internal clock which is equal to the serial bit rate divided by 2. In eighth rate mode, the latency measurement function runs off of a clock which is equal to the serial bit rate.

The latency measurement does not include the low speed side transmit SERDES contribution as well as part of the channel synchronization block. The latency introduced by those two is up to (18 + 10) x N high speed side unit intervals (UIs), where N = 2, 4 is the multiplex factor. The latency measurement also doesn't account for the low speed side receive SERDES contribution which is estimated to be up to 20 x N high speed side UIs.

The latency measurement accuracy in all cases is equal to plus or minus one latency measurement clock period. The measurement clock can be divided down if a longer duration measurement is required, in which case the accuracy of the measurement is accordingly reduced. The high speed latency measurement clock is divided by either 1, 2, 4, or 8 via register settings. The measurement clock used is always selected by the channel under test. The high speed latency measurement clock may only be used when operating at one of the serial rates specified in the CPRI/OBSAI specifications. It is also possible to run the latency measurement function off of the recovered byte clock for the channel under test (giving a latency measurement clock frequency equal to the serial bit rate divided by 20).

The accuracy for the standard based CPRI/OBSAI application rates is shown in Table 7-1, and assumes the latency measurement clock is not divided down per user selection (division is required to measure a duration greater than 682us). For each division of 2 in the measurement clock, the accuracy is also reduced by a factor of two.

Table 7-1. CPRI/OBSAI Latency Measurement Function Accuracy (Undivided Measurement Clock)

LINE RATE (Gbps)	RATE	LATENCY CLOCK FREQUENCY (GHz)	ACCURACY (± ns)
1.2288	Eighth	1.2288	0.8138
1.536	Quarter	0.768	1.302
2.4576	Quarter	1.2288	0.8138
3.072	Half	0.768	1.302
3.84	Half	0.96	1.0417
4.9152	Half	1.2288	0.8138
6.144	Full	0.768	1.302
7.68	Full	0.96	1.0417
9.8304	Full	1.2288	0.8138

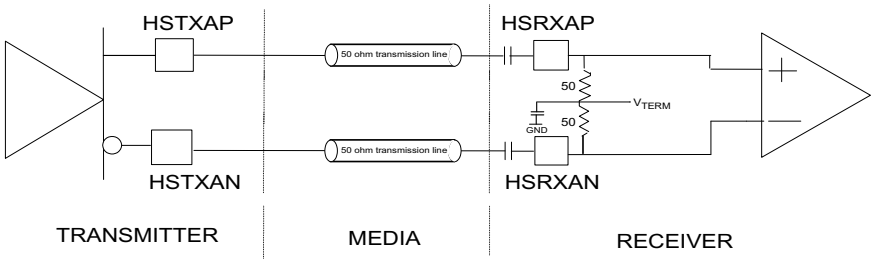
7.5 Power Down Mode

The TLK10232 can be put in power down either through device input pins or through MDIO control register 1E.0001.

- PDTRXA_N: Active low, powers down channel A.
- PDTRXB_N: Active low, powers down channel B.

7.5.1 High Speed CML Output

The high speed data output driver is implemented using Current Mode Logic (CML) with integrated pull up resistors. The transmit outputs must be AC coupled.



NOTE: Channel A HS Side is Shown

Figure 7-3. Example of High Speed I/O AC Coupled Mode

Current Mode Logic (CML) drivers often require external components. The disadvantage of the external component is a limited edge rate due to package and line parasitic. The CML driver on TLK10232 has on-chip 50Ω termination resistors terminated to VDDT, providing optimum performance for increased speed requirements. The transmitter output driver is highly configurable allowing output amplitude and de-emphasis to be tuned to a channel's individual requirements. Software programmability allows for very flexible output amplitude control. Only AC coupled output mode is supported.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to dielectric losses and the skin effect of the media. This causes a “smearing” of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, 4-tap finite impulse response (FIR) transmit de-emphasis is implemented. A highly configurable output driver maximizes flexibility in the end system by allowing de-emphasis and output amplitude to be tuned to a channel’s individual requirements. Output swing control is via MDIO.

7.5.2 High Speed Receiver

The high speed receiver is differential CML with internal termination resistors. The receiver requires AC coupling. The termination impedances of the receivers are configured as 100 Ω with the center tap weakly tied to 0.7×VDDT, and a capacitor is used to create an AC ground (see Figure 7-3).

TLK10232 serial receivers incorporate adaptive equalizers. This circuit compensates for channel insertion loss by amplifying the high frequency components of the signal, reducing inter-symbol interference. Equalization can be enabled or disabled per register settings. Both feed-forward equalization (FFE) and decision feedback equalization (DFE) are used to minimize the pre-cursor and post-cursor components (respectively) of intersymbol interference.

7.5.3 Loss of Signal Output Generation (LOS)

Loss of input signal detection is based on the voltage level of each serial input signal IN*P/N, HSRX*P/N. When LOS indication is enabled and a channel's differential serial receive input level is < 75mVpp, that channel's respective LOS indicator (LOSA or LOSB) will be asserted (high true). If the input signal is >150mVpp, the LOS indicator will be deasserted (low false). Outside of these ranges, the LOS indication is undefined. The LOS indicators can also directly be read through the MDIO interface.

The following additional critical status conditions can be combined with the loss of signal condition enabling additional real-time status signal visibility on the LOS* outputs per channel:

1. Loss of Channel Synchronization Status – Logically OR'd with LOS condition(s) when enabled. Loss of channel synchronization can be optionally logically OR'd (disabled by default) with the internally generated LOS condition (per channel).
2. Loss of PLL Lock Status on LS and HS sides – Logically OR'd with LOS condition(s) when enabled. The internal PLL loss of lock status bit is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
3. Receive 8B/10B Decode Error (Invalid Code Word or Running Disparity Error) – Logically OR'd with LOS condition(s) when enabled. The occurrence of an 8B/10B decode error (invalid code word or disparity error) is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
4. AGCLOCK (Active Gain Control Currently Locked) – Inverted and Logically OR'd with LOS condition(s) when enabled. HS RX SERDES adaptive gain control unlocked indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
5. AZDONE (Auto Zero Calibration Done) - Inverted and Logically OR'd with LOS conditions(s) when enabled. HS RX SERDES auto-zero not done indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).

Refer to Figure 7-4, which shows the detailed implementation of the LOSA signal along with the associated MDIO control registers for the General Purpose SERDES mode. More details about LOS settings including configurations related to the 10GBASE-KR mode can be found in the Programmers Reference section.

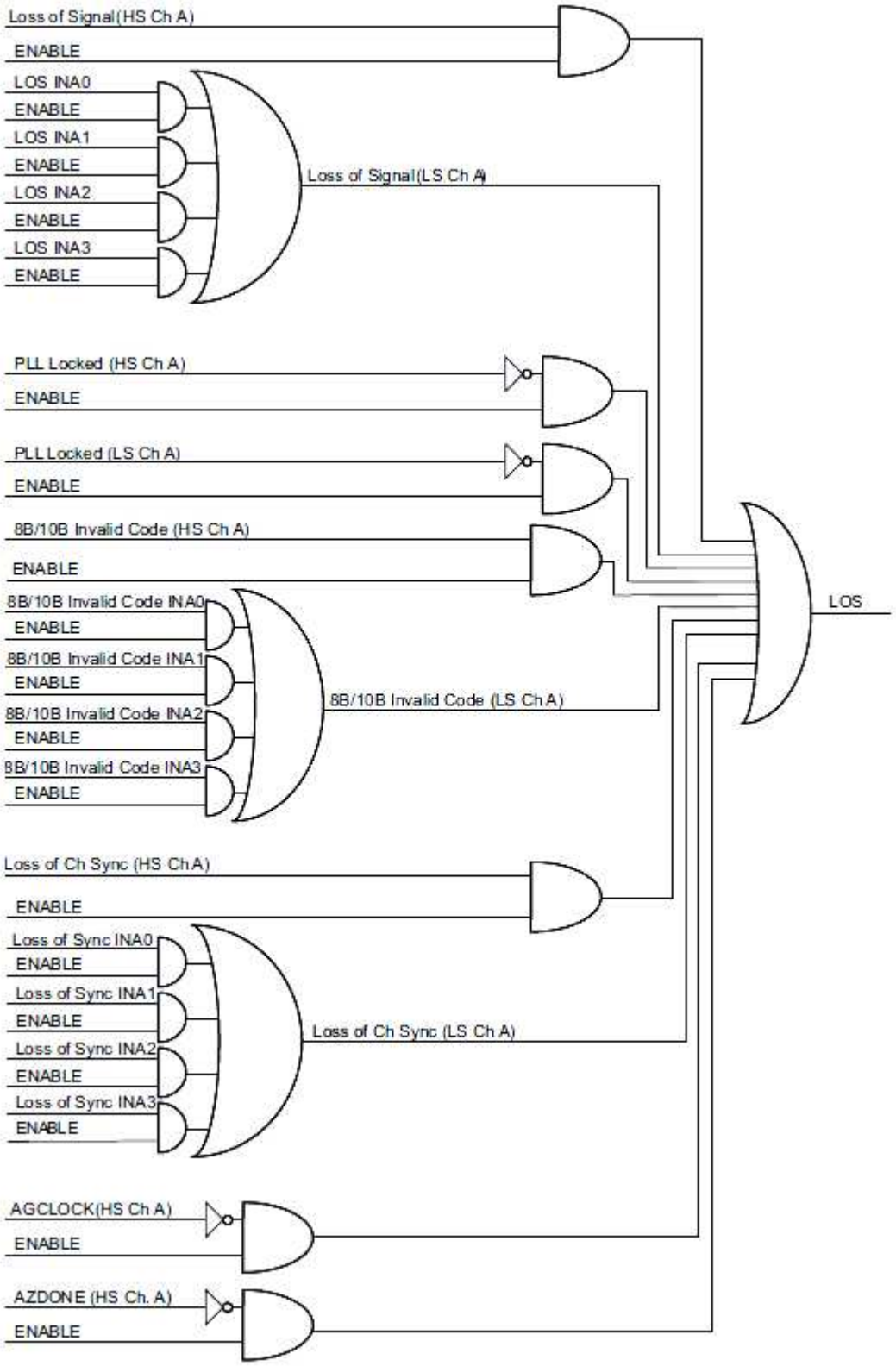


Figure 7-4. LOSA – Logic Circuit Implementation

7.6 MDIO Management Interface

The TLK10232 supports the Management Data Input/Output (MDIO) Interface as defined in Clauses 22 and 45 of the IEEE 802.3-2008 Ethernet specification. The MDIO allows register-based management and control of the serial links.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The device identification and port address are determined by control pins (see Table 2-1). Also, whether the device responds as a Clause 22 or Clause 45 device is also determined by control pin ST (see Table 2-1).

In Clause 45 (ST = 0) and Clause 22 (ST = 1), the top 4 control pins PRTAD[4:1] determine the device port address. In this mode, TLK10232 will respond if the PHY address field on the MDIO protocol (PA[4:1]) matches PRTAD[4:1] pin value. In both these modes the 2 individual channels in TLK10232 are classified as 2 different ports. So for any PRTAD[4:1] value there will be 2 ports per TLK10232. The LSB of PHY address field (PA[0]) will determine which channel/port within TLK10232 to respond.

If PA[0] = 1'b0, TLK10232 Channel A will respond.
If PA[0] = 1'b1, TLK10232 Channel B will respond.

In Clause 22 (ST = 1) mode, only 32 (5'b00000 to 5'b11111) register addresses can be accessed through standard protocol. Due to this limitation, an indirect addressing method (More description in Clause 22 Indirect Addressing section) is implemented to provide access to all device specific control/status registers that cannot be accessed through the standard Clause 22 register address space.

Write transactions which address an invalid register or device or a read only register will be ignored. Read transactions which address an invalid register or device will return a 0.

7.7 MDIO Protocol Timing

Timing for a Clause 45 address transaction is shown in Figure 7-5. The Clause 45 timing required to write to the internal registers is shown in Figure 7-6. The Clause 45 timing required to read from the internal registers is shown in Figure 7-7. The Clause 45 timing required to read from the internal registers and then increment the active address for the next transaction is shown in Figure 7-8. The Clause 22 timing required to read from the internal registers is shown in Figure 7-9. The Clause 22 timing required to write to the internal registers is shown in Figure 7-10.

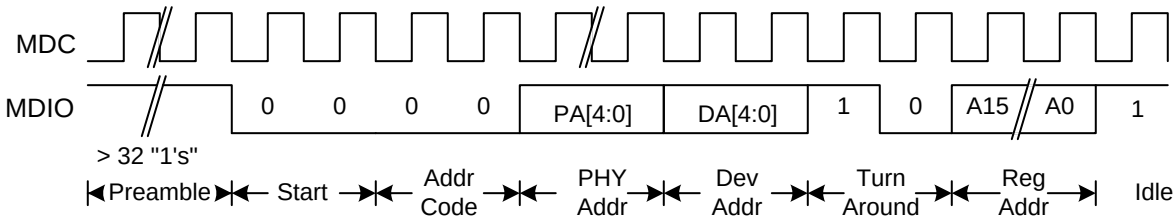


Figure 7-5. CL45 - Management Interface Extended Space Address Timing

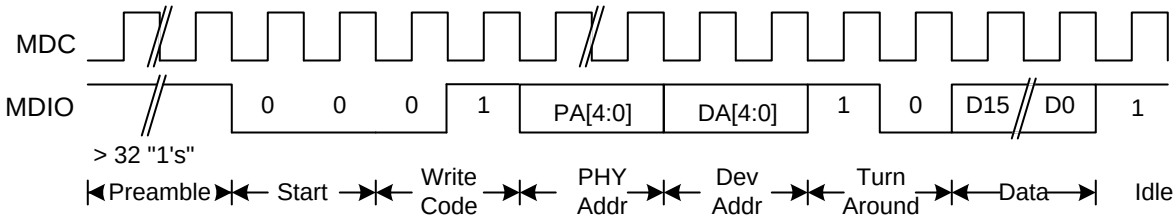


Figure 7-6. CL45 - Management Interface Extended Space Write Timing

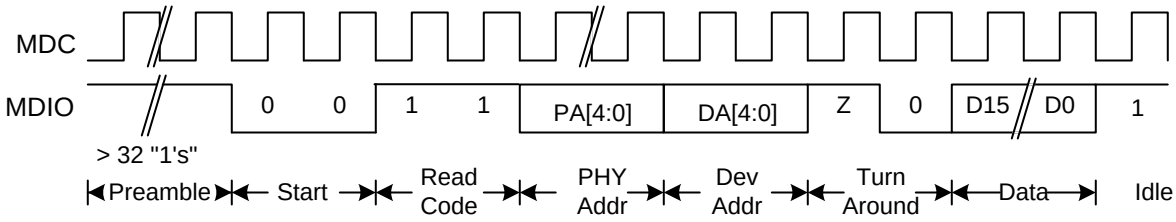


Figure 7-7. CL45 - Management Interface Extended Space Read Timing

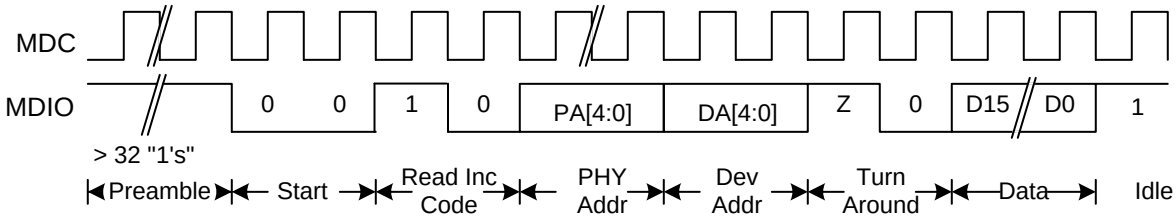


Figure 7-8. CL45 - Management Interface Extended Space Read And Increment Timing

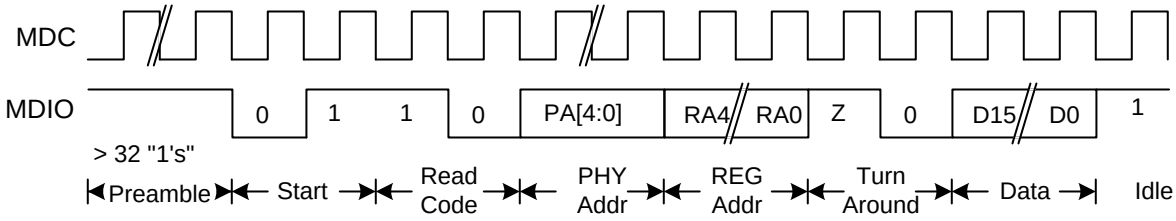


Figure 7-9. CL22 - Management Interface Read Timing

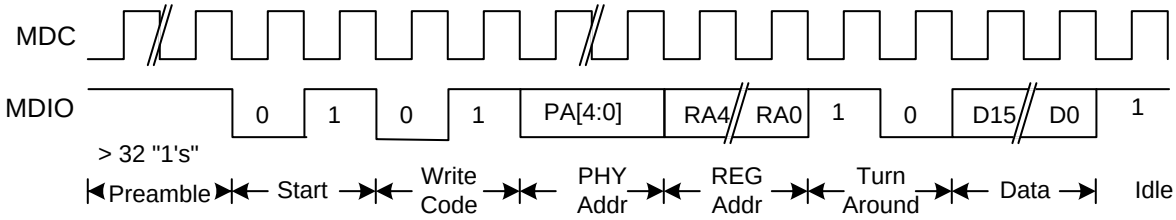


Figure 7-10. CL22 - Management Interface Write Timing

The IEEE 802.3 Clause 22/45 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

7.8 Clause 22 Indirect Addressing

Due to Clause 22 register space limitations, an indirect addressing method is implemented so that the extended register space can be accessed through Clause 22. All the device specific control and status registers that cannot be accessed through Clause 22 direct addressing can be accessed through this indirect addressing method. To access this register space, an address control register (Reg 30, 5'h1E) should be written with the register address followed by a read/write transaction to address content register (Reg 31, 5'h1F) to access the contents of the address specified in address control register. Following timing diagrams illustrate an example write transaction to Register 16'h9000 using indirect addressing in Clause 22.

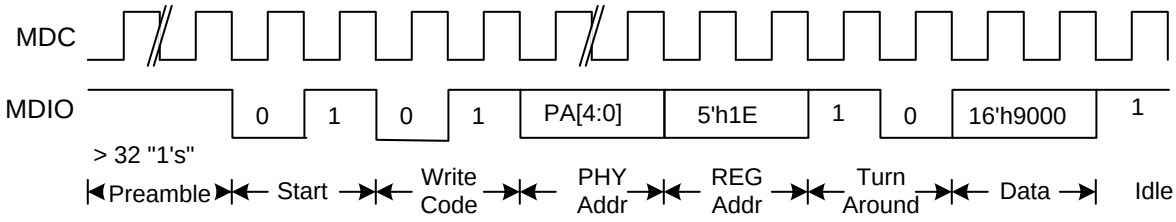


Figure 7-11. CL22 – Indirect Address Method – Address Write

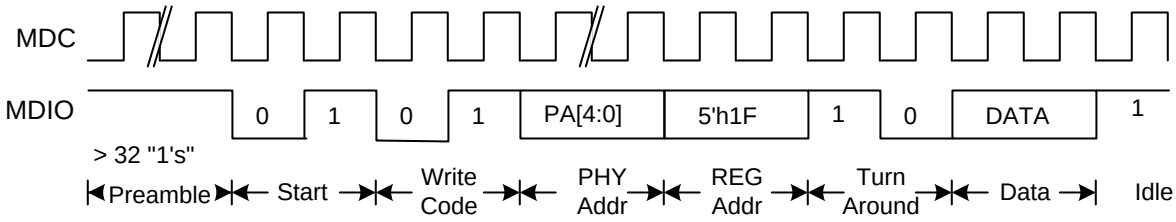


Figure 7-12. CL22 - Indirect Address Method – Data Write

Following timing diagrams illustrate an example read transaction to read contents of Register 16'h9000 using indirect addressing in Clause 22.

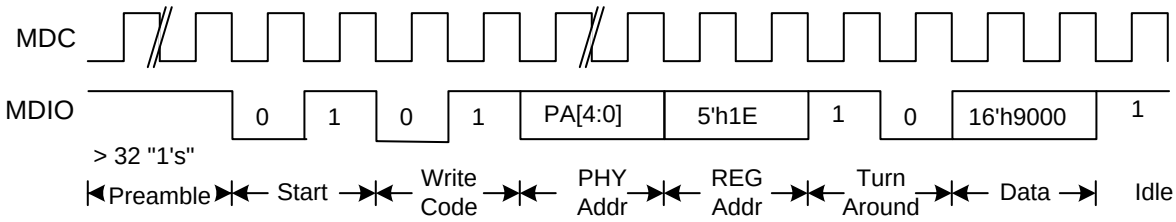


Figure 7-13. CL22 - Indirect Address Method – Address Write

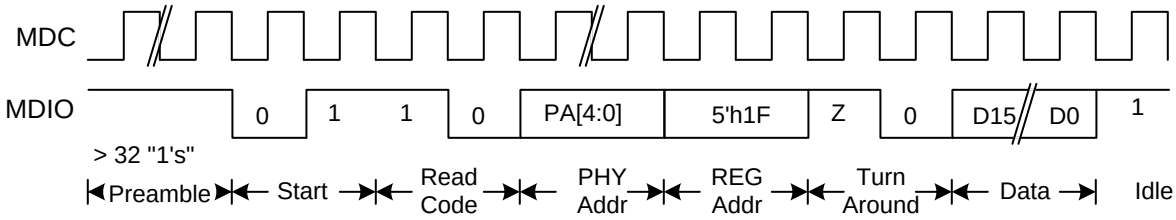


Figure 7-14. CL22 - Indirect Address Method – Data Read

7.9 Programmers Reference

Channel identification is based on PHY (Port) address field. Channel A can be accessed by setting LSB of PHY address to 0. Channel B can be accessed by setting LSB of PHY address to 1.

7.10 Register Bit Definitions

RW: Read-Write
User can write 0 or 1 to this register bit. Reading this register bit returns the same value that has been written.

RW/SC: Read-Write Self-Clearing
User can write 0 or 1 to this register bit. Writing a "1" to this register creates a high pulse. Reading this register bit always returns 0.

RO: Read-Only
This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value.

RO/LH: Read-Only Latched High
This register can only be read. Writing to this register bit has no effect. Reading a "1" from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a "0" from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched high register, when read high, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read low. If it is still occurring, the second read will read high. Reading this register bit automatically resets its value to 0.

RO/LL: Read-Only Latched Low
This register can only be read. Writing to this register bit has no effect. Reading a "0" from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a "1" from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched low register, when read low, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read high. If it is still occurring, the second read will read low. Reading this register bit automatically sets its value to 1.

COR: Clear-On-Read
This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value, then resets its value to 0. Counter value freezes at Max.

Following code letters in Name field of each control/status register bit(s) indicate the mode that they are applicable/valid.

R = Indicates control/status bit(s) valid in 10GKR mode

X = Indicates control/status bit(s) valid in 1GKX mode

G = Indicates control/status bit(s) valid in 10G general purpose serdes mode

8 DEVICE REGISTERS

8.1 Vendor Specific Device Registers

Below registers can be accessed directly through Clause 22 and Clause 45. In Clause 45 mode, these registers can be accessed by setting device address field to 0x1E (DA[4:0] = 5'b11110). In Clause 22 mode, these registers can be accessed by setting 5 bit register address field to same value as 5 LSB bits of Register Address field specified for each register. For example, 16 bit register address 0x001C in clause 45 mode can be accessed by setting register address field to 5'h1C in clause 22 mode.

Table 8-1. GLOBAL_CONTROL_1 (1)

Device Address: 0x1E	**Register Address:0x0000**	**Default: 0x0610**	
Bit(s)	**Name**	**Description**	**Access**
15	GLOBAL_RESET (RXG)	Global reset. 0 = Normal operation (Default 1'b0) 1 = Resets TX and RX data path including MDIO registers. Equivalent to asserting RESET_N.	RW SC (2)
14:12	PRTAD0_PIN_EN_SEL[2:0] (RXG)	PRTAD0 pin selection control. Valid only when 1E.0000 bit 5 is 1. PRTAD0 is used for the assignment specified below. 000 = Channel A stopwatch (Default 3'b000) 001 = Channel B stopwatch 010 = Channel A Tx data switch 011 = Channel A Rx data switch 100 = Channel B Tx data switch 101 = Channel B Rx data switch 11x = Reserved	RW
11	GLOBAL_WRITE (RXG)	Global write enable. 0 = Control settings are specific to channel addressed (Default 1'b0) 1 = Control settings in channel specific registers are applied to all 4 channels regardless of channel addressed	RW
10:7	RESERVED	For TI use only (Default 5'b1100)	RW
6	RESERVED	For TI use only. Always reads 0.	RW
5	PRTAD0_PIN_EN (RXG)	PRTAD0 pin enable control. 0 = Input pin (PRTAD0) is used for the assignment specified in 1E.0000 bits 14:12 (Default 1'b0) 1 = Input pin (PRTAD0) is not used for the assignment specified in 1E.0000 bits 14:12	RW
4:0	PRBS_PASS_OVERLAY[4:0] (RXG)	PRBS_PASS pin status selection. Applicable only when PRBS test pattern verification is enabled on HS side or LS side. PRBS_PASS pin reflects PRBS verification status on selected Channel HS/LS side. PRBS_PASS pin reflects PRBS verification status on selected Channel HS/LS side. LS Serdes lanes 1/2/3 are not applicable in 1GKX modes. 1xx00 = PRBS_PASS reflects combined status of Channel A/B HS serdes PRBS verification. If PRBS verification fails on any channel HS serdes, PRBS_PASS will be asserted low. (Default 5'b10000) 00000 = Status from Channel A HS Serdes side 00001 = Reserved 0001x = Reserved 00100 = Status from Channel A LS Serdes side Lane 0 00101 = Status from Channel A LS Serdes side Lane 1 00110 = Status from Channel A LS Serdes side Lane 2 00111 = Status from Channel A LS Serdes side Lane 3 01000 = Status from Channel B HS Serdes side 01001 = Reserved 0101x = Reserved 01100 = Status from Channel B LS Serdes side Lane 0 01101 = Status from Channel B LS Serdes side Lane 1 01110 = Status from Channel B LS Serdes side Lane 2 01111 = Status from Channel B LS Serdes side Lane 3	RW

(1) This global register is channel independent.
(2) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 8-2. CHANNEL_CONTROL_1

Device Address: 0x1E	Register Address:0x0001	Default: 0x0B00	
Bit(s)	**Name**	**Description**	**Access**
15	POWERDOWN (RXG)	Setting this bit high powers down entire data path with exception that MDIO interface stays active. 0 = Normal operation (Default 1'b0) 1 = Power Down mode is enabled.	RW
14	LT_TRAINING_CONTROL (XG)	Link training control. Valid in 10G and 1GKX modes only. 0 = Link training disabled(Default 1'b0) 1 = Link training enable control dependent on LT_TRAINING_ENABLE (1E.0036 bit 1).	RW
13	10G_RX_MODE_SEL (G)	RX mode selection. Valid in 10G only. 0 = RX mode dependent upon RX_DEMUX_SEL(Default 1'b0) 1 = Enables 1 to 1 mode on receive channel.	RW
12	10G_TX_MODE_SEL (G)	TX mode selection Valid in 10G only. 0 = TX mode dependent upon TX_MUX_SEL (Default 1'b0) 1 = Enables 1 to 1 mode on transmit channel.	RW
11	SW_PCS_SEL (RX)	Applicable in Clause 45 mode only. Valid only when MODE_SEL pin is 0, AN_ENABLE (07.0000 bit 12) is 0 and SW_DEV_MODE_SEL (1E.0001 bit 10) is 0. 1 = Set device to 10G-KR mode(Default 1'b1) 0 = Set device to 1G-KX mode	RW
10	SW_DEV_MODE_SEL (RXG)	Valid only when MODE_SEL pin is 0 1 = Device set to 10G mode 0 = In clause 45 mode, device mode is set using Auto negotiation. In clause 22 mode, device set to 1G-KX mode(Default 1'b0)	RW
9	10G_RX_DEMUX_SEL (G)	RX De-Mux selection control for lane de-serialization on receive channel. Valid in 10G and when 10G_RX_MODE_SEL (1E.0001 bit 13) is LOW 0 = 1 to 2 1 = 1 to 4 (Default 1'b1)	RW
8	10G_TX_MUX_SEL (G)	TX Mux selection control for lane serialization on transmit channel. Valid in 10G and when 10G_TX_MODE_SEL (1E.0001 bit 12) is LOW 0 = 2 to 1 1 = 4 to 1 (Default 1'b1)	RW
7:2	RESERVED	For TI use only	RO
1	REFCLK_SW_SEL (RXG)	Channel HS Reference clock selection. 0 = Selects REFCLK_0_P/N as clock reference to Channel x HS side serdes macro(Default 1'b0) 1 = Selects REFCLK_1_P/N as clock reference to Channel x HS side serdes macro	RW
0	LS_REFCLK_SEL (RXG)	Channel LS Reference clock selection. 0 = LS side serdes macro reference clock is same as HS side serdes reference clock (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_0_P/N is selected as LS side serdes macro reference clock and vice versa) (Default 1'b0) 1 = Alternate reference clock is selected as clock reference to Channel x LS side serdes macro (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_1_P/N is selected as LS side serdes macro reference clock and vice versa)	RW

Table 8-3. HS_SERDES_CONTROL_1

Device Address: 0x1E	Register Address:0x0002	Default: 0x831D	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only (Default 6'b100000)	RW
9:8	HS_LOOP_BANDWIDTH[1:0] (RXG)	HS Serdes PLL Loop Bandwidth settings 00 = Medium Bandwidth 01 = Low Bandwidth 10 = High Bandwidth 11 = Ultra High Bandwidth. (Default 2'b11)	RW
7	RESERVED	For TI use only (Default 1'b0)	RW

Table 8-3. HS_SERDES_CONTROL_1 (continued)

Device Address: 0x1E	Register Address:0x0002	Default: 0x831D	
Bit(s)	**Name**	**Description**	**Access**
6	HS_VRANGE (RXG)	HS Serdes PLL VCO range selection. 0 = VCO runs at higher end of frequency range (Default 1'b0) 1 = VCO runs at lower end of frequency range This bit needs to be set HIGH if VCO frequency (REFCLK *HS_PLL_MULT) is below 2.5 Ghz.	RW
5	RESERVED	For TI use only (Default 1'b0)	RW
4	HS_ENPLL (RXG)	HS Serdes PLL enable control. HS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH. 0 = Disables PLL in HS serdes 1 = Enables PLL in HS serdes (Default 1'b1)	RW
3:0	HS_PLL_MULT[3:0] (RXG)	HS Serdes PLL multiplier setting (Default 4'b1101). Refer : Table 8-4 HS PLL multiplier control	RW

Table 8-4. HS PLL Multiplier Control

HS_PLL_MULT[3:0]		HS_PLL_MULT[3:0]	
Value	**PLL Multiplier factor**	**Value**	**PLL Multiplier factor**
0000	Reserved	1000	12x
0001	Reserved	1001	12.5x
0010	4x	1010	15x
0011	5x	1011	16x
0100	6x	1100	16.5x
0101	8x	1101	20x
0110	8.25x	1110	25x
0111	10x	1111	Reserved

Table 8-5. HS_SERDES_CONTROL_2

Device Address: 0x1E	Register Address:0x0003	Default:0xA848	
Bit(s)	**Name**	**Description**	**Access**
15:12	HS_SWING[3:0] (RXG)	Transmitter Output swing control for HS Serdes. (Default 4'b1010) Refer Table 8-6.	RW
11	HS_ENTX (RXG)	HS Serdes transmitter enable control. HS Serdes transmitter is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH. 0 = Disables HS serdes transmitter 1 = Enables HS serdes transmitter (Default 1'b1)	RW
10	HS_EQHLD (RXG)	HSRX Equalizer hold control. 0 = Normal operation (Default 1'b0) 1 = Holds equalizer and long tail correction in its current state	RW
9:8	HS_RATE_TX [1:0] (RXG)	HS Serdes TX rate settings. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate	RW
7:6	HS_AGCCTRL[1:0] (RXG)	Adaptive gain control loop. 00 = Attenuator will not change after lock has been achieved, even if AGC becomes unlocked 01 = Attenuator will not change when in lock state, but could change when AGC becomes unlocked (Default 2'b01) 10 = Force the attenuator off 11 = Force the attenuator on	RW
5:4	HS_AZCAL[1:0] (RXG)	Auto zero calibration. 00 = Auto zero calibration initiated when receiver is enabled (Default 2'b00) 01 = Auto zero calibration disabled 10 = Forced with automatic update. 11 = Forced without automatic update	RW

Table 8-5. HS_SERDES_CONTROL_2 (continued)

Device Address: 0x1E	Register Address:0x0003	Default:0xA848	
Bit(s)	**Name**	**Description**	**Access**
3	HS_ENRX (RXG)	HS Serdes receiver enable control. HS Serdes receiver is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH. 0 = Disables HS serdes receiver 1 = Enables HS serdes receiver (Default 1'b1)	RW
2:0	HS_RATE_RX [2:0] (RXG)	HS Serdes RX rate settings. This setting is automatically controlled and value set through these register bits is ignored unless REFCLK_FREQ_SEL_1 or related OVERRIDE bit is set. 000 = Full rate (Default 3'b000) 101 = Half rate 110 = Quarter rate 111 = Eighth rate 001 = Reserved 01x = Reserved 100 = Reserved	RW

Table 8-6. HSTX AC Mode Output Swing Control

HS_SWING[3:0]	AC MODE
	TYPICAL AMPLITUDE (mVdfpp)
0000	130
0001	220
0010	300
0011	390
0100	480
0101	570
0110	660
0111	750
1000	830
1001	930
1010	1020
1011	1110
1100	1180
1101	1270
1110	1340
1111	1400

Table 8-7. HS_SERDES_CONTROL_3

Device Address: 0x1E		Register Address:0x0004 Default:0x1500	
Bit(s)	**Name**	**Description**	**Access**
15	HS_ENTRACK (RXG)	HSRX ADC Track mode. 0 = Normal operation (Default 1'b0) 1 = Forces ADC into track mode	RW
14:12	HS_EQPRE[2:0] (RXG)	Serdes Rx precursor equalizer selection 000 = 1/9 cursor amplitude 001 = 3/9 cursor amplitude (Default 3'b001) 010 = 5/9 cursor amplitude 011 = 7/9 cursor amplitude 100 = 9/9 cursor amplitude 101 =11/9 cursor amplitude 110 = 13/9 cursor amplitude 111 = Disable	RW
11:10	HS_CDRFMULT[1:0] (RXG)	Clock data recovery algorithm frequency multiplication selection (Default 2'b01) 00 = First order. Frequency offset tracking disabled 01 = Second order. 1x mode 10 = Second order. 2x mode 11 = Reserved	RW
9:8	HS_CDRTHR[1:0] (RXG)	Clock data recovery algorithm threshold selection (Default 2'b01) 00 = Four vote threshold 01 = Eight vote threshold 10 = Sixteen vote threshold 11 = Thirty two vote threshold	RW
7	RESERVED	For TI use only (Default 1'b0)	RW
6	HS_PEAK_DISABLE (RXG)	HS Serdes PEAK_DISABLE control 0 = Normal operation (Default 1'b0) 1 = Disables high frequency peaking. Suitable for <6 Gbps operation	RW
5	HS_H1CDRMODE (RXG)	HS_Serdes H1CDRMODE control 0 = Normal operation (Default 1'b0) 1 = Enables CDR mode suitable for short channel operation.	RW
4:0	HS_TWCRF[4:0] (RXG)	Cursor Reduction Factor (Default 5'b00000). Refer to Table 8-8.	RW

Table 8-8. HSTX Cursor Reduction Factor Weights

HS_TWCRF[4:0]		HS_TWCRF[4:0]	
Value	**Cursor reduction (%)**	**Value**	**Cursor reduction (%)**
00000	0	10000	17
00001	2.5	10001	20
00010	5.0	10010	22
00011	7.5	10011	25
00100	10.0	10100	27
00101	12	10101	30
00110	15	10110	32
00111	Reserved	10111	35
01000		11000	37
01001		11001	40
01010		11010	42
01011		11011	45
01100		11100	47
01101		11101	50
01110		11110	52
01111		11111	55

Table 8-9. HS_SERDES_CONTROL_4

Device Address: 0x1E	Register Address:0x0005		Default:0x2000
Bit(s)	**Name**	**Description**	**Access**
15	HS_RX_INVPAIR (RXG)	Receiver polarity. 0 = Normal polarity. HSRXxP considered positive data. HSRXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSRXxP considered negative data. HSRXxN considered positive data	RW
14	HS_TX_INVPAIR (RXG)	Transmitter polarity. 0 = Normal polarity. HSTXxP considered positive data and HSTXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSTXxP considered negative data and HSTXxN considered positive data	RW
13	RESERVED	For TI use only (Default 1'b1)	RW
12:8	HS_TWPOST1[4:0] (RXG)	Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform. (Default 5'b00000) Refer Table 8-10.	RW
7:4	HS_TWPRE[3:0] (RXG)	Precursor Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer Table 8-12.	RW
3:0	HS_TWPOST2[3:0] (RXG)	Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer Table 8-11.	RW

Table 8-10. HSTX Post-Cursor1 Transmit Tap Weights

HS_TWPOST1[4:0]		HS_TWPOST1[4:0]	
Value	**Tap weight (%)**	**Value**	**Tap weight (%)**
00000	0	10000	0
00001	+2.5	10001	–2.5
00010	+5.0	10010	–5.0
00011	+7.5	10011	–7.5
00100	+10.0	10100	–10.0
00101	+12.5	10101	–12.5
00110	+15.0	10110	–15.0
00111	+17.5	10111	–17.5
01000	+20.0	11000	–20.0
01001	+22.5	11001	–22.5
01010	+25.0	11010	–25.0
01011	+27.5	11011	–27.5
01100	+30.0	11100	–30.0
01101	+32.5	11101	–32.5
01110	+35.0	11110	–35.0
01111	+37.5	11111	-37.5

Table 8-11. HSTX Post-Cursor2 Transmit Tap Weights

HS_TWPOST2[3:0]		HS_TWPOST2[3:0]	
Value	**Tap weight (%)**	**Value**	**Tap weight (%)**
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0

Table 8-11. HSTX Post-Cursor2 Transmit Tap Weights (continued)

HS_TWPOST2[3:0]		HS_TWPOST2[3:0]	
Value	Tap weight (%)	Value	Tap weight (%)
0111	+17.5	1111	–17.5

Table 8-12. HSTX Pre-Cursor Transmit Tap Weights

HS_TWPRE[3:0]		HS_TWPRE[3:0]	
Value	Tap weight (%)	Value	Tap weight (%)
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

Table 8-13. LS_SERDES_CONTROL_1

Device Address: 0x1E	Register Address:0x0006	Default:0xF115	
Bit(s)	**Name**	**Description**	**Access**
15:12	LS_LN_CFG_EN[3:0] (RXG)	Configuration control for LS Serdes Lane settings (Default 4'b1111) [3] corresponds to LN3, [2] corresponds to LN2 [1] corresponds to LN1, [0] corresponds to LN0 0 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers do not affect respective LS Serdes lane 1 = Writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 control registers affect respective LS Serdes lane For example, if subsequent writes to LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers need to affect the settings in Lanes 0 and 1, LS_LN_CFG_EN[3:0] should be set to 4'b0011 Read values in LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 reflect the settings value for Lane selected through LS_LN_CFG_EN[3:0]. To read Lane 0 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0001 To read Lane 1 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0010 To read Lane 2 settings, LS_LN_CFG_EN[3:0] should be set to 4'b0100 To read Lane 3 settings, LS_LN_CFG_EN[3:0] should be set to 4'b1000 Read values of LS_SERDES_CONTROL_2 and LS_SERDES_CONTROL_3 and LS_CH_CONTROL_1 registers are not valid for any other LS_LN_CFG_EN[3:0] combination	RW
11:10	RESERVED	For TI use only (Default 2'b00)	RW
9:8	LS_LOOP_BANDWIDTH[1:0] (RXG)	LS Serdes PLL Loop Bandwidth settings 00 = Reserved 01 = Applicable when external JC_PLL is NOT used (Default 2'b01) 10 = Applicable when external JC_PLL is used 11 = Reserved	RW
7:5	RESERVED	For TI use only (Default 3'b000)	RW
4	LS_ENPLL (RXG)	LS Serdes PLL enable control. LS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH. 0 = Disables PLL in LS serdes 1 = Enables PLL in LS serdes (Default 1'b1)	RW
3:0	LS_MPY[3:0] (RXG)	LS Serdes PLL multiplier setting (Default 4'b0101). Refer 10GKR supported rates for valid PLL Multiplier values. Refer to Table 8-14.	RW

Table 8-14. LS PLL Multiplier Control

LS_MPY[3:0]		LS_MPY[3:0]	
Value	**PLL Multiplier factor**	**Value**	**PLL Multiplier factor**
0000	4x	1000	15x
0001	5x	1001	20x
0010	6x	1010	25x
0011	Reserved	1011	Reserved
0100	8x	1100	Reserved
0101	10x	1101	50x
0110	12x	1110	65x
0111	12.5x	1111	Reserved

Table 8-15. LS_SERDES_CONTROL_2

Device Address: 0x1E	**Register Address:0x0007**	**Default:0xDC04**	
Bit(s)	**Name**	**Description**	**Access**
15	RESERVED	For TI use only.	RW
14:12	LS_SWING[2:0] (RXG)	Output swing control on LS Serdes side. (Default 3'b101) Refer to Table 8-16.	RW
11	LS_LOS (RXG)	LS Serdes LOS detector control 0 = Disable Loss of signal detection on LS serdes lane inputs 1 = Enable Loss of signal detection on LS serdes lane inputs (Default 1'b1)	RW
10	LS_TX_ENRX (RXG)	LS Serdes enable control on the transmit channel. LS Serdes per lane on transmitter channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH. Lanes 3 and 2 are automatically disabled when in 2ln 10G mode on transmit channel. Lanes 3, 2 and 1 are automatically disabled when in 1ln 10G mode or 1G-KX mode on transmit channel. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
9:8	LS_TX_RATE [1:0] (RXG)	LS Serdes lane rate settings on transmit channel. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW
7:4	LS_DE[3:0] (RXG)	LS Serdes De-emphasis settings. (Default 4'b0000) Refer to Table 8-17.	RW
3	RESERVED	For TI use only.	RW
2	LS_RX_ENTX (RXG)	LS Serdes lane enable control on receive channel. LS Serdes per lane on receiver channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1E.0001 bit 15 is set HIGH. Lanes 3 and 2 are automatically disabled when in 2ln 10G mode on receive channel. Lanes 3, 2 and 1 are automatically disabled when in 1ln 10G or 1G-KX mode on receive channel. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
1:0	LS_RX_RATE [1:0] (RXG)	LS Serdes lane rate settings on receive channel. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Reserved	RW

Table 8-16. LSRX Output AC Mode Output Swing Control

LS_SWING[2:0]	AC MODE
	TYPICAL AMPLITUDE (mVdfpp)
000	190
001	380
010	560

Table 8-16. LSRX Output AC Mode Output Swing Control (continued)

LS_SWING[2:0]	AC MODE
	TYPICAL AMPLITUDE (mVdfpp)
011	710
100	850
101	950
110	1010
111	1050

Table 8-17. LSRX Output De-emphasis

LS_DE[3:0]			LS_DE[3:0]		
Value	Amplitude reduction		Value	Amplitude reduction	
	(%)	dB		(%)	dB
0000	0	0	1000	38.08	–4.16
0001	4.76	–0.42	1001	42.85	–4.86
0010	9.52	–0.87	1010	47.61	–5.61
0011	14.28	–1.34	1011	52.38	–6.44
0100	19.04	–1.83	1100	57.14	–7.35
0101	23.8	–2.36	1101	61.9	–8.38
0110	28.56	–2.92	1110	66.66	–9.54
0111	33.32	–3.52	1111	71.42	–10.87

Table 8-18. LS_SERDES_CONTROL_3

Device Address: 0x1E	Register Address:0x0008	Default:0x000D	
Bit(s)	**Name**	**Description**	**Access**
15	LS_RX_INVPAIR (RXG)	LS Serdes lane outputs polarity on the receive channel. (x = Channel A or B, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. OUTxyP considered positive data. OUTxyN considered negative data (Default 1’b0) 1 = Inverted polarity. OUTxyP considered negative data. OUTxyN considered positive data	RW
14	LS_TX_INVPAIR (RXG)	LS Serdes lane inputs polarity on the transmit channel. (x = Channel A or B, y = Lane 0 or 1 or 2 or 3) 0 = Normal polarity. INxyP considered positive data and INxyN considered negative data (Default 1’b0) 1 = Inverted polarity. INxyP considered negative data and INxyP considered positive data	RW
13:12	RESERVED	For TI use only (Default 2’b00)	RW
11:8	LS_EQ[3:0] (RXG)	LS Serdes Equalization control (Default 4’b0000). Table 8-19	RW
7:0	RESERVED	For TI use only (Default 8'b00001101)	RW

Table 8-19. LS_EQ Serdes Equalization

LS_EQ[3:0]			LS_EQ[3:0]		
Value	Low Freq Gain	Zero Freq	Value	Low Freq Gain	Zero Freq
0000	Maximum		1000	Adaptive	365 MHz
0001	Adaptive		1001		275 MHz
0010	Reserved		1010		195 MHz
0011			1011		140 MHz
0100			1100		105 MHz
0101			1101		75 MHz
0110			1110		55 MHz
0111			1111		50 MHz

Table 8-20. HS_OVERLAY_CONTROL

Device Address: 0x1E Register Address:0x0009 Default:0x0380			
Bit(s)	**Name**	**Description**	**Access**
15:14	LS_OK_OUT_GATE[1:0] (G)	LS_OK_OUT gating control X0 = Gating disabled (Default 2'b00) 01 = Gating enabled. LS_OK_OUT gated to LOW 11 = Gating enabled. LS_OK_OUT gated to HIGH	RW
13:12	LS_OK_IN_GATE[1:0] (G)	LS_OK_IN gating control X0 = Gating disabled (Default 2'b00) 01 = Gating enabled. LS_OK_IN gated to LOW 11 = Gating enabled. LS_OK_IN gated to HIGH	RW
11:8	RESERVED	For TI use only. (Default 4'b0011)	RW
7	HS_LOS_MASK (G)	0 = HS Serdes LOS status is used to generate HS channel synchronization status. If HS Serdes indicates LOS, channel synchronization indicates synchronization is not achieved 1 = HS Serdes LOS status is not used to generate HS channel synchronization status (Default 1'b1)	RW
6	RESERVED	For TI use only. Always reads 0.	RW
5	HS_CH_SYNC_OVERLAY (RXG)	0 = LOSx pin does not reflect receive channel loss of block lock (Default 1'b0) 1 = Allows channel loss of block lock to be reflected on LOSx pin	RW
4	HS_INVALID_CODE_OVERLAY (RXG)	0 = LOSx pin does not reflect receive channel invalid code word error (Default 1'b0) 1 = Allows invalid code word error to be reflected on LOSx pin	RW
3	HS_AGCLOCK_OVERLAY (RXG)	0 = LOSx pin does not reflect HS Serdes AGC unlock status (Default 1'b0) 1 = Allows HS Serdes AGC unlock status to be reflected on LOSx pin	RW
2	HS_AZDONE_OVERLAY (RXG)	0 = LOSx pin does not reflect HS Serdes auto zero calibration not done status (Default 1'b0) 1 = Allows auto zero calibration not done status to be reflected on LOSx pin	RW
1	HS_PLL_LOCK_OVERLAY (RXG)	0 = LOSx pin does not reflect loss of HS Serdes PLL lock status (Default 1'b0) 1 = Allows HS Serdes loss of PLL lock status to be reflected on LOSx pin	RW
0	HS_LOS_OVERLAY (RXG)	0 = LOSx pin does not reflect HS Serdes Loss of signal condition (Default 1'b0) 1 = Allows HS Serdes Loss of signal condition to be reflected on LOSx pin	RW

Table 8-21. LS_OVERLAY_CONTROL

Device Address: 0x1E Register Address:0x000A Default:0x4000			
Bit(s)	**Name**	**Description**	**Access**
15:13	RESERVED	For TI use only (Default 3'b010)	RW
12	LS_PLL_LOCK_OVERLAY (RXG)	0 = LOSx pin does not reflect loss of LS SERDES PLL lock status (Default 1'b0) 1 = Allows LS SERDES loss of PLL lock status to be reflected on LOSx pin	RW

Table 8-21. LS_OVERLAY_CONTROL (continued)

Device Address: 0x1E Register Address:0x000A Default:0x4000			
Bit(s)	**Name**	**Description**	**Access**
11:8	LS_CH_SYNC_OVERLAY_LN[3:0] (RXG)	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane loss of synchronization condition (Default 1'b0) 1 = Allows LS serdes lane loss of synchronization condition to be reflected on LOSx pin	RW
7:4	LS_INVALID_CODE_OVERLAY_LN[3:0] (RXG)	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane invalid code condition (Default 1'b0) 1 = Allows LS serdes lane invalid code condition to be reflected on LOSx pin	RW
3:0	LS_LOS_OVERLAY_LN[3:0] (RXG)	[3] Corresponds to Lane 3, [2] Corresponds to Lane 2 [1] Corresponds to Lane 1, [0] Corresponds to Lane 0 0 = LOSx pin does not reflect LS Serdes lane Loss of signal condition (Default 1'b0) 1 = Allows LS serdes lane Loss of signal condition to be reflected on LOSx pin	RW

Table 8-22. LOOPBACK_TP_CONTROL

Device Address: 0x1E Register Address:0x000B Default:0x0D10			
Bit(s)	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only. (Default 2'b00)	RW
13	HS_TP_GEN_EN (RXG)	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits 1E.000B bits 10:8	RW
12	HS_TP_VERIFY_EN (RXG)	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits 1E.000B bits 10:8	RW
11	LS_TEST_PATT_SEL[2] (RXG)	See selection in 1E.000B bits 5:4	RW
10:8	HS_TEST_PATT_SEL[2:0] (RXG)	Test Pattern Selection. Refer Refer to TLK10232 Bringup Procedure (a separate document) for more information. H/L/M/CRPAT valid in 1GKX/10G modes 000 = High Frequency Test Pattern 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Long 100 = CRPAT Short PRBS pattern valid in 1GKX/10G/10GKR modes. 101 = 2^7 - 1 PRBS pattern (Default 3'b101) 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern Errors can be checked by reading HS_ERROR_COUNT register. For KR standard pattern generation and verification, please refer to Register 03.002A	RW
7	LS_TP_GEN_EN (RXG)	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits {1E.000B bit 11, 1E.000B bits 5:4} on the LS side	RW
6	LS_TP_VERIFY_EN (RXG)	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits {1E.000B bit 11, 1E.000B bits 5:4} on the LS side	RW
5:4	LS_TEST_PATT_SEL[1:0] (RXG)	LS Test Pattern Selection LS_TEST_PATT_SEL[2:0]. LS_TEST_PATT_SEL[2] is 1E.000B bit 11 000 = High Frequency Test Pattern 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Long (In 1GKX mode only) 100 = CRPAT Short (In 1GKX mode only) 101 = 2^7 - 1 PRBS pattern (Default 3'b101) 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern For XAUI standard test pattern generation and verification in KR mode, please refer register 01.8002 and 01.8003	RW

Table 8-22. LOOPBACK_TP_CONTROL (continued)

Device Address: 0x1E	Register Address:0x000B	Default:0x0D10	
Bit(s)	**Name**	**Description**	**Access**
3	DEEP_REMOTE_LPBK (RXG)	0 = Normal functional mode (Default 1'b0) 1 = Enable deep remote loopback mode	RW
2	RESERVED	For TI use only (Default 1'b0)	RW
1	RESERVED	For TI use only (Default 1'b0)	RW
0	SHALLOW_LOCAL_LPBK (RXG)	0 = Normal functional mode (Default 1'b0) 1 = Enable shallow local loopback mode	RW

Table 8-23. LS_CONFIG_CONTROL

Device Address: 0x1E	Register Address:0x000C	Default:0x0330	
Bit(s)	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only (Default 2'b00)	RW
13:12	LS_STATUS_CFG[1:0] (RG)	Selects selected lane status to be reflected in LS_STATUS_1 register 1E.0015 bit 14 00 = Lane 0 (Default 2'b00) 01 = Lane 1 10 = Lane 2 11 = Lane 3	RW
11:10	RESERVED	For TI use only. Always reads 0.	RW
9:8	RESERVED	For TI use only. (Default 2'b11)	RW
7:6	RESERVED	For TI use only.	RO
5	LS_LOS_MASK (G)	0 = LS Serdes LOS status of enabled lanes is used to generate link status 1 = LS Serdes LOS status of enabled lanes is not used to generate link status (Default 1'b1)	RW
4	LS_PLL_LOCK_MASK (G)	0 = LS Serdes PLL Lock status is used to generate link status 1 = LS Serdes PLL Lock status is not used to generate link status (Default 1'b1)	RW
3	RESERVED	For TI use only. Always reads 0.	RW
2	FORCE_LM_REALIGN (G)	0 = Normal operation (Default 1'b0) 1 = Force lane realignment in Link status monitor	RW/SC
1:0	RESERVED	For TI use only	RO

Table 8-24. CLK_CONTROL (1)

Device Address: 0x1E	Register Address:0x000D	Default: 0x2F80	
Bit(s)	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only. Always reads 0.	RW
13	CLKOUT_ EN (RXG)	Output clock enable. 0 = Holds CLKOUTx_P/N output to a fixed value. 1 = Allows CLKOUTx_P/N output to toggle normally. (Default 1'b1)	RW
12	CLKOUT_POWERDOWN (RXG)	0 = Normal operation (Default 1'b0) 1 = Enable CLKOUTx_P/N Power Down.	RW
11:8	RESERVED	For TI use only. (Default 4'b1111)	RW

(1) This register is channel independent.

Table 8-24. CLK_CONTROL[1] (continued)

Device Address: 0x1E	Register Address:0x000D	Default: 0x2F80	
Bit(s)	**Name**	**Description**	**Access**
7:4	CLKOUT_DIV[3:0] (RXG)	CLKOUT Output clock divide setting. This value is used to divide selected clock (Selected using CLKOUT_SEL) before giving it out onto respective channel CLKOUTx_P/N. 0000 = Divide by 1 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 (Default 4'b1000) 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
3:0	CLKOUT_SEL[3:0] (RXG)	CLKOUT Output clock select. Selects Recovered clock sent out on CLKOUTx_P/N pins (Default 4'b0000) 00x0 = Selects Ch A HS recovered byte clock as output clock 00x1 = Selects Ch A HS transmit byte clock as output clock 010x = Selects Ch A HSRX VCO divide by 4 clock as output clock 0110 = Selects Ch A LS recovered byte clock as output clock 0111 = Selects Ch A LS transmit byte clock as output clock 10x0 = Selects Ch B HS recovered byte clock as output clock 10x1 = Selects Ch B HS transmit byte clock as output clock 110x = Selects Ch B HSRX VCO divide by 4 clock as output clock 1110 = Selects Ch B LS recovered byte clock as output clock 1111 = Selects Ch B LS transmit byte clock as output clock	RW

Table 8-25. RESET_CONTROL

Device Address: 0x1E	Register Address:0x000E	Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:8	RESERVED	For TI use only. Always reads 0.	RW
7:4	RESERVED	For TI use only. (Default 4'b0000)	RW
3	DATAPATH_RESET (RXG)	Channel datapath reset control. Required once the desired functional mode is configured. 0 = Normal operation. (Default 1'b0) 1 = Resets channel logic excluding MDIO registers. (Resets both Tx and Rx datapath)	RW SC[1]
2	TXFIFO_RESET (G)	Transmit FIFO reset control. Applicable in 10G mode only. Not required in 10GKR mode as 10GKR FIFO is self centering. 0 = Normal operation. (Default 1'b0) 1 = Resets transmit datapath FIFO.	
1	RXFIFO_RESET (G)	Receive FIFO reset control. Applicable in 10G mode only. Not required in 10GKR mode as 10GKR FIFO is self centering. 0 = Normal operation. (Default 1'b0) 1 = Resets receive datapath FIFO.	
0	RESERVED	For TI use only. (Default 1'b0)	RW

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 8-26. CHANNEL_STATUS_1

Device Address: 0x1E	Register Address:0x000F	Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	HS_TP_STATUS (XG)	Test Pattern status for High/Low/Mixed/CRPAT test patterns. Valid in 10G/1GKX modes. 1 = Alignment has achieved and correct pattern has been received. Any bit errors are reflected in HS_ERROR_COUNTER register (0x10) 0 = Alignment has not been determined	RO
14	LS_ALIGN_STATUS (RXG)	Lane alignment status 1 = Lane alignment is achieved on the LS side 0 = Lane alignment is not achieved on the LS side	RO/LL
13	HS_LOS (RXG)	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on HS serial receive inputs	RO/LH
12	HS_AZ_DONE (RXG)	Auto zero complete indicator. When high, indicates auto zero calibration is complete	RO/LL
11	HS_AGC_LOCKED (RXG)	Adaptive gain control loop lock indicator. When high, indicates AGC loop is in locked state	RO/LL
10	HS_CHANNEL_SYNC (RXG)	Channel synchronization status indicator. When high, indicates channel synchronization has achieved	RO/LL
9	RESERVED	For TI use only.	RO/LH
8	HS_DECODE_INVALID (RXG)	Valid when decoder is enabled and during CRPAT test pattern verification. When high, indicates decoder received an invalid code word, or a 8b/10b disparity error. In functional mode, number of DECODE_INVALID errors are reflected in HS_ERROR_COUNTER register (0x10)	RO/LH
7	TX_FIFO_UNDERFLOW (RG)	Not applicable in 1GKX mode. When high, indicates underflow has occurred in the transmit datapath (CTC) FIFO.	RO/LH
6	TX_FIFO_OVERFLOW (RXG)	When high, in 10GKR and 10G modes indicates overflow has occurred in the transmit datapath (CTC) FIFO.	RO/LH
5	RX_FIFO_UNDERFLOW (RG)	Not applicable in 1GKX mode. When high, indicates underflow has occurred in the receive datapath (CTC) FIFO.	RO/LH
4	RX_FIFO_OVERFLOW (RXG)	In 10GKR and 10G modes, high indicates overflow has occurred in the receive datapath (CTC) FIFO. In 1G-KX mode, high indicates a FIFO error.	RO/LH
3	RX_LS_OK (G)	Receive link status indicator from system side. Applicable in 10G mode only When high, indicates receive link status is achieved on the system side .	RO/LL
2	TX_LS_OK (G)	Link status indicator from Lane alignment/Link training slave inside TLK10232. When high, indicates 10G Link align achieved sync and alignment .	RO/LL
1	LS_PLL_LOCK (RXG)	LS Serdes PLL lock indicator When high, indicates LS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	RO/LL
0	HS_PLL_LOCK (RXG)	HS Serdes PLL lock indicator When high, indicates HS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	RO/LL

Table 8-27. HS_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0010	Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	HS_ERR_COUNT[15:0] (RXG)	In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder. In 10GKR mode, reading this register also clears value in 03.0021 bits 7:0. In 10GKR mode, default value for this register is 16'h0000. In HS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 10:8 When PRBS_EN pin is set, this counter reflects error count for selected PRBS pattern. Counter value cleared to 16'h0000 when read.	COR

Table 8-28. LS_LN0_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0011	Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	LS_LN0_ERR_COUNT[15:0] (RXG)	Lane 0 Error counter In 10GKR/1GKX functional modes, this counter reflects number of invalid code words (includes disparity errors) received by decoder In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 5:4 Counter value cleared to 16'h0000 when read.	COR

Table 8-29. LS_LN1_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0012	Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	LS_LN1_ERR_COUNT[15:0] (RG)	Lane 1 Error counter In 10GKR/1GKX functional modes, this counter reflects number of invalid code words (includes disparity errors) received by decoder In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 5:4 Counter value cleared to 16'h0000 when read.	COR

Table 8-30. LS_LN2_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0013	Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	LS_LN2_ERR_COUNT[15:0] (RG)	Lane 2 Error counter In 10GKR/1GKX functional modes, this counter reflects number of invalid code words (includes disparity errors) received by decoder In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 5:4 Counter value cleared to 16'h0000 when read.	COR

Table 8-31. LS_LN3_ERROR_COUNTER

Device Address: 0x1E	Register Address:0x0014	Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	LS_LN3_ERR_COUNT[15:0] (RG)	Lane 3 Error counter In 10GKR/1GKX functional modes, this counter reflects number of invalid code words (includes disparity errors) received by decoder In 10G functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder in lane alignment slave. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 1E.000B bits 5:4 Counter value cleared to 16'h0000 when read.	COR

Table 8-32. LS_STATUS_1

Device Address: 0x1E	Register Address:0x0015	Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:12	RESERVED	For TI use only.	RO
11	LS_INVALID_DECODE (RXG)	LS Invalid decode error for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 1E.000C). Error count for each lane can also be monitored through respective LS_LNx_ERR_COUNT registers	RO/LH

Table 8-32. LS_STATUS_1 (continued)

Device Address: 0x1E	Register Address:0x0015	Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
10	LS_LOS (RXG)	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on LS serial receive inputs for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 1E.000C)	RO/LH
9	LS_LN_ALIGN_FIFO_ERR (RG)	LS Lane alignment FIFO error status 1 = Lane alignment FIFO on LS side has error 0 = Lane alignment FIFO on LS side has no error	RO/LH
8	LS_CH_SYNC_STATUS (RXG)	LS Channel sync status for selected lane. Lane can be selected through LS_STATUS_CFG[1:0] (Register 1E.000C)	RO/LL
7:4	RESERVED	For TI use only.	RO
3:0	LS_CHSYNC_ROT[3:0] (RXG)	Channel synchronization pointer on LS side. Required for latency measurement function. See Latency Measurement function section for more details.	RO

Table 8-33. HS_STATUS_1

Device Address: 0x1E	Register Address:0x0016	Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:7	RESERVED	For TI use only.	RO
6:4	HS_KR_CH_SYNC_ROT[6:4] (RXG)	Channel synchronization pointer on HS side in 10GKR mode. Required for latency measurement function. See Latency Measurement function section for more details. In 10GKR mode, [6:4] reflects 3 MSB's of 7 bit HS sync rotation. In 1GKX and 10G modes, indicates channel synchronization state on HS side.	RO
3:0	HS_KR_CH_SYNC_ROT[3:0] (RXG)	Channel synchronization pointer on HS side. Required for latency measurement function. See Latency Measurement function section for more details. In 10GKR mode, reflects 4 LSB's of 7 bit HS sync rotation. In 10G and 1GKX modes, reflects 4 bit HS sync rotation.	RO

Table 8-34. DST_CONTROL_1

Device Address: 0x1E	Register Address:0x0017	Default:0x2000	
Bit(s)	**Name**	**Description**	**Access**
15:13	RESERVED	For TI use only (Default 3'b001)	RW
12	DST_PIN_SW_EN (RXG)	1 = Enable pin switch feature using top level pin. Ignore MDIO software switch. Requires setting PRTAD0_PIN_EN to high and setting PRTAD0_PIN_EN_SEL to control applicable channel Tx data switch. 0 = Disable pin switch feature. Only MDIO software switch is used (Default 1'b0)	RW
11:10	DST_PIN_SW_SRC_1[1:0] (RXG)	Applicable when top level pin (PRTAD0) is assigned to control transmit dataswitch source input and if PRTAD0 is HIGH. 00 = Select same channel LS input(Default 2'b00) 01 = Select same channel HS input 10 = Select alternate channel LS input 11 = Select alternate channel HS output	RW
9:8	DST_PIN_SW_SRC_0[1:0] (RXG)	Applicable when top level pin (PRTAD0) is assigned to control transmit dataswitch source input and if PRTAD0 is LOW. 00 = Select same channel LS input(Default 2'b00) 01 = Select same channel HS input 10 = Select alternate channel LS input 11 = Select alternate channel HS output	RW
7	DST_OFF_SEL (RX)	Applicable only in KR & KX modes. Selects data pattern to trigger OFF condition (Default 1'b0) KR Mode: 1 = Local Fault (0x0100009c) 0 = IDLE (0x07 on all lanes) KX Mode: 1 = Match DST_OFF_CHAR specified in 1E.802AB 0 = IDLE (Either /I1/ or /I2/)	RW

Table 8-34. DST_CONTROL_1 (continued)

Device Address: 0x1E	Register Address:0x0017	Default:0x2000	
Bit(s)	**Name**	**Description**	**Access**
6	DST_ON_SEL (RX)	Applicable only in KR & KX modes. Selects data pattern to trigger ON condition (Default 1'b0) KR Mode: 1 = Local Fault (0x0100009c) 0 = IDLE (0x07 on all lanes) KX Mode: 1 = Match DST_ON_CHAR specified in 1E.802A 0 = IDLE (Either /I1/ or /I2/)	RW
5	DST_STUFF_SEL (RX)	Applicable only in KR & KX modes. Selects data pattern to stuff the output during data switching (Default 1'b0) KR Mode: 1 = Local Fault (0x0100009c) 0 = IDLE (0x07 on all lanes) KX Mode: 1 = /V/ Error propagation (K30.7) 0 = /I2/ (/K28.5/D16.2/)	RW
4:0	RESERVED	For TI use only (Default 5'b00000)	RW

Table 8-35. DST_CONTROL_2

Device Address: 0x1E	Register Address:0x0018	Default:0x0C20	
Bit(s)	**Name**	**Description**	**Access**
15:14	DST_DATA_SRC_SEL[1:0] (RXG)	Data selection for transmit data switch source input. Applicable when DST_PIN_SW_EN is LOW. 00 = Select same channel LS input(Default 2'b00) 01 = Select same channel HS input 10 = Select alternate channel LS input 11 = Select alternate channel HS output	RW
13:12	DST_DATA_SW_MODE[1:0] (RXG)	Selects condition to trigger data switch for the selected ON/OFF condition. (Default 2'b00) OFF condition: 00 = Wait for OFF trigger 01 = Any data 10 = Any data 11 = Wait for OFF trigger ON condition: 00 = Wait for ON trigger 01 = Wait for ON trigger 10 = Any data 11 = Any data	RW
11:8	RESERVED	For TI use only (Default 4'b1100)	RW
7:0	DST_MASK_CYCLES[7:0] (RXG)	Duration of clock cycles that the data-switch output data is masked with the data pattern selected through DST_STUFF_SEL. (Default 8'b0010_0000)	RW

Table 8-36. DSR_CONTROL_1

Device Address: 0x1E	Register Address:0x0019	Default:0x2500	
Bit(s)	**Name**	**Description**	**Access**
15:13	RESERVED	For TI use only (Default 3'b001)	RW
12	DSR_PIN_SW_EN (RXG)	1 = Enable pin switch feature using top level pin. Ignore MDIO software switch. Requires setting PRTAD0_PIN_EN to high and setting PRTAD0_PIN_EN_SEL to control applicable channel Rx data switch. 0 = Disable pin switch feature. Only MDIO software switch is used (Default 1'b0)	RW
11:10	DSR_PIN_SW_SRC_1[1:0] (RXG)	Applicable when top level pin (PRTAD0) is assigned to control receive dataswitch source input and if PRTAD0 is HIGH. 00 = Select same channel LS input 01 = Select same channel HS input(Default 2'b01) 10 = Select alternate channel LS input 11 = Select alternate channel HS output	RW

Table 8-36. DSR_CONTROL_1 (continued)

Device Address: 0x1E	Register Address:0x0019	Default:0x2500	
Bit(s)	**Name**	**Description**	**Access**
9:8	DSR_PIN_SW_SRC_0[1:0] (RXG)	Applicable when top level pin (PRTAD0) is assigned to control receive dataswitch source input and if PRTAD0 is LOW. 00 = Select same channel LS input 01 = Select same channel HS input(Default 2'b01) 10 = Select alternate channel LS input 11 = Select alternate channel HS output	RW
7	DSR_OFF_SEL (RX)	Applicable only in KR & KX modes. Selects data pattern to trigger OFF condition (Default 1'b0) KR Mode: 1 = Local Fault (0x0100009c) 0 = IDLE (0x07 on all lanes) KX Mode: 1 = Match DSR_OFF_CHAR specified in 1E.802E 0 = IDLE (Either /I1/ or /I2/)	RW
6	DSR_ON_SEL (RX)	Applicable only in KR & KX modes. Selects data pattern to trigger ON condition (Default 1'b0) KR Mode: 1 = Local Fault (0x0100009c) 0 = IDLE (0x07 on all lanes) KX Mode: 1 = Match DSR_ON_CHAR specified in 1E.802D 0 = IDLE (Either /I1/ or /I2/)	RW
5	DSR_STUFF_SEL (RX)	Applicable only in KR & KX modes. Selects data pattern to stuff the output during data switching (Default 1'b0) KR Mode: 1 = Local Fault (0x0100009c) 0 = IDLE (0x07 on all lanes) KX Mode: 1 = /V/ Error propagation (K30.7) 0 = /I2/ (/K28.5/D16.2/)	RW
4:0	RESERVED	For TI use only (Default 5'b00000)	RW

Table 8-37. DSR_CONTROL_2

Device Address: 0x1E	Register Address:0x001A	Default:0x4C20	
Bit(s)	**Name**	**Description**	**Access**
15:14	DSR_DATA_SRC_SEL[1:0] (RXG)	Data selection for receive data switch source input. Applicable when DST_PIN_SW_EN is LOW. 00 = Select same channel LS input 01 = Select same channel HS input(Default 2'b01) 10 = Select alternate channel LS input 11 = Select alternate channel HS output	RW
13:12	DSR_DATA_SW_MODE[1:0] (RXG)	Selects condition to trigger data switch for the selected ON/OFF condition. (Default 2'b00) OFF condition: 00 = Wait for OFF trigger 01 = Any data 10 = Any data 11 = Wait for OFF trigger ON condition: 00 = Wait for ON trigger 01 = Wait for ON trigger 10 = Any data 11 = Any data	RW
11:8	RESERVED	For TI use only (Default 4'b1100)	RW
7:0	DSR_MASK_CYCLES[7:0] (RXG)	Duration of clock cycles that the data-switch output data is masked with the data pattern selected through DST_STUFF_SEL. (Default 8'b0010_0000)	RW

Table 8-38. DATA_SWITCH_STATUS

Device Address: 0x1E	Register Address:0x001B	Default:0x1020	
Bit(s)	**Name**	**Description**	**Access**
15:12	DST_EN[3:0] (RXG)	Source input data selection status on transmit side. 0001 = Same channel LS data 0010 = Same channel HS data 0100 = Alternate channel LS data 1000 = Alternate channel HS data	RO
11	DST_SW_PENDING (RXG)	When HIGH, indicates data switching event is pending to be completed in the transmit side based on selected data source input	RO
10	DST_SW_DONE (RXG)	When HIGH, indicates data switching event has occurred in the transmit side based on selected data source input	RO/LH
9	DST_ON (RXG)	ON condition indicator from transmit data switch. When HIGH, indicates an ON condition has occurred in transmit data switch	RO/LH
8	DST_OFF (RXG)	OFF condition indicator from transmit data switch. When HIGH, indicates an OFF condition has occurred in transmit data switch.	RO/LH
7:4	DSR_EN[3:0] (RXG)	Source input data selection status on receive side. 0001 = Same channel LS data 0010 = Same channel HS data 0100 = Alternate channel LS data 1000 = Alternate channel HS data	RO
3	DSR_SW_PENDING (RXG)	When HIGH, indicates data switching event is pending to be completed in the receive side based on selected data source input	RO
2	DSR_SW_DONE (RXG)	When HIGH, indicates data switching event has occurred in the receive side based on selected data source input	RO/LH
1	DSR_ON (RXG)	ON condition indicator from receive data switch. When HIGH, indicates an ON condition has occurred in receive data switch.	RO/LH
0	DSR_OFF (RXG)	OFF condition indicator from receive data switch. When HIGH, indicates an OFF condition has occurred in receive data switch.	RO/LH

Table 8-39. LS_CH_CONTROL_1

Device Address: 0x1E	Register Address:0x001C	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:7	RESERVED	For TI use only. Always reads 0.	RW
6	RESERVED	For TI use only. (Default 1'b0)	RW/SC
5:2	RESERVED	For TI use only. (Default 4'b0000)	RW
1:0	LS_CH_SYNC_HYS_SEL[1:0] (RG)	LS Channel synchronization hysteresis selection for selected lane. Lane can be selected in LS_SERDES_CONTROL_1. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the LOS state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to LOS 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS	RW

Table 8-40. HS_CH_CONTROL_1

Device Address: 0x1E	Register Address:0x001D	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only (Default 2'b00)	RW
13	REFCLK_FREQ_SEL_1 (RX)	Input REFCLK frequency selection MSB. When set, HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE settings can be set through related control bits specified in registers 1E.0002, 1E.0003, 1E.0006 0 = HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE are set automatically based on input REFCLK frequency as specified in REFCLK_FREQ_SEL_0(1E.001D bit 12) (Default 1'b0) 1 = Set this value if HS_PLL_MULT, LS_MPY and HS/LS TX/RX RATE values are NOT to be set automatically.	RW
12	REFCLK_FREQ_SEL_0 (RXG)	Input REFCLK frequency selection LSB. Applicable when REFCLK_FREQ_SEL_1(1E.001D bit 13) is set to 0. 0 = Set this value if REFCLK frequency is 156.25 MHz (Default 1'b0) 1 = Set this value if REFCLK frequency is 312.5 MHz	RW
11	RX_CTC_BYPASS (RX)	0 = Normal operation. (Default 1'b0) 1 = Disables RX CTC operation.	RW
10	TX_CTC_BYPASS (RX)	0 = Normal operation. (Default 1'b0) 1 = Disables TX CTC operation.	RW
7:4	RESERVED	For TI use only (Default 4'b0000)	RW
3	HS_ENC_BYPASS (RXG)	0 = Normal operation. (Default 1'b0) 1 = Disables 8B/10B encoder on HS side.	RW
2	HS_DEC_BYPASS (RXG)	0 = Normal operation. (Default 1'b0) 1 = Disables 8B/10B decoder on HS side.	RW
1:0	HS_CH_SYNC_HYSTERESIS[1:0] (RXG)	Channel synchronization hysteresis control on the HS receive channel. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the unsynchronized state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to unsync 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync	RW

Table 8-41. EXT_ADDRESS_CONTROL

Device Address: 0x1E	Register Address:0x001E	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	EXT_ADDR_CONTROL[15:0] (XG)	Applicable in Clause 22 mode only. This register should be written with the extended register address to be written/read. Contents of address written in this register can be accessed from Reg 1E.0x001F (Default 16'h0000)	RW

Table 8-42. EXT_ADDRESS_DATA

Device Address: 0x1E	Register Address:0x001F	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	EXT_ADDR_DATA[15:0] (XG)	Applicable in Clause 22 mode only. This register contains the data associated with the register address written in Register 1E.0x001E	RW

The registers below can be accessed directly through Clause 45 or indirectly through Clause 22. Contains mode specific control/status registers and implemented per channel basis.

Table 8-43. VS_10G_LN_ALIGN_ACODE_P

Device Address: 0x1E	Register Address:0x8003	Default: 0x0283	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9:0	LN_ALIGN_ACODE_P[9:0] (G)	10 bit Alignment character to be matched (Default 10'h283)	RW

Table 8-44. VS_10G_LN_ALIGN_ACODE_N

Device Address: 0x1E	Register Address:0x8004	Default: 0x017C	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9:0	LN_ALIGN_ACODE_N[9:0] (G)	10 bit Alignment character to be matched (Default 10'h17C)	RW

Table 8-45. MC_AUTO_CONTROL

Device Address: 0x1E	Register Address:0x8021	Default: 0x000F	
Bit(s)	**Name**	**Description**	**Access**
15:7	RESERVED	For TI use only. Always reads 0.	RW
6	HS_PLL_LOCK_CHECK_DISABLE (RXG)	1 = Disable auto HS pll lock status check. 0 = Enable auto HS pll lock status check (Default 1'b0)	RW
5	HS_LOS_CHECK_DISABLE (RXG)	1 = Disable auto HS los status check 0 = Enable auto HS los sync status check (Default 1'b0)	RW
4	SYNC_STATUS_CHECK_DISABLE (RXG)	This bit needs to be set to 1 for PRBS testing. 1 = Disable auto sync status check. 0 = Enable auto sync status check (Default 1'b0)	RW
3	CLKOUT_EN_AUTO_DISABL E (RXG)	This bit controls the signal which flat lines CLKOUT and applicable only when CLKOUT is selected to have HS Recovered byte clock 1 = CLKOUT clock flat lined if HS LOS is detected (Default 1'b1) 0 = CLKOUT clock not flat lined if HS LOS is detected	RW
2:0	RESERVED	For TI use only (Default 3'b111)	RW

Table 8-46. DST_ON_CHAR_CONTROL

Device Address: 0x1E	Register Address:0x802A	Default: 0x02FD	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9:0	DST_ON_CHAR[9:0] (XG)	Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger ON condition if matched on transmit side (Default 10'h2FD)	RW

Table 8-47. DST_OFF_CHAR_CONTROL

Device Address: 0x1E	Register Address:0x802B	Default: 0x02FD	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9:0	DST_OFF_CHAR[9:0] (XG)	Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger OFF condition if matched on transmit side (Default 10'h2FD)	RW

Table 8-48. DST_STUFF_CHAR_CONTROL

Device Address: 0x1E	Register Address:0x802C	Default: 0x0207	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9:0	DST_STUFF_CHAR[9:0] (G)	Applicable only in 10G mode. 10 bit data pattern to stuff the output of data switch on transmit side (Default 10'h207)	RW

Table 8-49. DSR_ON_CHAR_CONTROL

Device Address: 0x1E	Register Address:0x802D	Default: 0x02FD	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9:0	DSR_ON_CHAR[9:0] (XG)	Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger ON condition if matched on receive side (Default 10'h2FD)	RW

Table 8-50. DSR_OFF_CHAR_CONTROL

Device Address: 0x1E	Register Address:0x802E	Default: 0x02FD	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9:0	DSR_OFF_CHAR[9:0] (XG)	Applicable only in 1GKX and 10G modes. 10 bit data pattern to trigger OFF condition if matched on receive side (Default 10'h2FD)	RW

Table 8-51. DSR_STUFF_CHAR_CONTROL

Device Address: 0x1E	Register Address:0x802F	Default: 0x0207	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	
9:0	DSR_STUFF_CHAR[9:0] (G)	Applicable only in 10G mode. 10 bit data pattern to stuff the output of data switch on receive side (Default 10'h207)	RW

Table 8-52. LATENCY_MEASURE_CONTROL

Device Address: 0x1E	Register Address:0x8040	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:8	RESERVED	For TI use only. Always reads 0.	RW
7:6	LATENCY_MEAS_STOP_SEL[1: 0] (RXG)	Latency measurement stop point selection 00 = Selects LS RX as stop point (Default 2 'b00) 01 = Selects HS TX as stop point 1x = Selects external pin (PRTAD0) as stop point	RW

Table 8-52. LATENCY_MEASURE_CONTROL (continued)

Device Address: 0x1E	Register Address:0x8040	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
5:4	LATENCY_MEAS_CLK_DIV[1:0] (RXG)	Latency measurement clock divide control. Valid only when bit 1E.8040 bit 2 is 0. Divides clock to needed resolution. Higher the divide value, lesser the latency measurement resolution. Divider value should be chosen such that the divided clock doesn't result in clock slower than the high speed byte clock. 00 = Divide by 1 (Default 2'b00) (Most Accurate Measurement) 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 (Longest Measurement Capability)	RW
3:2	LATENCY_MEAS_START_SEL[1:0] (RXG)	Latency measurement start point selection 00 = Selects LS TX as start point (Default 2'b00) 01 = Selects HS RX as start point 1x = Selects external pin (PRTAD0) as start point	RW
1	LATENCY_MEAS_EN (RXG)	Latency measurement enable 0 = Disable Latency measurement (Default 'b0) 1 = Enable Latency measurement	RW
0	LATENCY_MEAS_CLK_SEL (RXG)	Latency measurement clock selection. 0 = Selects VCO clock as per Latency measurement table. Bits 1E.8040 bits 5:4 can be used to divide this clock to achieve needed resolution. (Default 1'b0) 1 = Selects respective channel recovered byte clock	RW

Table 8-53. LATENCY_COUNTER_2

Device Address: 0x1E	Register Address:0x8041	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:12	LATENCY_MEAS_START_COMMA[3:0] (RXG)	Latency measurement start comma location status. "1" indicates start comma location found. If LS TX is selected as start point (1E.8040 bit 7 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS RX is selected as start point (1E.8040 bit 7 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused. Reading this register will clear Latency stopwatch status specified in LATENCY_COUNTER_1 & LATENCY_COUNTER_2 registers. Below sequence of reads needs to be performed for accurate and repeat stopwatch measurements. See Latency measurement procedure more information. READ 0x8041 READ 0x8042	RO/LH
11:8	LATENCY_MEAS_STOP_COMMA[3:0] (RXG)	Latency measurement stop comma location status. "1" indicates stop comma location found. If LS RX is selected as stop point (1E.8040 bit 6 = 0), [3:0] indicates status for lane3, lane2, lane1, lane0. If HS TX is selected as stop point (1E.8040 bit 6 = 1), [0] indicates status for data[9:0], [1] indicates status for data[19:10]. [3:2] is unused.	RO/LH
4	LATENCY_ MEAS_READY (RXG)	Latency measurement ready indicator 0 = Indicates latency measurement not complete. 1 = Indicates latency measurement is complete and value in latency measurement counter (LATENCY_MEAS_COUNT[19:0]) is ready to be read.	RO/LH
3:0	LATENCY_MEAS_COUNT[19:16] (RXG)	Bits[19:16] of 20 bit wide latency measurement counter. Latency measurement counter value represents the latency in number of clock cycles. Each clock cycle is half of the period of the measurement clock as determined by register 1E.8040 bits 5:4 and 1E.8040 bit 0. This counter will return 20'h00000 if it's read before rx comma is received. If latency is more than 20'hFFFFF clock cycles then this counter returns 20'hFFFFF.	RO

Table 8-54. LATENCY_COUNTER_1

Device Address: 0x1E	Register Address:0x8042	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	LATENCY_MEAS_COUNT[15:0] (RXG)	Bits[15:0] of 20 bit wide latency measurement counter. Below sequence of reads needs to be performed for accurate and repeat stopwatch measurements. READ 0x8041 READ 0x8042	COR (1)

(1) Latency measurement counter value resets to 20'h00000 when this register is read. Start and Stop Comma (1E.8041 bits 15:12 & 1E.8041 bits 11:8) and count valid (1E.8041 bit 4) bits are also cleared when this register is read

Table 8-55. TRIGGER_LOAD_CONTROL

Device Address: 0x1E	Register Address:0x8100	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:11	RESERVED	For TI use only. Always reads 0.	RW
10:3	RESERVED	For TI use only. (Default 8'b00000000)	RW
2	DEFAULT_TX_LOAD_TRIGGER (RXG)	Valid only when DEFAULT_TX_TRIGGER_EN is HIGH 1 = Trigger loading default HS TX setting values 0 = Normal operation (Default 1'b0) This bit needs to be written HIGH and then LOW to load the HS Tx default values. Applicable when link training is enabled.	RW
1:0	RESERVED	For TI use only. (Default 2'b00)	RW

Table 8-56. TRIGGER_EN_CONTROL

Device Address: 0x1E	Register Address:0x8101	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:11	RESERVED	For TI use only. Always reads 0.	RW
10:3	RESERVED	For TI use only. (Default 8'b00000000)	RW
2	DEFAULT_TX_TRIGGER_EN (RXG)	1 = Enable loading of Tx default values through DEFAULT_TX_LOAD_TRIGGER 0 = Normal operation (Default 1'b0)	RW
1:0	RESERVED	For TI use only. (Default 2'b00)	RW

8.2 PMA/PMD Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x01 (DA[4:0] = 5'b00001).

NOTE: Link training registers can also be accessed in Clause 22 mode using indirect address method and in Clause 45 mode with device address field set to 0x1E (DA[4:0] = 5'b11110). Link training registers are also applicable in 10G and 1GKX modes.

Table 8-57. PMA_CONTROL_1

Device Address: 0x01	Register Address:0x0000	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	RESET (RX)	1 = Global reset. Resets datapath and MDIO registers of all channels. Equivalent to asserting RESET_N. 0 = Normal operation (Default 1'b0)	RW/SC
14:12	RESERVED	For TI use only. Always reads 0.	RW
11	POWERDOWN (RX)	1 = Enable power down mode 0 = Normal operation (Default 1'b0)	RW
10:1	RESERVED	For TI use only. Always reads 0.	RW
0	LOOPBACK (RX)	1 = Enables loopback on HS side. LS data traverses through entire Tx datapath excluding HS serdes and will be available at LS output side 0 = Normal operation (Default 1'b0)	RW

Table 8-58. PMA_STATUS_1

Device Address: 0x01	Register Address:0x0001	Default: 0x0002	
Bit(s)	**Name**	**Description**	**Access**
7	FAULT (RX)	1 = Fault condition detected on either Tx or Rx side 0 = No fault condition detected This bit is cleared after Register 01.0008 is read and no fault condition occurs after 01.0008 is read.	RO
2	RX_LINK (RX)	1 = Receive link is up 0 = Receive link is down	RO/LL

Table 8-58. PMA_STATUS_1 (continued)

Device Address: 0x01	Register Address:0x0001	Default: 0x0002	
Bit(s)	**Name**	**Description**	**Access**
1	LOW_POWER_ABILITY (RX)	Always reads 1. 1 = Supports low power mode 0 = Does not support low power mode	RO

Table 8-59. PMA_DEV_IDENTIFIER_1

Device Address: 0x01	Register Address:0x0002	Default: 0x4000	
Bit(s)	**Name**	**Description**	**Access**
15:0	DEV_IDENTIFIER[31:16] (RX)	16 MSB of 32 bit unique device identifier. See Table 8-61 for identifier code details.	RO

Table 8-60. PMA_DEV_IDENTIFIER_2

Device Address: 0x01	Register Address:0x0003	Default: 0x5100	
Bit(s)	**Name**	**Description**	**Access**
15:0	DEV_IDENTIFIER[15:0] (RX)	16 LSB of 32 bit unique device identifier. SeeTable 8-61 for identifier code details	RO

Table 8-61. UNIQUE DEVICE IDENTIFIER(1)

Register address	Value	Description
01.0002 bits 15:0	16'b0100_0000_0000_0000	OUI[3-18]
01.0003 bits 15:10	6'b010100	OUI[19-24]
01.0003 bits 9:4	6'b010000	6-bit Manufacturer device model number
01.0003 bits 3:0	4'b0000	4-bit Manufacturer device revision number

(1) The identifier code is composed of bits 3-24 of 25-bit organizationally unique identifier (OUI) assigned to Texas Instruments by IEEE. The 6-bit Manufacturer device model number is unique to TLK10232. The 4-bit Manufacturer device revision number denotes the current revision of TLK10232.

Table 8-62. PMA_SPEED_ABILITY

Device Address: 0x01	Register Address: 0x0004	Default: 0x0011	
Bit(s)	**Name**	**Description**	**Access**
4	SPEED_1G (RX)	Always reads 1. 1 = Capable of operating at 1000 Mb/s 0 = Not capable of operating at 1000 Mb/s	RO
0	SPEED_10G (RX)	Always reads 1. 1 = Capable of operating at 10 Gb/s 0 = Not capable of operating at 10 Gb/s	RO

Table 8-63. PMA_DEV_PACKAGE_1

Device Address: 0x01	Register Address: 0x0005	Default: 0x000B	
Bit(s)	**Name**	**Description**	**Access**
3	PCS_ PRESENT (RX)	Always reads 1. 1 = PCS present in the package 0 = PCS not present in the package	RO
1	PMA_PMD_PRESENT (RX)	Always reads 1. 1 = PMA/PMD present in the package 0 = PMA/PMD not present in the package	RO
0	CL22_PRESENT (RX)	Always reads 1. 1 = Clause 22 registers present in the package 0 = Clause 22 registers not present in the package	RO

Table 8-64. PMA_DEV_PACKAGE_2

Device Address: 0x01	Register Address: 0x0006	Default: 0x4000	
Bit(s)	**Name**	**Description**	**Access**
15	VS_DEV2_PRESENT (RX)	Always reads 0. 1 = Vendor specific device 2 present in the package 0 = Vendor specific device 2 not present in the package	RO
14	VS_DEV1_PRESENT (RX)	Always reads 1. 1 = Vendor specific device 1 present in the package 0 = Vendor specific device 1 not present in the package	RO

Table 8-65. PMA_STATUS_2

Device Address: 0x01	Register Address: 0x0008	Default: 0xB000	
Bit(s)	**Name**	**Description**	**Access**
15:14	DEV_PRESENT (RX)	Always reads 2'b10 0x = No device responding at this address 10 = Device responding at this address 11 = No device responding at this address	RO
13	TX_FAULT_ABILITY (RX)	Always reads 1'b1. 1 = Able to detect fault condition on Tx path 0 = Not able to detect fault condition on Tx path	RO
12	RX_FAULT_ABILITY (RX)	Always reads 1'b1. 1 = Able to detect fault condition on Rx path 0 = Not able to detect fault condition on Rx path	RO
11	TX_FAULT (RX)	1 = Fault condition detected on transmit path 0 = No fault condition detected on transmit path	RO/LH
10	RX_FAULT (RX)	1 = Fault condition detected on receive path 0 = No fault condition detected on receive path	RO/LH
8	TX_DISABLE_ABILITY (RX)	Always reads 1'b0. 1 = Able to perform transmit disable function 0 = Not able to perform transmit disable function	RO

Table 8-66. PMA_RX_SIGNAL_DET_STATUS

Device Address: 0x01	Register Address: 0x000A	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
0	RX_SIGNAL_DET (RX)	1 = Signal detected on serial Rx pins 0 = Signal not detected on serial Rx pins	RO

Table 8-67. PMA_EXTENDED_ABILITY

Device Address: 0x01	Register Address: 0x000B	Default: 0x0050	
Bit(s)	**Name**	**Description**	**Access**
6	KX_ABILITY (RX)	Always reads 1'b11 = Able to perform 1000BASE-KX 0 = Not able to perform 1000BASE-KX	RO
4	KR_ABILITY (RX)	Always reads 1'b11 = Able to perform 10GBASE-KR 0 = Not able to perform 10GBASE-KR	RO

Table 8-68. LT_TRAIN_CONTROL

Device Address: 0x01	Register Address: 0x0096	Default: 0x0002	
Bit(s)	**Name**	**Description**	**Access**
15:2	RESERVED	For TI use only. Always reads 0.	RW
1	LT_TRAINING_ENABLE (RXG)	1 = Enable start-up protocol as per 10GBASE-KR standard(Default 1'b1) 0 = Disable start-up protocol This bit should be set to HIGH for autotrain mode to function correctly	RW
0	LT_RESTART_TRAINING (RXG)	1 = Reset link/auto train 0 = Normal operation (Default 1'b0)	RW/SC

Table 8-69. LT_TRAIN_STATUS

Device Address: 0x01	Register Address: 0x0097	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
3	LT_TRAINING_FAIL (RXG)	1 = Training failure has been detected 0 = Training failure has not been detected	RO
2	LT_START_PROTOCOL (RXG)	1 = Start up protocol in progress 0 = Start up protocol complete	RO
1	LT_FRAME_LOCK (RXG)	1 = Training frame delineation detected 0 = Training frame delineation not detected	RO
0	LT_RX_STATUS (RXG)	1 = Receiver trained and ready to receive data 0 = Receiver training in progress	RO

Table 8-70. LT_LINK_PARTNER_CONTROL

Device Address: 0x01	Register Address: 0x0098	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
13	LT_LP_PRESET (RXG)	1 = KR preset coefficients 0 = Normal operation	RO
12	LT_LP_INITIALIZE (RXG)	1 = Initialize KR coefficients 0 = Normal operation	RO
9	LT_LP_COEFF_SWG (RXG)	Swing update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO
7	LT_LP_COEFF_PS2 (RXG)	Post2 tap control update 11 = Reserved01 = Increment 10 = Decrement 00 = Hold	RO
5	LT_LP_COEFF_P1 (RXG)	Coefficient K(+1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO
3	LT_LP_COEFF_0 (RXG)	Coefficient K(0) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO
1	LT_LP_COEFF_M1 (RXG)	Coefficient K(-1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO

Table 8-71. LT_LINK_PARTNER_STATUS

Device Address: 0x01	Register Address: 0x0099	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	LT_LP_RX_READY (RXG)	1 = LP receiver has determined that training is complete and prepared to receive data 0 = LP receiver is requesting that training continue	RO
9:8	LT_LP_COEFF_SWG_STAT (RXG)	Swing update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
7:6	LT_LP_COEFF_PS2_STAT (RXG)	Post2 tap control update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO

Table 8-71. LT_LINK_PARTNER_STATUS (continued)

Device Address: 0x01	Register Address: 0x0099	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
5:4	LT_LP_COEFF_P1_STAT (RXG)	Coefficient K(+1) update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
3:2	LT_LP_COEFF_0_STAT (RXG)	Coefficient K(0) update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
1:0	LT_LP_COEFF_M1_STAT (RXG)	Coefficient K(-1) update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO

Table 8-72. LT_LOCAL_DEVICE_CONTROL

Device Address: 0x01	Register Address: 0x009A	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	RESERVED	For TI use only. Always reads 0.	RO
13	LT_LD_PRESET (RXG)	1 = KR preset coefficients 0 = Normal operation (Default 1'b0)	RO
12	LT_ LD_INITIALIZE (RXG)	1 = Initialize KR coefficients 0 = Normal operation (Default 1'b0)	RO
9:8	LT_LD_COEFF_SWG (RXG)	Swing update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
7:6	LT_LD_COEFF_PS2 (RXG)	Post2 tap control update 11 = Reserved01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
5:4	LT_ LD_COEFF_P1 (RXG)	Coefficient K(+1) update 11 = Reserved01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
3:2	LT_ LD_COEFF_0 (RXG)	Coefficient K(0) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
1:0	LT_ LD_COEFF_M1 (RXG)	Coefficient K(-1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO

Table 8-73. LT_LOCAL_DEVICE_STATUS

Device Address: 0x01	Register Address: 0x009B	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	LT_ LD_RX_READY (RXG)	1 = LD receiver has determined that training is complete and prepared to receive data 0 = LD receiver is requesting that training continue	RO

Table 8-73. LT_LOCAL_DEVICE_STATUS (continued)

Device Address: 0x01	Register Address: 0x009B	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4	LT_ LD_COEFF_P1_STAT (RXG)	Coefficient K(+1) update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
3:2	LT_ LD_COEFF_0_STAT (RXG)	Coefficient K(0) update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
1:0	LT_ LD_COEFF_M1_STAT (RXG)	Coefficient K(-1) update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO

Table 8-74. KX_STATUS

Device Address: 0x01	Register Address: 0x00A1	Default: 0x3000	
Bit(s)	**Name**	**Description**	**Access**
13	KX_TX_FAULT_ABILITY (X)	Always reads 1. 1 = Able to detect fault condition on transmit path 0 = Not able to detect fault condition on transmit path	RO
12	KX_RX_FAULT_ABILITY (X)	Always reads 1. 1 = Able to detect fault condition on receive path 0 = Not able to detect fault condition on receive path	RO
11	KX_TX_FAULT (X)	1 = Fault condition detected on transmit path 0 = No fault condition detected on transmit path	RO/LH
10	KX_RX_FAULT (X)	1 = Fault condition detected on receive path 0 = No fault condition detected on receive path	RO/LH
0	KX_RX_SIGNAL_DETECT (X)	1 = Signal detected 0 = Signal not detected	RO

Table 8-75. KR_FEC_ABILITY

Device Address: 0x01	Register Address: 0x00AA	Default: 0x0003	
Bit(s)	**Name**	**Description**	**Access**
1	KR_FEC_ERR_ABILITY (R)	Always reads 1. 1 = Device supports 10GBASE-R FEC error indication to PCS 0 = Device does not support 10GBASE-R FEC function error indication tx PCS	RO
0	KR_FEC_ABILITY (R)	Always reads 1. 1 = Device supports 10GBASE-R FEC function 0 = Device does not support 10GBASE-R FEC function	

Table 8-76. KR_FEC_CONTROL

Device Address: 0x01	Register Address: 0x00AB	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:2	RESERVED	For TI use only. Always reads 0.	RW
1	KR_FEC_ERR_IND_EN (R)	1 = Enable FEC decoder to indicate errors to PCS 0 = Disable FEC decoder error indication to PCS (Default 1'b0)	RW
0	KR_FEC_EN (R)	1 = Enable 10GBASE-R FEC function 0 = Disable 10GBASE-R FEC function (Default 1'b0)	RW

Table 8-77. KR_FEC_C_COUNT_1(1)

Device Address: 0x01	Register Address: 0x00AC	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	KR_FEC_C_COUNT[15:0] (R)	Lower 16 bits of FEC corrected blocks counter	COR

(1) To get correct 32 bit counter value of KR_FEC_C_COUNT, Register 01.00AC should be read first followed by Register 01.00AD

Table 8-78. KR_FEC_C_COUNT_2

Device Address: 0x01	Register Address: 0x00AD	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	KR_FEC_C_COUNT[31:16] (R)	Upper 16 bits of FEC corrected blocks counter	COR

Table 8-79. KR_FEC_UC_COUNT_1(1)

Device Address: 0x01	Register Address: 0x00AE	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	KR_FEC_UC_COUNT[15:0] (R)	Lower 16 bits of FEC Uncorrected blocks counter	COR

(1) To get correct 32 bit counter value of KR_FEC_UC_COUNT, Register 01.00AE should be read first followed by Register 01.00AF

Table 8-80. KR_FEC_UC_COUNT_2

Device Address: 0x01	Register Address: 0x00AF	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	KR_FEC_UC_COUNT[31:16] (R)	Lower 16 bits of FEC Uncorrected blocks counter	COR

Table 8-81. KR_VS_FIFO_CONTROL_1

<table>
<tr><td colspan="4">Device Address: 0x01 Register Address: 0x8001 Default: 0xCC4C</td></tr>
<tr><td>Bit(s)</td><td>Name</td><td>Description</td><td>Access</td></tr>
<tr><td>15</td><td>RESERVED</td><td>For TI use only (Default 1’b1)</td><td>RW</td></tr>
<tr><td>14:12</td><td>RX_FIFO_DEPTH[2:0] (R)</td><td>Rx CTC FIFO depth selection
1xx = 32 deep (Default 3’b100)
011 = 24 deep
010 = 16 deep
001 = 12 deep
000 = 8 deep (No CTC function)</td><td>RW</td></tr>
<tr><td>11:10</td><td>RX_CTC_WMK_SEL[1:0] (R)</td><td>Water mark selection for receive CTC
Works in conjunction with RX_FIFO_DEPTH_SEL setting (Default 2’b11)
<table>
<tr><td>Depth-></td><td>32</td><td>24</td><td>26</td><td>12/8</td></tr>
<tr><td>11</td><td>High</td><td>High</td><td>High</td><td>NA</td></tr>
<tr><td>10</td><td>Mid-high</td><td>Mid</td><td>High</td><td></td></tr>
<tr><td>01</td><td>Mid</td><td>Low</td><td>Low</td><td></td></tr>
<tr><td>00</td><td>Low</td><td>Low</td><td>Low</td><td></td></tr>
</table></td><td>RW</td></tr>
<tr><td>9</td><td>RX_Q_CNT_IPG (R)</td><td>0 = Normal operation. (Default 1’b0)
1 = Sequence columns are counted as IPG.</td><td>RW</td></tr>
<tr><td>8</td><td>RX_CTC_Q_DROP_EN (R)</td><td>0 = Normal operation. (Default 1’b0)
1 = Enable Q column drop in RX CTC.</td><td>RW</td></tr>
<tr><td>7</td><td>XMIT_IDLE (R)</td><td>1 = Transmit idle pattern onto LS side
0 = Normal operation (Default 1’b0)</td><td>RW</td></tr>
</table>

Table 8-81. KR_VS_FIFO_CONTROL_1 (continued)

Device Address: 0x01	Register Address: 0x8001	Default: 0xCC4C	
Bit(s)	**Name**	**Description**	**Access**
6:4	TX_FIFO_DEPTH[2:0] (R)	Tx CTC FIFO depth selection 1xx = 32 deep (Default 3'b100)011 = 24 deep 010 = 16 deep001 = 12 deep 000 = 8 deep (No CTC function)	RW
3:2	TX_CTC_WMK_SEL[1:0] (R)	Water mark selection for receive CTC Works in conjunction with TX_FIFO_DEPTH_SEL setting (Default 2'b11)	RW
1	TX_Q_CNT_IPG (R)	0 = Normal operation. (Default 1'b0) 1 = Sequence columns are counted as IPG.	RW
0	TX_CTC_Q_DROP_EN (R)	0 = Normal operation. (Default 1'b0) 1 = Enable Q column drop in TX CTC.	RW

Depth->	32	24	26	12/8
11	High	High	High	NA
10	Mid-high	Mid	High	
01	Mid	Low	Low	
00	Low	Low	Low	

Table 8-82. KR_VS_TP_GEN_CONTROL

Device Address: 0x01	Register Address:0x8002	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:6	RESERVED	For TI use only. Always reads 0.	RW
5:4	RX_TPG_HLM_TEST_SEL[1:0] (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 00 = High Frequency test pattern(Default 2'b00) 01 = Low Frequency test pattern 10 = Mixed Frequency test pattern 11 = Normal operation	RW
3	RX_TPG_CRPAT_TEST_EN (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables CRPAT test pattern generation	RW
2	RX_TPG_CJPAT_TEST_EN (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables CJPAT test pattern generation	RW
1	RX_TPG_10GFC_TEST_EN (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables 10 GFC CJPAT test pattern generation	RW
0	RX_TPG_HLM_TEST_EN (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables H/L/M test pattern generation	RW

Table 8-83. KR_VS_TP_VER_CONTROL

Device Address: 0x01	Register Address:0x8003	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only. Always reads 0.	RW
13:12	TX_TPV_HLM_TEST_SEL[1:0] (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 00 = High Frequency test pattern(Default 2'b00) 01 = Low Frequency test pattern 10 = Mixed Frequency test pattern 11 = Normal operation	RW

Table 8-83. KR_VS_TP_VER_CONTROL (continued)

Device Address: 0x01	Register Address:0x8003	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
11	TX_TPV_CRPAT_TEST_EN (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables CRPAT test pattern verification	RW
10	TX_TPV_CJPAT_TEST_EN (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables CJPAT test pattern verification	RW
9	TX_TPV_10GFC_TEST_EN (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables 10 GFC CJPAT test pattern verification	RW
8	TX_TPV_HLM_TEST_EN (R)	XAUI based test pattern selection on LS side. See Test pattern procedures for more information. 0 = Normal operation. (Default 1'b0) 1 = Enables HL/M test pattern verification	RW
7:0	RESERVED	For TI use only(Default 8'b00000000)	RW

Table 8-84. KR_VS_CTC_ERR_CODE_LN0

Device Address: 0x01	Register Address: 0x8005	Default: 0xCE00	
Bit(s)	**Name**	**Description**	**Access**
15:7	KR_CTC_ERR_CODE_LN0 (R)	Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 0 corresponds to 8'h9C with the control bit being 1'b1. The default values for lanes 0~3 correspond to ||LF||	RW
6:0	RESERVED	For TI use only. Always reads 0.	RW

Table 8-85. KR_VS_CTC_ERR_CODE_LN1

Device Address: 0x01	Register Address: 0x8006	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:7	KR_CTC_ERR_CODE_LN1 (R)	Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 1 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW
6:0	RESERVED	For TI use only. Always reads 0.	RW

Table 8-86. KR_VS_CTC_ERR_CODE_LN2

Device Address: 0x01	Register Address: 0x8007	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:7	KR_CTC_ERR_CODE_LN2 (R)	Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 2 corresponds to 8'h00 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW
6:0	RESERVED	For TI use only. Always reads 0.	RW

Table 8-87. KR_VS_CTC_ERR_CODE_LN3

Device Address: 0x01	Register Address: 0x8008	Default: 0x0080	
Bit(s)	**Name**	**Description**	**Access**
15:7	KR_CTC_ERR_CODE_LN3 (R)	Applicable in 10G-KR mode only. XGMII code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 3 corresponds to 8'h01 with the control bit being 1'b0. The default values for lanes 0~3 correspond to ||LF||	RW
6:0	RESERVED	For TI use only. Always reads 0.	RW

Table 8-88. KR_VS_LN0_EOP_ERROR_COUNTER

Device Address: 0x01	Register Address: 0x8010	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	KR_LN0_EOP_ERR_COUNT (R)	Lane 0 End of packet Error counter. End of packet error is detected when Terminate character is in lane 0 and one or both of the following holds: ● Terminate character is not followed by /K/ characters in lanes 1, 2 and 3 ● The column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 8-89. KR_VS_LN1_EOP_ERROR_COUNTER

Device Address: 0x01	Register Address: 0x8011	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	KR_LN1_EOP_ERR_COUNT (R)	Lane 1 End of packet Error counter. End of packet error is detected when Terminate character is in lane 1 and one or both of the following holds: ● Terminate character is not followed by /K/ characters in lanes 2 and 3 ● The column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 8-90. KR_VS_LN2_EOP_ERROR_COUNTER

Device Address: 0x01	Register Address: 0x8012	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	KR_LN2_EOP_ERR_COUNT (R)	Lane 2 End of packet Error counter. End of packet error is detected when Terminate character is in lane 2 and one or both of the following holds: ● Terminate character is not followed by /K/ characters in lane 3 ● The column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 8-91. KR_VS_LN3_EOP_ERROR_COUNTER

Device Address: 0x01	Register Address: 0x8013	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	KR_LN3_EOP_ERR_COUNT (R)	Lane 3 End of packet Error counter. End of packet error is detected when Terminate character is in lane 3 and the column following the terminate column is neither ||K|| nor ||A||. Counter value cleared to 16'h0000 when read.	COR

Table 8-92. KR_VS_TX_CTC_DROP_COUNT

Device Address: 0x01	Register Address: 0x8014	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_CTC_DROP_COUNT (R)	Counter for number of idle drops in the transmit CTC.	COR

Table 8-93. KR_VS_TX_CTC_INSERT_COUNT

Device Address: 0x01	Register Address: 0x8015	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_CTC_INS_COUNT (R)	Counter for number of idle inserts in the transmit CTC.	COR

Table 8-94. KR_VS_RX_CTC_DROP_COUNT

Device Address: 0x01	Register Address: 0x8016	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	RX_CTC_DROP_COUNT (R)	Counter for number of idle drops in the receive CTC.	COR

Table 8-95. KR_VS_RX_CTC_INSERT_COUNT

Device Address: 0x01	Register Address: 0x8017	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	RX_CTC_INS_COUNT (R)	Counter for number of idle inserts in the receive CTC.	COR

Table 8-96. KR_VS_STATUS_1

Device Address: 0x01	Register Address: 0x8018	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	TX_TPV_TP_SYNC (R)	0 = Test pattern sync is not achieved on on Tx side 1 = Test pattern sync is achieved on on Tx side	RO
11	RESERVED	For TI use only	
5	INVALID_S_COL_ERR (R)	1 = Indicates invalid start (S) column error detected	RO/LH
4	INVALID_T_COL_ERR (R)	1 = Indicates invalid terminate (T) column error detected	
3	INVALID_XGMII_LN3 (R)	1 = Indicates invalid XGMII character detected in Lane 3	
2	INVALID_XGMII_LN2 (R)	1 = Indicates invalid XGMII character detected in Lane 2	
1	INVALID_XGMII_LN1 (R)	1 = Indicates invalid XGMII character detected in Lane 1	
0	INVALID_XGMII_LN0 (R)	1 = Indicates invalid XGMII character detected in Lane 0	

Table 8-97. KR_VS_TX_CRCJ_ERR_COUNT_1

Device Address: 0x01	Register Address: 0x8019	Default: 0xFFFF	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_TPV_CR_CJ_ERR_COUNT[31:16] (R)	Error Counter for CR/CJ test pattern verification on Tx side. MSBs [31:16]	COR

Table 8-98. KR_VS_TX_CRCJ_ERR_COUNT_2

Device Address: 0x01	Register Address: 0x801A	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_TPV_CR_CJ_ERR_COUNT[15:0] (R)	Error Counter for CR/CJ test pattern verification on Tx side LSBs [15:0]	COR

Table 8-99. KR_VS_TX_LN0_HLM_ERR_COUNT

Device Address: 0x01	Register Address: 0x801B	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_TPV_LN0_ERR_COUNT[15:0] (R)	Error Counter for H/L/M test pattern verification on Lane 0 of Tx side	COR

Table 8-100. KR_VS_TX_LN1_HLM_ERR_COUNT

Device Address: 0x01	Register Address: 0x801C	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_TPV_LN1_ERR_COUNT[15:0] (R)	Error Counter for H/L/M test pattern verification on Lane 1 of Tx side	COR

Table 8-101. KR_VS_TX_LN2_HLM_ERR_COUNT

Device Address: 0x01	Register Address: 0x801D	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_TPV_LN2_ERR_COUNT[15:0] (R)	Error Counter for H/L/M test pattern verification on Lane 2 of Tx side	COR

Table 8-102. KR_VS_TX_LN3_HLM_ERR_COUNT

Device Address: 0x01	Register Address: 0x801E	Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_TPV_LN3_ERR_COUNT[15:0] (R)	Error Counter for H/L/M test pattern verification on Lane 3 of Tx side	COR

Table 8-103. LT_VS_CONTROL_2

Device Address: 0x01	Register Address: 0x9001	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only (Default 2'b00)	RW
13:12	RESERVED	For TI use only (Default 2'b00)	RW/SC
11:9	AP_SEARCH_MODE[2:0] (RXG)	000 = Auto search, autotrain disabled (Default 3'b000) 001 = Full region search, autotrain disabled 010 = Auto search, autotrain enabled 011 = Full region search, autotrain enabled 1xx = Manual search	RW
8:0	RESERVED	For TI use only (Default 9'b000000000)	RW

8.3 PCS Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x03 (DEVADD [4:0] = 5'b00011). Valid only when device is in 10GBASE-KR mode.

Table 8-104. PCS_CONTROL

Device Address: 0x03	Register Address: 0x0000	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	PCS_RESET (R)	1 = Resets datapath and MDIO registers of all channels. Equivalent to asserting RESET_N. 0 = Normal operation (Default 1'b0)	RW/SC
14	PCS_LOOPBACK (R)	1 = Enables PCS loopback 0 = Normal operation (Default 1'b0) Requires Auto Negotiation and Link Training to be disabled.	RW
13:12	RESERVED	For TI use only. Always reads 0.	RW
11	PCS_LP_MODE (R)	1 = Enable power down mode 0 = Normal operation (Default 1'b0)	RW
10:0	RESERVED	For TI use only. Always reads 0.	RW

Table 8-105. PCS_STATUS_1

Device Address: 0x03	Register Address: 0x0001	Default: 0x0002	
Bit(s)	**Name**	**Description**	**Access**
7	PCS_FAULT (R)	1 = Fault condition detected on either PCS TX or PCS RX 0 = No fault condition detected This bit is cleared after Register 03.0008 is read and no fault condition occurs after 03.0008 is read.	RO
2	PCS_RX_LINK (R)	1 = PCS receive link is up 0 = PCS receive link is down	RO/LL
1	PCS_LP_ABILITY (R)	Always reads 1. 1 = Supports low power mode 0 = Does not support low power mode	RO

Table 8-106. PCS_STATUS_2

Device Address: 0x03	Register Address: 0x0008	Default: 0x8001	
Bit(s)	**Name**	**Description**	**Access**
15:14	DEV_PRESENT (R)	Always reads 2'b10. 0x = No device responding at this address 10 = Device responding at this address 11 = No device responding at this address	RO
11	PCS_TX_FAULT (R)	1 = Fault condition detected on transmit path 0 = No fault condition detected on transmit path	RO/LH
10	PCS_RX_FAULT (R)	1 = Fault condition detected on receive path 0 = No fault condition detected on receive path	RO/LH
0	PCS_10GBASER_CAPABLE (R)	Always reads 1. 1 = PCS is able to support 10GBASE-R PCS type 0 = PCS not able to support 10GBASE-R PCS type	RO

Table 8-107. KR_PCS_STATUS_1

Device Address: 0x03	Register Address: 0x0020	Default: 0x0004	
Bit(s)	**Name**	**Description**	**Access**
12	PCS_RX_LINK_STATUS (R)	1 = 10GBASE-R PCS receive link up 0 = 10GBASE-R PCS receive link down	RO
2	PCS_PRBS31_ABILITY (R)	Always reads 1. 1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 testing	RO

Table 8-107. KR_PCS_STATUS_1 (continued)

Device Address: 0x03	Register Address: 0x0020	Default: 0x0004	
Bit(s)	**Name**	**Description**	**Access**
1	PCS_HI_BER (R)	1 = High BER condition detected 0 = High BER condition not detected	RO
0	PCS_BLOCK_LOCK (R)	1 = PCS locked to receive blocks 0 = PCS not locked to receive blocks	RO

Table 8-108. KR_PCS_STATUS_2

Device Address: 0x03	Register Address: 0x0021	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	PCS_BLOCK_LOCK_LL (R)	1 = PCS locked to receive blocks 0 = PCS not locked to receive blocks	RO/LL
14	PCS_HI_BER_LH (R)	1 = High BER condition detected 0 = High BER condition not detected	RO/LH
13:8	PCS_BER_COUNT[5:0] (R)	Value indicating number of times BER state machine enters BER_BAD_SH state	COR
7:0	PCS_ERR_BLOCK_COUNT[7:0] (R)	Value indicating number of times RX decode state machine enters RX_E state. Same value is also reflected in 1E.0010 and reading either register clears the counter value.	COR

Table 8-109. PCS_TP_SEED_A0

Device Address: 0x03	Register Address: 0x0022	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_A[15:0] (R)	Test pattern seed A bits 15-0	RW

Table 8-110. PCS_TP_SEED_A1

Device Address: 0x03	Register Address: 0x0023	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_A[31:16] (R)	Test pattern seed A bits 31-16	RW

Table 8-111. PCS_TP_SEED_A2

Device Address: 0x03	Register Address: 0x0024	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_A[47:32] (R)	Test pattern seed A bits 47-32	RW

Table 8-112. PCS_TP_SEED_A3

Device Address: 0x03	Register Address: 0x0025	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9:0	PCS_TP_SEED_A[57:48] (R)	Test pattern seed A bits 57-48	RW

Table 8-113. PCS_TP_SEED_B0

Device Address: 0x03	Register Address: 0x0026	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_B[15:0] (R)	Test pattern seed B bits 15-0	RW

Table 8-114. PCS_TP_SEED_B1

Device Address: 0x03	Register Address: 0x0027	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_B[31:16] (R)	Test pattern seed B bits 31-16	RW

Table 8-115. PCS_TP_SEED_B2

Device Address: 0x03	Register Address: 0x0028	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	PCS_TP_SEED_B[47:32] (R)	Test pattern seed B bits 47-32	RW

Table 8-116. PCS_TP_SEED_B3

Device Address: 0x03	Register Address: 0x0029	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9:0	PCS_TP_SEED_B[57:48] (R)	Test pattern seed B bits 57-48	RW

Table 8-117. PCS_TP_CONTROL

Device Address: 0x03	Register Address: 0x002A	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:6	RESERVED	For TI use only. Always reads 0.	RW
5	PCS_PRBS31_RX_TP_EN (R)	1 = Enable PRBS31 test pattern verification on receive path 0 = Normal operation (Default 1'b0)	RW
4	PCS_PRBS31_TX_TP_EN (R)	1 = Enable PRBS31 test pattern generation on transmit path 0 = Normal operation (Default 1'b0)	RW
3	PCS_TX_TP_EN (R)	1 = Enable transmit test pattern generation 0 = Normal operation (Default 1'b0)	RW
2	PCS_RX_TP_EN (R)	1 = Enable receive test pattern verification 0 = Normal operation (Default 1'b0)	RW
1	PCS_TP_SEL (R)	1 = Square wave test pattern 0 = Pseudo random test pattern (Default 1'b0)	RW
0	PCS_DP_SEL (R)	1 = 0'S data pattern 0 = LF data pattern (Default 1'b0)	RW

Table 8-118. PCS_TP_ERR_COUNT

Device Address: 0x03	Register Address: 0x002B	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	PCS_TP_ERR_COUNT[15:0] (R)	Test pattern error counter. This counter reflects number of errors occurred during the test pattern mode selected through PCS_TP_CONTROL. In PRBS31 test pattern verification mode, counter value indicates the number of received bytes that have 1 or more bit errors.	COR

Table 8-119. PCS_VS_CONTROL

Device Address: 0x03	Register Address: 0x8000	Default: 0x00B0	
Bit(s)	**Name**	**Description**	**Access**
15:8	RESERVED	For TI use only. Always reads 0.	RW
7:4	PCS_SQWAVE_N (R)	Sets number of repeating 0's followed by repeating 1's during square wave test pattern generation mode (Default 4'1011)	RW
3	RESERVED	For TI use only (Default 1'b0)	RW

Table 8-119. PCS_VS_CONTROL (continued)

Device Address: 0x03	Register Address: 0x8000	Default: 0x00B0	
Bit(s)	**Name**	**Description**	**Access**
2	PCS_RX_DEC_CTRL_CHAR (R)	PCS RX Decode control character selection. Determines what control characters are passed 0 = A/K/R control characters are changed to Idles. Reserved characters passed through (Default 1'b0) 1 = A/K/R control characters are passed through as is RW	RW
1	PCS_DESCR_DISABLE (R)	De-scrambler control in 10GKR RX PCS 1 = Disable descrambler 0 = Enable descrambler (Default 1'b0)	RW
0	PCS_SCR_DISABLE (R)	Scrambler control in 10GKR TX PCS 1 = Disable scrambler 0 = Enable scrambler (Default 1'b0)	RW

Table 8-120. PCS_VS_STATUS

Device Address: 0x03	Register Address: 0x8010	Default: 0x00FD	
Bit(s)	**Name**	**Description**	**Access**
13	UNCORR_ERR_STATUS (R)	1 = Uncorrectable block error found	RO/LH
12	CORR_ERR_STATUS (R)	1 = Correctable block error found	RO/LH
8	PCS_TP_ERR (R)	PCS test pattern verification status PCS_SCR_DISABLE 1 = Error occurred during pseudo random test pattern verification Number of errors can be checked by reading PCS_TP_ERR_COUNT (03.002B) register	RO/LH
7:0	RESERVED	For TI use only.	COR

8.4 Auto-Negotiation Registers

The registers below can be accessed only in Clause 45 mode and with device address field set to 0x07 (DA[4:0] = 5'b00111)

Table 8-121. AN_CONTROL

Device Address: 0x07	Register Address: 0x0000	Default: 0x3000	
Bit(s)	**Name**	**Description**	**Access**
15	AN_RESET (RX)	1 = Resets Auto Negotiation 0 = Normal operation (Default 1'b0)	RW/SC
14	RESERVED	For TI use only. Always reads 0.	RW
13	RESERVED	For TI use only (Default 1'b1)	RW
12	AN_ENABLE (RX)	1 = Enable Auto Negotiation (Default 1'b1) 0 = Disable Auto Negotiation	RW
11:10	RESERVED	For TI use only. Always reads 0.	RW
9	AN_RESTART (RX)	1 = Restart Auto Negotiation 0 = Normal operation (Default 1'b0) If set, a read of this register is required to clear AN_RESTART bit.	RW/SC (1)
8:0	RESERVED	For TI use only. Always reads 0.	RW

(1) If set, a read of register 07.0000 is required to clear AN_RESTART bit.

Table 8-122. AN_STATUS

Device Address: 0x07	Register Address: 0x0001	Default: 0x0088	
Bit(s)	**Name**	**Description**	**Access**
9	AN_PAR_DET_FAULT (RX)	1 = Fault has been detected via parallel detection function 0 = Fault has not been detected via parallel detection function	RO/LH
7	AN_EXP_NP_STATUS (RX)	1 = Extended next page is used 0 = Extended next page is not allowed	RO

Table 8-122. AN_STATUS (continued)

Device Address: 0x07	Register Address: 0x0001	Default: 0x0088	
Bit(s)	**Name**	**Description**	**Access**
6	AN_PAGE_RCVD (RX)	1 = A page has been received 0 = A page has not been received	RO/LH
5	AN_COMPLETE (RX)	1 = Auto Negotiation process is completed 0 = Auto Negotiation process not completed	RO
4	REMOTE_FAULT (RX)	1 = Remote fault detected by AN 0 = Remote fault not detected by AN	RO/LH
3	AN_ABILITY (RX)	Always reads 1. 1 = Device is able to perform Auto Negotiation 0 = Device not able to perform Auto Negotiation	RO
2	LINK_STATUS (RX)	1 = Link is up 0 = Link is down	RO/LL
0	AN_LP_ABILITY (RX)	1 = LP is able to perform Auto Negotiation 0 = LP not able to perform Auto Negotiation	RO

Table 8-123. AN_DEV_PACKAGE

Device Address: 0x07	Register Address: 0x0005	Default: 0x0080	
Bit(s)	**Name**	**Description**	**Access**
7	AN_PRESENT (RX)	Always reads 1 1 = Auto Negotiation present in the package 0 = Auto Negotiation not present in the package	RO

Table 8-124. AN_ADVERTISEMENT_1

Device Address: 0x07	Register Address: 0x0010	Default: 0x1001	
Bit(s)	**Name**	**Description**	**Access**
15	AN_NEXT_PAGE (RX)	NP bit (D15) in base link codeword 1 = Next page available 0 = Next page not available (Default 1'b0)	RW
14	AN_ACKNOWLEDGE (RX)	Acknowledge bit (D14) in base link codeword. Always reads 0.	RO
13	AN_REMOTE_FAULT (RX)	RF bit (D13) in base link codeword 1 = Sets RF bit to 1 0 = Normal operation (Default 1'b0)	RW
12:10	AN_CAPABILITY[2:0] (RX)	Value to be set in D12:D10 bits of the base link codeword. Consists of abilities like PAUSE, ASM_DIR (Default 3'b100)	RW
9:5	AN_ECHO_NONCE[4:0] (RX)	Value to be set in D9:D5 bits of the base link codeword. Consists of Echo nonce value. Transmitted in base page only until local device and link Partner have exchanged unique Nonce values, at which time transmitted Echoed Nonce will change to Link Partner's Nonce value. Read value always reflects the value written, not the actual Echoed Nonce. (Default 5'b00000)	RW
4:0	AN_SELECTOR[4:0] (RX)	Value to be set in D4:D0 bits of the base link codeword. Consists of selector field value (Default 5'b00001)	RW

Table 8-125. AN_ADVERTISEMENT_2

Device Address: 0x07	Register Address: 0x0011	Default: 0x0080	
Bit(s)	**Name**	**Description**	**Access**
15:8	AN_ABILITY[10:3] (RX)	Value to be set in D31:D24 bits of the base link codeword. Consists of technology ability field bits [10:3] (Default 9'b000000000)	RW
7	AN_ABILITY[2] (RX)	Value to be set in D23 bits of the base link codeword. Consists of technology ability field bits [2]. When set, indicates device supports 10GBASE-KR (Default 1'b1)	RW
6	AN_ABILITY[1] (RX)	Value to be set in D22 bits of the base link codeword. Consists of technology ability field bits [1]. Always set to 0 (Default 1'b0)	RW

Table 8-125. AN_ADVERTISEMENT_2 (continued)

Device Address: 0x07	Register Address: 0x0011	Default: 0x0080	
Bit(s)	**Name**	**Description**	**Access**
5	AN_ABILITY[0] (RX)	Value to be set in D21 bits of the base link codeword. Consists of technology ability field bit [0]. When set, indicates device supports 1000BASE-KX (Default 1'b0)	RW
4:0	AN_TRANS_NONCE_ FIELD[4:0] (RX)	Not used. Transmitted Nonce field is generated by hardware random number generator. Read value always reflects value written, not the actual Transmitted Nonce (Default 5'b00000)	RW

Table 8-126. AN_ADVERTISEMENT_3

Device Address: 0x07	Register Address: 0x0012	Default: 0x4000	
Bit(s)	**Name**	**Description**	**Access**
15	AN_FEC_REQUESTED (RX)	Value to be set in D47 bits of the base link codeword. When set, indicates a request to enable FEC on the link (Default 1'b0)	RW
14	AN_FEC_ABILITY (RX)	Value to be set in D46 bits of the base link codeword. When set, indicates 10GBASE-KR has FEC ability (Default 1'b1)	
13:0	AN_ABILITY[24:11] (RX)	Value to be set in D45:D32 bits of the base link codeword. Consists of technology ability field bits [24:11] (Default 14'b00000000000000)	

Table 8-127. AN_LP_ADVERTISEMENT_1(1)

Device Address: 0x07	Register Address: 0x0013	Default: 0x0001	
Bit(s)	**Name**	**Description**	**Access**
15	AN_LP_NEXT_PAGE (RX)	NP bit (D15) in link partner base page 1 = Next page available in link partner 0 = Next page not available in link partner	RO
14	AN_LP_ACKNOWLEDGE (RX)	Acknowledge bit (D14) in link partner base page.	RO
13	AN_LP_REMOTE_FAULT (RX)	RF bit (D13) in link partner base page 1 = Remote fault detected in link partner 0 = Remote fault not detected in link partner	RO
12:10	AN_ LP_CAPABILITY (RX)	D12:D10 bits of the link partner base page. Consists of abilities like PAUSE, ASM_DIR	RO
9:5	AN_ LP_ECHO_NONCE (RX)	D9:D5 bits of the link partner base page. Consists of Echo nonce value	RO
4:0	AN_LP_SELECTOR[4:0] (RX)	D4:D0 bits of the link partner base page. Consists of selector field value Always reads 5'b00001	RO

(1) To get accurate AN_LP_ADVERTISEMENT read value, Register 07.0013 should be read first before reading 07.0014 and 07.0015

Table 8-128. AN_LP_ADVERTISEMENT_2

Device Address: 0x07	Register Address: 0x0014	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:8	AN_ LP_ABILITY[10:3] (RX)	D31:D24 bits of the link partner base page. Consists of technology ability field bits [10:3]	RO
7	AN_LP_ABILITY[2] (RX)	D23 bits of the link partner base page. Consists of technology ability field bits [2]. When high, indicates link partner supports 10GBASE-KR	
6	AN_LP_ABILITY[1] (RX)	D22 bits of the link partner base page. Consists of technology ability field bits [1].	
5	AN_LP_ABILITY[0] (RX)	D21 bits of the link partner base page. Consists of technology ability field bit [0]. When high, indicates link partner supports 1000BASE-KX	
4:0	AN_LP_TRANS_NONCE_ FIELD (RX)	D20:D16 bits of the link partner base page. Consists of transmitted nonce value	

Table 8-129. AN_LP_ADVERTISEMENT_3

Device Address: 0x07	Register Address: 0x0015	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	AN_LP_FEC_REQUESTED (RX)	D47 bits of the link partner base page. When high, indicates link partner request to enable FEC on the link	RO
14	AN_LP_FEC_ABILITY (RX)	D46 bits of the link partner base page. When high, indicates link partner has FEC ability	
13:0	AN_LP_ABILITY[24:11] (RX)	D45:D32 bits of the link partner base page. Consists of link partner technology ability field bits [24:11]	

Table 8-130. AN_XNP_TRANSMIT_1

Device Address: 0x07	Register Address: 0x0016	Default: 0x2000	
Bit(s)	**Name**	**Description**	**Access**
15	AN_XNP_NEXT_PAGE (RX)	NP bit (D15) in next page code word 1 = Next page available 0 = Next page not available (Default 1'b0)	RW
14	RESERVED	Always reads 0.	RO
13	AN_MP (RX)	Message page bit (D13) in next page code word 1 = Sets MP bit to 1 indicating next page is a message page (Default 1'b1) 0 = Sets MP bit to 0 indicating next page is unformatted next page	RW
12	AN_ACKNOWLEDGE_2 (RX)	Value to be set in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	RW
11	AN_TOGGLE (RX)	Not used. Toggle value is generated by hardware. Read value always reflects value written, not the actual Toggle field (Default 1'b0)	RW
10:0	AN_CODE_FIELD (RX)	Value to be set in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b00000000000)	RW

Table 8-131. AN_XNP_TRANSMIT_2

Device Address: 0x07	Register Address: 0x0017	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	AN_MSG_CODE_1 (RX)	Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RW

Table 8-132. AN_XNP_TRANSMIT_3

Device Address: 0x07	Register Address: 0x0018	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	AN_MSG_CODE_2 (RX)	Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RW

Table 8-133. AN_LP_XNP_ABILITY_1 (1)

Device Address: 0x07	Register Address: 0x0019	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	AN_LP_XNP_NEXT_PAGE (RX)	NP bit (D15) in next page code word 1 = Next page available 0 = Next page not available (Default 1'b0)	RO
14	AN_LP_XNP_ACKNOWLEDGE (RX)	Value in D14 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	RO
13	AN_LP_MP (RX)	Message page bit (D13) in next page code word 1 = Sets MP bit to 1 indicating next page is a message page 0 = Sets MP bit to 0 indicating next page is unformatted next page (Default 1'b0)	RO
12	AN_LP_ACKNOWLEDGE_2 (RX)	Value in D12 bit of the next page code word. When set, indicates device is able to act on the information defined in the message (Default 1'b0)	RO

(1) To get accurate AN_LP_XNP_ABILITYT read value, Register 07.0019 should be read first before reading 07.001A and 07.001B

Table 8-133. AN_LP_XNP_ABILITY_1[(1)] (continued)

Device Address: 0x07	Register Address: 0x0019	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
11	AN_LP_TOGGLE (RX)	Value of D11 bit of the next page code word. Consists of Toggle field value(Default 1'b0)	RO
10:0	AN_ LP_CODE_FIELD (RX)	Value in D10:D0 bits of the next page code word. Consists of Message/Unformatted code field value (Default 11'b00000000000)	RO

Table 8-134. AN_LP_XNP_ABILITY_2

Device Address: 0x07	Register Address: 0x001A	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	AN_LP_MSG_CODE_1 (RX)	Value to be set in D31:D16 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RO

Table 8-135. AN_LP_XNP_ABILITY_3

Device Address: 0x07	Register Address: 0x001B	Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	AN_LP_MSG_CODE_2 (RX)	Value to be set in D47:D32 bits of the next page code word. Consists of Message/Unformatted code field value (Default 16'b0000000000000000)	RO

Table 8-136. AN_BP_STATUS

Device Address: 0x07	Register Address: 0x0030	Default: 0x0001	
Bit(s)	**Name**	**Description**	**Access**
4	AN_10G_KR_FEC (RX)	1 = PMA/PMD is negotiated to perform 10GBASE-KR FEC	RO
3	AN_10G_KR (RX)	1 = PMA/PMD is negotiated to perform 10GBASE-KR	
1	AN_1G_KX (RX)	1 = PMA/PMD is negotiated to perform 1000BASE-KX	
0	AN_BP_AN_ABILITY (RX)	Always reads 1. 1 = Indicates 1000BASE-KX, 10GBASE-KR is implemented	

Table 8-137. TI_Reserved Control and Status Registers

Register Name	Register Address	Default Value	Access		Register Name	Register Address	Default Value	Access
TI_RESERVED_CONTROL	1E.8000	0x04C0	RW		TI_RESERVED_STATUS	1E.A014	0x0000	RO
TI_RESERVED_CONTROL	1E.8001	0x0207	RW		TI_RESERVED_STATUS	1E.A015	0x0000	RO
TI_RESERVED_CONTROL	1E.8002	0x02FE	RW		TI_RESERVED_STATUS	1E.A016	0x0000	RO
TI_RESERVED_CONTROL	1E.8005	0x0000	RW		TI_RESERVED_STATUS	1E.A017	0x0000	RO
TI_RESERVED_CONTROL	1E.8006	0x0000	RW		TI_RESERVED_STATUS	1E.A018	0x0000	RO
TI_RESERVED_CONTROL	1E.8007	0x8000	RW		TI_RESERVED_CONTROL	1E.A116	0x0000	RW
TI_RESERVED_CONTROL	1E.8008	0x0000	RW		TI_RESERVED_CONTROL	1E.A117	0x0000	RW
TI_RESERVED_CONTROL	1E.8009	0xFC00	RW		TI_RESERVED_STATUS	1E.A118	0x0000	RO
TI_RESERVED_CONTROL	1E.800A	0xBC3C	RW		TI_RESERVED_STATUS	1E.A119	0x0000	RO
TI_RESERVED_CONTROL	1E.800B	0x0000	RW		TI_RESERVED_CONTROL	01.8000	0x4800	RW
TI_RESERVED_CONTROL	1E.800C	0x0000	RW		TI_RESERVED_STATUS	01.801F	0xFFFD	COR
TI_RESERVED_CONTROL	1E.800D	0x01FC	RW		TI_RESERVED_STATUS	01.8020	0xFFFD	COR
TI_RESERVED_CONTROL	1E.800E	0x0000	RW		TI_RESERVED_STATUS	01.8021	0xFFFD	COR
TI_RESERVED_CONTROL	1E.800F	0x00C0	RW		TI_RESERVED_STATUS	01.8022	0xFFFD	COR
TI_RESERVED_CONTROL	1E.8011	0x7F00	RW		TI_RESERVED_STATUS	01.8023	0xFFFF	COR
TI_RESERVED_STATUS	1E.8012	0xFFFD	COR		TI_RESERVED_STATUS	01.8024	0xFFFD	COR

Table 8-137. TI_Reserved Control and Status Registers (continued)

Register Name	Register Address	Default Value	Access		Register Name	Register Address	Default Value	Access
TI_RESERVED_STATUS	1E.8013	0xFFFD	COR		TI_RESERVED_CONTROL	01.9000	0x0249	RW
TI_RESERVED_STATUS	1E.8014	0x0000	RO/LH		TI_RESERVED_CONTROL	01.9002	0x1335	RW
TI_RESERVED_STATUS	1E.8015	0x0000	RO		TI_RESERVED_CONTROL	01.9003	0x5E29	RW
TI_RESERVED_CONTROL	1E.8019	0xFC00	RW		TI_RESERVED_CONTROL	01.9004	0x007F	RW
TI_RESERVED_CONTROL	1E.801A	0xBC3C	RW		TI_RESERVED_CONTROL	01.9005	0x1C00	RW
TI_RESERVED_CONTROL	1E.801C	0x0000	RW		TI_RESERVED_CONTROL	01.9006	0x0000	RW
TI_RESERVED_CONTROL	1E.801D	0x01FC	RW		TI_RESERVED_CONTROL	01.9007	0x5120	RW
TI_RESERVED_CONTROL	1E.801E	0x0000	RW		TI_RESERVED_CONTROL	01.9008	0xC018	RW
TI_RESERVED_CONTROL	1E.801F	0x00C0	RW		TI_RESERVED_CONTROL	01.9009	0xE667	RW
TI_RESERVED_CONTROL	1E.8020	0x0200	RW		TI_RESERVED_CONTROL	01.900A	0x5E8F	RW
TI_RESERVED_CONTROL	1E.8022	0x0000	RW		TI_RESERVED_CONTROL	01.900B	0xAFAF	RW
TI_RESERVED_CONTROL	1E.8023	0x0000	RW		TI_RESERVED_CONTROL	01.900C	0x0800	RW
TI_RESERVED_CONTROL	1E.8024	0x0000	RW		TI_RESERVED_CONTROL	01.900D	0x461A	RW
TI_RESERVED_CONTROL	1E.8025	0xF000	RW		TI_RESERVED_CONTROL	01.900E	0x1723	RW
TI_RESERVED_STATUS	1E.8030	0x0000	RO		TI_RESERVED_CONTROL	01.900F	0x7003	RW
TI_RESERVED_STATUS	1E.8031	0x0000	RO		TI_RESERVED_CONTROL	01.9010	0x0851	RW
TI_RESERVED_STATUS	1E.8032	0x0000	RO		TI_RESERVED_CONTROL	01.9011	0x1EFF	RW
TI_RESERVED_STATUS	1E.8033	0x0000	RO		TI_RESERVED_STATUS	01.9020	0x0000	RO
TI_RESERVED_STATUS	1E.8034	0x0000	RO		TI_RESERVED_STATUS	01.9021	0xFFFD	COR
TI_RESERVED_STATUS	1E.8035	0x0000	RO		TI_RESERVED_STATUS	01.9022	0x0000	RO
TI_RESERVED_CONTROL	1E.8050	0x0000	RW		TI_RESERVED_STATUS	01.9023	0x0000	RO
TI_RESERVED_CONTROL	1E.8102	0xF280	RW		TI_RESERVED_STATUS	01.9024	0x0000	RO
TI_RESERVED_CONTROL	1E.A000	0x0000	RW		TI_RESERVED_STATUS	01.9025	0x0000	RO
TI_RESERVED_STATUS	1E.A010	0x0000	RO		TI_RESERVED_STATUS	01.9026	0x0000	RO
TI_RESERVED_STATUS	1E.A011	0x0000	RO		TI_RESERVED_STATUS	01.9027	0x0000	RO
TI_RESERVED_STATUS	1E.A012	0x0000	RO		TI_RESERVED_STATUS	01.9028	0x0000	RO
TI_RESERVED_STATUS	1E.A013	0x0000	RO		TI_RESERVED_STATUS	01.9029	0x0000	RO

9 ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	DVDD, VDDA_LS/HS, VDDT_LS/HS, VPP, VDDD	–0.3	1.4	V
	VDDRA/B_LS/HS, VDDO[1:0]	–0.3	2.2	V
Input Voltage, V_I, (LVCMOS/CML/Analog)		–0.3	Supply + 0.3	V
Storage temperature		–65	150	°C
Operating Junction Temperature			105	°C
Electrostatic Discharge:	HBM		1	kV
	CDM		500	V
Characterized free-air operating temperature range		–40	85	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground (VSS).

9.2 Recommended Operating Conditions

PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Digital / analog supply voltages	VDDD, VDDA_LS/HS, DVDD, VDDT_LS/HS, VPP		0.95	1.00	1.05	V
	SERDES PLL regulator voltage	VDDRA_LS/HS, VDDRB_LS/HS	1.5V Nominal	1.425	1.5	1.575	V
			1.8V Nominal	1.71	1.8	1.89	
	LVCMOS I/O supply voltage	VDDO[1:0]	1.5V Nominal	1.425	1.5	1.575	V
			1.8V Nominal	1.71	1.8	1.89	
I_{DD}	Supply current	VDDD	10.3 Gbps			650	mA
		VDDA_LS/HS				650	
		DVDD + VPP				700	
		VDDT_LS/HS				600	
		VDDRA/B_LS				70	
		VDDRA/B_HS				70	
		VDDO[1:0]				10	
P_D	Power dissipation		Nominal		1.6		W
			Worst case supply voltage, temperature, and process. 10GBASE-KR, Both channels active, default swing and Clkout settings			2.3	
I_{SD}	Shutdown current	VDDD	PD* Asserted			300	mA
		VDDA				85	
		DVDD + VPP				250	
		VDDT				65	
		VDDRA_HS/LS + VDDRB_HS/LS				7	
		VDDO				5	
J_R	REFCLK0P/N, REFCLK1P/N Random Jitter		12kHz to 20MHz			1	ps

9.3 High Speed Side Serial Transmitter Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{OD(p-p)}$	TX Output differential peak-to-peak voltage swing, transmitter enabled	SWING = 0000	50	130	220	mV_{pp}
		SWING = 0001	110	220	320	
		SWING = 0010	180	300	430	
		SWING = 0011	250	390	540	
		SWING = 0100	320	480	650	
		SWING = 0101	390	570	770	
		SWING = 0110	460	660	880	
		SWING = 0111	530	750	1000	
		SWING = 1000	590	830	1100	
		SWING = 1001	660	930	1220	
		SWING = 1010	740	1020	1320	
		SWING = 1011	820	1110	1430	
		SWING = 1100	890	1180	1520	
		SWING = 1101	970	1270	1610	
		SWING = 1110	1060	1340	1680	
		SWING = 1111	1090	1400	1740	
		Transmitter disabled			30	
$V_{pre/post}$	TX Output pre/post cursor emphasis voltage	See register bits TWPOST1, TWPOST2, and TWPRE for de-emphasis settings. See Figure 9-2	–17.5/ –37.5%		+17.5/ +37.5%	
V_{CMT}	TX Output common mode voltage	100-Ω differential termination. DC-coupled.		V_{DDT} - 0.25 * $V_{OD(p-p)}$		mV
t_{skew}	Intra-pair output skew	Serial Rate = 9.8304 Gbps			0.045	UI
T_r, T_f	Differential output signal rise, fall time (20% to 80%), Differential Load = 100Ω		24			ps
J_{T1}	Serial output total jitter (CPRI LV/LV-II/LV-III, OBSAI and 10GBASE-KR Rates)	Serial Rate ≤ 3.072Gbps			0.35	UI_{pp}
		Serial Rate > 3.072Gbps			0.28	
J_{D1}	Serial output deterministic jitter (CPRI LV/LV-II/LV-III, OBSAI and 10GBASE-KR Rates)	Serial Rate ≤ 3.072Gbps			0.17	UI_{pp}
		Serial Rate > 3.072Gbps			0.15	
J_{R1}	Serial output random jitter (CPRI LV/LV-II/LV-III, OBSAI and 10GBASE-KR Rates)	Serial Rate > 3.072Gbps			0.15	UI_{pp}
J_{T2}	Serial output total jitter (CPRI E.12.HV)	Serial Rate = 1.2288Gbps			0.279	UI_{pp}
J_{D2}	Serial output deterministic jitter (CPRI E.12.HV)				0.14	
SDD22	Differential output return loss	50 MHz < f < 2.5 GHz			9	dB
		2.5 GHz < f < 7.5 GHz			See (1)	dB
SCC22	Common-mode output return loss	50 MHz < f < 2.5 GHz			6	dB
		2.5 GHz < f < 7.5 GHz			See (2)	dB
$T_{(LATENCY)}$	Transmit path latency	10GBASE-KR mode		see Figure 3-5		
		1GBASE-KX mode		see Figure 4-2		
		General Purpose mode		see Figure 5-4		

(1) Differential input return loss, SDD22 = 9 – 12 $\log_{10}$(f / 2500MHz)) dB
(2) Common-mode output return loss, SDD22 = 6 – 12 log10(f / 2500MHz)) dB

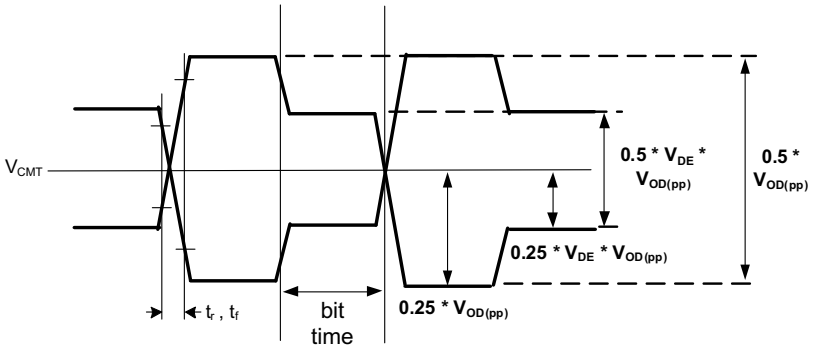
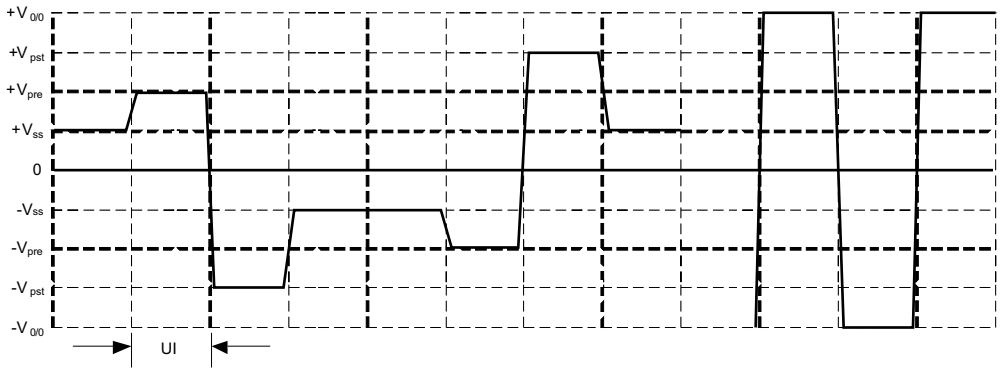


Figure 9-1. Transmit Output Waveform Parameter Definitions



h_{-1} = TWPRE (0% ≥ -17.5% for typical application) setting

h_1 = TWPOST1 (0% ≥ -37.5% for typical application) setting

$h_0 = 1 - |h_1| - |h_{-1}|$

$V_{0/0}$ = Output Amplitude with TWPRE = 0%, TWPOST = 0%.

V_{ss} = Steady State Output Voltage = $V_{0/0} * | h_1 + h_0 + h_{-1}|$

V_{pre} = PreCursor Output Voltage = $V_{0/0} * | -h_1 - h_0 + h_{-1}|$

V_{pst} = PostCursor Output Voltage = $V_{0/0} * | -h_1 + h_0 + h_{-1}|$

Figure 9-2. Pre/Post Cursor Swing Definitions

9.4 High Speed Side Serial Receiver Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{ID}	RX Input differential voltage, |RXP – RXN|	Full Rate, AC Coupled	50		600	mV
		Half/Quarter/Eighth Rate, AC Coupled	50		800	
$V_{ID(pp)}$	RX Input differential peak-to-peak voltage swing, 2×|RXP – RXN|	Full Rate, AC Coupled	100		1200	mV_{pp}
		Half/Quarter/Eighth Rate, AC Coupled	100		1600	
C_I	RX Input capacitance				2	pF
J_{TOL}	10GBASE-KR Jitter tolerance, test channel with mTC =1 (see Figure 9-3 for attenuation curve), PRBS31 test pattern at 10.3125 Gbps	Applied sinusoidal jitter			0.115	UI_{pp}
		Applied random jitter			0.130	
		Applied duty cycle distortion			0.035	
		Broadband noise amplitude (RMS)			5.2	
SDD11	Differential input return loss	50 MHz < f < 2.5 GHz	9			dB
		2.5 GHz < f < 7.5 GHz	See (1)			
t_{skew}	Intra-pair input skew				0.23	UI

(1) Differential input return loss, SDD11 = 9 – 12 $\log_{10}$(f / 2.5GHz)) dB

High Speed Side Serial Receiver Characteristics *(continued)*

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(LATENCY)}$	Receive path latency	10GBASE-KR mode		see Figure 3-5		
		1GBASE-KX mode		see Figure 4-2		
		General Purpose mode		see Figure 5-4		

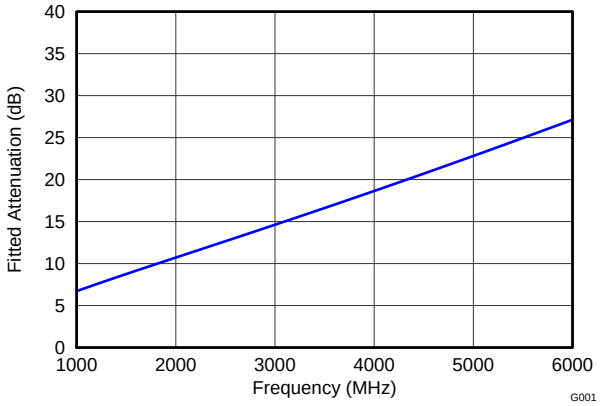


Figure 9-3. 10GBASE-KR Fitted Channel Attenuation Limit

9.5 Low Speed Side Serial Transmitter Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{OD(pp)}$	Transmitter output differential peak-to-peak voltage swing	SWING = 000	110	190	280	mVpp
		SWING = 001	280	380	490	
		SWING = 010	420	560	700	
		SWING = 011	560	710	870	
		SWING = 100	690	850	1020	
		SWING = 101	760	950	1150	
		SWING = 110	800	1010	1230	
		SWING = 111	830	1050	1270	
DE	Transmitter output de-emphasis voltage swing reduction	DE = 0000		0		dB
		DE = 0001		0.42		
		DE = 0010		0.87		
		DE = 0011		1.34		
		DE = 0100		1.83		
		DE = 0101		2.36		
		DE = 0110		2.92		
		DE = 0111		3.52		
		DE = 1000		4.16		
		DE = 1001		4.86		
		DE = 1010		5.61		
		DE = 1011		6.44		
		DE = 1100		7.35		
		DE = 1101		8.38		
		DE = 1110		9.54		
		DE = 1111		10.87		
V_{CMT}	Transmitter output common mode voltage	100-Ω differential termination. DC-coupled.		V_{DDT} - 0.5 * $V_{OD(p-p)}$		mV
t_{skew}	Intra-pair output skew				0.045	UI

Low Speed Side Serial Transmitter Characteristics *(continued)*

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_R, t_F	Differential output signal rise, fall time (20% to 80%) Differential Load = 100Ω		30			ps
J_T	Serial output total jitter				0.35	UI
J_D	Serial output deterministic jitter				0.17	UI
t_{skew}	Lane-to-lane output skew				50	ps

9.6 Low Speed Side Serial Receiver Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{ID}	Receiver input differential voltage, |INP – INN|	Full Rate, AC Coupled	50		600	mV
		Half/Quarter Rate, AC Coupled	50		800	
$V_{ID(pp)}$	Receiver input differential peak-to-peak voltage swing 2×|INP – INN|	Full Rate, AC Coupled	100		1200	mV_{dfpp}
		Half/Quarter Rate, AC Coupled	100		1600	
C_I	Receiver input capacitance				2	pF
J_{TOL}	Jitter tolerance, total jitter at serial input (DJ + RJ) (BER 10^{-15})	Zero crossing, Half/Quarter Rate			0.66	UI_{p-p}
		Zero crossing, Full Rate			0.65	
J_{DR}	Serial input deterministic jitter (BER 10^{-15})	Zero crossing, Half/Quarter Rate			0.50	UI_{p-p}
		Zero crossing, Full Rate			0.35	
t_{skew}	Intra-pair input skew				0.23	UI
$t_{lane-skew}$	Lane-to-lane input skew				30	UI

9.7 Reference Clock Characteristics (REFCLK0P/N, REFCLK1P/N)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F	Frequency		122.88		425	MHz
FHS_{offset}	Accuracy	Relative to Nominal HS Serial Data Rate	–100		100	ppm
		Relative to Incoming HS Serial Data Rate	–200		200	
DC	Duty cycle	High Time	45%	50%	55%	
V_{ID}	Differential input voltage		250		2000	mV_{pp}
C_{IN}	Input capacitance				1	pF
R_{IN}	Differential input impedance			100		Ω
T_{RISE}	Rise/fall time	10% to 90%	50		350	ps

9.8 Differential Output Clock Characteristics (CLKOUTA/BP/N)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OD}	Differential output voltage	Peak to peak	1000		2000	mV_{dfpp}
T_{RISE}	Output rise time	10% to 90%, 2pF lumped capacitive load, AC-Coupled			350	ps
R_{TERM}	Output termination	CLKOUT×P/N to DVDD		50		Ω
F	Output frequency		0		500	MHz

9.9 LVCMOS Electrical Characteristics (VDDO):

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2 mA, Driver Enabled (1.8V)	VDDO – 0.45		VDDO	V
		I_{OH} = 2 mA, Driver Enabled (1.5V)	0.75 × VDDO		VDDO	

LVCMOS Electrical Characteristics (VDDO): *(continued)*

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = –2 mA, Driver Enabled (1.8V)	0		0.45	V
		I_{OL} = –2 mA, Driver Enabled (1.5V)	0		0.25 × VDDO	
V_{IH}	High-level input voltage		0.65 × VDDO		VDDO + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.35 × VDDO	V
I_{IH}, I_{IL}	Receiver only	Low/High Input Current			±170	µA
I_{OZ}	Driver only	Driver Disabled			±25	µA
	Driver/Receiver With Pullup/Pulldown	Driver disabled With Pull Up/Down Enabled			±195	
CIN	Input capacitance				3	pF

9.10 MDIO Timing Requirements

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{period}	MDC period	See Figure 9-4	100			ns
t_{setup}	MDIO setup to ↑ MDC		10			ns
t_{hold}	MDIO hold to ↑ MDC		10			ns
T_{valid}	MDIO valid from MDC ↑		0		40	ns

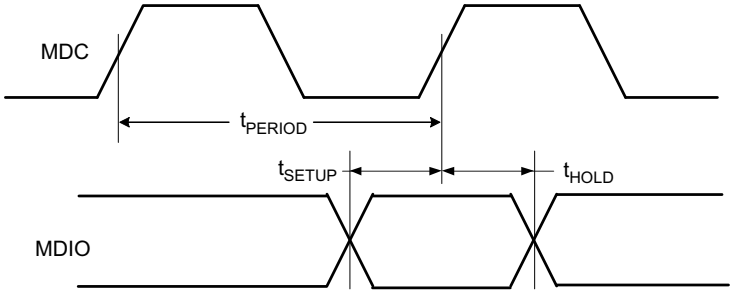


Figure 9-4. MDIO Read/Write Timing

9.11 JTAG Timing Requirements

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T_{PERIOD}	TCK period	See Figure 9-5	66.67			ns
T_{SETUP}	TDI/TMS/TRST_N setup to ↑ TCK		3			
T_{HOLD}	TDI/TMS/TRST_N hold from ↑ TCK		5			
T_{VALID}	TDO delay from TCK Falling		0		10	ns

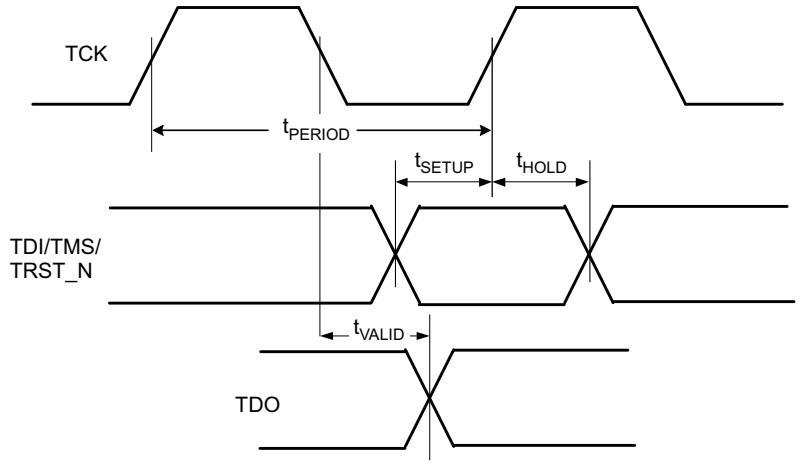


Figure 9-5. JTAG Timing

9.12 Power Sequencing Guidelines

The TLK10232 allows either the core or I/O power supply to be powered up for an indefinite period of time while the other supply is not powered up, if all of the following conditions are met:

1. All maximum ratings and recommending operating conditions are followed
2. Bus contention while 1.5/1.8V power is applied (>0V) must be limited to 100 hours over the projected lifetime of the device.
3. Junction temperature is less than 105°C during device operation. Note: Voltage stress up to the absolute maximum voltage values for up to 100 hours of lifetime operation at a TJ of 105°C or lower will minimally impact reliability.

The TLK10232 LVCMOS I/O are not failsafe (i.e. cannot be driven with the I/O power disabled). TLK10232 inputs should not be driven high until their associated power supply is active.

10 MECHANICAL AND THERMAL DATA

10.1 Package Thermal Dissipation Ratings

Table 10-1 details the thermal characteristics of the TLK10232 package.

Table 10-1. Package Thermal Characteristics

JEDEC STANDARD BOARD		
PARAMETER		**VALUE**
Θ_{JA}	Theta-JA	25.5
Ψ_{JT}	Psi-JT	1.8
Ψ_{JB}	Psi-JB	13.7
CUSTOM TYPICAL APPLICATION BOARD (1)		
Θ_{JA}	Theta-JA	24.5
Ψ_{JT}	Psi-JT	0.9
Ψ_{JB}	Psi-JB	11

(1) Custom Typical Application Board Characteristics:
- 10x15 inches
- 12 layer
  - 8 power/ground layers – 95% copper (1oz)
  - 4 signal layers – 20% copper (1oz)

$\Psi_{JB} = (T_J - T_B)/(\text{Total Device Power Dissipation})$
T_J = Device Junction Temperature
T_B = Temperature of PCB 1 mm from device edge.

$\Psi_{JT} = (T_J - T_C)/(\text{Total Device Power Dissipation})$
T_J = Device Junction Temperature
T_C = Hottest temperature on the case of the package.

Table 10-2. ORDERING INFORMATION

Generic Part Number	Orderable Part Number
TLK10232	TLK10232CTR

11 APPENDIX A: PROVISIONABLE XAUI CLOCK TOLERANCE COMPENSATION

The XAUI interface is defined to allow for separate clock domains on each side of the link. Though the reference clocks for two devices on a XAUI/KR link have the same specified frequencies, there are slight differences that, if not compensated for, will lead to over or under run of the FIFOs on the receive/transmit data paths.

The XAUI CTC block performs the clock domain transition and rate compensation by utilizing a FIFO that is 32 deep and 40-bits wide. The usable FIFO size in the RX and TX directions is dependent upon the RX_FIFO_DEPTH and TX_FIFO_DEPTH MDIO fields, respectively. The word format is illustrated in Figure 11-1.

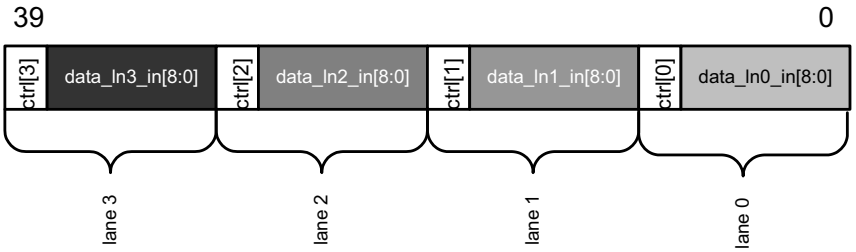


Figure 11-1. XAUI CTC FIFO Word Format

The XAUI CTC performs one of the following operations to compensate the clock rate difference:

1. Delete Idle column from the data stream
2. Delete Sequence column from the data stream (enabled via MDIO)
3. Insert Idle column to the data stream.

The following rules apply for insertion/removal:

- Idle insertion/deletion occurs in groups of 4 idle characters (i.e., in columns)
- Idle characters are added following Idle or Sequence ordered_set
- Idle characters are not added while data is being received
- When deleting Idle characters, minimum IPG of 5 characters is maintained. /T/ characters are counted towards IPG.
- The first Idle column after /T/ is never deleted
- Sequence ordered_sets are deleted only when two consecutive Sequence columns are received. In this case, only one of the two Sequence columns will be deleted.

Insertion: When the FIFO fill level is ***at or below LOW watermark (insertion is triggered)***, the XAUI CTC needs to insert an IDLE column. It does so by skipping a read from the FIFO and inserting IDLE column to the data stream. It continues the insertion until the FIFO fill level is above the mid point. This occurs on the read side of the FIFO.

Removal: When the FIFO fill level is ***at or above HIGH watermark (deletion is triggered),*** the XAUI CTC needs to remove an IDLE column. It does so by skipping a write to the FIFO and discarding the IDLE column or Sequence ordered_set. It continues the deletion until the FIFO fill level is below the mid point. This occurs on the write side of the FIFO.

On the write side of the XAUI CTC FIFO a 40-bit write is performed at every cycle of the 312.5 MHz clock except during removal when it discards the IDLE or sequence ordered_set. On the read side of the XAUI CTC FIFO a 40-bit read is performed at every cycle of the 312.5 MHz clock except during insertion when it generates IDLE columns to the output while not reading the FIFO at all.

In IEEE 802.3-2008 the XAUI clock rate tolerance is given as 3.125 GHz ± 100 ppm, the XGMII clock rate tolerance is given as 156.25 MHz ± 0.02% (which is equivalent to 200ppm), and the Jumbo packet size is 9600 bytes which is equivalent to 2400 cycles of 312.5 MHz clock. The average inter-frame gap is 12 bytes (3 columns), which implies that there is one opportunity to insert/delete a column in between every packet on average. This gives one column deletion/insertion in every 2400 columns which results in a 400 ppm tolerance capability. If the IPG increases, then more clock rate variance or larger packet size can be supported. Note that the maximum frequency tolerance is limited by the frequency accuracy requirement of the reference clock.

The number of words in the FIFO (fifo_depth[2:0]) and the HIGH/LOW watermark levels (wmk_sel[1:0]) are set through MDIO register 01.8001, and determine the allowable difference between the write clock and the read clock as well as the maximum packet size that can be processed without FIFO collision. At these watermarks the drop and insert start respectively and must happen before it hits overflow/underflow condition. Although the FIFO is supposed to never overflow/underflow given the average IPG, if it ever happens the overflow/underflow indications signal the error to the MDIO interface and the FIFO is reset. Note that the overflow/underflow status indications are latched high and cleared when read.

Table 11-1 shows XAUI CTC FIFO configuration and capabilities:

Table 11-1. XAUI CTC FIFO Configurations

fifo_depth[2:0]	FIFO Depth	wmk_sel[1:0]	LOW Watermark	HIGH Watermark	Max Latency (Cycles)	Nom Latency (Cycles)	Min Latency (Cycles)	Max pkt size (400ppm)	Max pkt size (200ppm)	Max pkt size (100ppm)	Max pkt size (50ppm)	Min #of removable columns in IPG to support the max pkt size	
1xx	32	11	15	18	28	16	4	100KB	200KB	400KB	800KB	10	default
		10	13	20	28	16	4	80KB	160KB	320KB	640KB	8	
		01	10	23	28	16	4	50KB	100KB	200KB	400KB	5	
		00	6	27	28	16	4	10KB	20KB	40KB	80KB	1	
011	24	11	11	14	20	12	4	60KB	120KB	240KB	480KB	6	
		10	9	16	20	12	4	40KB	80KB	160KB	320KB	4	
		0x	6	19	20	12	4	10KB	20KB	40KB	80KB	1	
010	16	1x	7	10	13	8	3	30KB	60KB	120KB	240KB	3	
		0x	5	12	13	8	3	10KB	20KB	40KB	80KB	1	
001	12	xx	5	8	9	6	3	10KB	20KB	40KB	80KB	1	
000	8	Plain FIFO, No CTC			7	4	1	No limit on pkt size (needs 0 ppm to work)					

Note: To support the max packet sizes as shown in Table 11-1, it is assumed that there are enough IDLE columns in IPG for deletion. Below is one example:

Configure the FIFO to be 32-deep (fifo_depth[2:0] = 3'b1xx) and set the LOW/HIGH Watermarks to 10/23 (wmk_sel[1:0] = 2'b01). If the write clock is faster than the read clock by 200ppm, to support the max packet size of 100KB, a minimum of 5 removable columns in IPG is required (either IDLE columns or Sequence ordered_sets). If there are only 4 removable columns in IPG, the max packet size supported is dropped to 80KB. If there are only 3 removable columns in IPG, the max packet size supported is dropped to 60KB, and so on. As a rule of thumb, one removable column in IPG corresponds to 10KB at 400ppm, 20KB at 200ppm, 40KB at 100ppm, and 80KB at 50ppm

The following figures illustrate XAUI CTC FIFO configuration and capabilities. The green region (the middle of the FIFO fill level) indicates that the FIFO is operating stably without insertion or deletion. The more green bars in the figure, the more clock wander it can tolerate. The more yellow bars in the figure, the bigger packet size it can support.

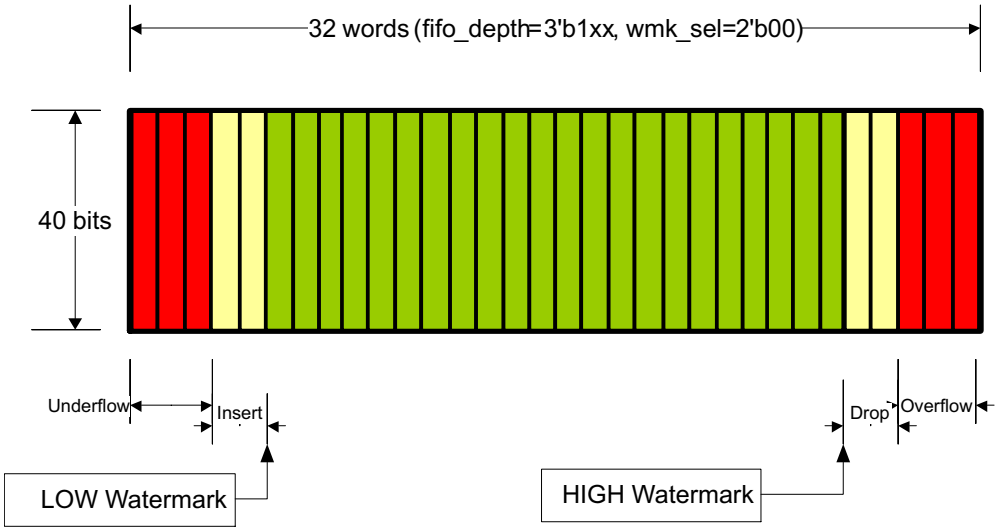


Figure 11-2. Organization of the XAUI CTC FIFO (32-Deep, Low Watermark)

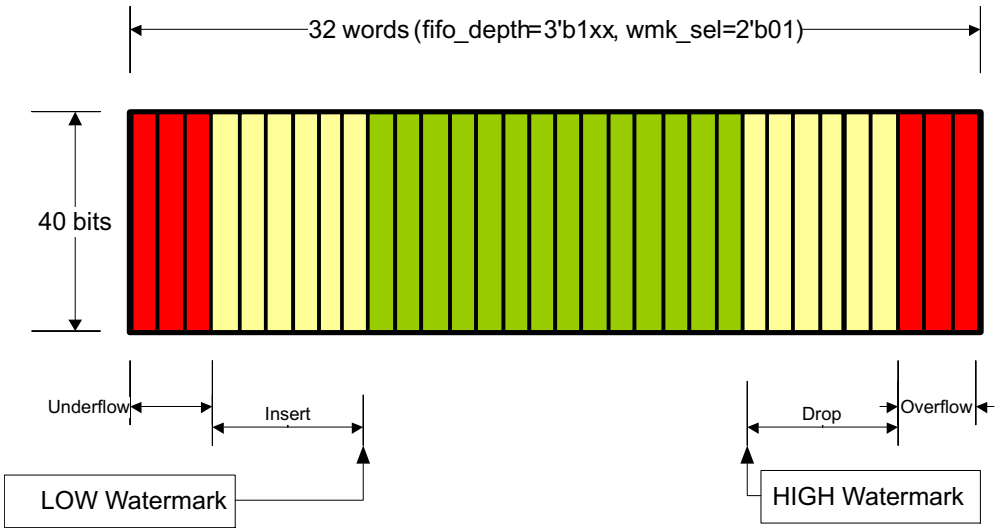


Figure 11-3. Organization of the XAUI CTC FIFO (32-Deep, Mid Watermark)

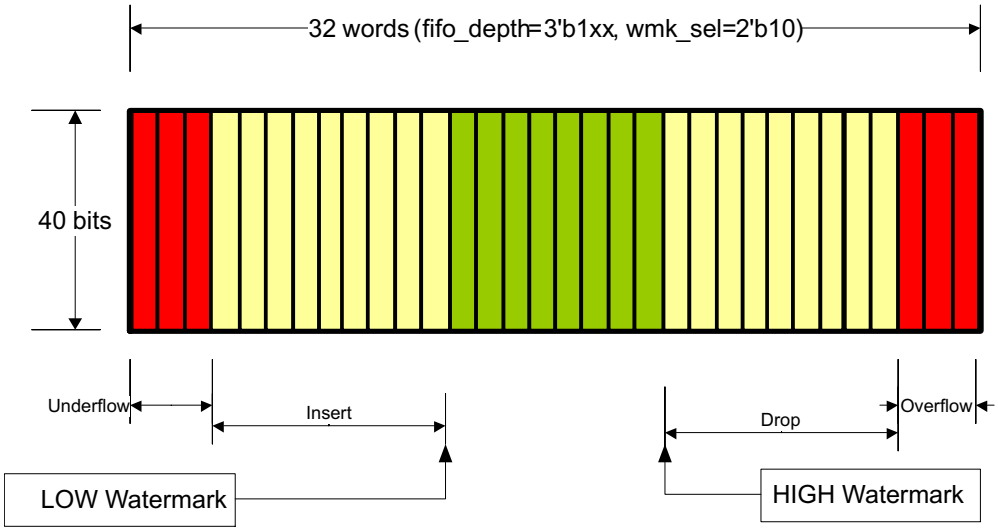


Figure 11-4. Organization of the XAUI CTC FIFO (32-Deep, Mid-High Watermark)

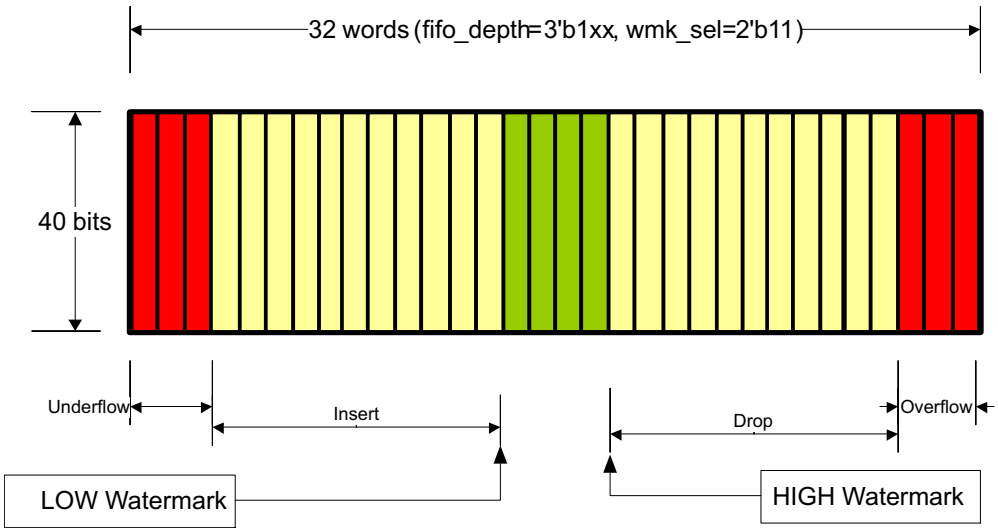


Figure 11-5. Organization of the XAUI CTC FIFO (32-Deep, High Watermark)

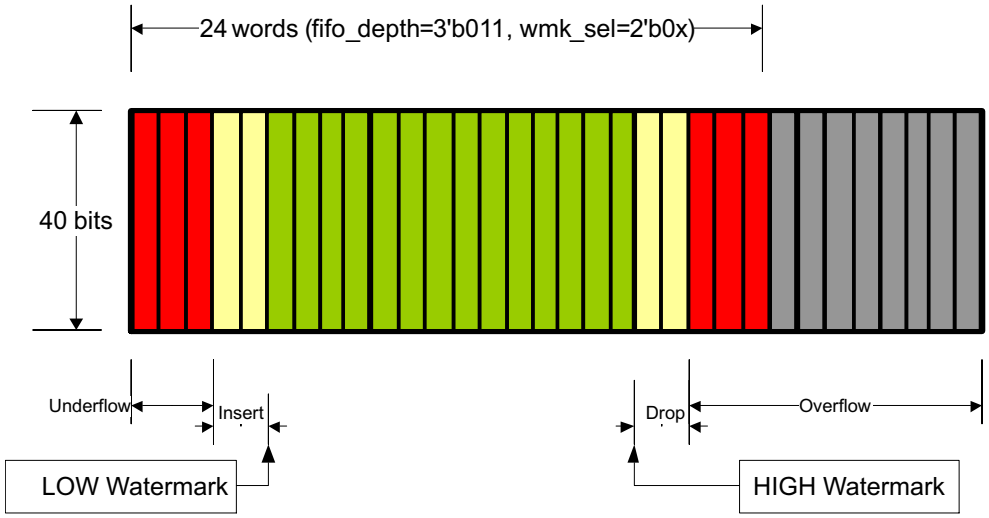


Figure 11-6. Organization of the XAUI CTC FIFO (24-Deep, Low Watermark)

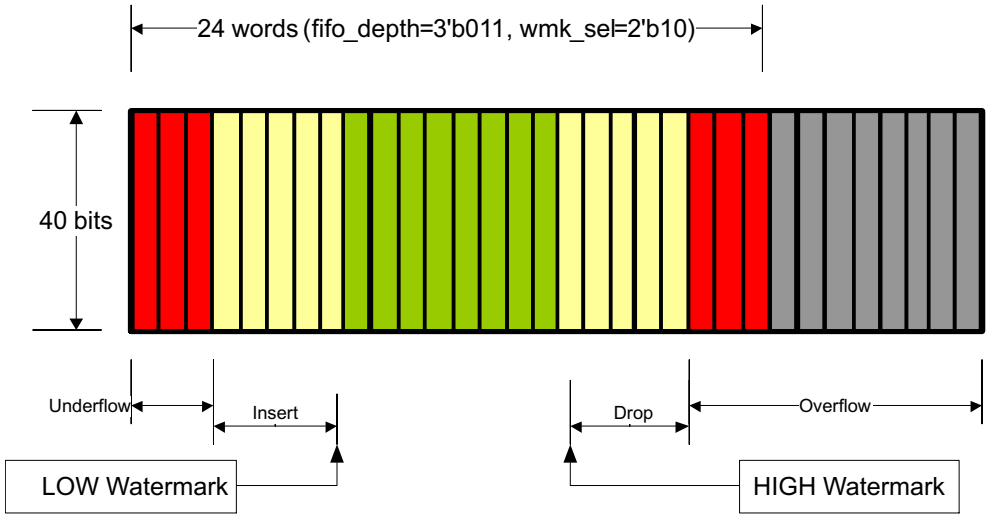


Figure 11-7. Organization of the XAUI CTC FIFO (24-Deep, Mid Watermark)

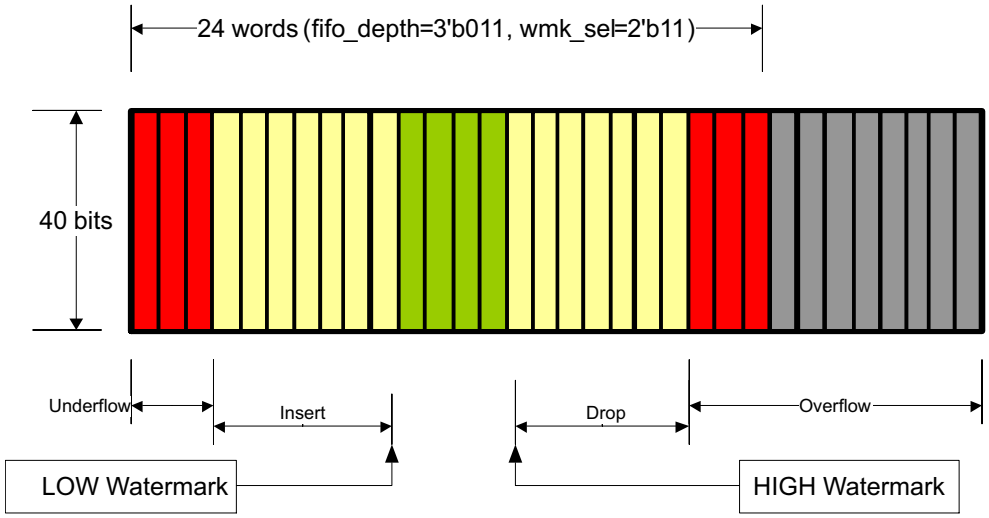


Figure 11-8. Organization of the XAUI CTC FIFO (24-Deep, High Watermark)

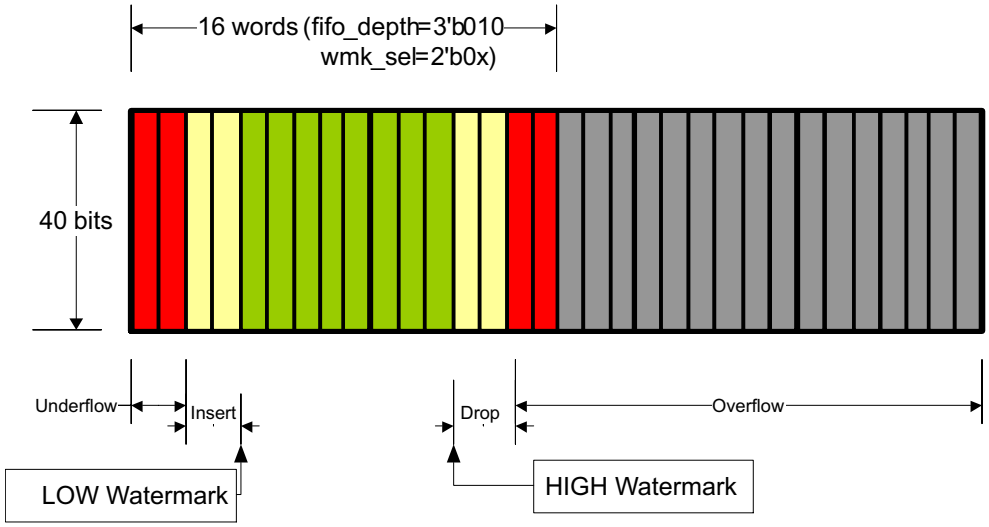


Figure 11-9. Organization of the XAUI CTC FIFO (16-Deep, Low Watermark)

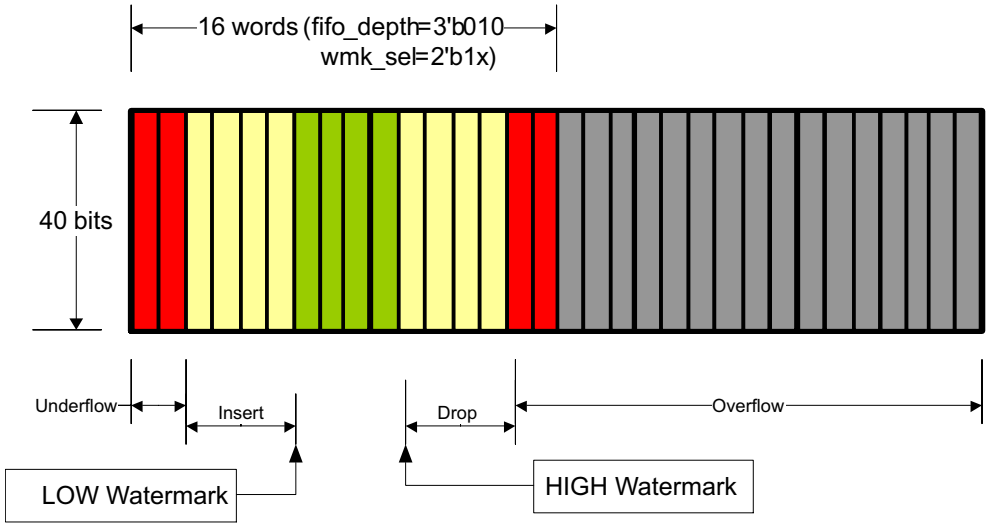


Figure 11-10. Organization of the XAUI CTC FIFO (16-Deep, High Watermark)

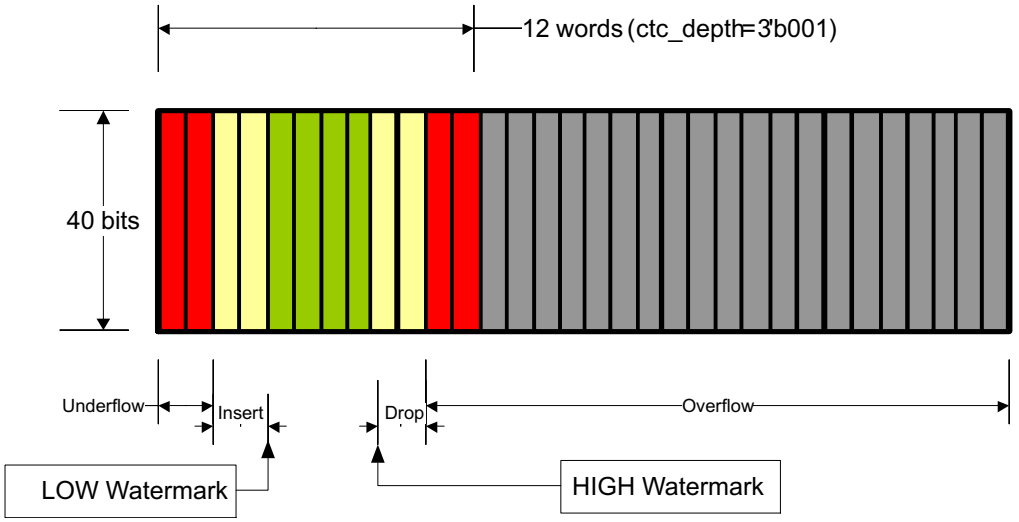


Figure 11-11. Organization of the XAUI CTC FIFO (12-Deep)

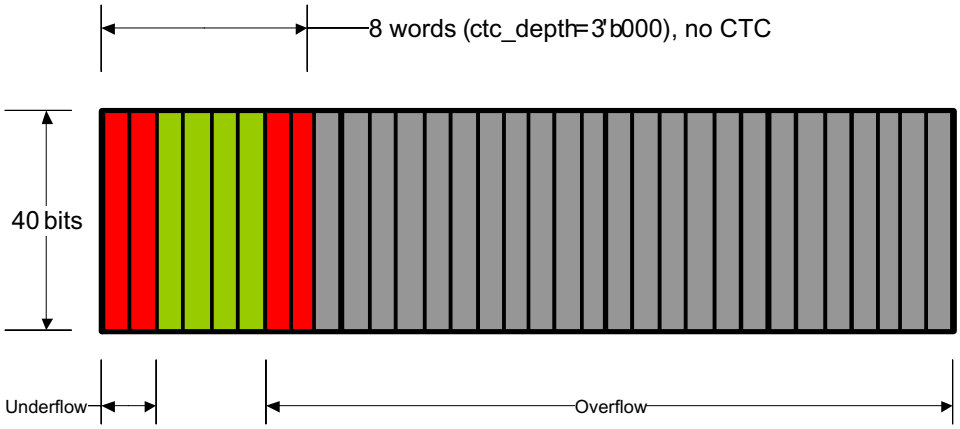


Figure 11-12. Organization of the XAUI CTC FIFO (8-Deep)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK10232CTR	ACTIVE	FCBGA	CTR	144	119	RoHS & Green	SNAGCU	Level-4-260C-72 HR	-40 to 85	TLK10232	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

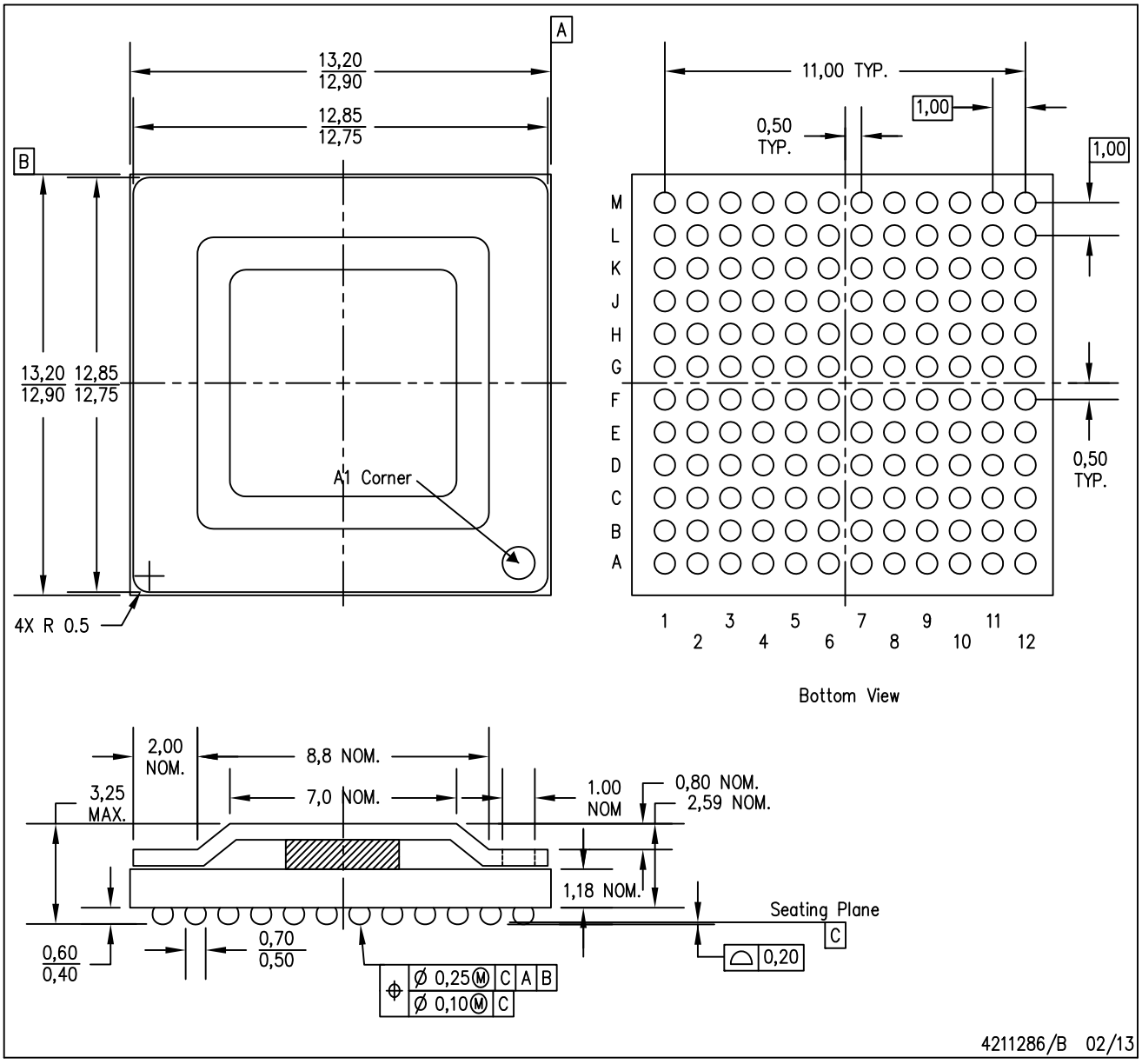
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

CTR (S–PBGA–N144) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

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