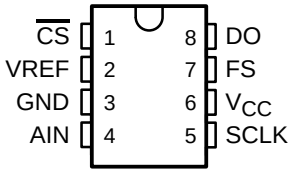
- **Fast Throughput Rate: 1.25 MSPS**
- **8-Pin SOIC Package**
- **Differential Nonlinearity Error: < ±1 LSB**
- **Integral Nonlinearity Error: < ±1 LSB**
- **Signal-to-Noise and Distortion Ratio: 59 dB, $f_{(input)}$ = 500 kHz**
- **Single 3-V to 5-V Supply Operation**
- **Very Low Power: 8 mW at 3V; 25mW at 5 V**
- **Auto-Powerdown: 10 μA Maximum**
- **Glueless Serial Interface to TMS320 DSPs and (Q)SPI Compatible Micro-Controllers**
- **Inherent Internal Sample and Hold Operation**

D PACKAGE
(TOP VIEW)



Applications

- **Mass Storage and HDD**
- **Automotive**
- **Digital Servos**
- **Process Control**
- **General Purpose DSP**
- **Contact Image Sensor Processing**

description

The TLV1572 is a high-speed 10-bit successive-approximation analog-to-digital converter (ADC) that operates from a single 2.7-V to 5.5-V power supply and is housed in a small 8-pin SOIC package.

The TLV1572 accepts an analog input range from 0 to V_{CC} and digitizes the input at a maximum 1.25 MSPS throughput rate. The power dissipation is only 8 mW with a 3-V supply or 25 mW with a 5-V supply. The device features an auto-powerdown mode that automatically powers down to 10 μA whenever a conversion is not performed.

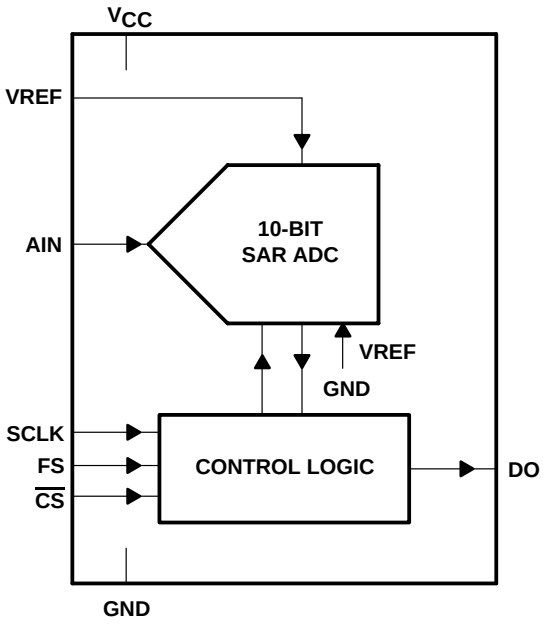
The TLV1572 communicates with digital microprocessors via a simple 3- or 4-wire serial port that interfaces directly to the Texas Instruments TMS320 DSPs and (Q)SPI compatible microcontrollers without using additional glue logic.

Very high throughput rate, simple serial interface, SO-8 package, 3-V operation, and low power consumption make the TLV1572 an ideal choice for compact or remote high-speed systems.

AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (D)
0°C to 70°C	TLV1572CD
–40°C to 85°C	TLV1572ID

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AIN	4	I	Analog input
$\overline{CS}$/Powerdown	1	I	Chip Select. A low on this input enables the TLV1572. A high disables the device and disconnects the power to the TLV1572.
DO	8	O	Serial data output. A/D conversion results are provided at this output pin.
FS	7	I	Frame sync input in DSP mode. The falling edge of the frame sync pulse from DSP indicates the start of a serial data frame shifted out of the TLV1572. The FS input is tied to V_{CC} when interfacing to a micro-controller.
GND	3		Ground
SCLK	5	I	Serial clock input. This clock synchronizes the serial data transfer and is also used for internal data conversion.
V_{CC}	6		Power supply, recommend connection to analog supply
V_{REF}	2	I	Reference voltage input. The voltage applied to this pin defines the input span of the TLV1572.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, GND to V_{CC} . . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . . –0.3 V to V_{CC} + 0.3 V
Reference input voltage . . . . . V_{CC} + 0.3 V
Digital input voltage range . . . . . –0.3 V to V_{CC} + 0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supply

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7		5.5	V

analog inputs

		MIN	MAX	UNIT
V_{AIN}	Analog input voltage	GND	V_{REF}	V
V_{REF}	Reference input voltage	2.7	V_{CC}	V

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	V_{CC} = 3 V to 5.5 V	2.1	2.4		V
Low-level input voltage, V_{IL}	V_{CC} = 3 V to 5.5 V			0.8	V
Input SCLK frequency	V_{CC} = 4.5 V to 5.5 V			20	MHZ
SCLK pulse duration, clock high, $t_{w(SCLKH)}$	V_{CC} = 4.5 V to 5.5 V	23			ns
SCLK pulse duration, clock low, $t_{w(SCLKL)}$	V_{CC} = 4.5 V to 5.5 V	23			ns
Input SCLK frequency	V_{CC} = 3 V			10	MHZ
SCLK pulse duration, clock high, $t_{w(SCLKH)}$	V_{CC} = 3 V	45			ns
SCLK pulse duration, clock low, $t_{w(SCLKL)}$	V_{CC} = 3 V	45			ns

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, V_{REF} = 5 V, f_{SCLK} = 20 MHz (unless otherwise noted)

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic inputs						
I_{IH}	High-level input current	V_{CC} = 5 V	–50		50	μA
I_{IL}	Low-level input current	V_{CC} = 5 V	–50		50	μA
C_i	input capacitance			5		pF
Logic outputs						
V_{OH}	High-level output voltage	I_{OH} = 50 μA – 0.5 mA	V_{CC}–0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 50 μA – 0.5 mA		0.4		V
I_{OZ}	High-impedance-state output current		–50		50	μA
C_O	Output capacitance			5		pF

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10		Bits
Accuracy						
INL	Integral nonlinearity	Best fit		±0.5	±1	LSB
DNL	Differential nonlinearity			±0.3	±1	LSB
	Offset error			±0.1	±0.15	%FSR
	Gain error			±0.1	±0.2	%FSR
Analog input						
	Input full scale range		GND		V_{CC}	V
	Input capacitance			15		pF
	input leakage current	V_{AIN} = 0 to V_{CC}			50	μA
Voltage reference input						
V_{REF+}	Positive reference voltage		3		V_{CC}	V
$V_{REF–}$	Negative reference voltage	Internally connects to GND		GND		V
	Input resistance		2			KΩ
	Input capacitance			300		pF
Power supply						
I_{CC} + I_{REF}	Operating supply current	V_{CC} = 5.5 V, f_{SCLK} = 20 MHz		5.5	8.5	mA
		V_{CC} = 3 V, f_{SCLK} = 10 MHz		2.7		
I_{PD}	Supply current in powerdown mode	V_{CC}			10	μA
	Power dissipation	V_{CC} = 5 V		25		mW
	Power dissipation	V_{CC} = 3 V		8		mW

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, V_{REF} = 5 V, f_{SCLK} = 20 MHz (unless otherwise noted) (continued)

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Signal-to-noise ratio + distortion	$f_{(input)}$ = 200 kHz	54	58		dB
THD	Total harmonic distortion	$f_{(input)}$ = 200 kHz	56	60		dB
	Effective number of bits	$f_{(input)}$ = 200 kHz	8.7	9.35		Bits
	Spurious-free dynamic range	$f_{(input)}$ = 200 kHz	57	62		dB
Analog Input						
BW	Full-power bandwidth	Source impedance = 1 kΩ		12		MHz
BW	Small-signal bandwidth	Source impedance = 1 kΩ		20		Mhz

timing specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	SCLK period	V_{CC} = 4.5 V – 5.5 V	50			ns
t_c	SCLK period	V_{CC} = 2.7 V – 3.3 V	100			ns
t_{rs}	Reset and sampling period			6		SLCK cycles
t_c	Conversion period			10		SLCK cycles
t_{su1}	FS setup time to SCLK falling edge in DSP mode		10			ns
t_{h1}	FS hold time to SCLK falling edge in DSP mode		4			ns
t_{su2}	FS setup time to $\overline{CS}$ falling edge in DSP mode		6			ns
t_{h2}	FS hold time to $\overline{CS}$ falling edge in DSP mode		9			ns
t_{d1}	Output delay after SCLK rising edge in DSP mode			15	25	ns
$t_{d(L)1}$	FS falling edge to next SCLK falling edge in DSP mode		6			ns
$t_{d(L)2}$	SCLK rising edge after $\overline{CS}$ falling edge in µC mode		4			ns
t_{d2}	Output delay after SCLK rising edge in µC mode			15	25	ns

Specifications subject to change without notice.

PARAMETER MEASUREMENT INFORMATION

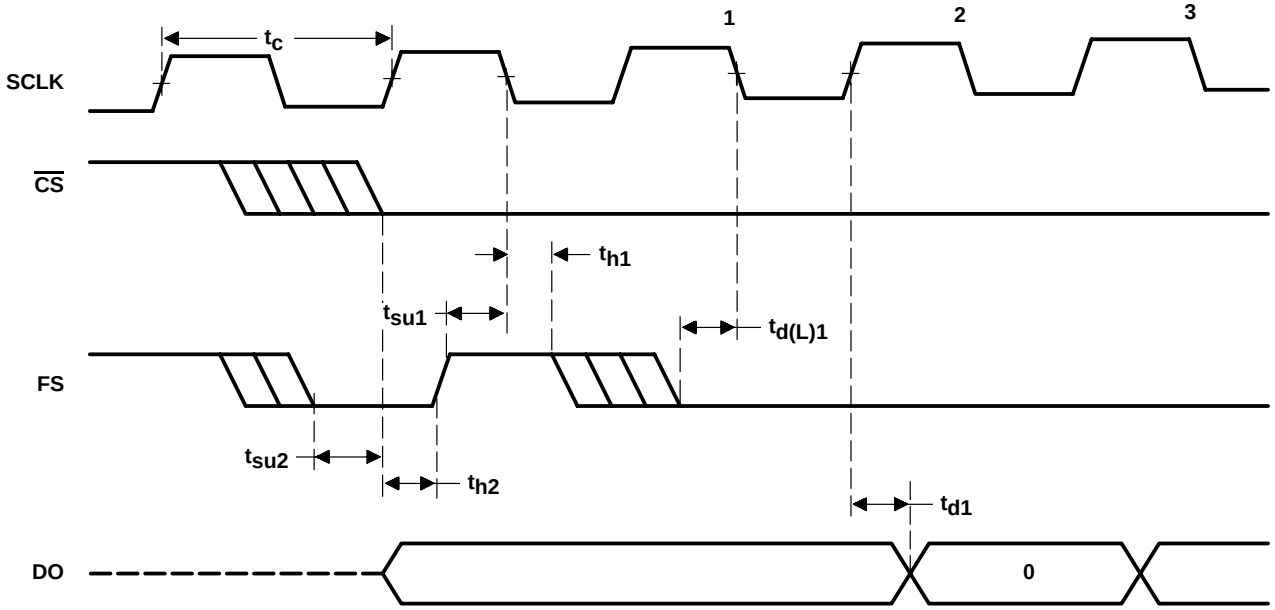


Figure 1. DSP Mode Timing Diagram

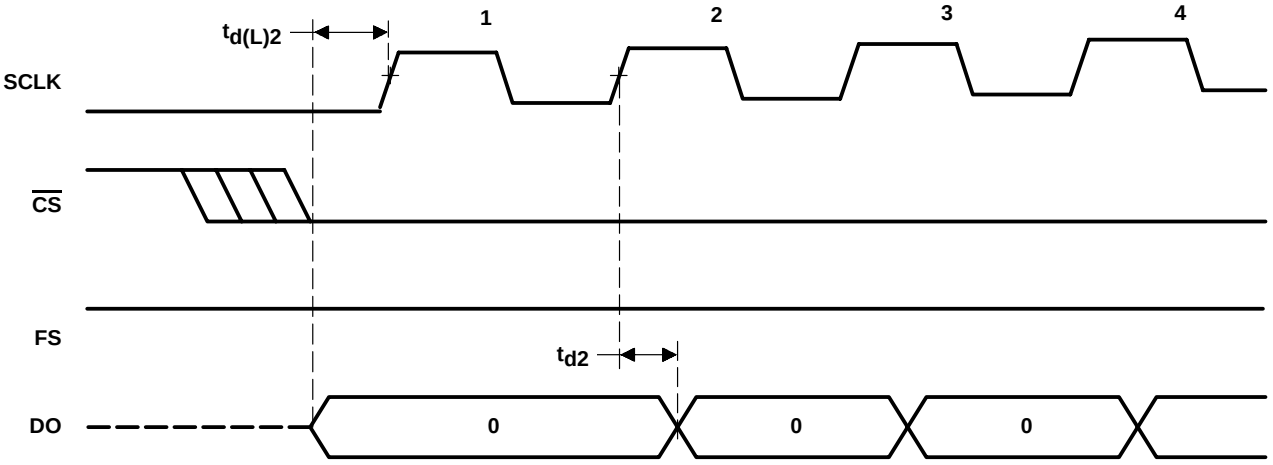


Figure 2. μC Mode Timing Diagram

definitions of specifications and terminology

integral nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

differential nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

zero offset

The first code transition ideally occurs at an analog value 1/2 LSB above $V_{REF}-$. The zero offset error is defined as the error between the ideal first transition point and the actual first transition. This error effectively shifts left or right an ADC transfer function

gain error

The first code transition occurs at an analog value 1/2 LSB above negative full scale. The last transition occurs at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

signal-to-noise ratio + distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD – 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the largest peak spurious signal.

APPLICATION INFORMATION

The TLV1572 is a 600-ns, 10-bit analog-to-digital converter with the throughput up to 1.25 MSPS at 5 V and up to 625 KSPS at 3 V respectively. To run at its fastest conversion rate, it must be clocked at 20 MHz at 5 V or 10 MHz at 3 V. The TLV1572 can be easily interfaced to microcontrollers, ASICs, DSPs, or shift registers. Its serial interface is designed to be fully compatible with Serial Peripheral Interface (SPI) and TMS320 DSP serial ports. It requires no hardware to interface between the TLV1572 and the microcontrollers (μCs) with the SPI serial port or the TMS320 DSPs. However, speed is limited by the SCLK rate of the μC or the DSP.

The TLV1572 interfaces to the DSPs over four lines: $\overline{CS}$, SCLK, DO, and FS, and interfaces to μCs over three lines: $\overline{CS}$, SCLK, and DO. The FS input must be pulled high in μC mode. The chip is in 3-state and powerdown mode when $\overline{CS}$ is high. After $\overline{CS}$ falls, the TLV1572 checks the FS input at the $\overline{CS}$ falling edge to determine the operation mode. If FS is low, DSP mode is set, else μC mode is set.

interfacing TLV1572 to TMS320 DSPs

The TLV1572 is compatible with Texas Instruments TMS320 DSP serial ports. Figures 3(a) and 3(b) show the pin connections to interface the TLV1572 to the TMS320 DSPs**.**

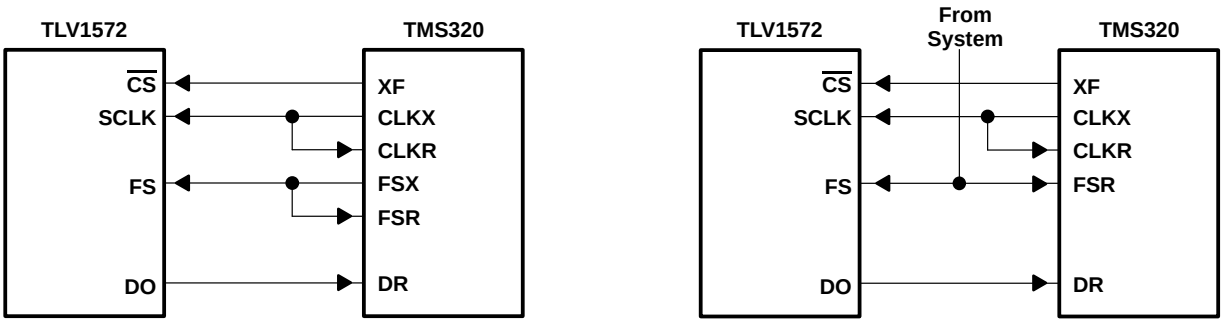


Figure 3. TLV1570 to DSP Interface

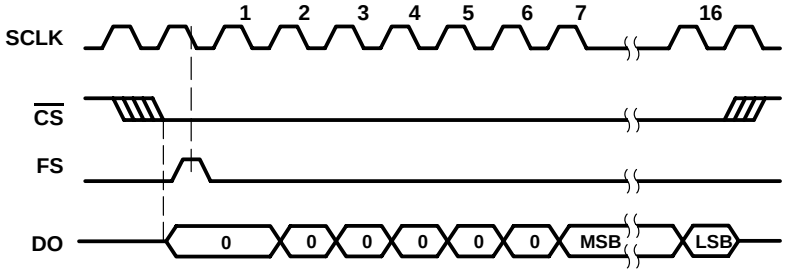


Figure 4. Typical Timing Diagram for DSP Application

In the DSP mode, the FS input must be low when the $\overline{CS}$ goes low. There is a hold time before the FS input can go high after the $\overline{CS}$ falling edge to ensure proper mode latching. With $\overline{CS}$ going low, DO comes out of 3-state but the device is still in powerdown until FS (frame sync signal from DSP) goes high.

The TLV1572 checks FS at the falling edges of SCLK. Once FS is detected high, the sampling of input is started. As soon as FS goes low, the device starts shifting the data out on the DO line. After six null bits, the A/D conversion data becomes available on the SCLK rising edges and is latched by DSP on the falling edges. Figure 4 shows the DSP mode timing diagram.

APPLICATION INFORMATION

interfacing TLV1572 to TMS320 DSPs (continued)

The TLV1572 goes into auto-powerdown after the LSB is shifted out. The next FS pulls it out of auto-powerdown as shown in Figure 5. If FS comes on the 16th bit, the next conversion cycle starts from the next rising edge of SCLK allowing back to back conversions as shown in Figure 6. An FS high in the middle of a conversion cycle resets the device and starts a new conversion cycle. Therefore variable-bit transfer is supported if FS appears earlier.

$\overline{CS}$ can be pulled high asynchronously to put the device into 3-state and powerdown. $\overline{CS}$ can also be pulled low asynchronously to start checking for FS on the falling edges of the clock.

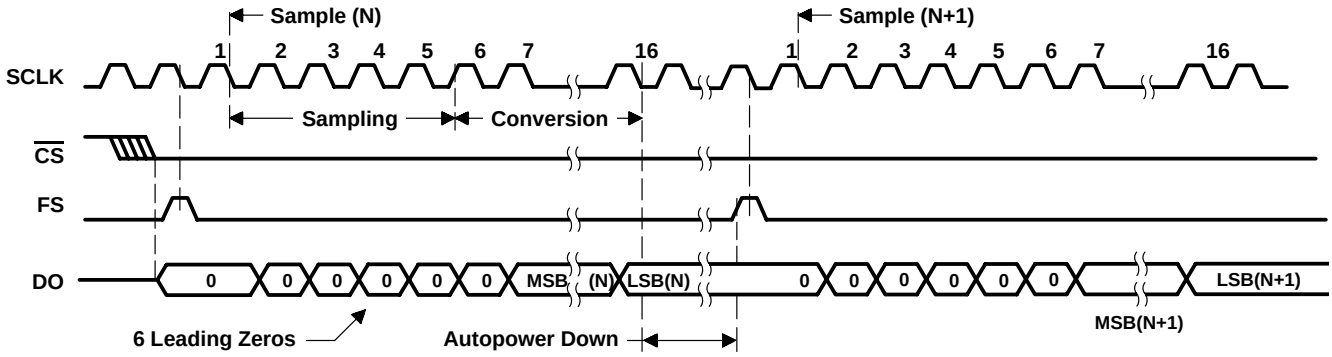


Figure 5. DSP Application Timing (Intermittent Conversion)

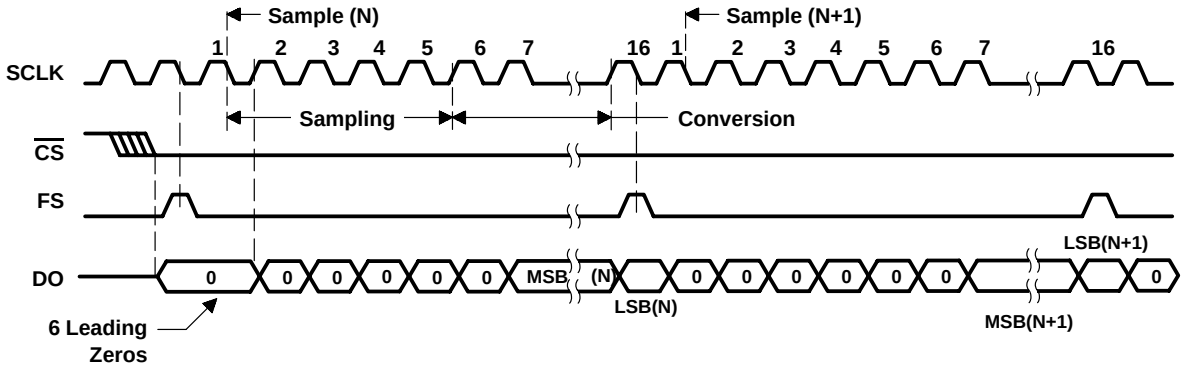


Figure 6. DSP Application Timing (Continuous Conversion)

key points

1. When $\overline{CS}$ goes low, if FS is low, it is in DSP mode. FS is sampled twice by a $\overline{CS}$ falling edge and again by an internally delayed $\overline{CS}$ falling edge. Even if a glitch appears and one latch latches 1 and another latches 0, the device goes into DSP mode (µC mode requires both latches to latch 1). There is a hold time before FS can go high again after the $\overline{CS}$ falling edge to ensure proper mode latching as detailed above. With $\overline{CS}$ going low, DO is in 3-state and the device is in powerdown until a FS rising edge.
2. The TLV1572 checks for FS at every falling edge of SCLK. If FS is detected high, the device goes into reset. When FS goes low, the TLV1572 waits for the DSP to latch the first 0 bit.
3. Sampling occurs from first falling edge of SCLK after FS going low until the rising edge when the 6th 0 bit is sent out. Thereafter decisions are taken on the rising edges and data is sent out on the rising edges (1 bit delayed). The DSP samples on the falling edge of SCLK. Data is padded with 6 leading zeros.

APPLICATION INFORMATION

key points (continued)

4. Note that the device goes into autopower down on the 17th falling edge of SCLK (just after the LSB). The FS rising edge pulls it out of autopower down. If FS comes on the 16th bit, the next conversion cycle starts from the next rising edge allowing back to back conversions. An FS in the middle of a conversion cycle starts a new conversion cycle. Thus variable-bit transfer is supported if FS appears earlier.
5. DO goes into 3-state on the 17th rising edge and comes out on a FS rising edge.
6. $\overline{CS}$ can be pulled high asynchronously to put the device into 3-state and powerdown. $\overline{CS}$ may also be pulled low asynchronously to start checking for FS on the falling edges of the clock.

For applications where the analog input must be sampled at a precise instant in time, data conversion can be initiated by an external conversion start pulse which is completely asynchronous to the SCLK as shown in Figure 4. When a conversion start pulse is received, the pulse is used as a frame sync (FS) signal to initiate the data conversion and transfer. The corresponding timing diagram is shown in Figure 6.

interfacing TLV1572 to SPI/QSPI compatible microcontrollers (μCs)

The TLV1572 is compatible with SPI and QSPI serial interface standards (Note: the TLV1572 supports the following SPI clock options: clock_polarity= 0, i.e. SCLK idles low, and clock_phase = 1). Figure 7 shows the pin connections to interface the TLV1572 to SPI/QSPI compatible microcontrollers.

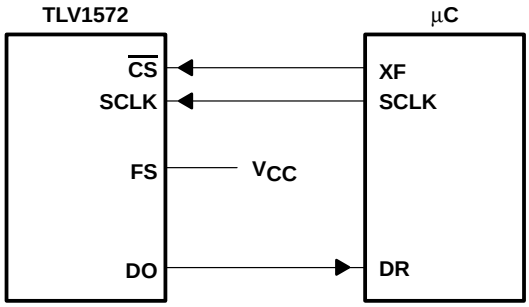


Figure 7. TLV1572 to μC Interface

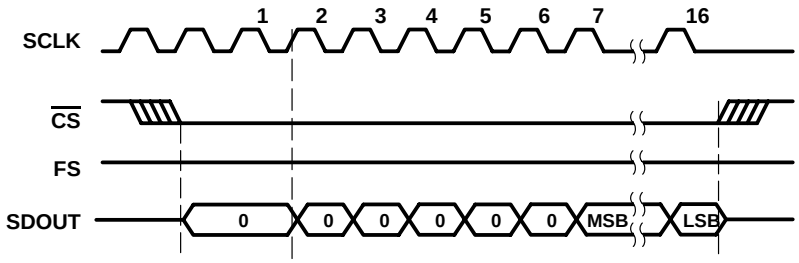


Figure 8. Typical Timing Diagram for μC Application

To use the TLV1572 in a non-DSP application, the FS input must be pulled high as shown in Figure 8.

A total of 16 clocks are normally supplied for each conversion. If the μC cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and next 8 bits with another 8 clocks. $\overline{CS}$ must be kept low throughout the conversion. The delay between these two 8-clock periods must not be longer than 100 μs.

APPLICATION INFORMATION

interfacing TLV1572 to SPI/QSPI compatible microcontrollers(μCs) (continued)

Unlike the DSP mode in which the conversion is initiated by the FS input signal from the DSP, the conversion is initiated by the incoming SCLK after $\overline{CS}$ falls. Sampling of the input is started on the first rising edge of SCLK after $\overline{CS}$ goes low. After six null bits, the A/D conversion data becomes available on SCLK rising edges and is latched by the μC on the falling edges. $\overline{CS}$ can be pulled high during the conversion before the LSB is shifted out to use the device as a lower resolution ADC. Figure 9 shows the μC mode timing diagram.

The device goes into autopower down after the LSB is shifted out and is brought out of powerdown by the next clock rising edge as shown in Figure 9.

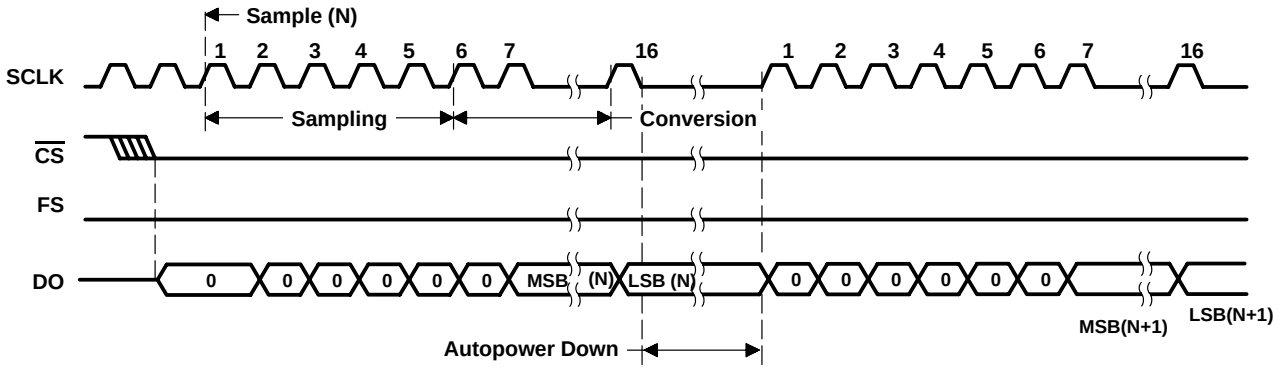


Figure 9. μC Application Timing Diagram

key points

1. When $\overline{CS}$ goes low, if FS is high, it is in μC ({Q}SPI) mode. Thus, FS is tied to V_{DD}. FS is latched twice, on the falling edge of $\overline{CS}$ and again on an internally delayed falling edge of $\overline{CS}$. Only if both latches latch 1, then μC mode is set else DSP mode is set. Only polarity = 0 is supported, i.e. SCLK idles low. Only clock_phase = 1 is supported as shown in the timing diagrams.
2. For each conversion 16 clocks have to be supplied. If the μC cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and the next 8 bits with another 8 clocks keeping $\overline{CS}$ low throughout the conversion. The delay between these two 8-clock periods must not be longer than 100 μs.
3. Sampling starts on the first rising edge of SCLK and ends on the edge when the 6th 0 bit is sent out. Decisions are made on the rising edge and data is output on the same edge but a bit delayed to avoid noise.
4. The device goes into autopower down on the falling edge of the 16th clock and is brought out of powerdown by next first (17th) clock rising edge.
5. If the (Q)SPI wants less than a 16-bit transfer, $\overline{CS}$ must go high after each transfer. The falling edge of $\overline{CS}$ resets the TLV1572 for the next conversion. Thus a 14-bit transfer is possible when using the device as an 8-bit A/D.
6. $\overline{CS}$ going high puts the device in 3-state and complete powerdown. $\overline{CS}$ going low sets the mode and pulls DO out of 3-state.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1572CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	V1572C	Samples
TLV1572CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	V1572C	Samples
TLV1572ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	V1572I	Samples
TLV1572IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	V1572I	Samples
TLV1572IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	V1572I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

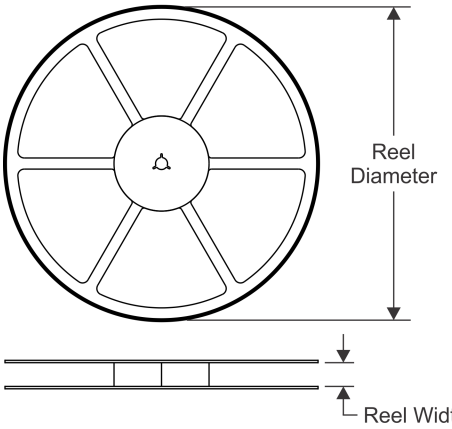
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

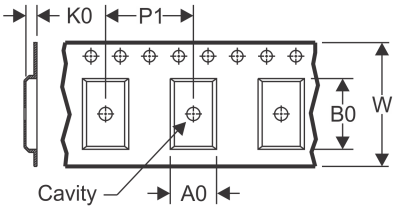
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

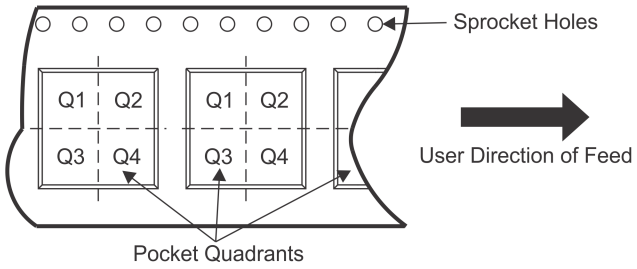


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

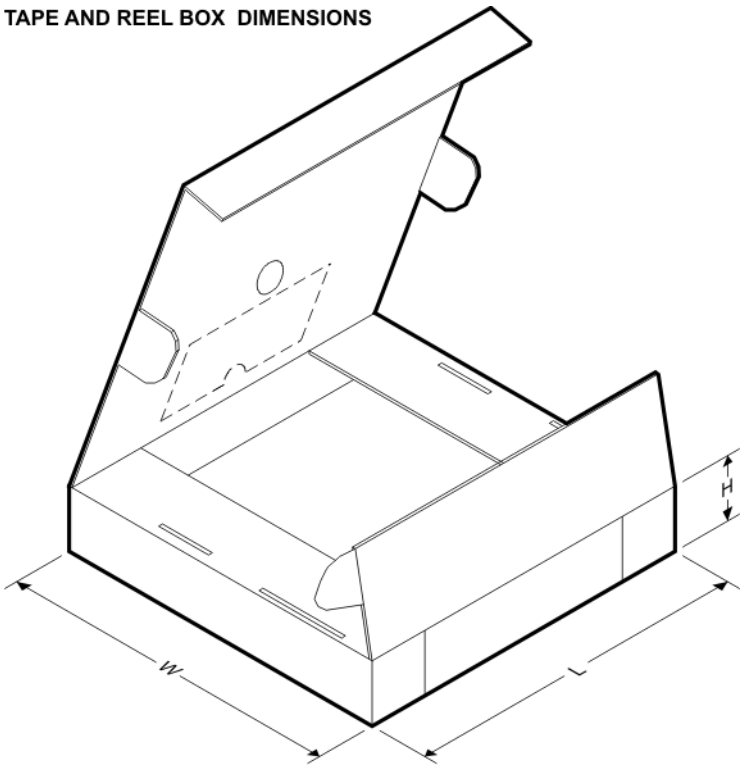
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1572CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1572IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

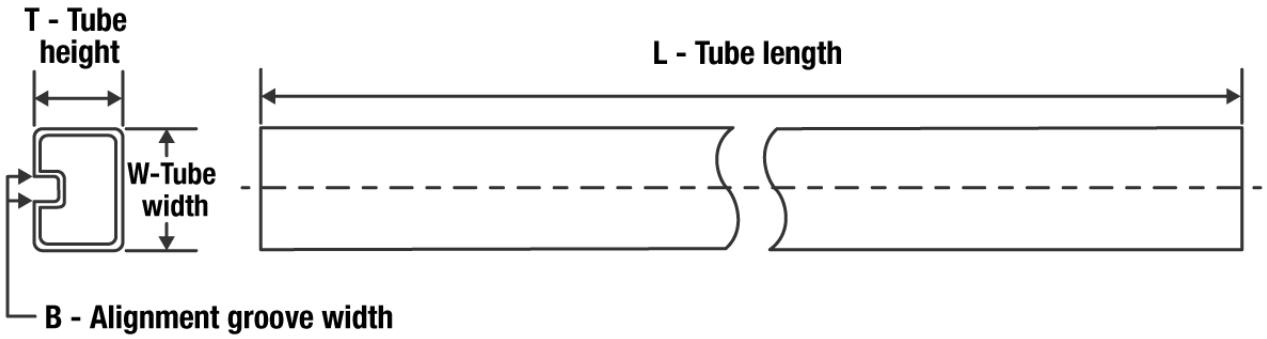
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1572CDR	SOIC	D	8	2500	350.0	350.0	43.0
TLV1572IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV1572CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV1572ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV1572IDG4	D	SOIC	8	75	505.46	6.76	3810	4

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