TEXAS INSTRUMENTS

**TLV705**, **TLV705P**

SBVS151F – DECEMBER 2010 – REVISED APRIL 2017

# TLV705 200-mA, Low $I_Q$, Low-Noise, Low-Dropout Regulator in Ultra-Small, 0.77-mm × 0.77-mm DSBGA and PicoStar™

## 1 Features

- Very Low Dropout:
  - 105 mV at $I_{OUT}$ = 150 mA
  - 145 mV at $I_{OUT}$ = 200 mA
- Accuracy: 0.5% Typical
- Low $I_Q$: 35 μA
- Available in Fixed-Output Voltages From 0.7 V to 4.8 V
- $V_{IN}$ Range: 2 V to 5.5 V
- High PSRR: 70 dB at 1 kHz
- Stable With Effective Capacitance of 0.1 μF
- Thermal Shutdown and Overcurrent Protection
- Available in an Ultra-Low Profile (0.15-mm Maximum Height) PicoStar Package Option

## 2 Applications

- Wireless Handsets
- Smart Phones
- Zigbee® Networks
- Bluetooth® Devices
- Other Li-Ion Operated Handheld Products
- WLAN and Other PC Add-On Cards

## 3 Description

The TLV705 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These devices are designed for power-sensitive applications, with a precision band gap. An error amplifier provides typical accuracy of 0.5%. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of LDOs ideal for a wide selection of battery-operated handheld equipment. All devices have a thermal shutdown and current limit for safety.

Furthermore, the TLV705 series is stable with an effective output capacitance of only 0.1 μF. This feature enables the use of cost-effective capacitors that have higher bias voltage and temperature derating. The devices regulate to the specified accuracy with zero output load. The TLV705P series also provides an active pulldown circuit to quickly discharge output.
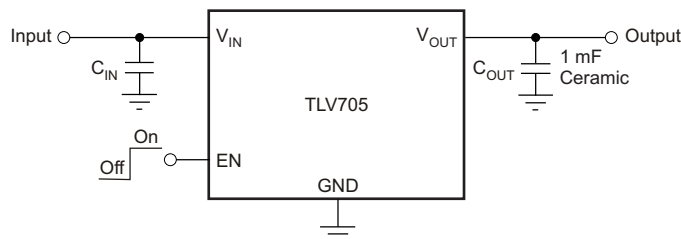
The TLV705 and TLV705P series are both available in 0.77-mm × 0.77-mm DSBGA and PicoStar packages with three height options that are optimal for handheld applications.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV705 | DSGBA (4) | 0.77 mm × 0.77 mm |
| | PicoStar (4) | 0.77 mm × 0.77 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application Circuit (Fixed-Voltage Versions)**



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# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision C (October 2012) to Revision D**                                                              **Page**

**Changes from Revision B (December 2011) to Revision C**                                                             **Page**

**Changes from Revision A (August 2011) to Revision B**                                                               **Page**

# 5 Pin Configuration and Functions

**YFF, YFP Packages**
**4-Pin DSBGA**
**Top View**

```
        EN      V_IN
2        ○       ○

        GND     V_OUT
1    •   ○       ○

        A       B
```
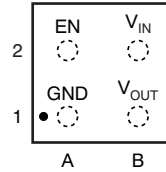
**YFM Package**
**4-Pin PicoStar**
**Top View**

```
        EN      V_IN
2        ○       ○

        GND     V_OUT
1    •   ○       ○

        A       B
```
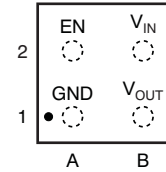
## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | A1 | — | Ground pin. |
| EN | A2 | I | Enable pin.<br>Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V places the regulator into shutdown mode, which reduces the operating current to 1 μA (nominal). |
| V_OUT | B1 | O | Regulated output voltage pin.<br>Placing a small 1-μF ceramic capacitor is required from this pin to ground to ensure stability.<br>See *Input and Output Capacitor Requirements* for more details. |
| V_IN | B2 | I | Input pin.<br>TI recommends placing a small 1-μF capacitor from this pin to ground for good transient performance.<br>See *Input and Output Capacitor Requirements* for more details. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

specified at $T_J$ = −40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage[2] | $V_{IN}$ | −0.3 | 6 | V |
| | $V_{EN}$ | −0.3 | 6 | V |
| | $V_{OUT}$ | −0.3 | 6 | V |
| Maximum output current | $I_{OUT}$ | Internally limited | | |
| Output short-circuit duration | | Indefinite | | |
| Temperature | Operating junction, $T_J$ | −55 | 150 | °C |
| | Storage, $T_{stg}$ | −55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground pin.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101[2] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2 | | 5.5 | V |
| $V_{OUT}$ | Output voltage | 0.7 | | 4.8 | V |
| $I_{OUT}$ | Output current | 0 | | 200 | mA |
| $T_J$ | Junction temperature | −40 | | 125 | °C |

## 6.4 Thermal Information

| | | TLV705 | | |
|---|---|---|---|---|
| THERMAL METRIC[1] | | YFF, YFP (DSBGA) | YFM (PicoStar) | UNIT |
| | | 4 PINS | 4 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 160 | 191.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 80 | 3.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 90 | 36.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | 2.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 78 | 26.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

at $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V (whichever is greater), $I_{OUT}$ = 10 mA, $V_{EN}$ = 0.9 V, and $C_{OUT}$ = 1 μF, unless otherwise noted. Typical values are at $T_J$ = 25°C.

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | | | 2 | | 5.5 | V |
| $V_{OUT}$ | Output voltage range | | | 0.7 | | 4.8 | V |
| $V_O$ | DC output accuracy | –40°C ≤ $T_J$ ≤ 125°C | 0 mA ≤ $I_{OUT}$ ≤ 200 mA, $V_{OUT}$ ≥ 1 V | –2% | ±0.5% | 2% | |
| | | | 0 mA ≤ $I_{OUT}$ ≤ 200 mA, $V_{OUT}$ < 1 V | –20 | ±5 | 20 | mV |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation | $V_{OUT(nom)}$ + 0.5 V ≤ $V_{IN}$ ≤ 5.5 V | | | 0.05 | 5 | mV |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation | 0 mA ≤ $I_{OUT}$ ≤ 200 mA | | | 1 | | mV |
| $V_{DO}$ | Dropout voltage[1] | $V_{IN}$ = 0.98 × $V_{OUT(nom)}$, $I_{OUT}$ = 200 mA | | | 145 | 250 | mV |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$, $T_J$ = 25°C | | 260 | 400 | 550 | mA |
| $I_{GND}$ | Ground pin current | $I_{OUT}$ = 0 mA | | | 35 | 55 | μA |
| | | $I_{OUT}$ = 200 mA | | | 315 | | μA |
| $I_{SHUTDOWN}$ | Shutdown ground pin current | $V_{EN}$ ≤ 0.4 V, 2 V ≤ $V_{IN}$ ≤ 4.5 V | | | 1 | 1.8 | μA |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = 2.3 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 10 mA, f = 10 kHz | | | 80 | | dB |
| | | $V_{IN}$ = 2.3 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 10 mA, f = 1 MHz | | | 55 | | dB |
| $V_n$ | Output noise voltage | BW = 100 Hz to 100 kHz, $I_{OUT}$ = 10 mA | $V_{IN}$ = 2.3 V, $V_{OUT}$ = 1.8 V | | 26.6 | | μV$_{RMS}$ |
| | | | $V_{IN}$ = 3.3 V, $V_{OUT}$ = 2.8 V | | 26.7 | | μV$_{RMS}$ |
| | | | $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V | | 28.2 | | μV$_{RMS}$ |
| | | BW = 10 Hz to 100 kHz, $I_{OUT}$ = 10 mA | $V_{IN}$ = 2.3 V, $V_{OUT}$ = 1.8 V | | 30.7 | | μV$_{RMS}$ |
| | | | $V_{IN}$ = 3.3 V, $V_{OUT}$ = 2.8 V | | 31.3 | | μV$_{RMS}$ |
| | | | $V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V | | 34.1 | | μV$_{RMS}$ |
| $t_{STR}$ | Start-up time[2] | $C_{OUT}$ = 1 μF, $I_{OUT}$ = 200 mA | | | 100 | | μs |
| $V_{HI}$ | Enable high (enabled) | | | 0.9 | | $V_{IN}$ | V |
| $V_{LO}$ | Enable low (disabled) | | | 0 | | 0.4 | V |
| $I_{EN}$ | EN pin current | $V_{EN}$ = 5.5 V | | | 0.01 | | μA |
| UVLO | Undervoltage lockout | $V_{IN}$ rising | | | 1.9 | | V |
| $t_{SD}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | | 160 | | °C |
| | | Reset, temperature decreasing | | | 140 | | °C |
| $T_J$ | Operating junction temperature | | | –40 | | 125 | °C |

(1) $V_{DO}$ is measured for devices with $V_{OUT(nom)}$ = 2.35 V so that $V_{IN}$ = 2.3 V.
(2) Start-up time = time from EN assertion to 0.98 × $V_{OUT(nom)}$.

Product Folder Links: *TLV705  TLV705P*

## 6.6  Typical Characteristics

over operating temperature range ($T_J$ = −40°C to +125°C), $I_{OUT}$ = 10 mA, $V_{EN}$ = 0.9 V, $C_{OUT}$ = 1 μF, and $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at $T_J$ = 25°C.
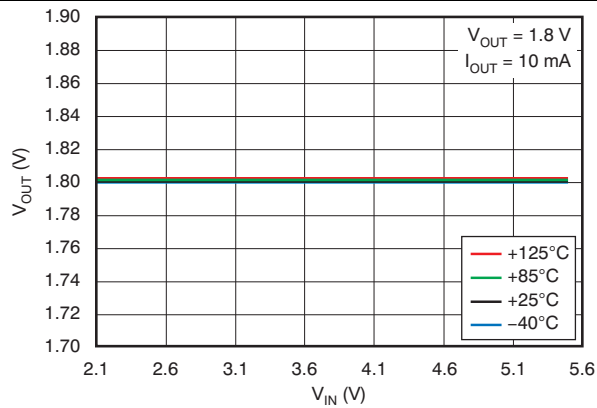


**Figure 1. Line Regulation**
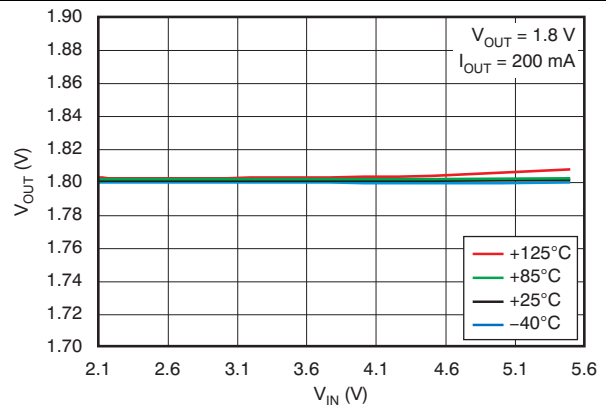


**Figure 2. Line Regulation**
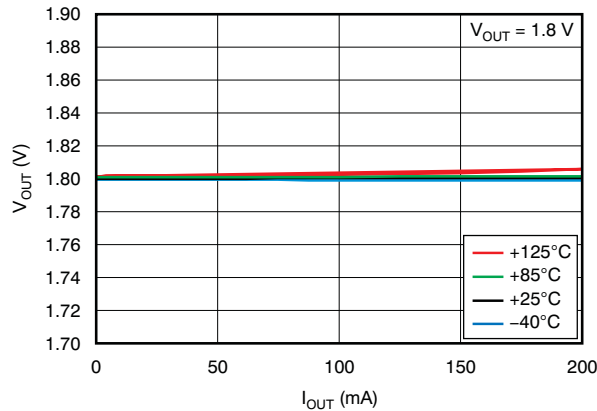


**Figure 3. Load Regulation ( 0 mA ≤ $I_{OUT}$ ≤ 200 mA)**
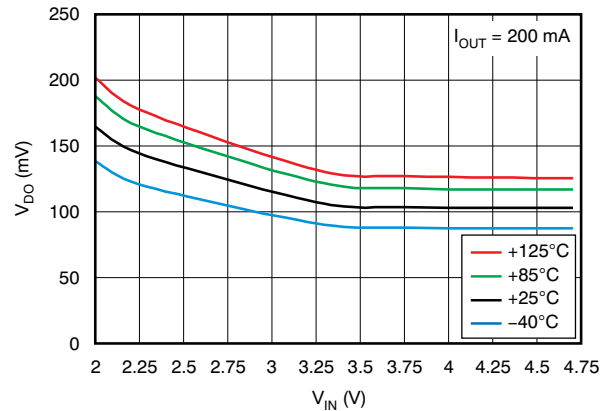


**Figure 4. Dropout Voltage vs Input Voltage**
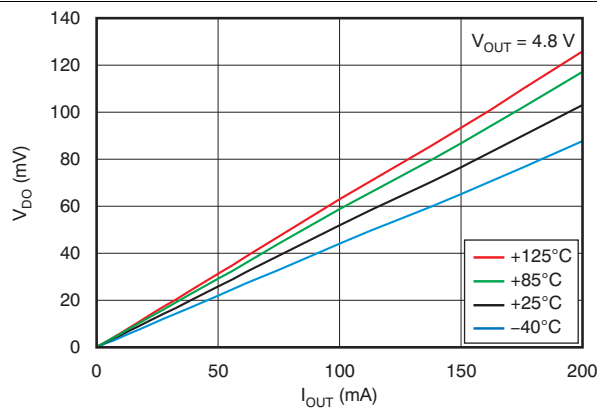


**Figure 5. Dropout Voltage vs Output Current**
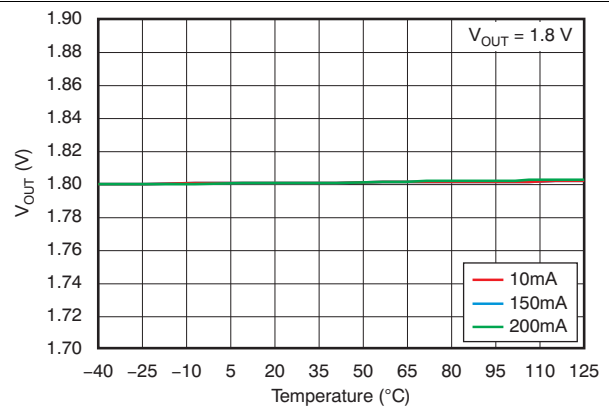


**Figure 6. Output Voltage vs Temperature**

## Typical Characteristics (continued)

over operating temperature range ($T_J$ = –40°C to +125°C), $I_{OUT}$ = 10 mA, $V_{EN}$ = 0.9 V, $C_{OUT}$ = 1 μF, and $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at $T_J$ = 25°C.
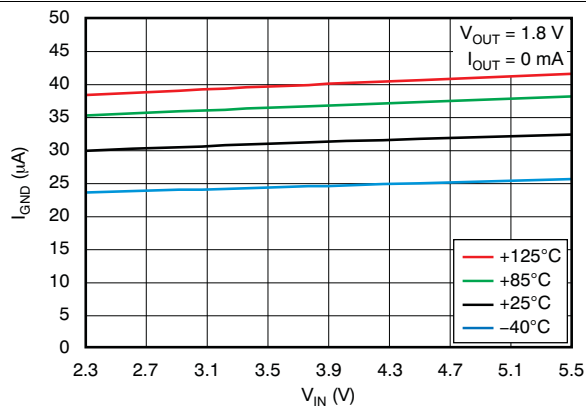


Figure 7. Ground Pin Current vs Input Voltage
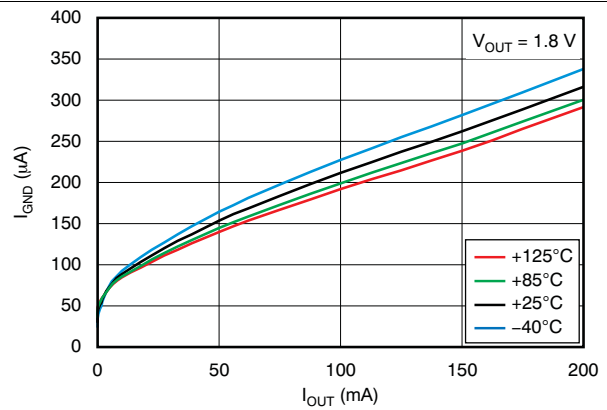


Figure 8. Ground Pin Current vs Output Current
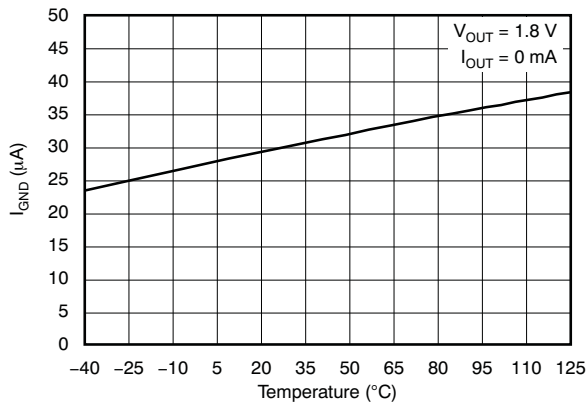


Figure 9. Ground Pin Current vs Temperature
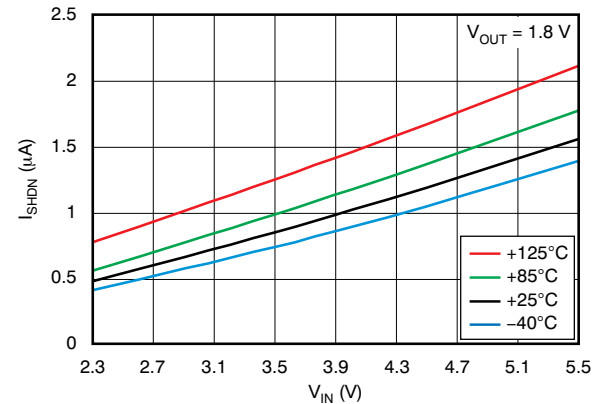


Figure 10. Shutdown Pin Current vs Input Voltage
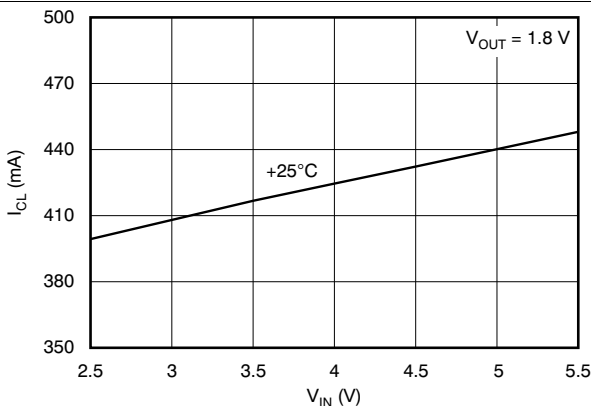


Figure 11. Current Limit vs Input Voltage
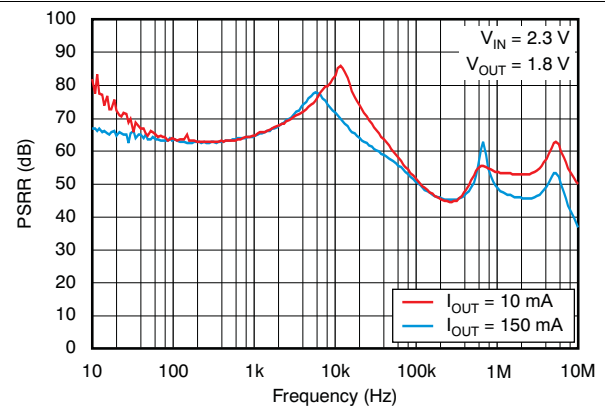


Figure 12. Power-Supply Rejection Ratio vs Frequency

## Typical Characteristics (continued)

over operating temperature range ($T_J$ = −40°C to +125°C), $I_{OUT}$ = 10 mA, $V_{EN}$ = 0.9 V, $C_{OUT}$ = 1 μF, and $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at $T_J$ = 25°C.
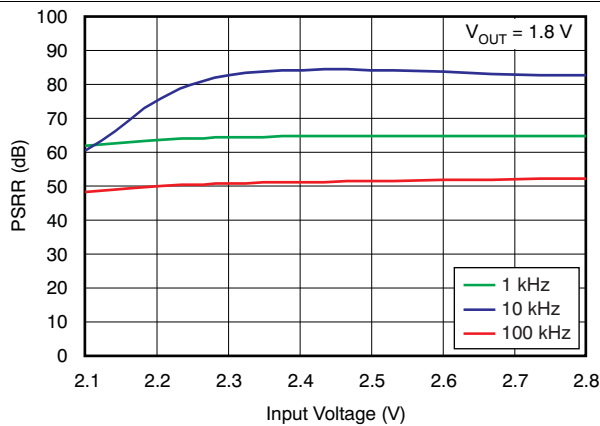


**Figure 13. Power-Supply Rejection Ratio vs Input Voltage**
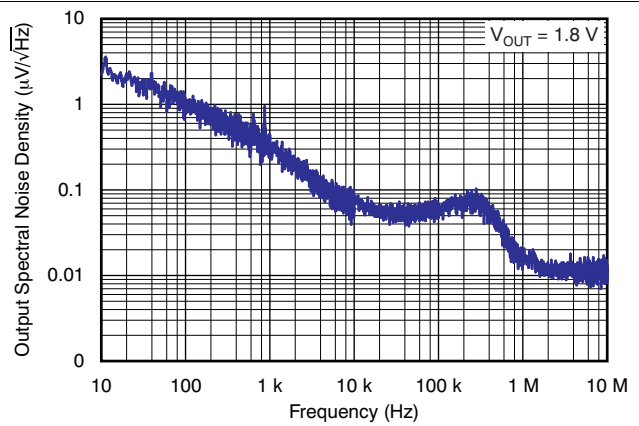


**Figure 14. Output Spectral Noise Density vs Frequency**
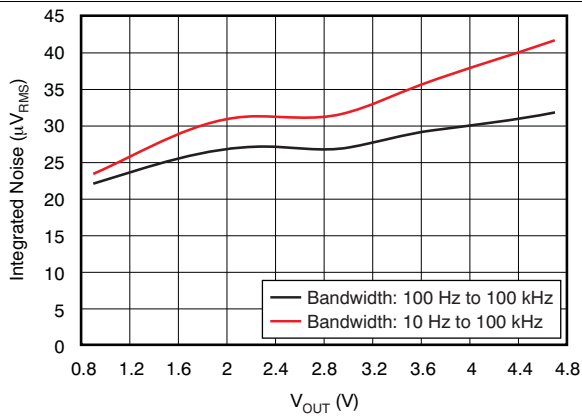


**Figure 15. Integrated Noise vs Output Voltage**
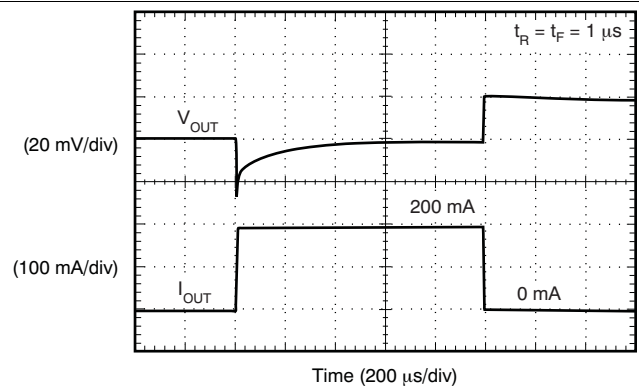


**Figure 16. Load Transient 0**
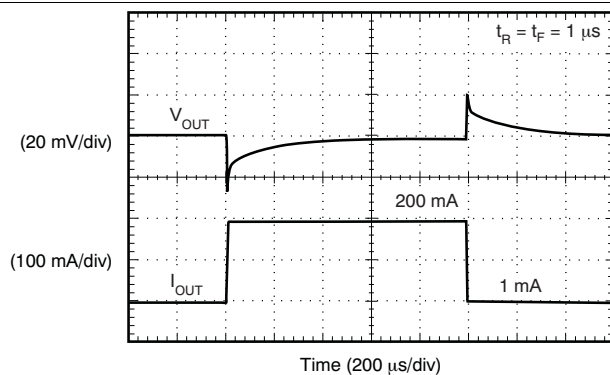


**Figure 17. Load Transient 1**
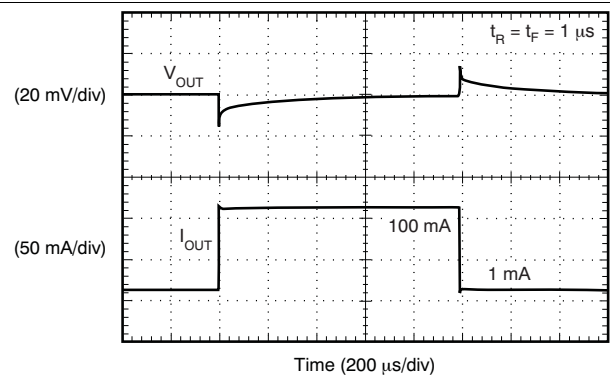


**Figure 18. Load Transient 3**

Product Folder Links: *TLV705  TLV705P*

## Typical Characteristics (continued)

over operating temperature range ($T_J$ = −40°C to +125°C), $I_{OUT}$ = 10 mA, $V_{EN}$ = 0.9 V, $C_{OUT}$ = 1 μF, and $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at $T_J$ = 25°C.
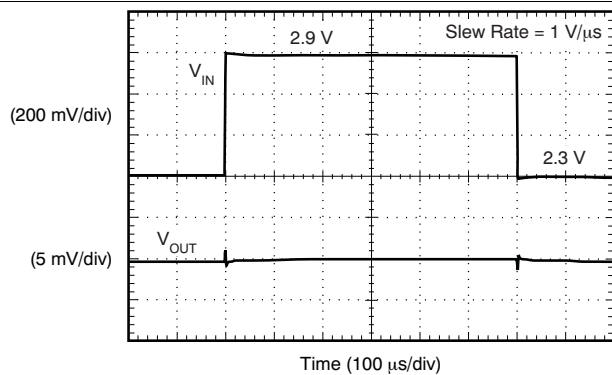
**Figure 19. Small-Step Line Transient (10 mA)**
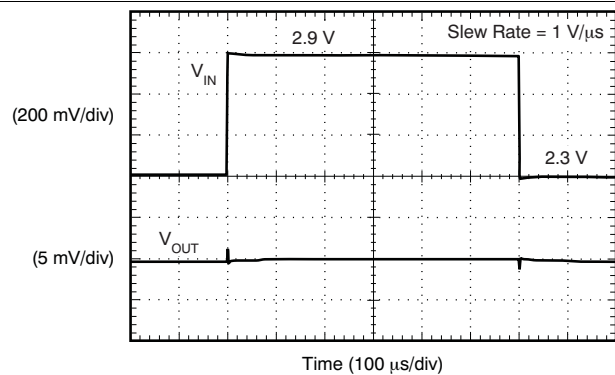
**Figure 20. Small-Step Line Transient (200 mA)**
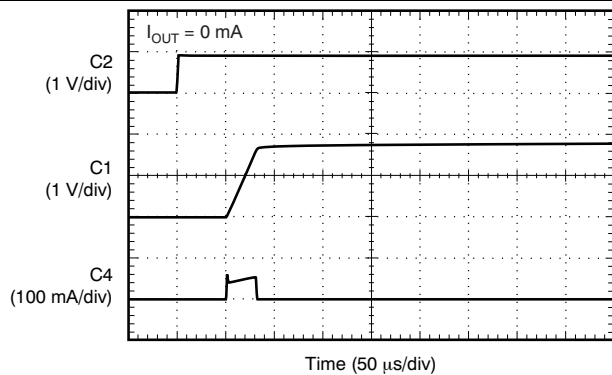
**Figure 21. V$_{IN}$ Inrush Current**
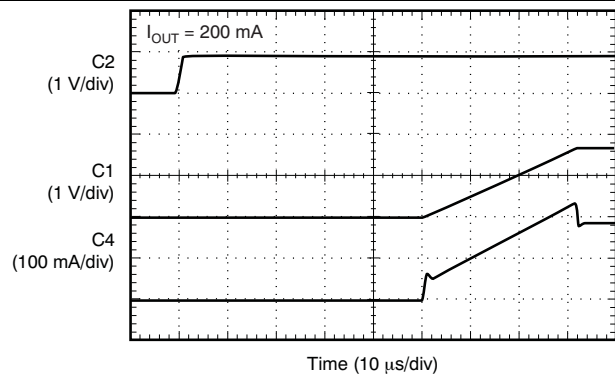
**Figure 22. V$_{IN}$ Inrush Current**
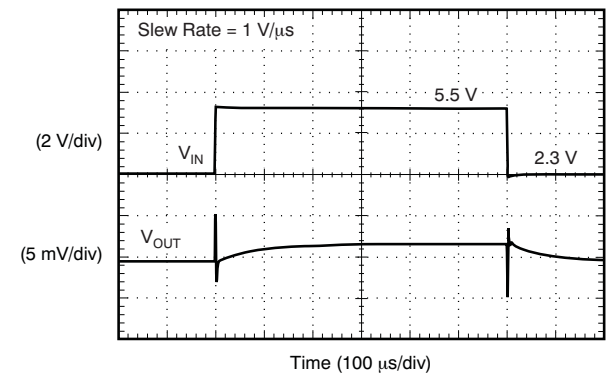
**Figure 23. Line Transient (10 mA)**
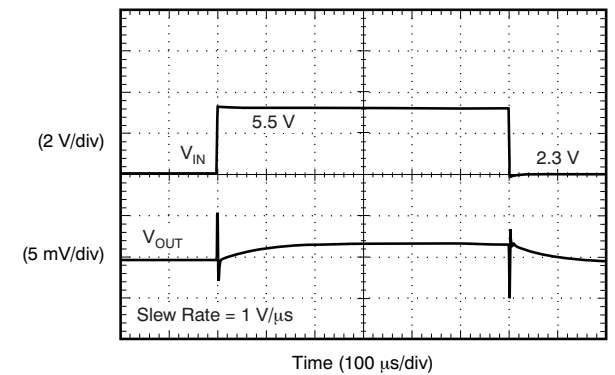
**Figure 24. Line Transient (200 mA)**

Product Folder Links: *TLV705 TLV705P*

## Typical Characteristics (continued)

over operating temperature range ($T_J$ = −40°C to +125°C), $I_{OUT}$ = 10 mA, $V_{EN}$ = 0.9 V, $C_{OUT}$ = 1 μF, and $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater, unless otherwise noted. Typical values are at $T_J$ = 25°C.
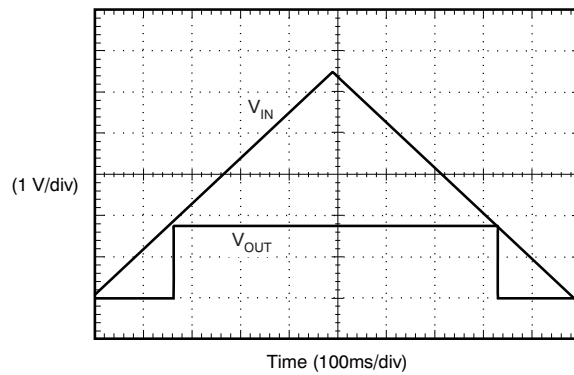


**Figure 25. Power-Up and Power-Down**

# 7 Detailed Description

## 7.1 Overview

The TLV705 and TLV705P series of devices belong to a family of next-generation value low-dropout (LDO) voltage regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. This performance, combined with low noise, very good PSRR with little ($V_{IN} - V_{OUT}$) headroom, makes these devices ideal for RF portable applications. This family of regulators offers sub-band-gap output voltages down to 0.7 V, current limit, and thermal protection, and are specified from –40°C to +125°C. The TLV705P provides an active pulldown circuit to quickly discharge the outputs.

## 7.2 Functional Block Diagrams
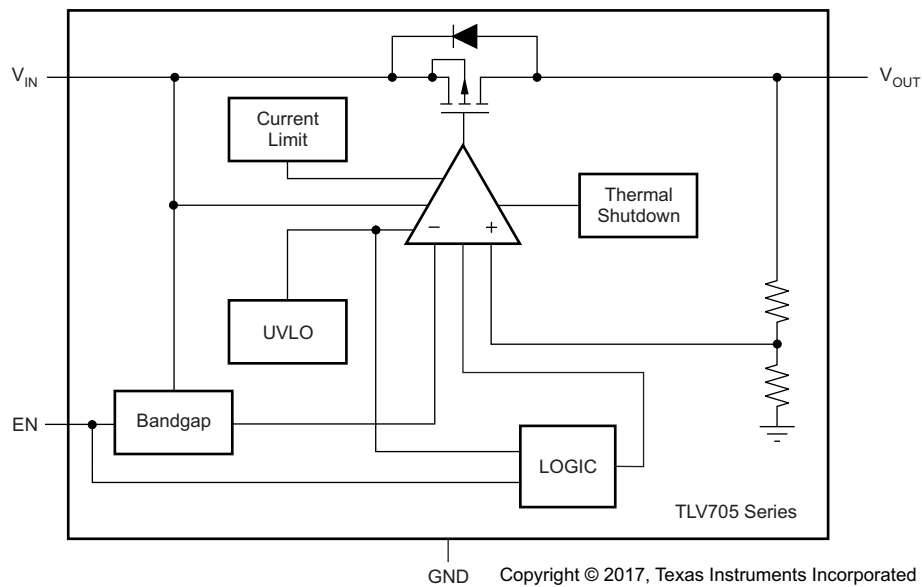


**Figure 26. TLV705 Series**
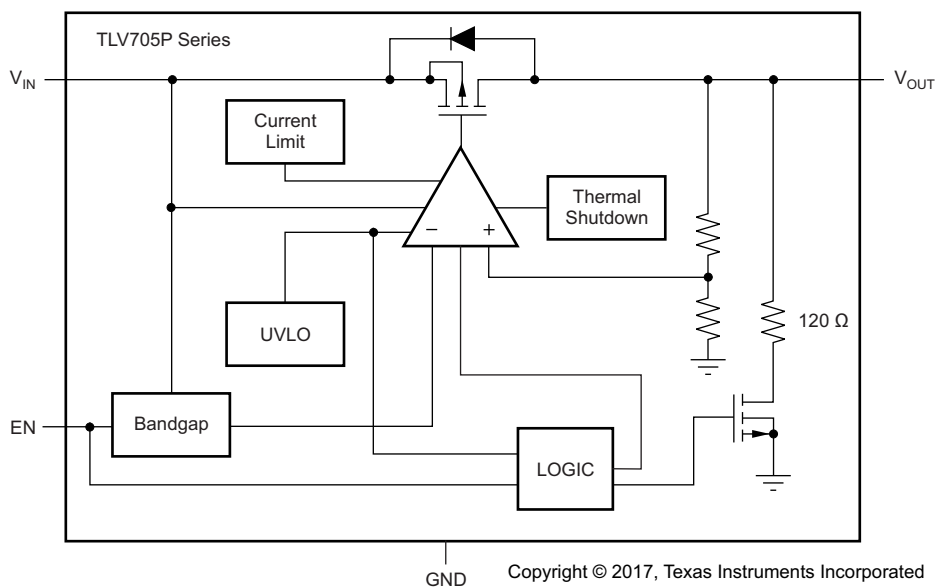


**Figure 27. TLV705P Series**

## 7.3 Feature Description

### 7.3.1 Internal Current Limit

The internal current limits of the TLV705 series help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $[(V_{IN} - V_{OUT}) \times I_{LIMIT}]$ until a thermal shutdown is triggered and the device turns off. When the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see *Power Dissipation and Junction Temperature* for more details.

The PMOS pass element in the TLV705 has a built-in body diode that conducts current when the voltage at $V_{OUT}$ exceeds the voltage at $V_{IN}$. This current is not limited, so if extended reverse voltage operation is anticipated, TI recommends external limiting to 5% of the rated output current.

### 7.3.2 Undervoltage Lockout (UVLO)

The TLV705 uses an UVLO circuit to keep the output shut off until the internal circuitry is operating properly.

### 7.3.3 Start-Up Current

The TLV705 uses a unique start-up architecture that creates a constant start-up time regardless of the output capacitor. The start-up current is given by Equation 1. Equation 1 shows that start-up current is directly proportional to $C_{OUT}$.

$$I_{STARTUP} = C_{OUT} (\mu F) \times 0.06 (V\mu s) + I_{LOAD} (mA) \tag{1}$$

The output voltage ramp rate is independent of $C_{OUT}$ and the load current, and has a typical value of 0.06 V/μs.

The TLV705 automatically adjusts the soft-start current to supply both the load current and the current to charge $C_{OUT}$. For example, if $I_{LOAD} = 0$ mA upon enabling the LDO, then $I_{STARTUP} = 1 \mu F \times 0.06 V\mu s + 0$ mA = 60 mA, which is the current that charges the output capacitor.

However, if $I_{LOAD} = 200$ mA, then $I_{STARTUP} = 1 \mu F \times 0.06 V / \mu s + 200$ mA = 260 mA, which is the required current to charge the output capacitor and supply the load current.

If the output capacitor and load increase such that the start-up current exceeds the output current limit, the start-up current is clamped at the typical current limit of 400 mA. For example, if $C_{OUT} = 10 \mu F$ and $I_{OUT} = 200$ mA, then 10 μF × 0.06 V / μs + 200 mA = 800 mA is not supplied and is instead clamped at 400 mA.

### 7.3.4 Dropout Voltage

The TLV705 uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage $(V_{DO})$, the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. $V_{DO}$ approximately scales with the output current because the PMOS device functions as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} - V_{OUT})$ approaches dropout. This effect is shown in Figure 13 in the *Typical Characteristics*.

### 7.3.5 Shutdown

The enable pin (EN) is active high. The device is enabled when the EN pin goes above 0.9 V. This relatively lower value of voltage required to turn the LDO on can power the device with the GPIO of recent processors with a GPIO voltage lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the $V_{IN}$ pin. The TLV705P version has internal active pulldown circuitry that discharges the output with a time constant of:

$$\tau = (120 \times R_L) / (120 + R_L) \times C_{OUT}$$

where

- $R_L$ = load resistance
- $C_{OUT}$ = output capacitor $\tag{2}$

Product Folder Links: *TLV705 TLV705P*

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The output current is less than the current limit.
- The input voltage is greater than the UVLO voltage.

### 7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer regulates the output voltage of the LDO. Line or load transients in dropout can result in large output voltage deviations.

Table 1 lists the conditions that lead to the different modes of operation.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | |
| --- | --- | --- |
| | $V_{IN}$ | $I_{OUT}$ |
| Normal mode | $V_{IN} > V_{OUT\ (nom)} + V_{DO}$ | $I_{OUT} < I_{CL}$ |
| Dropout mode | $V_{IN} < V_{OUT\ (nom)} + V_{DO}$ | $I_{OUT} < I_{CL}$ |
| Current limit | $V_{IN} > UVLO$ | $I_{OUT} > I_{CL}$ |

Product Folder Links: *TLV705  TLV705P*

# 8 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TLV705 is a LDO that offers very low dropout voltages in a tiny package. The operating junction temperature of this device is –40°C to +125°C.

## 8.2 Typical Application
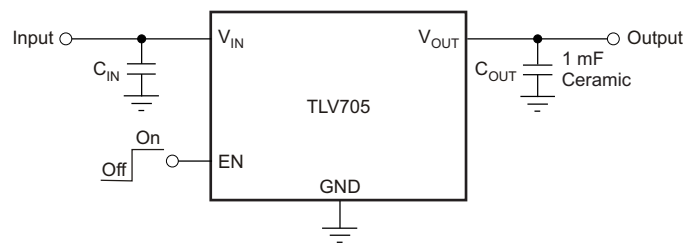


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**Figure 28.  Typical Application Circuit (Fixed-Voltage Versions)**

### 8.2.1  Design Requirements

Table 2 lists the design parameters.

**Table 2. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 2.5 V to 3.3 V |
| Output voltage | 1.8 V |
| Output current | 100 mA |

### 8.2.2  Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout. The input supply must also provide adequate current to account for the GND pin current and load current.

#### 8.2.2.1 Input and Output Capacitor Requirements

TI recommends using 1-μF X5R- and X7R-type ceramic capacitors because these components have minimal variation in value and equivalent series resistance (ESR) over temperature. However, the TLV705 series is designed to be stable with an effective capacitance of 0.1 μF or larger at the output. As a result, the device is stable with capacitors of other dielectrics as long as the effective capacitance under the operating bias voltage and temperature is greater than 0.1 μF. This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions (that is, the capacitance after taking the bias voltage and temperature derating into consideration). In addition to allowing the use of lower cost dielectrics, the effective capacitance enables using smaller footprint capacitors that have higher derating in space-constrained applications.

Using a 0.1-μF rating capacitor at the output of the LDO does not ensure stability because the effective capacitance under operating conditions is less than 0.1 μF. Maximum ESR must be less than 200 mΩ.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-μF to 1-μF low ESR capacitor across the $V_{IN}$ and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-μF input capacitor may be necessary to ensure stability.

#### 8.2.2.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases the duration of the transient response.

### 8.2.3 Application Curves



Figure 29. Power-Supply Rejection Ratio vs Frequency



Figure 30. Power-Up and Power-Down
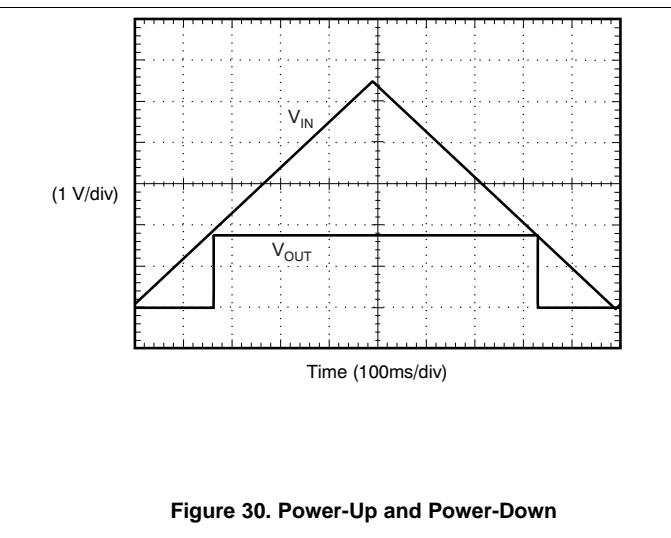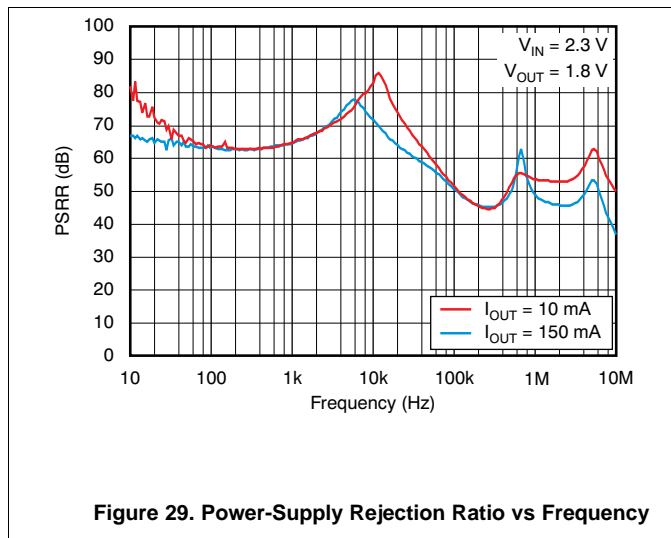
## 8.3 Do's and Don'ts

Place input and output capacitors as close as possible to the device.

Do not exceed the device absolute maximum ratings.

# 9 Power Supply Recommendations

Connect a low output impedance power supply directly to the $V_{IN}$ pin of the TLV705. Inductive impedances between the input supply and the $V_{IN}$ pin can create significant voltage excursions at the $V_{IN}$ pin during start-up or load transient events.

# 10 Layout

## 10.1 Layout Guidelines

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends designing the board with the input and output capacitors on opposite sides of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device. High ESR capacitors can degrade PSRR.

## 10.2 Layout Example
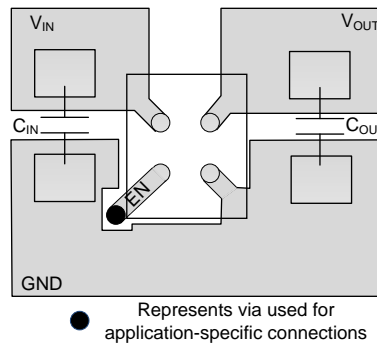


**Figure 31. Example PCB Layout**

## 10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the thermal dissipation.

See for thermal performance on the TLV705 evaluation module (EVM). The EVM is a 2-layer board with two ounces of copper per side.

Power dissipation depends on input voltage and load conditions. Power dissipation ($P_D$) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \qquad (3)$$

## 10.4 Power Dissipation and Junction Temperature

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, which protects the regulator from damage as a result of overheating.

For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV705 is designed to protect against overload conditions. Continuously running the TLV705 into thermal shutdown degrades device reliability.

## 10.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi ($\Psi$) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly discussing thermal resistances; rather, these metrics offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) are given in *Thermal Information* and are used in accordance with Equation 4.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- $P_D$ is the power dissipated, as explained in *Thermal Information*.
- $T_T$ is the temperature at the center-top of the device package, and
- $T_B$ is the PCB surface temperature measured 1 mm from the device package and centered on the package edge. (4)

Product Folder Links: *TLV705 TLV705P*

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### 11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV705. The TLV70533EVM-596 evaluation module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

#### 11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV705 is available through the product folders under *Tools & Software.*

### 11.1.2 Device Nomenclature

**Table 3. Available Options[1]**

| PRODUCT | V$_{OUT}$ |
|---|---|
| TLV705**xx(x)Pyyyz** | **xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 475 = 4.75 V).<br>**P** is optional; devices with P have an LDO regulator with an active output discharge.<br>**yyy** is package designator.<br>**z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces). |

(1)  For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

- *TLV70533EVM-596 Evaluation Module User's Guide* (SLVU439)

## 11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TLV705 | Click here | Click here | Click here | Click here | Click here |
| TLV705P | Click here | Click here | Click here | Click here | Click here |

## 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 Trademarks

E2E is a trademark of Texas Instruments.
PicoStar is a trademark of Texas Instruments, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
Zigbee is a registered trademark of ZigBee Alliance.
All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.7 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 12.1 Package Mounting

Solder pad footprint recommendations for the TLV705 are available from the Packaging Information page on TI's website through the TLV705 series product folders. The recommended land patterns for the YFF, YFP, and YFM packages are appended to this data sheet.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV705075YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 125 | 3V | Samples |
| TLV705075YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 125 | 3V | Samples |
| TLV70509YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 125 | 3W | Samples |
| TLV70509YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 125 | 3W | Samples |
| TLV70512YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | BU | Samples |
| TLV70512YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | BU | Samples |
| TLV70515YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | BV | Samples |
| TLV70515YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | BV | Samples |
| TLV705165YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 125 | CN | Samples |
| TLV705165YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 125 | CN | Samples |
| TLV705185YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | YS | Samples |
| TLV705185YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 125 | YS | Samples |
| TLV70518PYFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | EV | Samples |
| TLV70518PYFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | EV | Samples |
| TLV70518YFMR | ACTIVE | DSLGA | YFM | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| TLV70518YFMT | ACTIVE | DSLGA | YFM | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| TLV70518YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | WT | Samples |
| TLV70518YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | WT | Samples |
| TLV70525PYFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | EK | Samples |
| TLV70525PYFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | EK | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70525YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | YB | Samples |
| TLV70525YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | YB | Samples |
| TLV705285YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | BW | Samples |
| TLV705285YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | BW | Samples |
| TLV70528PYFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 125 | 4E | Samples |
| TLV70528PYFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 125 | 4E | Samples |
| TLV70528YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | WU | Samples |
| TLV70528YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | WU | Samples |
| TLV70530YFMR | ACTIVE | DSLGA | YFM | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| TLV70530YFMT | ACTIVE | DSLGA | YFM | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| TLV70530YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | XA | Samples |
| TLV70530YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | XA | Samples |
| TLV70533PYFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 5L | Samples |
| TLV70533PYFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 5L | Samples |
| TLV70533YFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | US | Samples |
| TLV70533YFFT | ACTIVE | DSBGA | YFF | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | US | Samples |
| TLV70533YFMR | ACTIVE | DSLGA | YFM | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| TLV70533YFMT | ACTIVE | DSLGA | YFM | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| TLV70533YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | VV | Samples |
| TLV70533YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | VV | Samples |
| TLV70534YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | B4 | Samples |

| Orderable Device (1) | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70534YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | B4 | Samples |
| TLV70536YFMR | ACTIVE | DSLGA | YFM | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| TLV70536YFMT | ACTIVE | DSLGA | YFM | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | | Samples |
| TLV70536YFPR | ACTIVE | DSBGA | YFP | 4 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | BX | Samples |
| TLV70536YFPT | ACTIVE | DSBGA | YFP | 4 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | BX | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

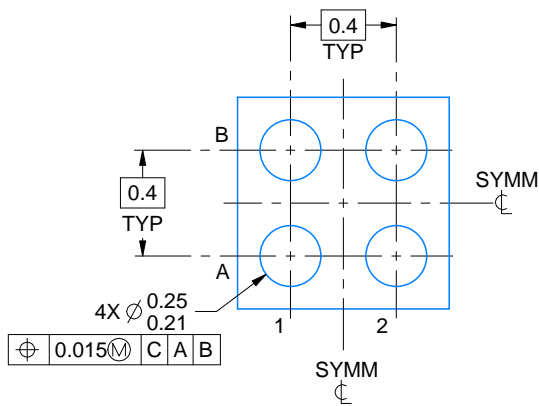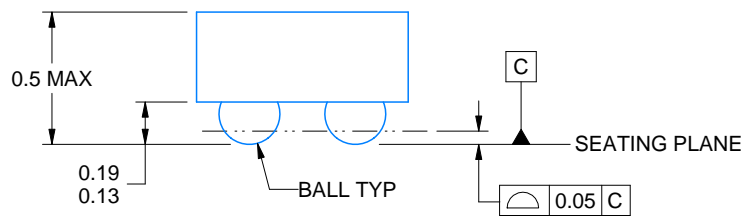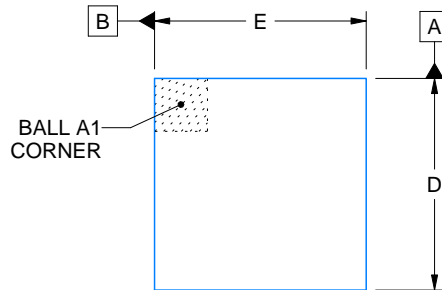| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV705075YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV705075YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70509YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70509YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70512YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70512YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70515YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70515YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV705165YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV705165YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV705185YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV705185YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70518PYFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70518PYFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70518YFMR | DSLGA | YFM | 4 | 3000 | 180.0 | 8.4 | 0.88 | 0.88 | 0.22 | 4.0 | 8.0 | Q1 |
| TLV70518YFMT | DSLGA | YFM | 4 | 250 | 180.0 | 8.4 | 0.88 | 0.88 | 0.22 | 4.0 | 8.0 | Q1 |
| TLV70518YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70518YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV70525PYFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70525PYFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70525YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70525YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV705285YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV705285YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70528PYFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70528PYFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70528YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70528YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70530YFMR | DSLGA | YFM | 4 | 3000 | 180.0 | 8.4 | 0.88 | 0.88 | 0.22 | 4.0 | 8.0 | Q1 |
| TLV70530YFMT | DSLGA | YFM | 4 | 250 | 180.0 | 8.4 | 0.88 | 0.88 | 0.22 | 4.0 | 8.0 | Q1 |
| TLV70530YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70530YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70533PYFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70533PYFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70533YFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TLV70533YFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.85 | 0.85 | 0.64 | 4.0 | 8.0 | Q1 |
| TLV70533YFMR | DSLGA | YFM | 4 | 3000 | 180.0 | 8.4 | 0.88 | 0.88 | 0.22 | 4.0 | 8.0 | Q1 |
| TLV70533YFMT | DSLGA | YFM | 4 | 250 | 180.0 | 8.4 | 0.88 | 0.88 | 0.22 | 4.0 | 8.0 | Q1 |
| TLV70533YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70533YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70534YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70534YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70536YFMR | DSLGA | YFM | 4 | 3000 | 180.0 | 8.4 | 0.88 | 0.88 | 0.22 | 4.0 | 8.0 | Q1 |
| TLV70536YFMT | DSLGA | YFM | 4 | 250 | 180.0 | 8.4 | 0.88 | 0.88 | 0.22 | 4.0 | 8.0 | Q1 |
| TLV70536YFPR | DSBGA | YFP | 4 | 3000 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |
| TLV70536YFPT | DSBGA | YFP | 4 | 250 | 180.0 | 8.4 | 0.86 | 0.86 | 0.59 | 4.0 | 8.0 | Q1 |

**TEXAS INSTRUMENTS**

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV705075YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV705075YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70509YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70509YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70512YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70512YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70515YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70515YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV705165YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV705165YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV705185YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV705185YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70518PYFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70518PYFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70518YFMR | DSLGA | YFM | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV70518YFMT | DSLGA | YFM | 4 | 250 | 210.0 | 185.0 | 35.0 |
| TLV70518YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70518YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70525PYFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70525PYFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV70525YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70525YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV705285YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV705285YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70528PYFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70528PYFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70528YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70528YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70530YFMR | DSLGA | YFM | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV70530YFMT | DSLGA | YFM | 4 | 250 | 210.0 | 185.0 | 35.0 |
| TLV70530YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70530YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70533PYFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70533PYFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70533YFFR | DSBGA | YFF | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70533YFFT | DSBGA | YFF | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70533YFMR | DSLGA | YFM | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV70533YFMT | DSLGA | YFM | 4 | 250 | 210.0 | 185.0 | 35.0 |
| TLV70533YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70533YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70534YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70534YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |
| TLV70536YFMR | DSLGA | YFM | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV70536YFMT | DSLGA | YFM | 4 | 250 | 210.0 | 185.0 | 35.0 |
| TLV70536YFPR | DSBGA | YFP | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV70536YFPT | DSBGA | YFP | 4 | 250 | 182.0 | 182.0 | 20.0 |

BALL A1
CORNER

B | E | A

D

0.5 MAX

0.19
0.13

BALL TYP

C

SEATING PLANE

⌒ | 0.05 | C

0.4
TYP

B

0.4
TYP

A

SYMM
₵

SYMM
₵

1    2

4X ⌀ 0.25
0.21

⊕ | 0.015Ⓜ | C | A | B

D: Max = 0.806 mm, Min =0.746 mm

E: Max = 0.806 mm, Min =0.746 mm
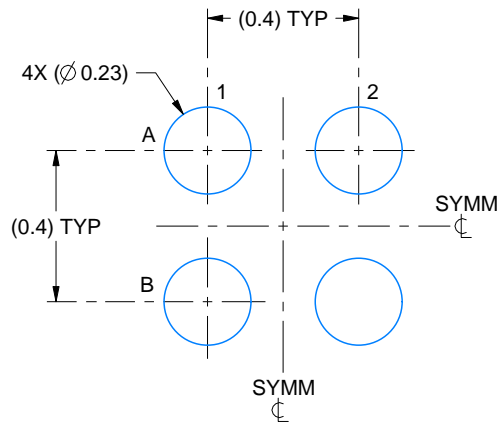
4223507/A   01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.

(0.4) TYP

4X (∅ 0.23)
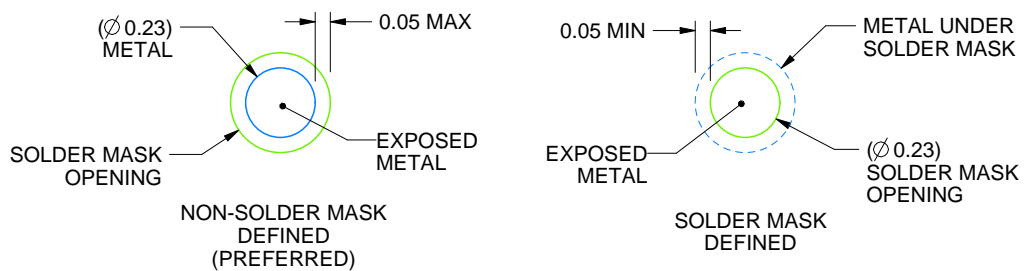
1    2

A

SYMM
℄

(0.4) TYP

B

SYMM
℄

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE:50X

(∅ 0.23)
METAL

0.05 MAX

SOLDER MASK
OPENING

EXPOSED
METAL

**NON-SOLDER MASK
DEFINED
(PREFERRED)**

0.05 MIN

METAL UNDER
SOLDER MASK

EXPOSED
METAL

(∅ 0.23)
SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**

**SOLDER MASK DETAILS**
NOT TO SCALE

4223507/A   01/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

(0.4) TYP

4X (□ 0.25)

(R0.05) TYP

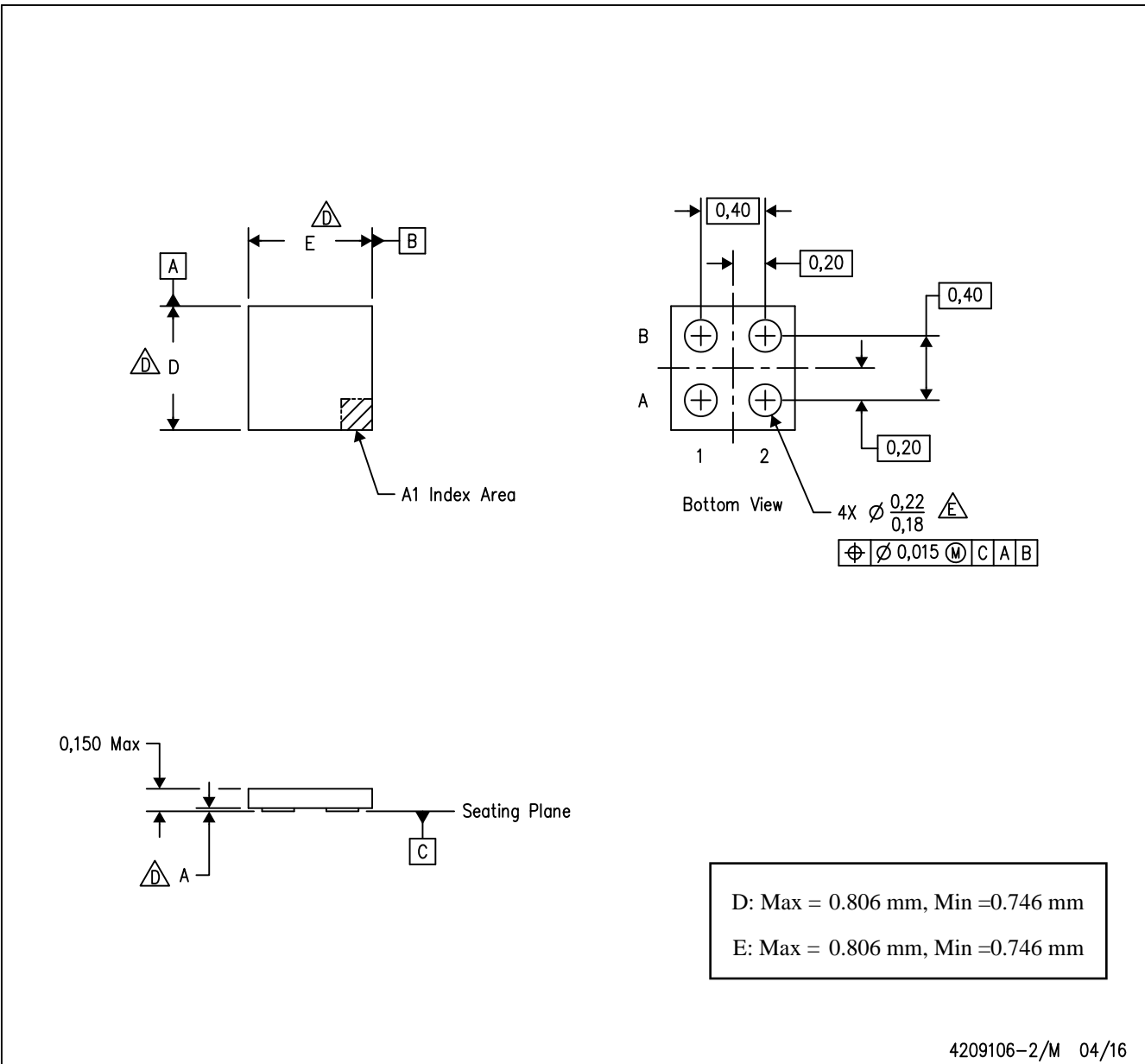1    2

A

SYMM ℄

(0.4) TYP

B

METAL TYP

SYMM ℄
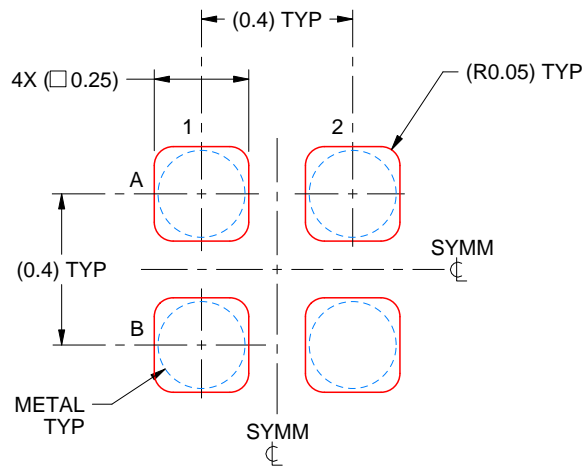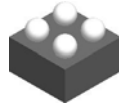
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A  01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

TEXAS
INSTRUMENTS
www.ti.com

YFM (S–pSTAR–N4)                                                                PicoStar™

E

B

A

D

A1 Index Area

0,40

0,20

0,40

B

A

1    2

Bottom View

4X Ø $\frac{0,22}{0,18}$

0,20

⌖ Ø 0,015 Ⓜ C A B

0,150 Max

Seating Plane

C

A

D: Max = 0.806 mm, Min =0.746 mm

E: Max = 0.806 mm, Min =0.746 mm

4209106–2/M   04/16

NOTES:    A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M–1994.
          B.   This drawing is subject to change without notice.
          C.   PicoStar™ package configuration.
          D.   The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version
               of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
          E.   Reference Product Data Sheet for array population.   2 x 2 matrix pattern is shown for illustration only.
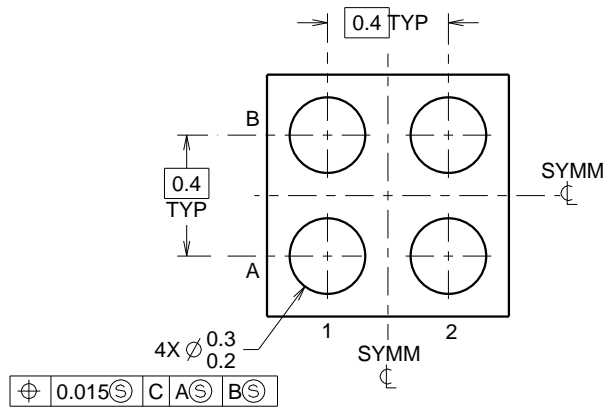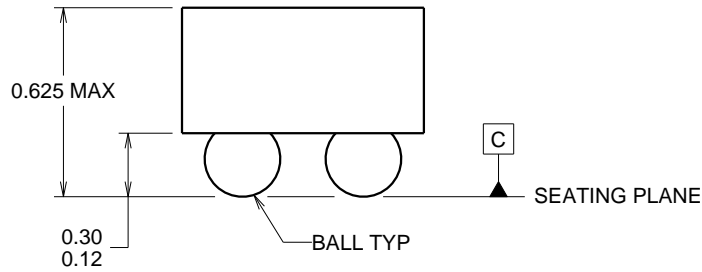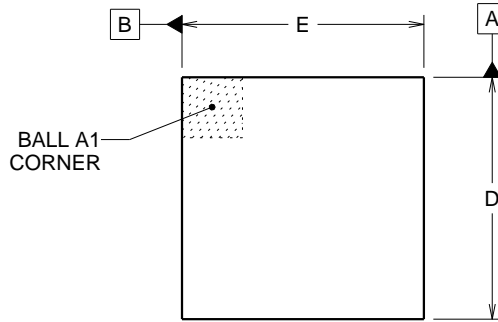          F.   This package is a Pb–free solder land design.

PicoStar is a trademark of Texas Instruments.

**TEXAS INSTRUMENTS**

www.ti.com

B ← E → A

BALL A1
CORNER

D

0.625 MAX

0.30
0.12

C

SEATING PLANE

BALL TYP

0.4 TYP

B

0.4
TYP

A

SYMM
₵

SYMM
₵

1    2

4X ⌀ 0.3
0.2

⊕ | 0.015Ⓢ | C | AⓈ | BⓈ

D: Max = 0.806 mm, Min =0.746 mm

E: Max = 0.806 mm, Min =0.746 mm

4219460/A   02/2014

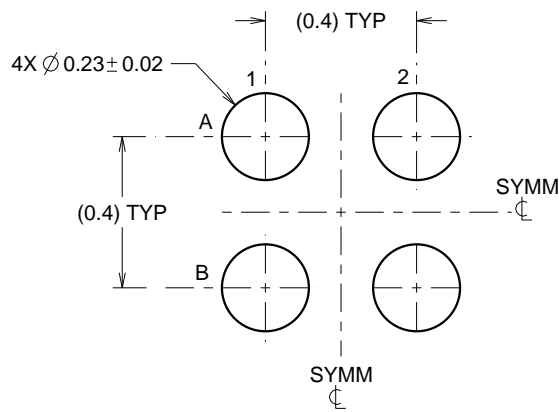NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

## YFF0004

4X ⌀ 0.23± 0.02
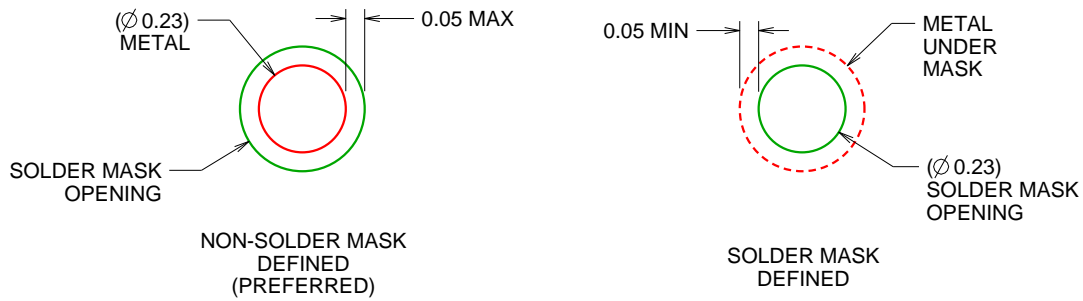
(0.4) TYP

(0.4) TYP

1

2

A

B

SYMM ℄

SYMM ℄

**LAND PATTERN EXAMPLE**
SCALE:50X

(⌀ 0.23) METAL

0.05 MAX

SOLDER MASK OPENING

**NON-SOLDER MASK DEFINED (PREFERRED)**

0.05 MIN

METAL UNDER MASK

(⌀ 0.23) SOLDER MASK OPENING

**SOLDER MASK DEFINED**

**SOLDER MASK DETAILS**
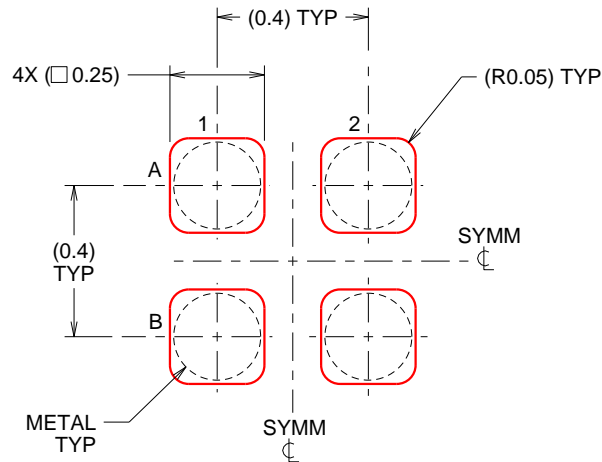NOT TO SCALE

4219460/A   02/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

(0.4) TYP

4X (□ 0.25)

(R0.05) TYP

1    2

A

(0.4)
TYP

SYMM
℄

B

METAL
TYP

SYMM
℄

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4219460/A   02/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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NCP4687DH15T1G  NCV8703MX30TCG  LP2951CN  NCV4269CPD50R2G  AP7315-25W5-7  NCV47411PAAJR2G  AP2111H-1.2TRG1
ZLDO1117QK50TC  AZ1117ID-ADJTRG1  NCV4263-2CPD50R2G  NCP114BMX075TCG  MC33269T-3.5G  TLE4471GXT  AP7315-33SA-7  NCV4266-2CST33T3G  NCP715SQ15T2G  NCV8623MN-50R2G  NCV563SQ18T1G  NCV8664CDT33RKG  NCV4299CD250R2G
NCP715MX30TBG  NCV8702MX25TCG  TLE7270-2E  NCV562SQ25T1G  AP2213D-3.3TRG1  AP2202K-2.6TRE1
NCV8170BMX300TCG  NCV8152MX300180TCG  NCP700CMT45TBG  AP7315-33W5-7  NCP154MX180300TAG  AP2113AMTR-G1
NJW4104U2-33A-TE1  MP2013AGG-5-P  NCV8775CDT50RKG  NJM2878F3-45-TE1  S-19214B00A-V5T2U7  S-19214B50A-V5T2U7  S-19213B50A-V5T2U7  S-19214BC0A-E8T1U7*1  S-19213B00A-V5T2U7  S-19213B33A-V5T2U7  S-19213BC0A-V5T2U7