TLV713P-Q1 面向便携式设备且具有折返电流限制的无电容 150mA 低压降稳压器

1 特性

- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 输入电压范围：1.4V 至 5.5V
- 有无电容器均可实现稳定运行
- 折返过流保护
- 封装：5 引脚小外形尺寸晶体管 (SOT)-23
- 超低压降：150mA 时为 230mV
- 准确度：1%
- 低 I_Q：50µA
- 可用固定输出电压范围：
  - 1V 至 3.3V
- 高电源抑制比 (PSRR)：1kHz 频率时为 65dB
- 有源输出放电

2 应用

- 汽车类主机
- 音频放大器
- DI 仪表板
- 高级驾驶员辅助系统 (ADAS) 电子控制单元 (ECU)
- 微处理器轨
- USB
- 车身电子装置

3 说明

TLV713P-Q1 系列低压降线性稳压器 (LDO) 具有较低的静态电流，并且线路和负载瞬态性能出色，适用于功耗敏感型应用。 此系列器件可提供典型值为 1% 的精度。

TLV713P-Q1 系列器件经过设计，无需使用输出电容即可稳定运行。 移除输出电容可实现极小的解决方案尺寸。 不过，TLV713P-Q1 系列器件与任何输出电容搭配使用时也可保持稳定（如果使用输出电容）。

TLV713P-Q1 还可在器件上电和使能期间提供浪涌电流控制。 TLV713P-Q1 会将输入电流限制为定义的电流限值，以防止从输入电源流出的电流过大。 此功能对于电池供电类器件尤为重要。

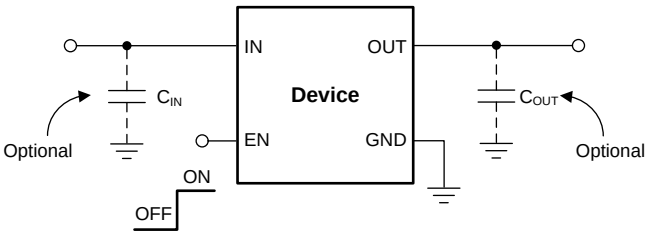
TLV713P-Q1 系列器件采用标准的 DBV 封装，并提供了一个有源下拉电路，用于使输出负载快速放电。 TLV713P-Q1 符合 AEC-Q100 1 级标准，因此适用于汽车应用。

器件信息(1)

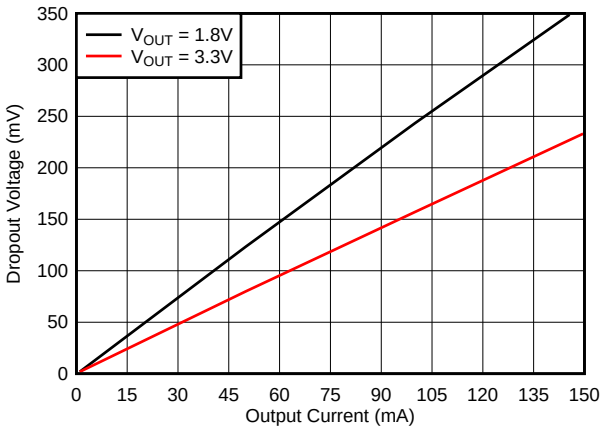
器件型号	封装	封装尺寸（标称值）
TLV713P-Q1	SOT-23 (5)	2.90mm x 1.60mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路



压降电压与输出电流间的关系



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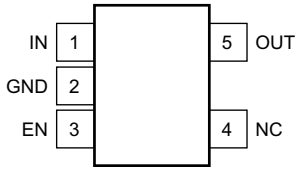
4 修订历史记录

日期	修订版本	注释
2015 年 5 月	*	首次发布。

5 Pin Configurations and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO. SOT-23		
EN	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	—	Ground pin
IN	1	I	Input pin. A small capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Considerations* section in the *Feature Description* for more details.
NC	4	—	No internal connection
OUT	5	O	Regulated output voltage pin. For best transient response, a small 1-µF ceramic capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Considerations* section in the *Feature Description* for more details.
Thermal pad		—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (T_J = 25°C), unless otherwise noted. All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	V_{IN} + 0.3	V
	Output, V_{OUT}	–0.3	3.6	V
Current	Maximum output, $I_{OUT(max)}$	Internally limited		
Output short-circuit duration		Indefinite		
Total power dissipation	Continuous, $P_{D(tot)}$	See the *Thermal Information*		
Temperature	Storage, T_{stg}	–55	150	°C
	Junction, T_J	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.4		5.5	V
V_{EN}	Enable range	0		V_{IN}	V
I_{OUT}	Output current	0		150	mA
C_{IN}	Input capacitor	0	1		µF
C_{OUT}	Output capacitor	0	0.1	100	µF
T_J	Operating junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		TLV713P-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	249	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	172.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	49.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

6.5 Electrical Characteristics

Over operating temperature range (T_J, T_A = –40°C to 125°C), $V_{IN(nom)} = V_{OUT(nom)} + 0.5$ V or $V_{IN(nom)} = 2$ V (whichever is greater), I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, and C_{OUT} = 0.47 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			1.4		5.5	V
V_{OUT}	Output voltage range			1		3.3	V
	DC output accuracy	$V_{OUT} \geq 1.8$ V; T_J, T_A = 25°C		–1%		1%	
		$V_{OUT} < 1.8$ V; T_J, T_A = 25°C		–20		20	mV
		$V_{OUT} \geq 1.2$ V; –40°C ≤ T_J, T_A ≤ 125°C		–1.5%		1.5%	
		$V_{OUT} < 1.2$ V; –40°C ≤ T_J, T_A ≤ 125°C		–50		50	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	Max [$V_{OUT(nom)}$ + 0.5 V, V_{IN} = 2.0 V] ≤ V_{IN} ≤ 5.5 V			1	5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	30	mV
V_{DO}	Dropout voltage	V_{OUT} = 0.98 × $V_{OUT(nom)}$; T_J, T_A = –40°C to 85°C	1 V ≤ V_{OUT} < 1.8 V, I_{OUT} = 150 mA		600	900	mV
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 30 mA		70		mV
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 150 mA		350	575	mV
			2.5 V ≤ V_{OUT} < 3 V, I_{OUT} = 30 mA		50		mV
			2.5 V ≤ V_{OUT} < 3 V, I_{OUT} = 150 mA		246	445	mV
			3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 30 mA		46		mV
			3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 150 mA		230	420	mV
		V_{OUT} = 0.98 × $V_{OUT(nom)}$; T_J, T_A = –40°C to 125°C	1 V ≤ V_{OUT} < 1.8 V, I_{OUT} = 150 mA		600	1020	mV
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 150 mA		350	695	mV
			2.5 V ≤ V_{OUT} < 3 V, I_{OUT} = 150 mA		246	600	mV
			3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 150 mA		230	560	mV
I_{GND}	Ground pin current	I_{OUT} = 0 mA			50	75	µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V; 2.0 V ≤ V_{IN} ≤ 5.5 V; T_J, T_A = 25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA	f = 100 Hz		70		dB
			f = 10 kHz		55		dB
			f = 1 MHz		55		dB
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			73		μV_{RMS}
t_{STR}	Start-up time	C_{OUT} = 1.0 µF, I_{OUT} = 150 mA			100		µs
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		µA
$R_{PULLDOWN}$	Pulldown resistor	V_{IN} = 4 V			120		Ω
I_{LIM}	Output current limit	V_{IN} = 3.8 V, V_{OUT} = 3.3 V		175			mA
		V_{IN} = 3.0 V, V_{OUT} = 2.5 V		175			mA
		V_{IN} = 2.3 V, V_{OUT} = 1.8 V		175			mA
		V_{IN} = 2.0 V, V_{OUT} = 1.2 V		175			mA
		V_{IN} = 2.0 V, V_{OUT} = 1.0 V		175			mA
I_{SC}	Short-circuit current	V_{OUT} = 0 V			40		mA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing			158		°C
		Reset, temperature decreasing			140		°C

6.6 Typical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.

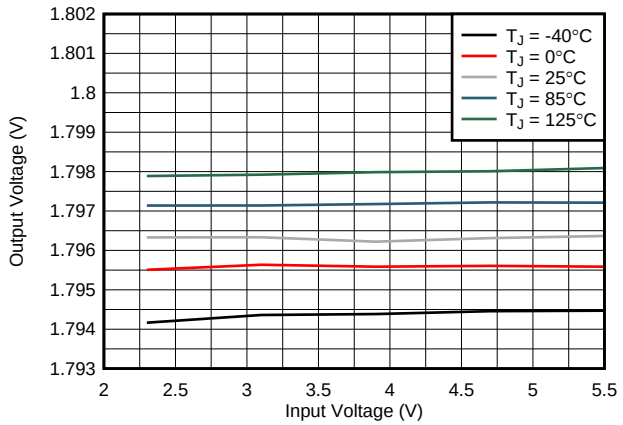


Figure 1. 1.8-V Line Regulation vs V_{IN} and Temperature

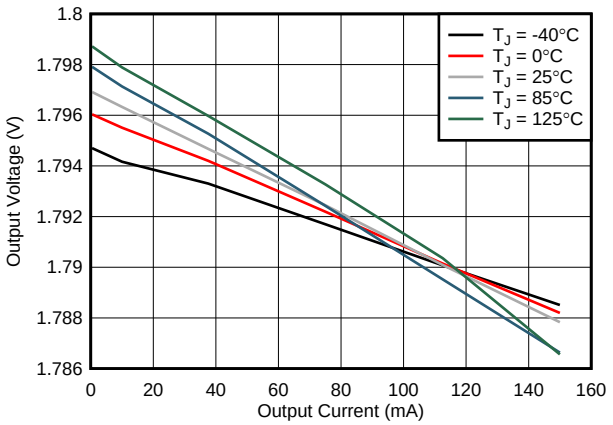


Figure 2. 1.8-V Load Regulation vs I_{OUT} and Temperature

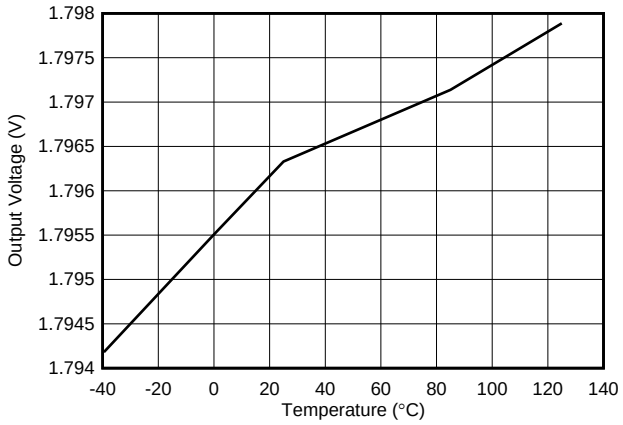


Figure 3. 1.8-V Output Voltage vs Temperature

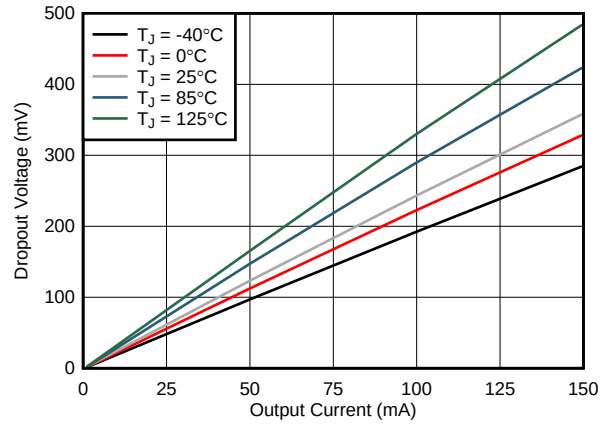


Figure 4. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

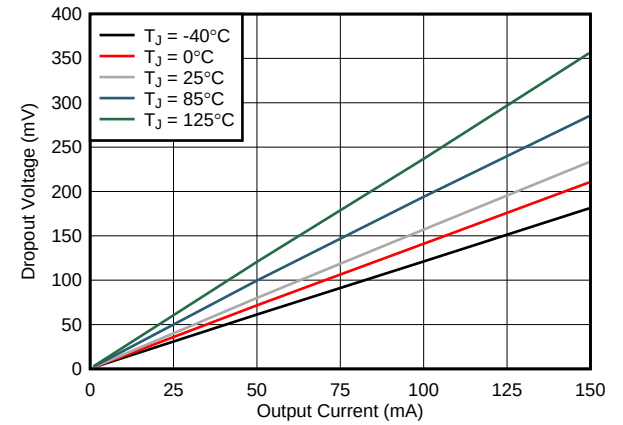


Figure 5. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

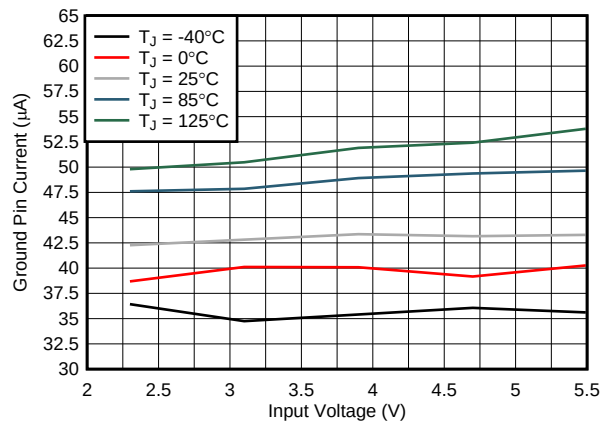


Figure 6. Ground Pin Current vs V_{IN} and Temperature

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.

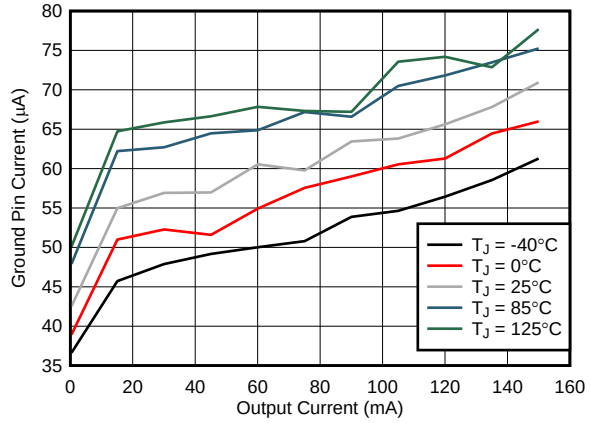


Figure 7. Ground Pin Current vs I_{OUT} and Temperature

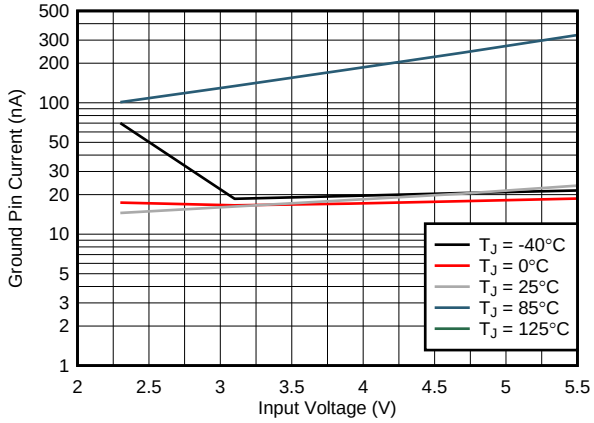


Figure 8. Shutdown Current vs V_{IN} and Temperature

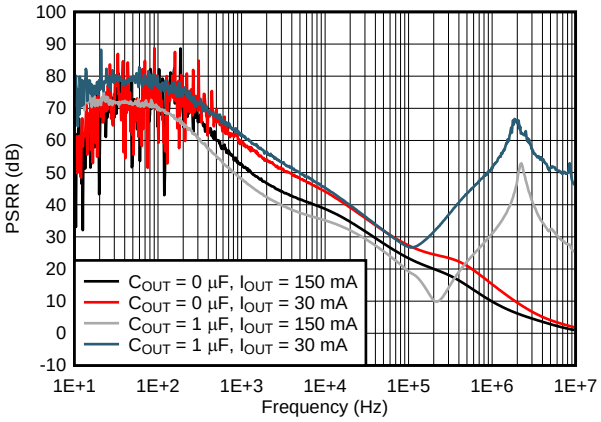


Figure 9. Power-Supply Rejection Ratio vs Frequency and C_{OUT}

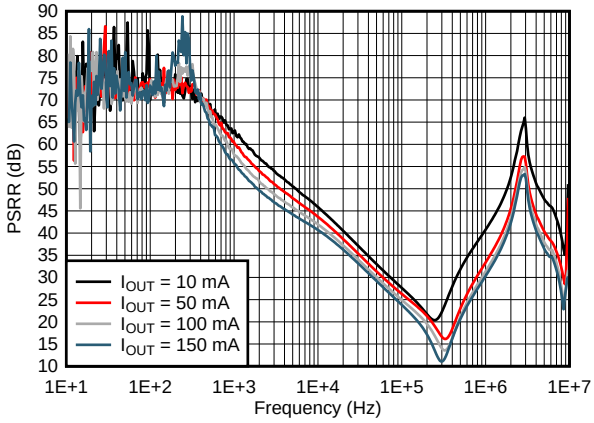


Figure 10. Power-Supply Rejection Ratio vs Frequency and I_{OUT}

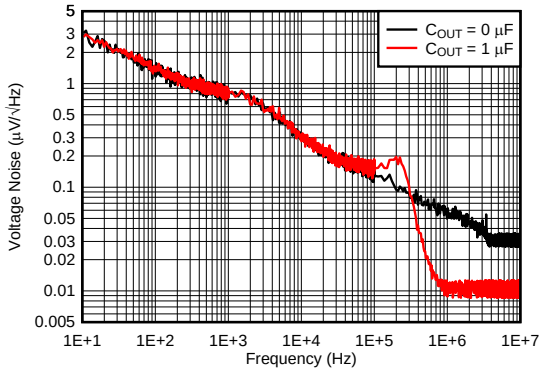
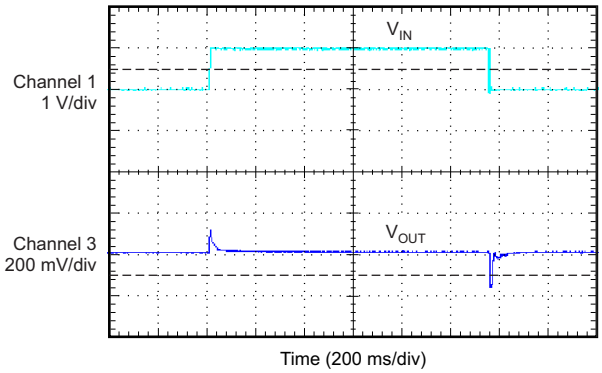


Figure 11. Output Spectral Noise Density

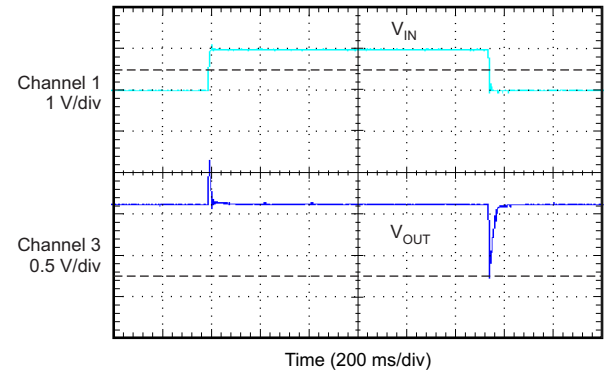


V_{IN} = 3 V to 4 V , I_{OUT} = 0 mA, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 12. Line Transient

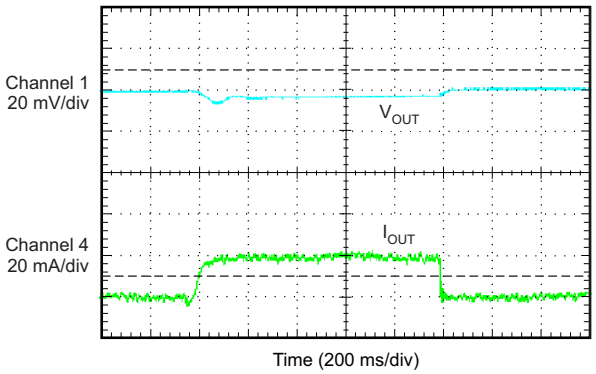
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.



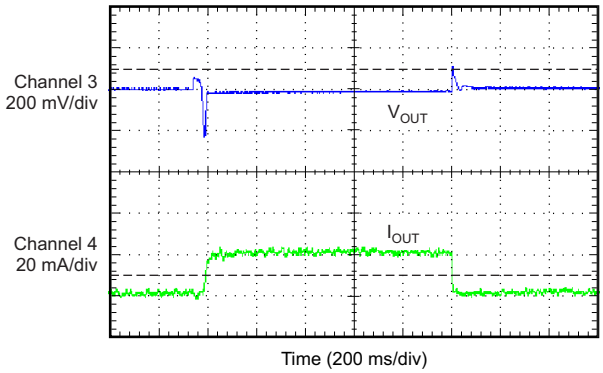
V_{IN} = 3 V to 4 V, I_{OUT} = 150 mA, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 13. Line Transient



V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 1 µF

Figure 14. 0-mA to 20-mA Load Transient



V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 15. 0-mA to 20-mA Load Transient

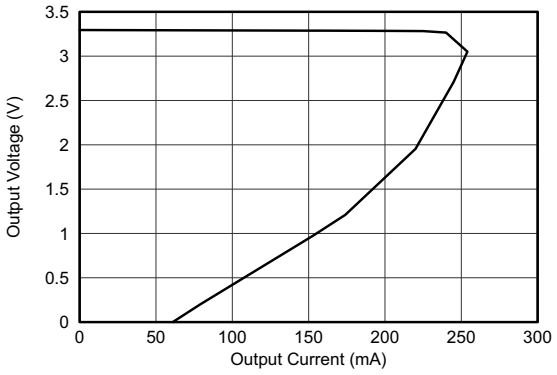
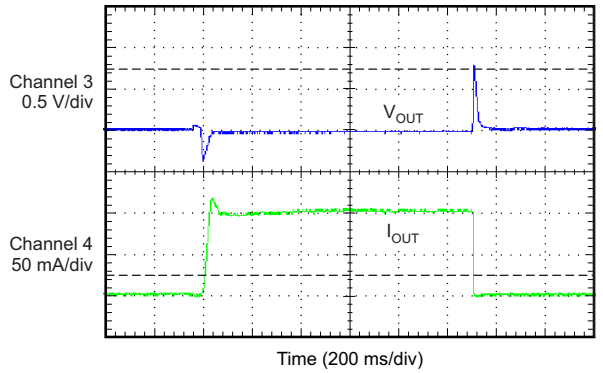


Figure 16. 3.3-V Output Voltage vs Output Current (Foldback Current Limit)



V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 17. 0-mA to 100-mA Load Transient

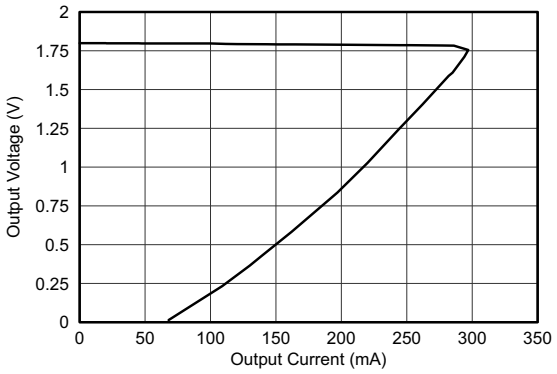
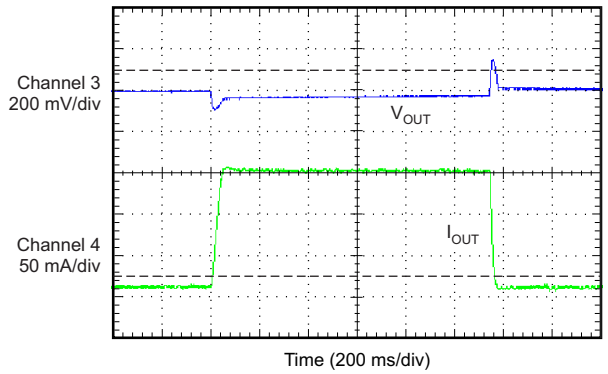


Figure 18. 1.8-V Output Voltage vs Output Current (Foldback Current Limit)

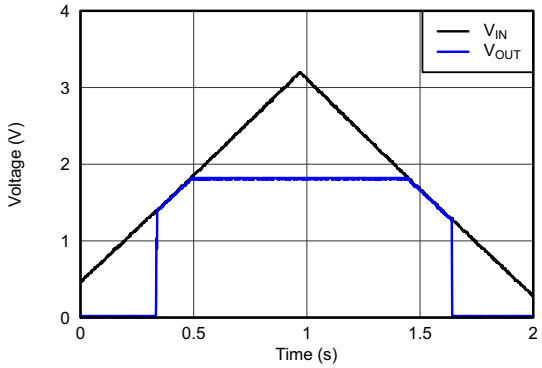
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.



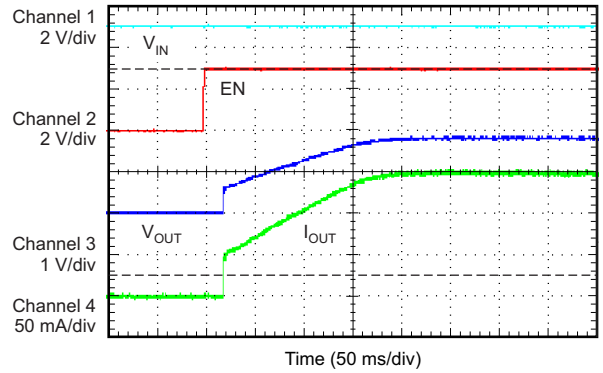
V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 19. 10-mA to 150-mA Load Transient



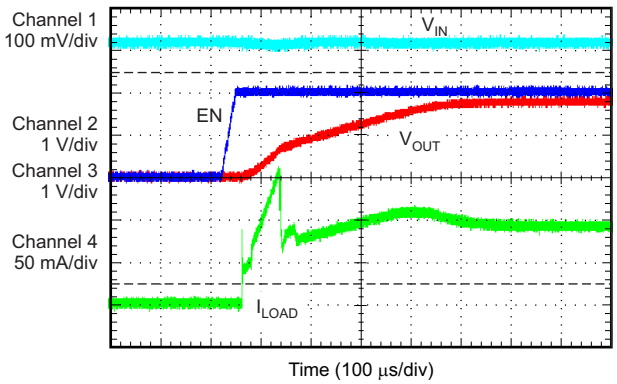
I_{OUT} = 150 mA

Figure 20. V_{IN} Power-Up and Power-Down



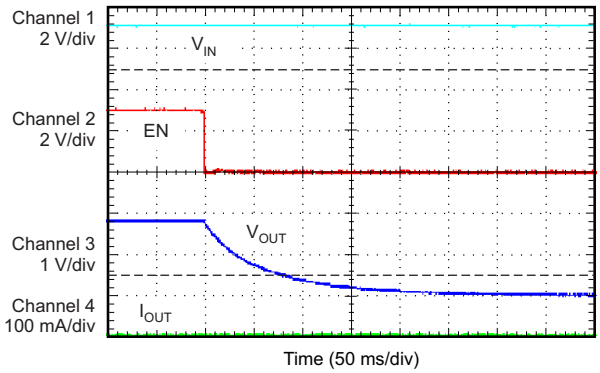
V_{IN} = 3 V, I_{OUT} = 150 mA, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 21. Start-Up With EN



V_{IN} = 2.3 V, I_{OUT} = 90 mA, C_{OUT} = 10 µF, V_{OUT} = 1.8 V, C_{IN} = 1 µF

Figure 22. Start-Up With EN



V_{IN} = 3 V, I_{OUT} = 0 mA, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 1 µF

Figure 23. Shutdown Response With Enable

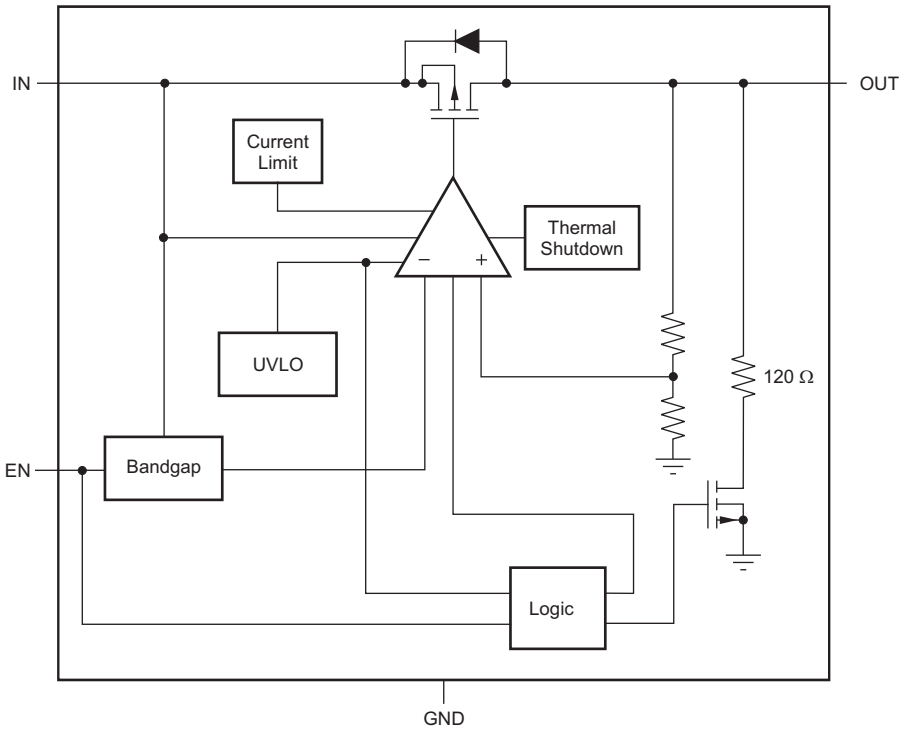
7 Detailed Description

7.1 Overview

These devices belong to a family of low-dropout (LDO) regulators that consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current limit and thermal protection. Device operating junction temperature is –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TLV713P-Q1 uses a UVLO circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$. During UVLO disable, the output of the TLV713P-Q1 is connected to ground with a 120-Ω pulldown resistor.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V. If shutdown capability is not required, connect EN to IN.

The TLV713P-Q1 has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. The time constant is calculated in Equation 1.

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

7.3.3 Foldback Current Limit

The TLV713P-Q1 has an internal foldback current limit that helps protect the regulator during fault conditions. The current supplied by the device is gradually reduced when the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is calculated by Equation 2:

$$V_{OUT} = I_{LIMIT} \times R_{LOAD} \quad (2)$$

The PMOS pass transistor dissipates $[(V_{IN} – V_{OUT}) \times I_{LIMIT}]$ until thermal shutdown is triggered and the device turns off. The device is turned on by the internal thermal shutdown circuit during cool down. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The TLV713P-Q1 PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV713P-Q1 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TLV713P-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 158°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Considerations

The TLV713P-Q1 uses an advanced internal control loop to obtain stable operation both with and without the use of input or output capacitors. The TLV713P-Q1 dynamic performance is improved with the use of an output capacitor. An output capacitance of 0.1 µF or larger generally provides good dynamic response. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

The TLV713P-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout.

8.1.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2 Typical Application

Several versions of the TPS713P-Q1 are ideal for powering the MSP430 microcontroller.

Figure 24 shows a diagram of the TLV713P-Q1 powering an MSP430 microcontroller. Table 2 shows potential applications of some voltage versions.

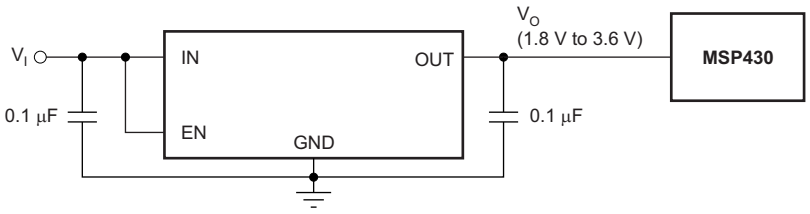


Figure 24. TLV713P-Q1 Powering a Microcontroller

Table 2. Typical MSP430 Applications

DEVICE	V_{OUT} (Typ)	APPLICATION
TLV71318P-Q1	1.8 V	Allows for lowest power consumption with many MSP430s
TLV71325P-Q1	2.5 V	2.2-V supply required by many MSP430s for flash programming and erasing

8.2.1 Design Requirements

Table 3 lists the design requirements.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2 V to 3 V (Lithium Ion battery)
Output voltage	1.8 V, ±1%
DC output current	10 mA
Peak output current	75 mA
Maximum ambient temperature	65°C

8.2.2 Detailed Design Procedure

An input capacitor is not required for this design because of the low impedance connection directly to the battery.

No output capacitor allows for the minimal possible inrush current during start-up, ensuring the 180-mA maximum input current limit is not exceeded.

8.2.3 Application Curves

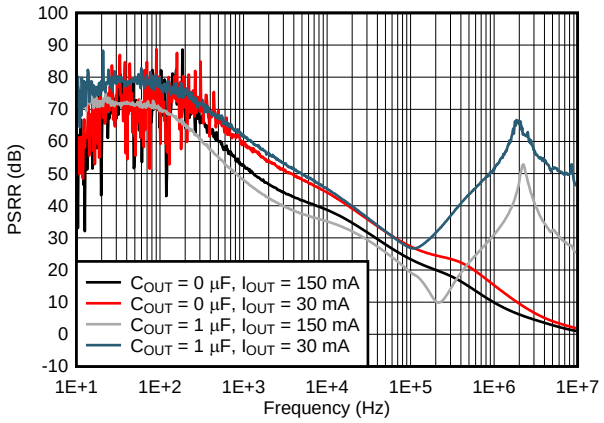


Figure 25. Power-Supply Rejection Ratio vs Frequency

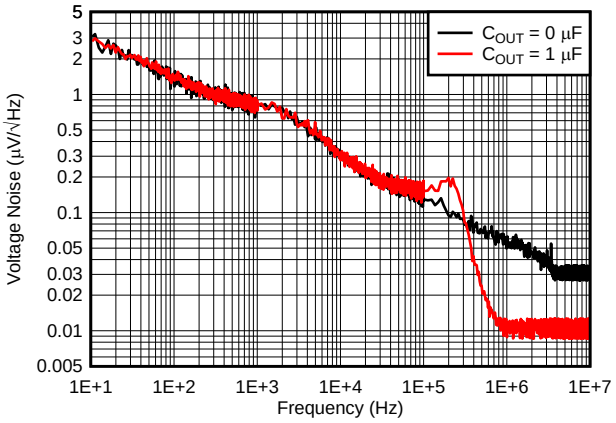


Figure 26. Output Spectral Noise Density

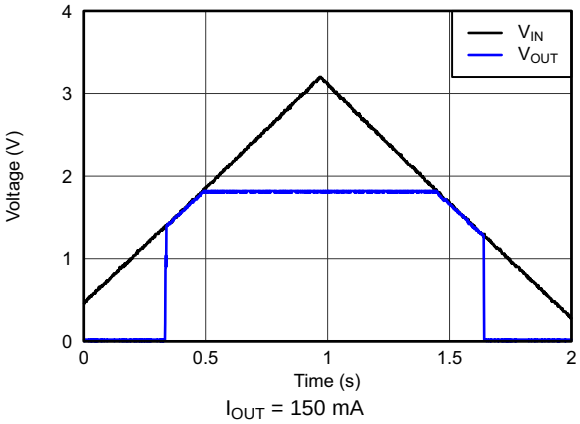


Figure 27. V_{IN} Power Up and Power Down

8.3 Do's and Don'ts

For best transient performance, place at least one 0.1-µF ceramic capacitor as close as possible to the OUT pin of the regulator and at least one 1-uF capacitor as close as possible to the IN pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not continuously operate the device in current limit or near thermal shutdown.

9 Power-Supply Recommendations

These devices are designed to operate from an input voltage supply range from 1.4 V to 5.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

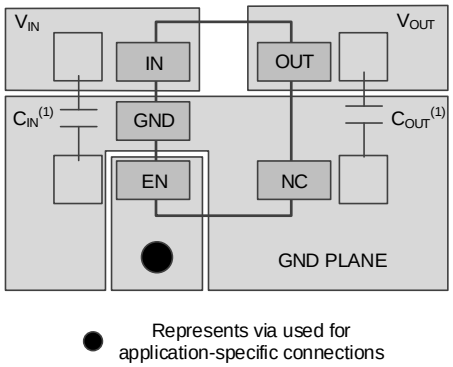
10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors must be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. High-ESR capacitors may degrade PSRR performance.

10.2 Layout Example



(1) Not required.

Figure 28. SOT-23 Layout Example

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 3.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (3)$$

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, as discussed in the table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 4.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \quad (4)$$

where

- P_D is the power dissipation shown by Equation 3,
- T_T is the temperature at the center-top of the device package,
- T_B is the PCB temperature measured 1 mm away from the device package *on the PCB surface*.

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

有三个评估模块 (EVM) 可与 TLV713P-Q1 配套使用，帮助评估初始电路性能：

- TLV71312PEVM-171
- TLV71318PEVM-171
- TLV71333PEVM-171

这些 EVM 预装有采用 DQN 封装的商业版器件，不过可以用于参数评估。 这些 EVM 可从德州仪器 (TI) 网站上的器件产品文件夹获取，也可直接从 TI 网上商店购买。

11.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。 您可以从产品文件夹中的*工具和软件*下获取 TLV713P-Q1 的 SPICE 模型。

11.1.2 器件命名规则

表 **4.** 订购信息(1) (2)

产品	V_{OUT}
TLV713P**xx**P**Q**yyyz**Q1**	**xx** 为标称输出电压。 对于分辨率为 100mV 的输出电压，订货编号中使用两位数字（例如，28 = 2.8V）。 **P** 为可选项；P 表示器件具有一个带有源输出放电功能的 LDO 稳压器。 **yyy** 为封装标识符。 **z** 为封装数量。 R 表示卷（3000 片），T 表示带（250 片）。

(1) 要获得最新的封装和订货信息，请参见本文档末尾的封装选项附录，或者访问器件产品文件夹（www.ti.com）。
(2) 可提供 1.0V 至 3.3V 范围内的输出电压（以 50mV 为单位增量）。 更多详细信息及可用性，请联系制造商。

11.2 文档支持

11.2.1 相关文档

- *《使用新的热指标》*，SBVA025
- *《TLV713xxEVM-171 用户指南》*，SLVU771

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序 ，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71310PQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBGW	Samples
TLV71312PQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBHW	Samples
TLV71318PQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBIW	Samples
TLV71325PQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBJW	Samples
TLV71333PQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBKW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

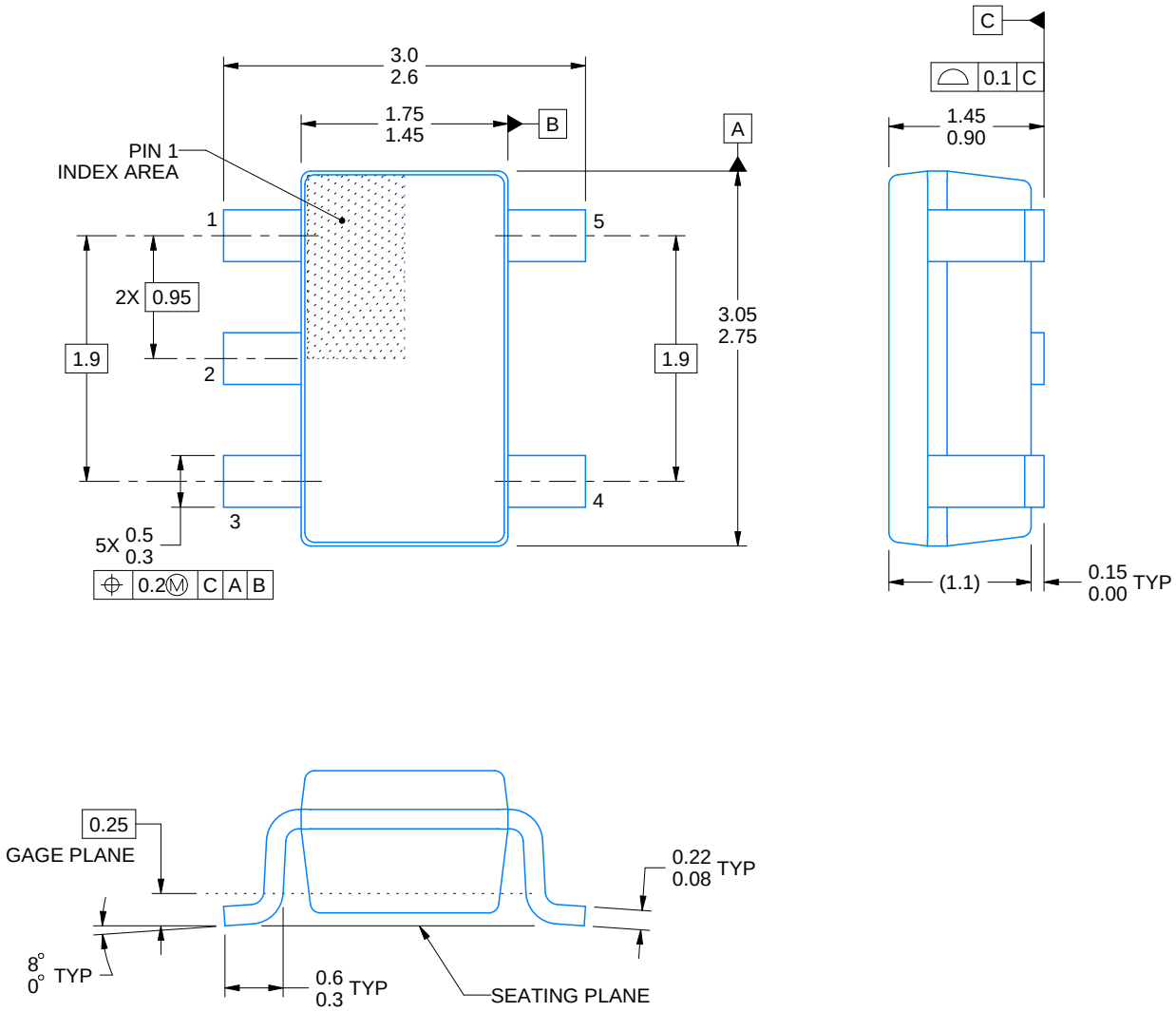
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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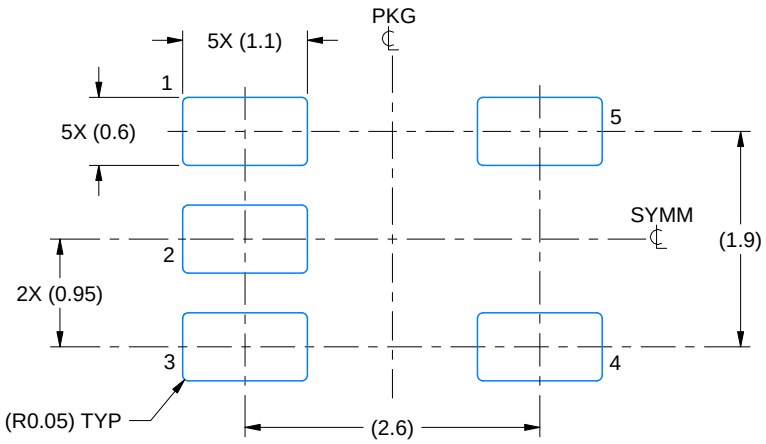
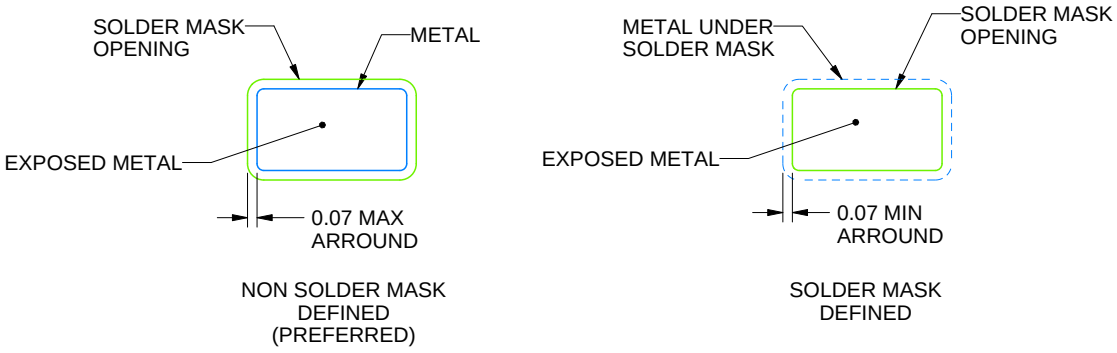
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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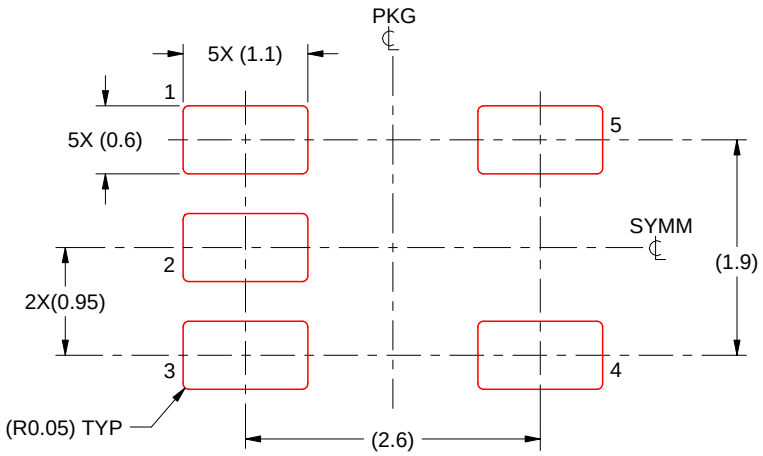
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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