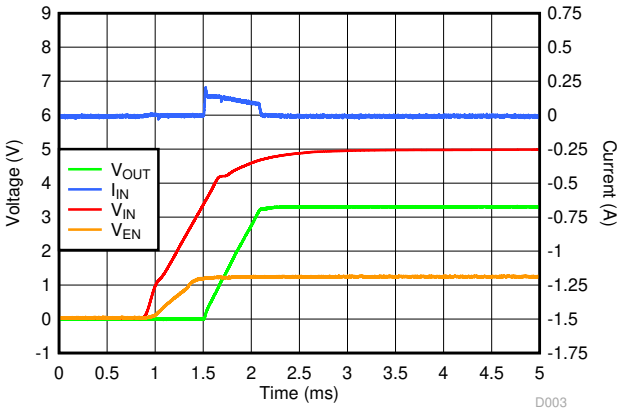
TLV767 1A、16V 精密线性稳压器

1 特性

- V_{IN}：2.5V 至 16V
- V_{OUT}：
  - 0.8V 至 14.6V（可调节）
  - 0.8V 至 6.6V（固定值，50mV 阶跃）
- 在整个负载和温度范围内的输出精度为 1%
- 低 I_Q：50μA（典型值，关断时约 1.5μA）
- 内部软启动时间：500μs（典型值）
- 折返电流限制和热保护
- 使用 1μF 陶瓷电容器实现稳定工作
- 高 PSRR：1kHz 频率下为 70dB，1MHz 频率下为 46dB
- 温度范围：–40°C 至 +125°C
- 封装：
  - 6 引脚 2mm × 2mm WSON
  - 8 引脚 3mm x 3mm HVSSOP
  - 5 引脚 2.9mm x 1.6mm SOT-23

2 应用

- 电器
- 电视、监控器和机顶盒
- 运动检测器（PIR、uWave 等）
- 电机驱动器和控制板
- 打印机和 PC 外设
- Wi-Fi 接入点设备和路由器



C_{OUT} 为 22μF 时减小的浪涌电流

3 说明

TLV767 是一种宽输入范围的线性稳压器，支持 2.5V 至 16 V 的输入电压范围和高达 1A 的负载电流。输出范围为 0.8V 至 6.6V，在可调版本中输出最高可达 14.6 V。

此外，TLV767 的输出精度为 1%，可满足低压微控制器 (MCU) 和处理器的需求。

根据设计，TLV767 的 I_Q 比传统的宽输入电压稳压器低得多，因此该器件能够充分满足日益严格的待机功耗要求。禁用时，TLV767 仅消耗 1.5μA 的 I_Q。

内部软启动时间和折返电流限制可减小启动期间的浪涌电流，从而最大限度降低输入电容。

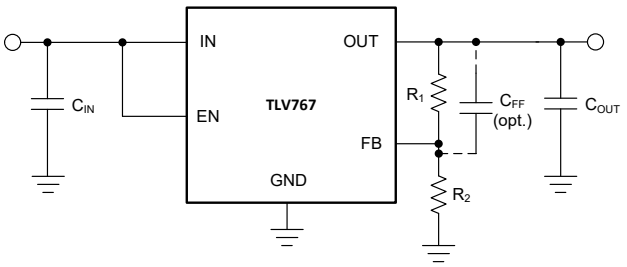
高带宽 PSRR 性能在 1kHz 时大于 70dB，在 1MHz 时大于 46dB，因此有助于衰减上游直流/直流转换器的开关频率，并最大限度减少后置稳压器滤波。为了提供更高的灵活性，TLV767 有固定电压和可调电压两种版本可供选用。

TLV767 可采用 6 引脚 2mm × 2mm WSON 封装、8 引脚 3mm x 3mm HVSSOP (DGN) 封装以及 5 引脚 2.9mm x 1.6mm SOT-23 (DBV) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV767	WSON (6)	2.00mm × 2.00mm
	HVSSOP (8)	3.00mm x 3.00mm
	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用电路

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (June 2020) to Revision D (July 2021)	Page
• 在文档中添加了 DBV (SOT-23) 封装	1
• 已将 VOUT 可调特性要点从 *0.8V 至 13.6V (可调)* 更改为 *0.8V 至 14.6V (可调)*	1
• 已将可调版本的最大输出范围从 *13.6V* 更改为 *14.6V*	1
• Added DBV pinout and pin information to *Pin Configuration and Functions* section	3
• Added *Layout Example for the Fixed DBV Version* figure to the *Layout Examples* section	24

Changes from Revision B (April 2019) to Revision C (June 2020)	Page
• 在文档中添加了 DGN (HVSSOP) 封装	1
• 更改了*应用* 部分	1
• Added DGN pinouts and pin information to *Pin Configuration and Functions* section	3
• Added HVSSOP thermal information	6
• Added *Layout Example for the Fixed HVSSOP Version* and *Layout Example for the Adjustable HVSSOP Version* figures to the *Layout Examples* section	24

5 Pin Configuration and Functions

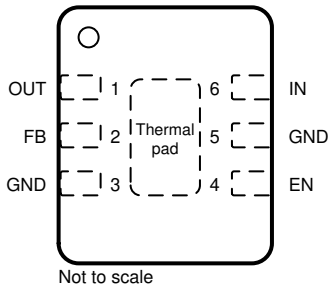


图 5-1. DRV Package (Adjustable), 6-Pin WSON, Top View

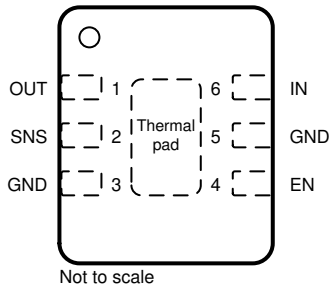


图 5-2. DRV Package (Fixed), 6-Pin WSON, Top View

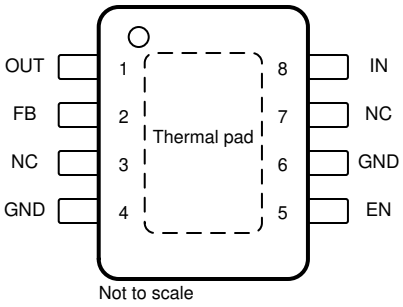


图 5-3. DGN Package (Adjustable), 8-Pin HVSSOP, Top View

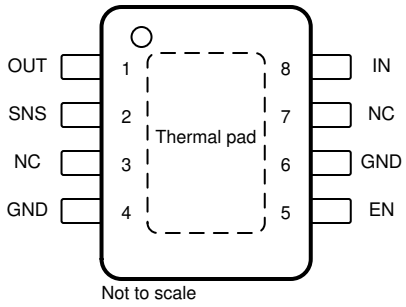


图 5-4. DGN Package (Fixed), 8-Pin HVSSOP, Top View

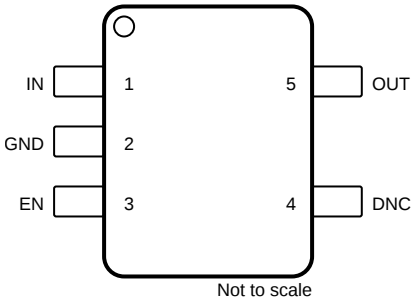


图 5-5. DBV Package (Fixed), 5-Pin SOT-23, Top View

表 5-1. Pin Functions

PIN						I/O	DESCRIPTION
NAME	DRV (Adj)	DRV (Fixed)	DGN (Adj)	DGN (Fixed)	DBV (Fixed)		
EN	4	4	5	5	3	I	Enable pin. Driving the enable pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. This pin has an internal pullup and can be left floating to enable the device or the pin can be connected to the input pin.
FB	2	—	2	—	—	I	Feedback pin. Input to the control-loop error amplifier. This pin is used to set the output voltage of the device with the use of external resistors. Do not float this pin. For adjustable-voltage version devices only.
GND	3, 5	3, 5	4, 6	4, 6	2	—	Ground pin. All ground pins must be grounded.
DNC	—	—	—	—	4	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating
IN	6	6	8	8	1	I	Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUT	1	1	1	1	5	O	Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
SNS	—	2	—	2	—	I	Output sense pin. Connect the SNS pin to the OUT pin, or to remotely sense the output voltage at the load, connect the SNS pin to the load. Do not float this pin. For fixed-voltage version devices only.
Thermal pad	Pad	Pad	Pad	Pad	—	—	Exposed pad of the package. Connect this pad to ground or leave floating. Connect the thermal pad to a large-area ground plane for best thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	V_{IN}	–0.3	18	V
	V_{OUT} (3)	–0.3	V_{IN} + 0.3	
	V_{SNS} (3)	–0.3	V_{IN} + 0.3	
	V_{FB}	–0.3	3	
	V_{EN}	–0.3	18	
Current	Maximum output current	Internally Limited		A
Temperature	Operating junction (T_J)	–50	150	°C
	Storage (T_{STG})	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.
(3) V_{IN} + 0.3 V or 18 V (whichever is smaller)

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		16	V
V_{EN}	Enable voltage	0		16	V
V_{OUT}	Output voltage	0.8		14.6	V
I_{OUT}	Output current (2.5 V ≤ V_{IN} < 3 V)	0		0.8	A
I_{OUT}	Output current (V_{IN} ≥ 3 V)	0		1	A
C_{OUT}	Output capacitor(1)	1	2.2	220	µF
C_{OUT} ESR	Output capacitor ESR	2		500	mΩ
C_{IN}	Input capacitor		1		µF
C_{FF}	Feed-forward capacitor (optional(2), for adjustable device only)		10		pF
$I_{FB\_DIVIDER}$	Feedback divider current(2) (adjustable device only)	5			µA
T_J	Junction temperature	–40		125	°C

(1) Effective output capacitance of 0.5 µF minimum required for stability.
(2) C_{FF} required for stability if the feedback divider current < 5 µA. Feedback divider current = V_{OUT} / (R_1 + R_2). See *Feed-Forward Capacitor (C_{FF})* section for details.

6.4 Thermal Information

THERMAL METRIC[1]		TLV767			UNIT
		DBV (SOT23)	DGN (HVSSOP)	DRV (WSON)	
		5 PINS	8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.7	60.1	77.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	81.7	92.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.9	32.8	40.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.6	6	4.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.6	32.7	40.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	15.5	18.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.5 V or V_{IN} = 2.5 V (whichever is greater), FB/SNS tied to OUT, I_{OUT} = 10 mA, V_{EN} = 2 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF (unless otherwise noted). Typical values are at T_J= 25ºC.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Nominal output accuracy	T_J = 25°C	–0.5		0.5	%
V_{OUT}	Output accuracy over temperature	$V_{IN} \geq$ 3.0 V, 1 mA $\leq I_{OUT} \leq$ 1 A	–1		1	%
		2.5 V $\leq V_{IN}$ < 3.0 V, 1 mA $\leq I_{OUT} \leq$ 800 mA	–1		1	
V_{FB}	Feedback voltage			0.8		V
V_{REF}	Internal reference (adjustable device)	T_J = 25ºC	–0.5		0.5	%
			–1		1	
I_{FB}	Feedback pin current	V_{FB} = 1 V		10	50	nA
$\Delta V_{OUT}(\Delta VIN)$	Line regulation[1]	$V_{OUT(NOM)}$ +1.5 V $\leq V_{IN} \leq$ 16 V, I_{OUT} = 10 mA			0.02	%/V
$\Delta V_{OUT}(\Delta IOUT)$	Load regulation	1 mA $\leq I_{OUT} \leq$ 1 A, $V_{IN} \geq$ 3.0 V		0.1	0.5	%/A
		1 mA $\leq I_{OUT} \leq$ 800 mA, 2.5 V $\leq V_{IN}$ < 3.0 V		0.1	0.5	
V_{DO}	Dropout voltage[2]	$V_{IN} \geq$ 3.0V, I_{OUT} = 1 A, DGN package		0.9	1.5	V
		$V_{IN} \geq$ 3.0V, I_{OUT} = 1 A, DRV package		0.9	1.4	
		2.5 V $\leq V_{IN}$ < 3.0 V, I_{OUT} = 800 mA		0.8	1.3	
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, $V_{IN} \geq$ 3.0V	1.1		1.6	A
		V_{OUT} = 0.9 x $V_{OUT(NOM)}$, 2.5 V $\leq V_{IN}$ < 3.0 V	0.81		1.6	
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V, DGN package		250		mA
		V_{OUT} = 0 V, DRV package	150	250	350	mA
I_Q	Quiescent current	I_{OUT} = 0 mA		50	80	µA
		Fixed output devices, I_{OUT} = 0 mA		60	95	
I_{GND}	Ground current	I_{OUT} = 1 A, $V_{IN} \geq$ 3.0 V		1.5		mA
$I_{SHUTDOWN}$	Shutdown current	$V_{EN} \leq$ 0.4 V, V_{IN} = 16 V		1.5	3	µA
$V_{EN(HIGH)}$	Enable pin logic high	2.5 V $\leq V_{IN} \leq$ 16 V	1.2			V
$V_{EN(LOW)}$	Enable pin logic low	2.5 V $\leq V_{IN} \leq$ 16 V			0.4	V
I_{EN}	Enable pullup current	V_{EN} = 0 V		400		nA
$I_{PULLDOWN}$	Output pulldown current	V_{IN} = 16 V, V_{OUT} = 2.5 V, V_{EN}=0V		1.2		mA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 300 mA, f = 120 Hz		70		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 3.3 V, V_{OUT} = 0.8 V, I_{OUT} = 100 mA		60		μV_{RMS}
V_{UVLO+}	UVLO threshold rising	V_{IN} rising		2.2	2.4	V

6.5 Electrical Characteristics (continued)

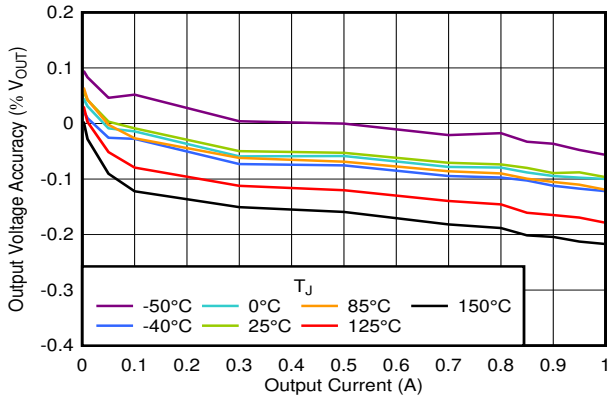
Specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.5 V or V_{IN} = 2.5 V (whichever is greater), FB/SNS tied to OUT, I_{OUT} = 10 mA, V_{EN} = 2 V, C_{IN} = 1.0 µF, C_{OUT} = 1.0 µF (unless otherwise noted). Typical values are at T_J= 25ºC.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(HYS)}$	UVLO hysteresis			130		mV
V_{UVLO-}	UVLO threshold falling	V_{IN} falling	1.9			V
$T_{SD(shutdown)}$	Thermal shutdown temperature	Temperature increasing		180		ºC
$T_{SD(reset)}$	Thermal shutdown reset temperature	Temperature falling		160		ºC

(1) Line regulation is measured with V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater)
(2) V_{DO} is measured with V_{IN} = 95% x $V_{OUT(nom)}$ for fixed output devices. V_{DO} is not measured for fixed output devices when V_{OUT} < 2.5 V. For adjustable output device, V_{DO} is measured with V_{FB} = 95% x $V_{FB(nom)}$

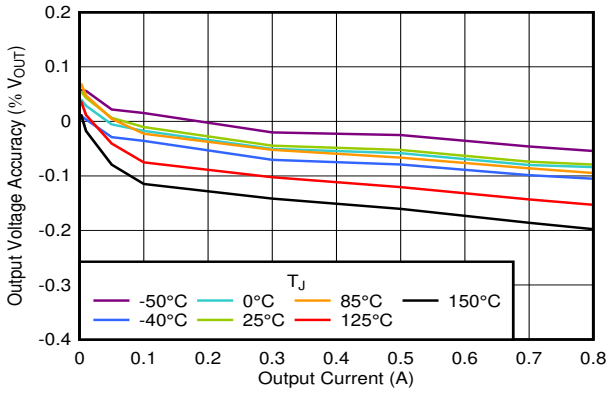
7 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



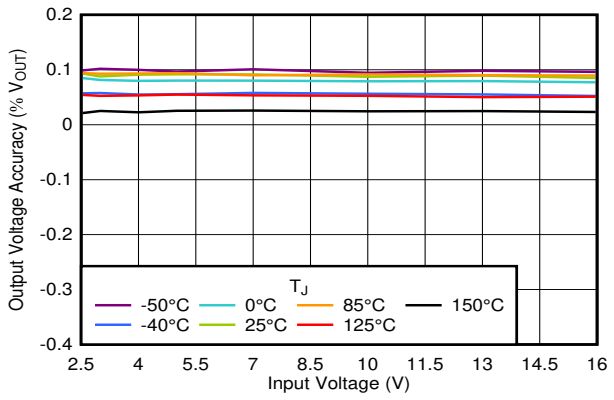
V_{IN} = 3.0 V

图 7-1. V_{OUT} Accuracy vs I_{OUT}



V_{IN} = 2.5 V

图 7-2. V_{OUT} Accuracy vs I_{OUT}



I_{OUT} = 10 mA

图 7-3. V_{OUT} Accuracy vs V_{IN}

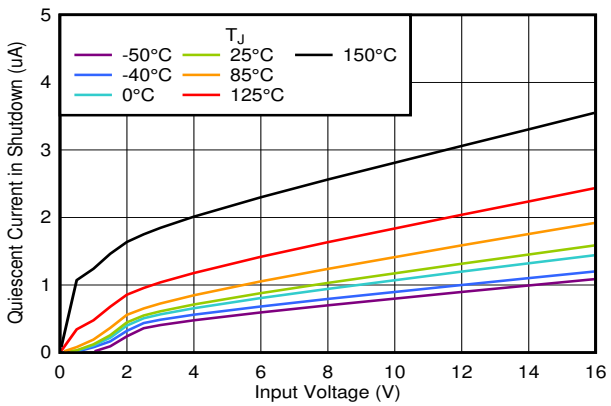
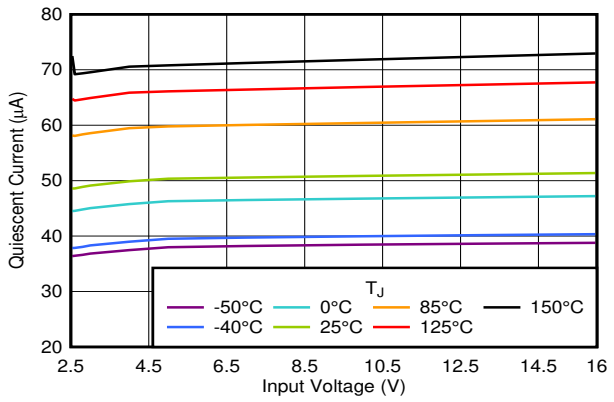
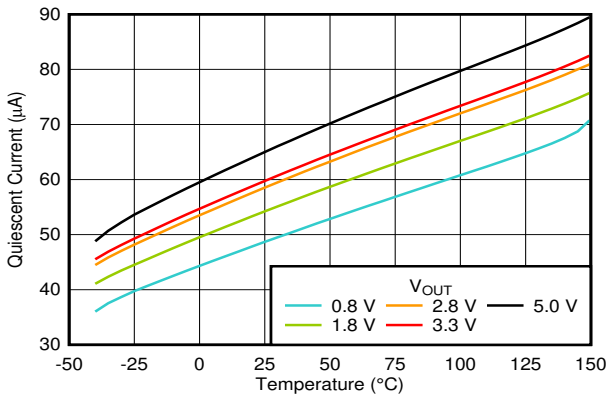


图 7-4. $I_{SHUTDOWN}$ vs V_{IN}



I_{OUT} = 0 mA, adjustable-voltage version devices

图 7-5. I_Q vs V_{IN}

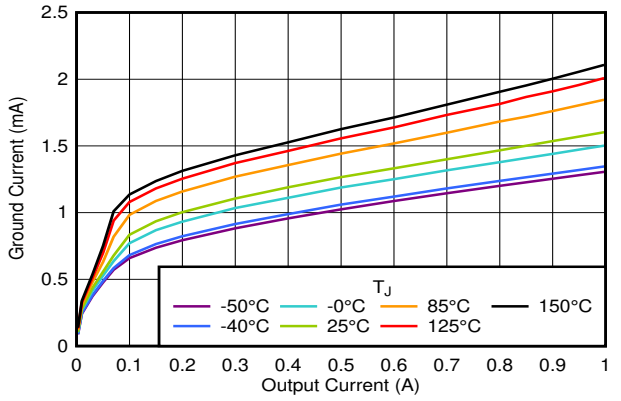


I_{OUT} = 0 mA, fixed-voltage version devices

图 7-6. I_Q vs Temperature

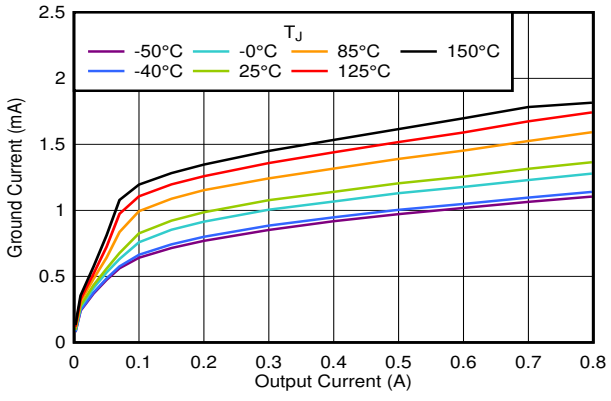
7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



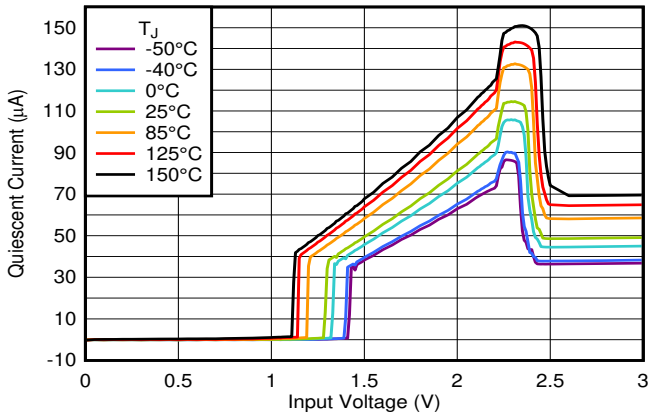
V_{IN} = 3.0 V

图 7-7. I_{GND} vs I_{OUT}



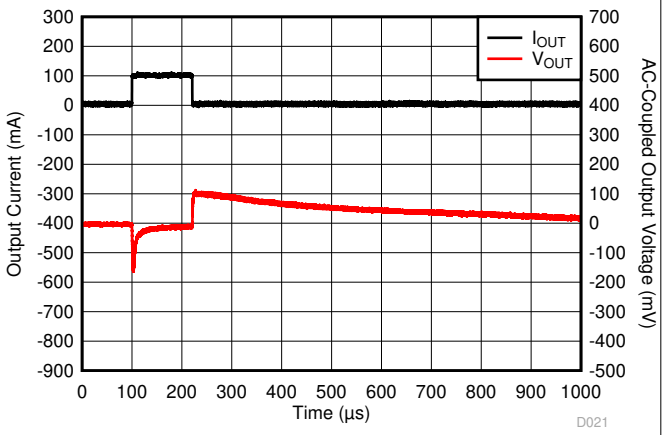
V_{IN} = 2.5 V

图 7-8. I_{GND} vs I_{OUT}



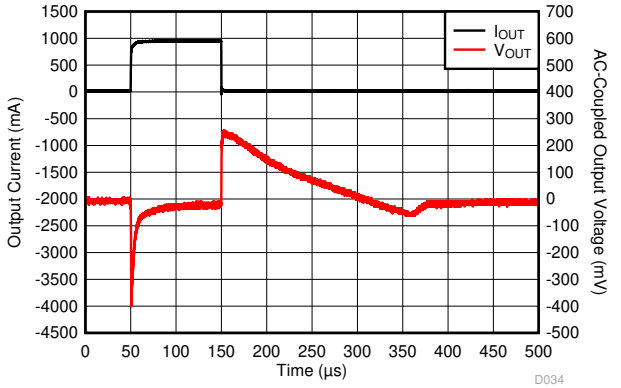
I_{OUT} = 0 mA

图 7-9. I_Q Increase Below Minimum V_{IN}



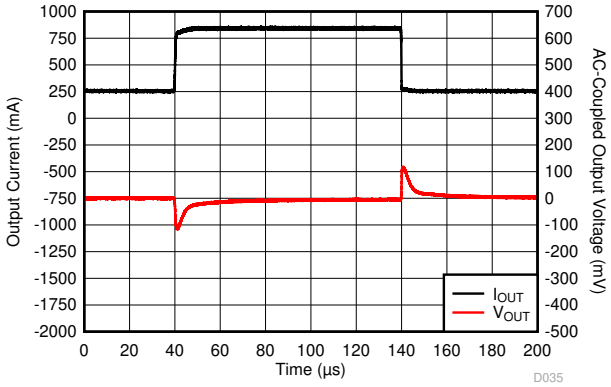
V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{FF} = 10 pF, ramp rate = 0.4 A/µs

图 7-10. I_{OUT} Transient From 0 mA to 100 mA



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{FF} = 10 pF, ramp rate = 0.5 A/µs

图 7-11. I_{OUT} Transient From 1 mA to 1 A

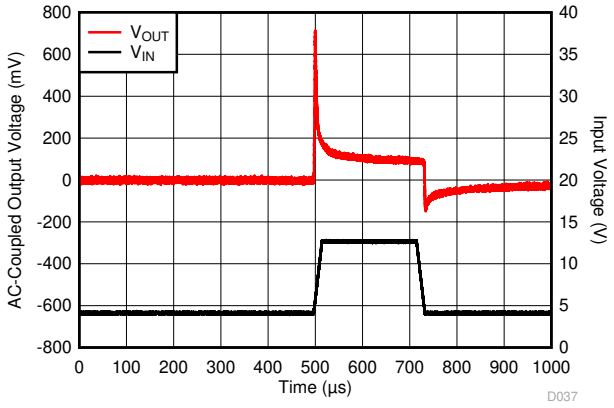


V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.8 A/µs

图 7-12. I_{OUT} Transient From 250 mA to 850 mA

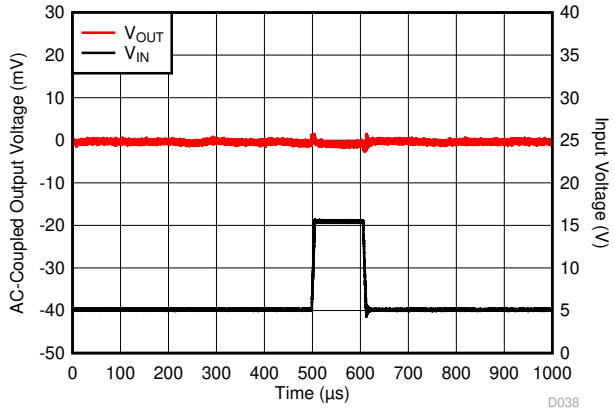
7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



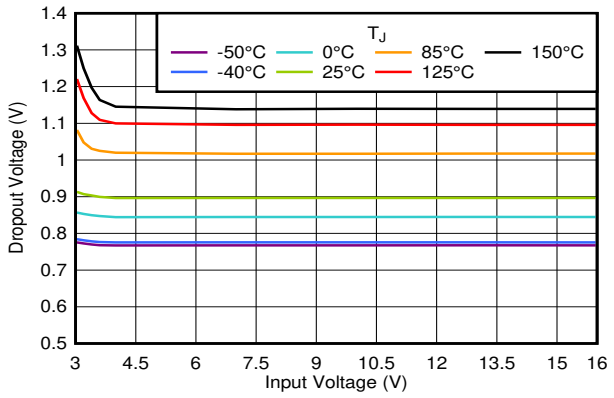
V_{OUT} = 3.3 V, I_{OUT} = 1 A, V_{IN} ramp rate = 0.6 V/µs

图 7-13. V_{IN} Transient in Dropout From 4 V to 13 V



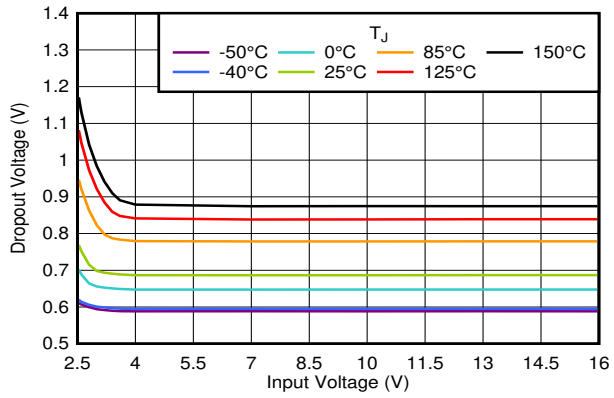
V_{OUT} = 3.3 V, I_{OUT} = 33 µA, V_{IN} ramp rate = 1.6 V/µs

图 7-14. V_{IN} Transient From 5 V to 16 V



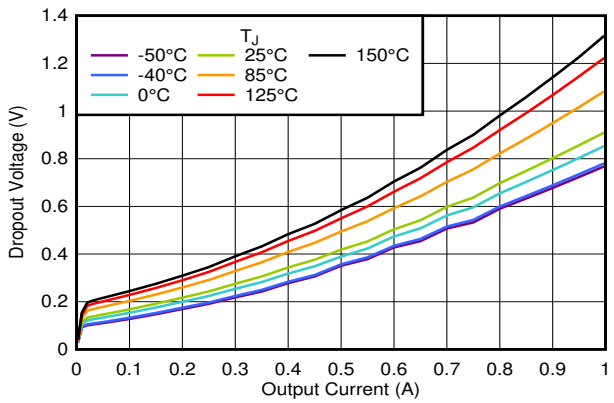
I_{OUT} = 1.0 A

图 7-15. V_{DO} vs V_{IN}



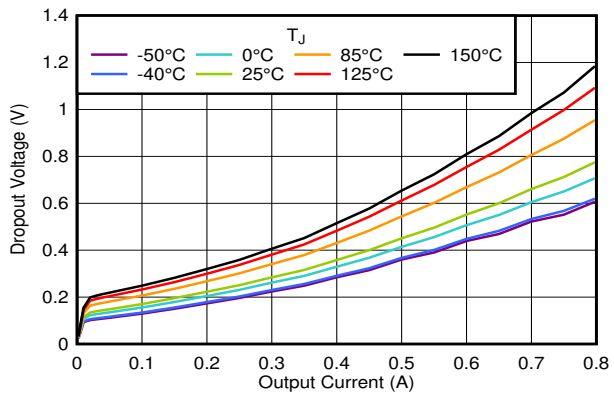
I_{OUT} = 0.8 A

图 7-16. V_{DO} vs V_{IN}



V_{IN} = 3.0 V

图 7-17. V_{DO} vs I_{OUT}

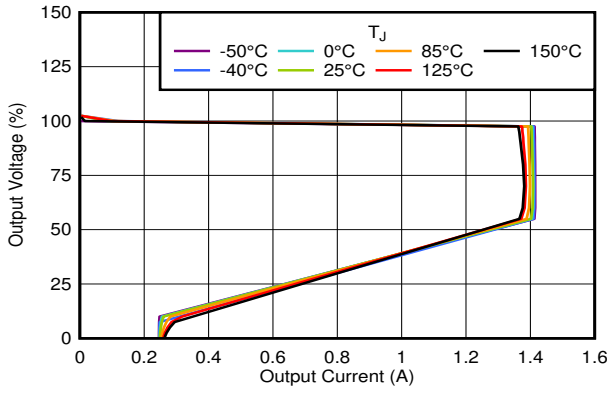


V_{IN} = 2.5 V

图 7-18. V_{DO} vs I_{OUT}

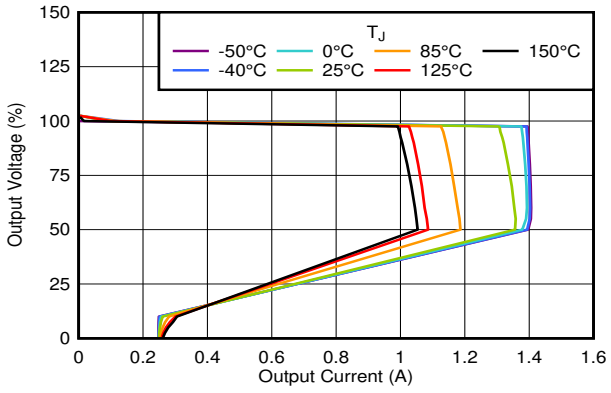
7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



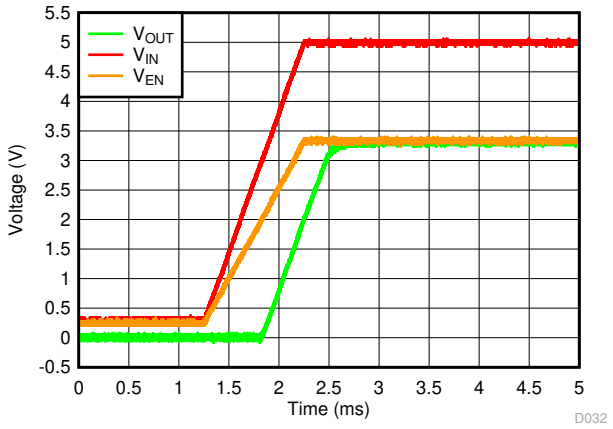
V_{IN} = 3.0 V

图 7-19. Foldback Current Limit vs Temperature



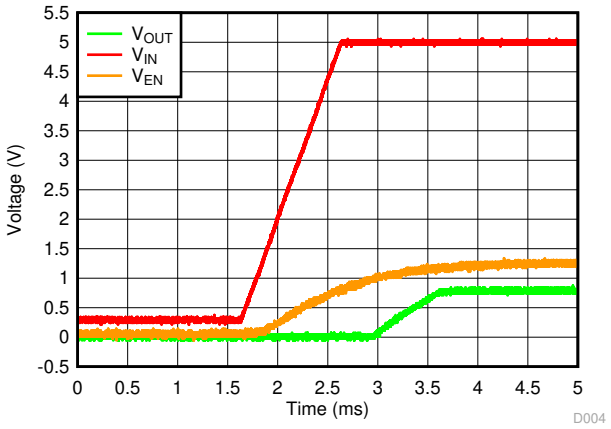
V_{IN} = 2.5 V

图 7-20. Foldback Current Limit vs Temperature



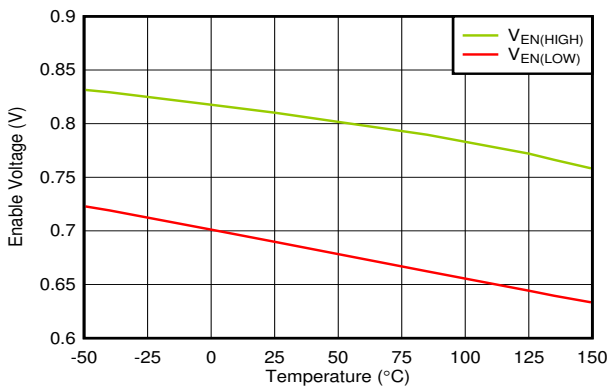
V_{OUT} = 3.3 V

图 7-21. Startup With Separate V_{EN} and V_{IN}



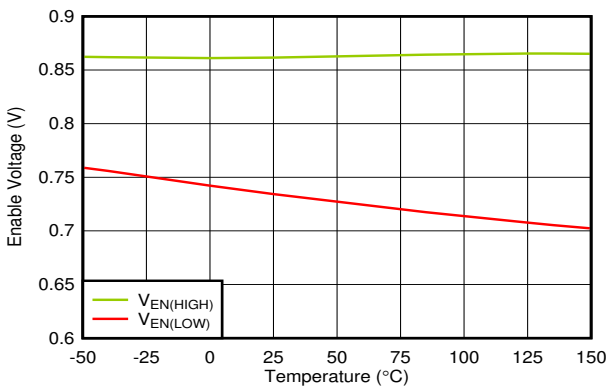
Enable pulled up internally, V_{OUT} = 0.8 V

图 7-22. Startup With V_{EN} Floating



V_{IN} = 2.5 V

图 7-23. V_{EN} Thresholds vs Temperature



V_{IN} = 16 V

图 7-24. V_{EN} Thresholds vs Temperature

7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)

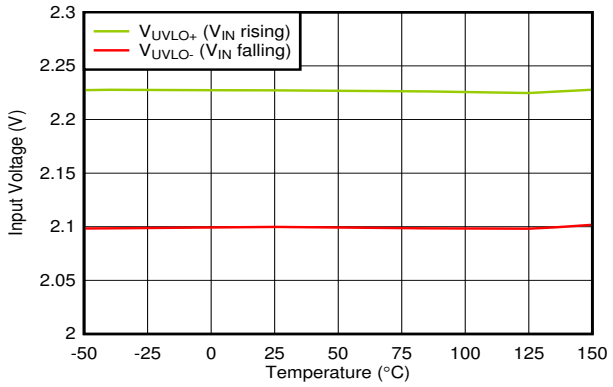
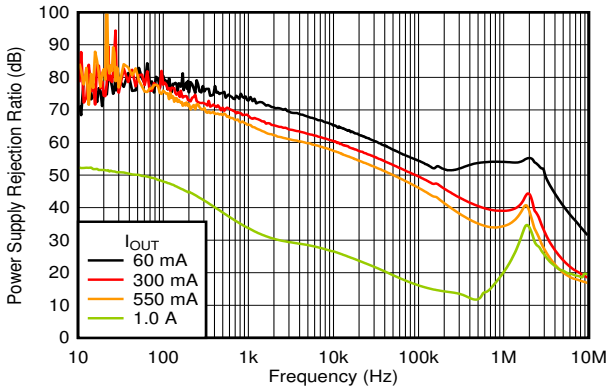
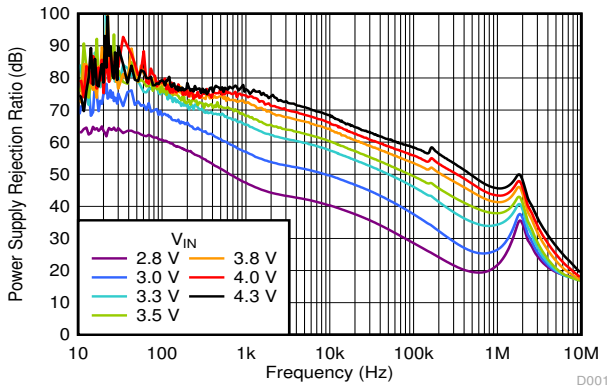


图 7-25. UVLO Thresholds vs Temperature



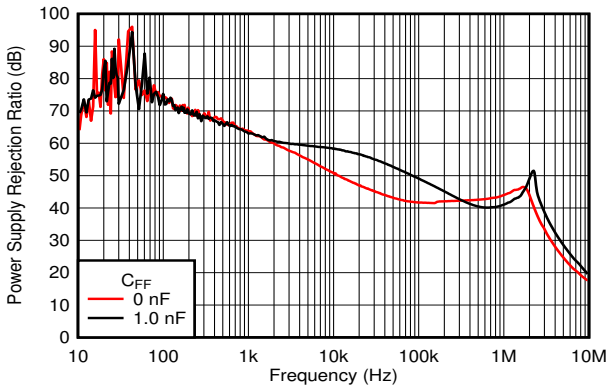
V_{OUT} = 1.8 V, V_{IN} = 3.3 V, C_{FF} = 1 nF

图 7-26. PSRR vs I_{OUT}



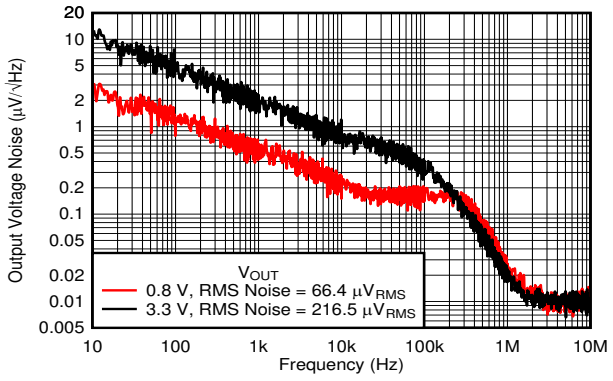
V_{OUT} = 1.8 V, I_{OUT} = 0.55 A, C_{FF} = 1 nF

图 7-27. PSRR vs V_{IN}



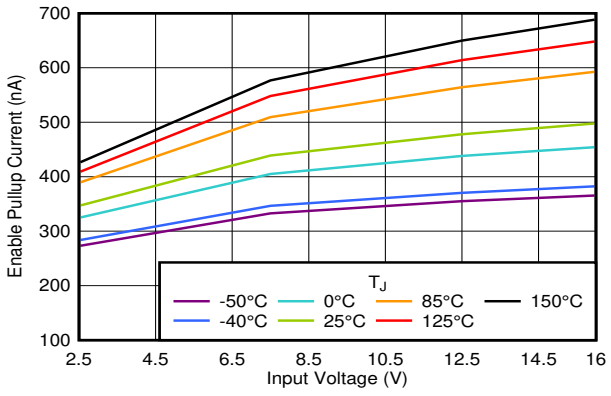
V_{OUT} = 3.3 V, V_{IN} = 4.8 V, I_{OUT} = 0.33 A

图 7-28. PSRR vs C_{FF}



C_{FF} = 0 nF, I_{OUT} = 0.1 A, RMS noise BW = 10 Hz to 100 kHz

图 7-29. Output Noise (V_n) vs V_{OUT}

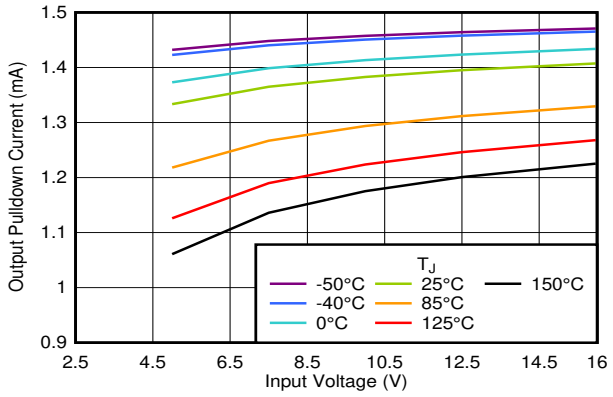


V_{EN} = 0 V

图 7-30. I_{EN} vs V_{IN}

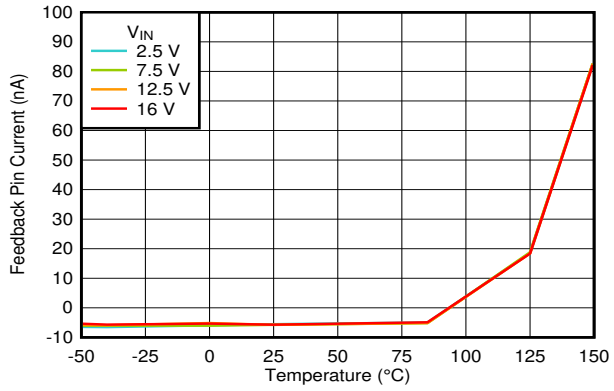
7 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



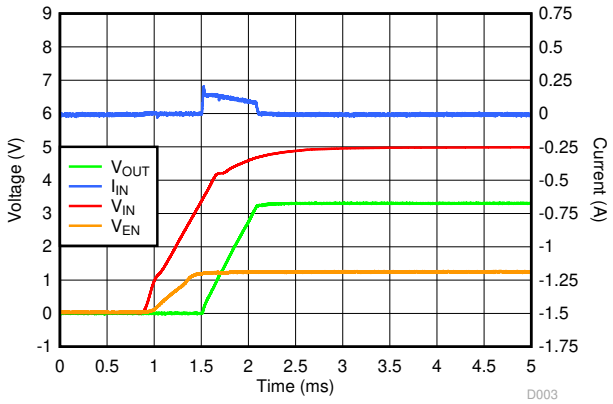
V_{OUT} = 2.5 V

图 7-31. $I_{PULLDOWN}$ vs V_{IN}



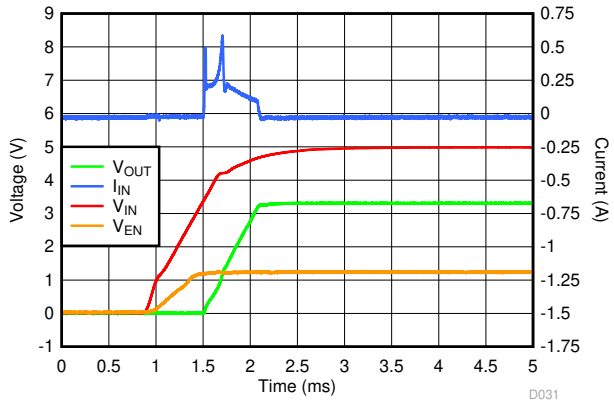
V_{FB} = 1.0 V

图 7-32. I_{FB} vs Temperature



V_{OUT} = 3.3 V, I_{OUT} = 33 µA

图 7-33. Startup Inrush Current With C_{OUT} = 22 µF



V_{OUT} = 3.3 V, I_{OUT} = 33 µA

图 7-34. Startup Inrush Current With C_{OUT} = 47 µF

8 Detailed Description

8.1 Overview

The TLV767 is a low quiescent current, high PSRR linear regulator capable of handling up to 1 A of load current. Unlike typical high current linear regulators, the TLV767 consumes significantly less quiescent current. This device is ideal for high current applications that require very sensitive power-supply rails.

This device features integrated foldback current limit, thermal shutdown, output enable, internal output pulldown and undervoltage lockout (UVLO). This device delivers excellent line and load transient performance. This device is low noise and exhibits a very good PSRR. The operating ambient temperature range of the device is –40°C to +125°C.

8.2 Functional Block Diagrams

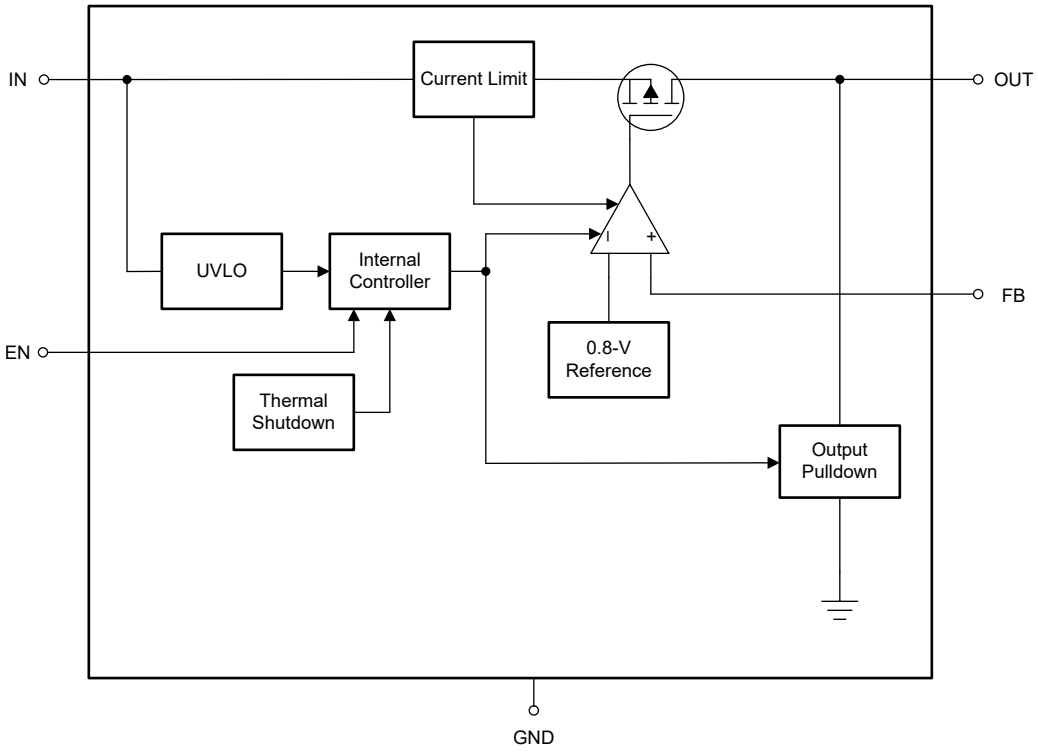


图 8-1. Adjustable Version Block Diagram

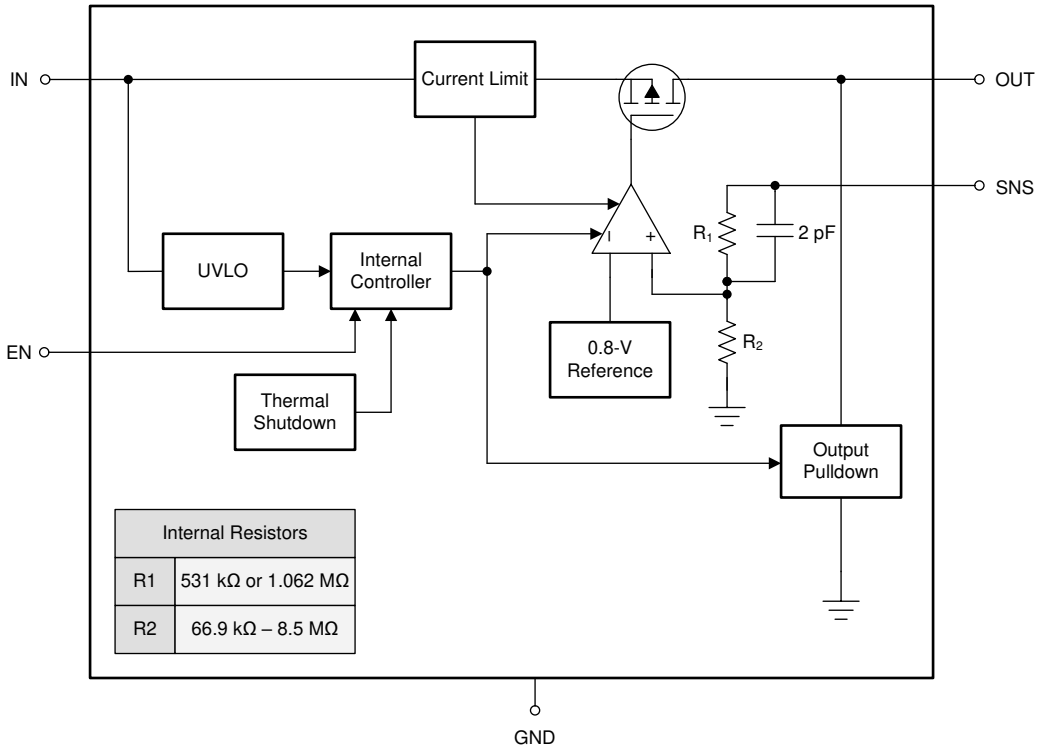


图 8-2. Fixed Version Block Diagram

8.3 Feature Description

8.3.1 Output Enable

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

This device has an internal pullup current on the EN pin. The EN pin can be left floating to enable the device.

The device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

8.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

8.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 50% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

图 8-3 shows a diagram of the foldback current limit.

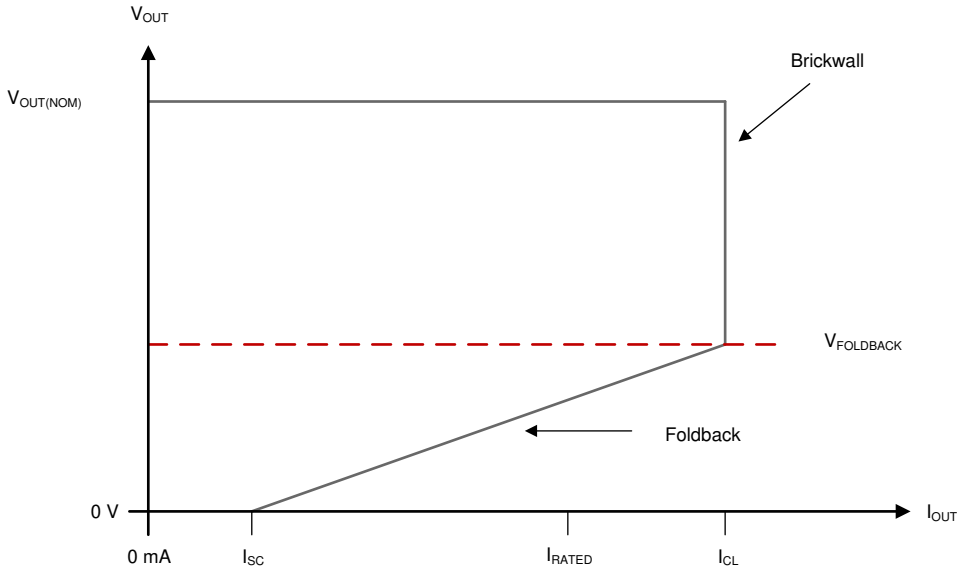


图 8-3. Foldback Current Limit

8.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

8.3.5 Output Pulldown

The device has an output pulldown circuit. V_{OUT} pulldown sink to ground capability is listed in the *Electrical Characteristics* table. The output pulldown activates under the following conditions:

- Device disabled
- 1.0 V < V_{IN} < V_{UVLO}

The output pulldown current for this device is 1.2 mA typical, as listed in the *Electrical Characteristics* table.

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

8.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

8.4 Device Functional Modes

8.4.1 Device Functional Mode Comparison

表 8-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 8-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

8.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

8.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

8.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leqslant V_{OUT} / (I_{FB} \times 100) \quad (3)$$

9.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

9.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

9.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leqslant V_{IN}$ + 0.3 V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

图 9-1 shows one approach for protecting the device.

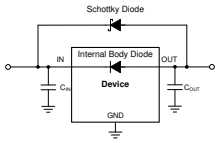


图 9-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

9.1.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geq 10$ pF is required for stability if the feedback divider current is less than 5 µA. 方程式 6 calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50$ µs.

For an output voltage of 0.8 V with the FB pin tied to the OUT pin, no C_{FF} is used.

9.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (7)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the

junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

9.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report.

9.2 Typical Application

This section discusses implementing this device for a typical application. 图 9-2 shows the application circuit.

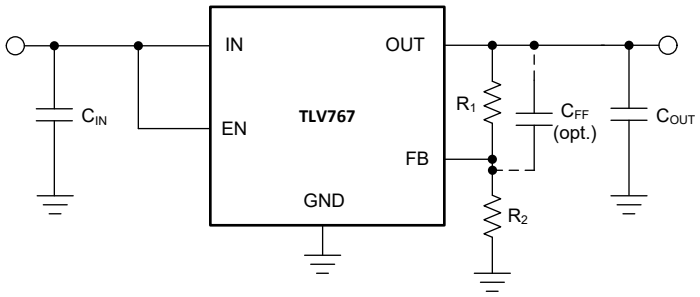


图 9-2. Typical Application Circuit

9.2.1 Design Requirements

表 9-1 summarizes the design requirements for this application.

表 9-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	5 V
Output voltage	3.3 V
Output current	100 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude. If load transients are expected with ramp rates greater than 0.5 A/µs, use a 2.2-µF or larger output capacitor.

9.2.2.2 Choose Feedback Resistors

For this design example, V_{OUT} is set to 3.3 V. 方程式 11 and 方程式 12 set the feedback divider resistors for the desired output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (11)$$

$$R_1 + R_2 \leqslant V_{OUT} / (I_{FB} \times 100) \quad (12)$$

For improved output accuracy, use 方程式 12 and I_{FB} = 50 nA as listed in the *Electrical Characteristics* table to calculate the upper limit for series feedback resistance ($R_1 + R_2 \leqslant 660$ kΩ).

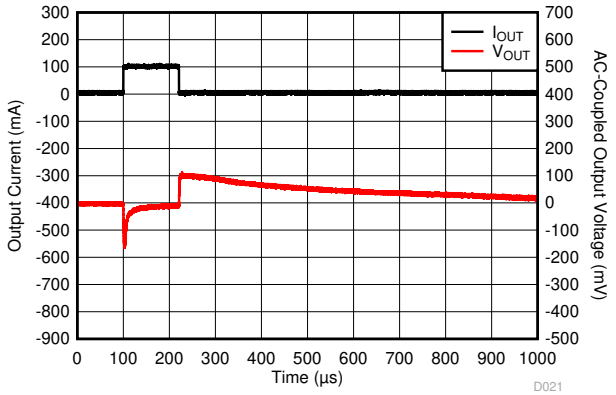
The control-loop error amplifier drives the FB pin to the same voltage as the internal reference (V_{FB} = 0.8 V, as listed in the *Electrical Characteristics* table). Use 方程式 11 to determine the ratio of $R_1 / R_2 = 3.125$. Use this ratio and solve 方程式 12 for R_2. Now calculate the upper limit for $R_2 \leqslant 160$ kΩ. Select a standard value resistor for R_2 = 160 kΩ.

Reference 方程式 11 and solve for R_1:

$$R_1 = (V_{OUT} / V_{FB} - 1) \times R_2 \quad (13)$$

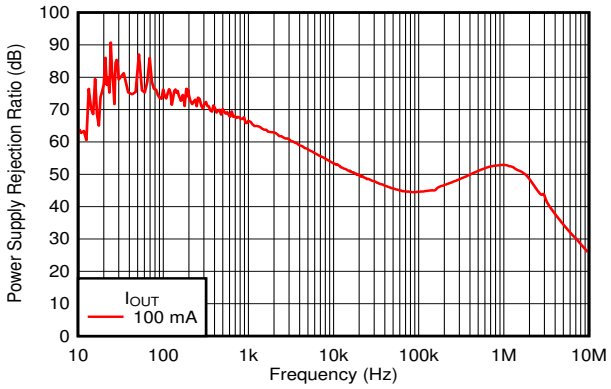
From 方程式 13, R_1 = 500 kΩ can be determined. Select a standard value resistor for R_1 = 499 kΩ. V_{OUT} = 3.3 V (as determined by 方程式 11).

9.2.3 Application Curves



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF, C_{FF} = 10 pF

图 9-3. Load Transient Response, I_{OUT} 0 mA to 100 mA



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF, C_{FF} = 0 pF

图 9-4. PSRR Performance

10 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.5 V to 16 V. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 1.5 V. For 1-A output current operation, the input supply must be 3 V or greater. Connect a low output impedance power supply directly to the input pin of the TLV767.

11 Layout

11.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible
- Use copper planes for device connections to IN, OUT, and GND pins to optimize thermal performance
- Place thermal vias around the device to distribute heat

11.2 Layout Examples

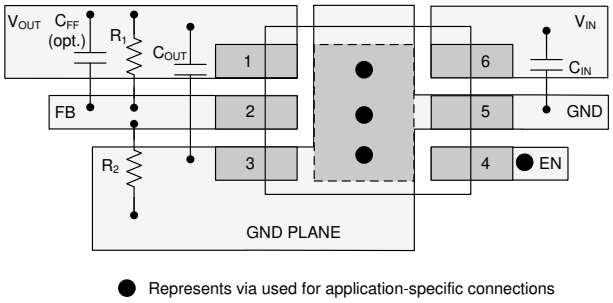


图 11-1. Layout Example for the Adjustable WSON Version

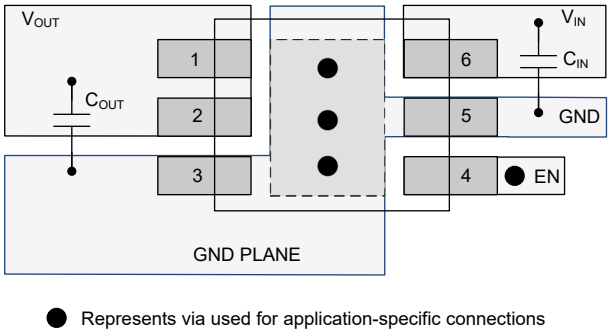


图 11-2. Layout Example for the Fixed WSON Version

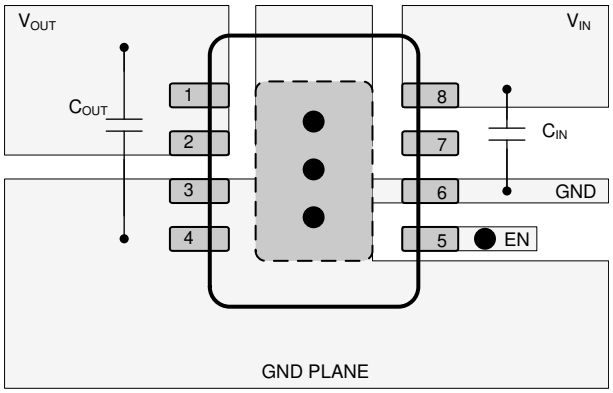


图 11-3. Layout Example for the Fixed HVSSOP Version

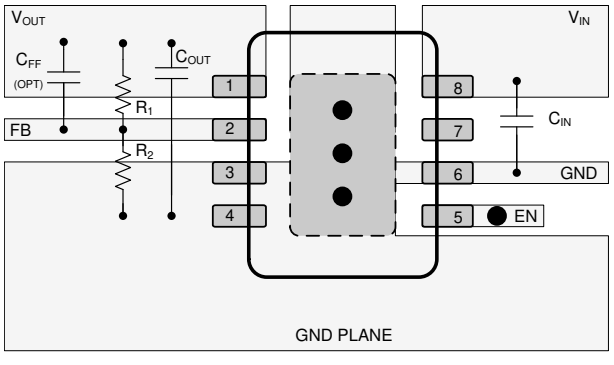


图 11-4. Layout Example for the Adjustable HVSSOP Version

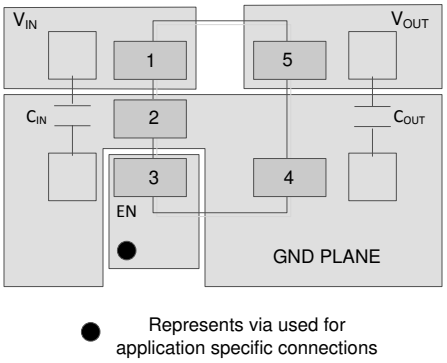


图 11-5. Layout Example for the Fixed DBV Version

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

表 12-1. Available Options[1]

PRODUCT	V_{OUT}
TLV767**xx(x)yyyz**	**xx(x)** is nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 33 = 3.3 V; 125 = 1.25 V). 01 indicates adjustable output version. **yyy** is package designator. **z** is package quantity. R is for large quantity reel, T is for small quantity reel.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLV767EVM-014 Evaluation module* user's guide
- Texas Instruments, *Pros and cons of using a feedforward capacitor with a low-dropout regulator* application report
- Texas Instruments, *Know your limits* application report
- Texas Instruments, *Universal low-dropout (LDO) linear voltage regulator MultiPkgLDOEVM-823 evaluation module* user's guide

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV76701DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2BKX	Samples
TLV76701DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RMH	Samples
TLV76701DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1RMH	Samples
TLV76708DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2BLX	Samples
TLV76708DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1RNH	Samples
TLV76708DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1RNH	Samples
TLV76718DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2BMX	Samples
TLV76718DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1ROH	Samples
TLV76718DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1ROH	Samples
TLV76725DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2GT7	Samples
TLV76728DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2BNX	Samples
TLV76728DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1RPH	Samples
TLV76728DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1RPH	Samples
TLV76733DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2BOX	Samples
TLV76733DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1RQH	Samples
TLV76733DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1RQH	Samples
TLV76750DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2BPX	Samples
TLV76750DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1RRH	Samples
TLV76750DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1RRH	Samples
TLV76780DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2D2T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV767 :

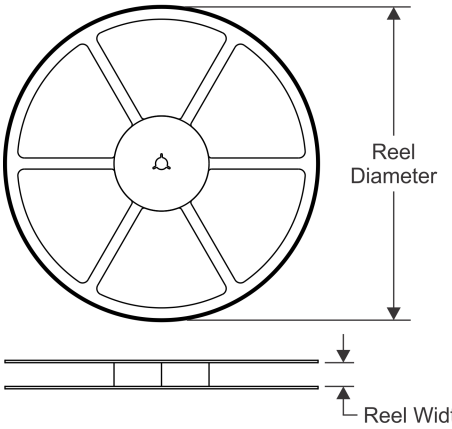
- Automotive : TLV767-Q1

NOTE: Qualified Version Definitions:

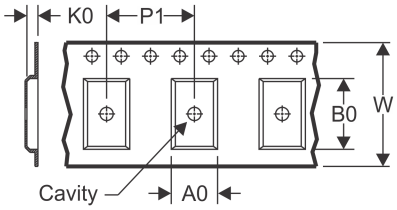
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

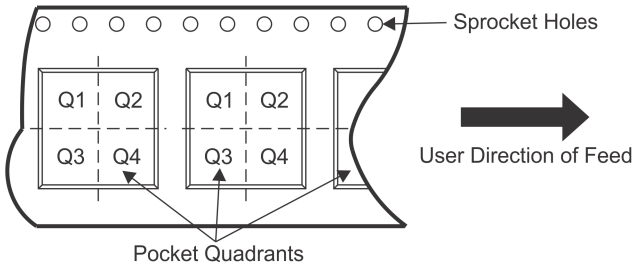


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

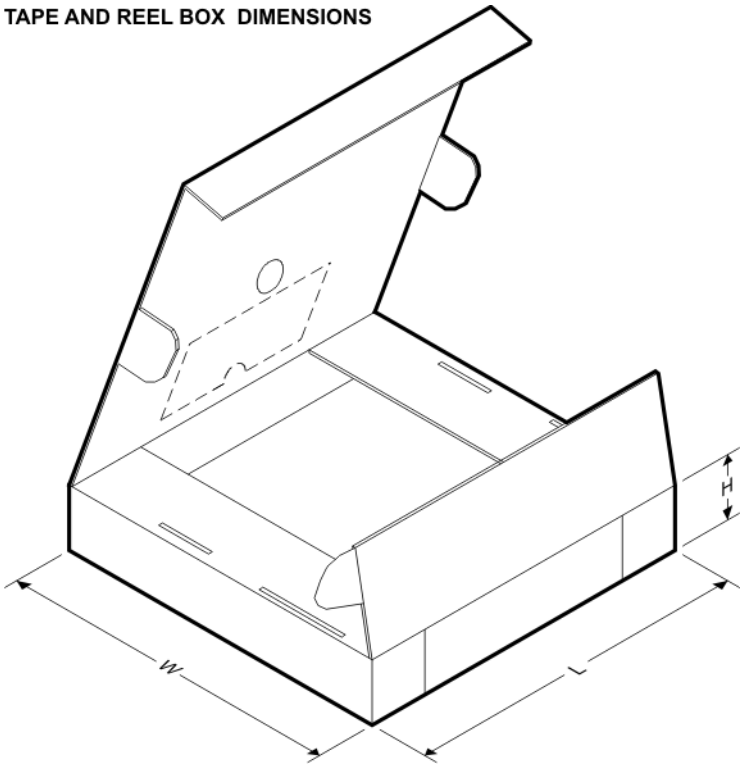


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV76701DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV76701DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76701DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76708DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV76708DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76708DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TLV76708DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76708DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TLV76718DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV76718DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76718DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TLV76718DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TLV76718DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76725DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV76728DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV76728DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TLV76728DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76728DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV76728DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76733DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV76733DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TLV76733DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76733DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TLV76733DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76750DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV76750DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76750DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TLV76750DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TLV76750DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV76780DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV76701DGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TLV76701DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV76701DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TLV76708DGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TLV76708DRVR	WSON	DRV	6	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV76708DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TLV76708DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TLV76708DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TLV76718DGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TLV76718DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV76718DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TLV76718DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TLV76718DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TLV76725DGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TLV76728DGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TLV76728DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TLV76728DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV76728DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TLV76728DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TLV76733DGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TLV76733DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TLV76733DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV76733DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TLV76733DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TLV76750DGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TLV76750DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV76750DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TLV76750DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TLV76750DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TLV76780DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

GENERIC PACKAGE VIEW

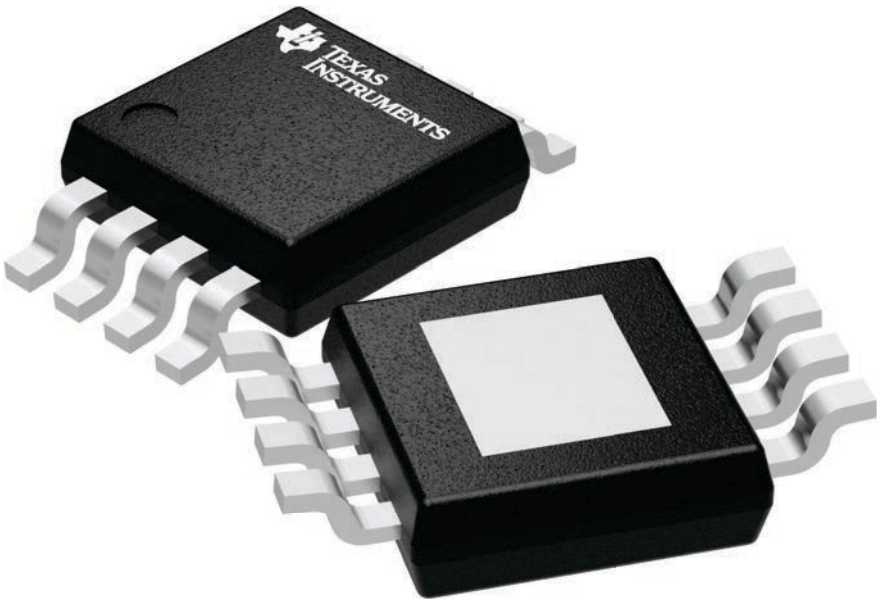
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

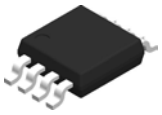
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

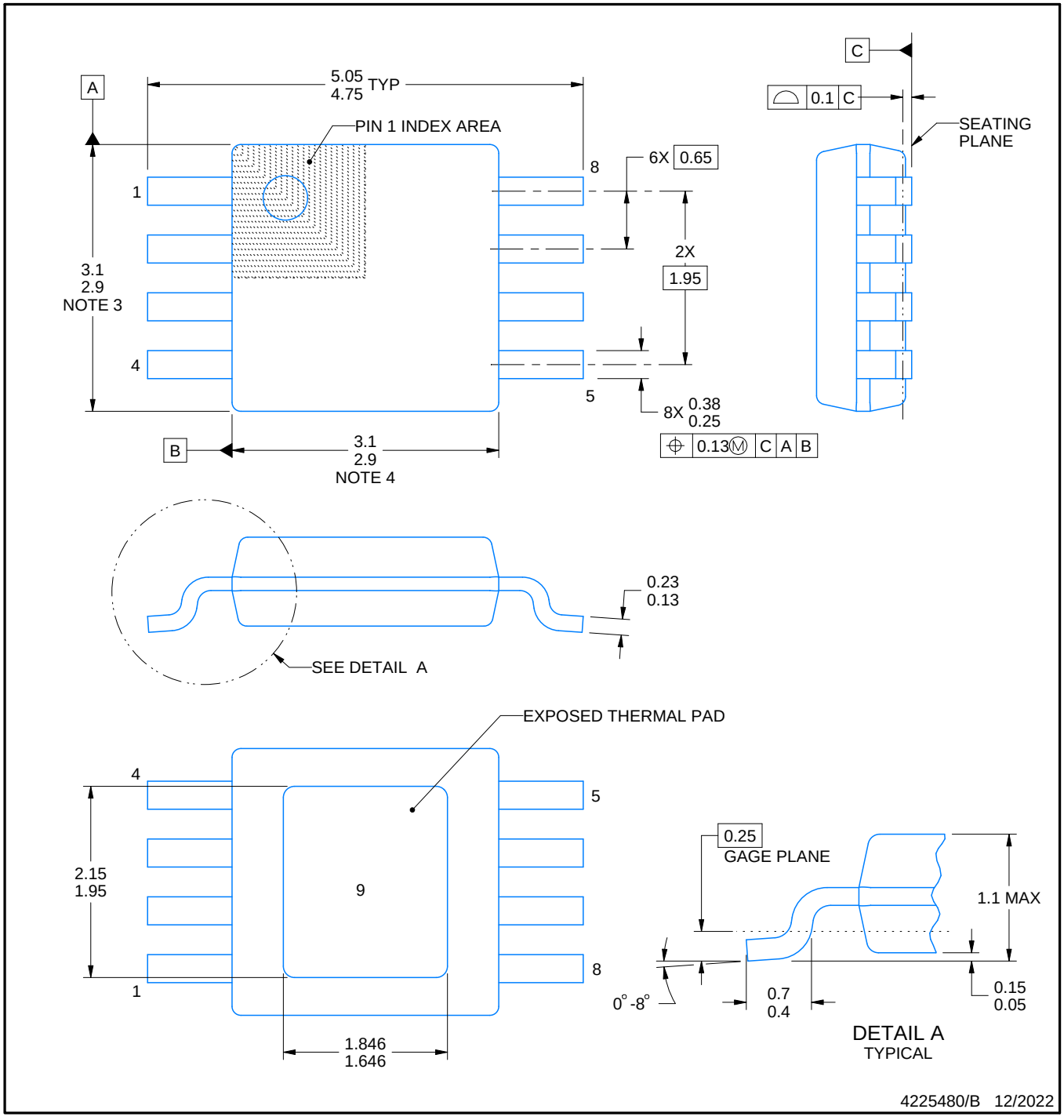
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

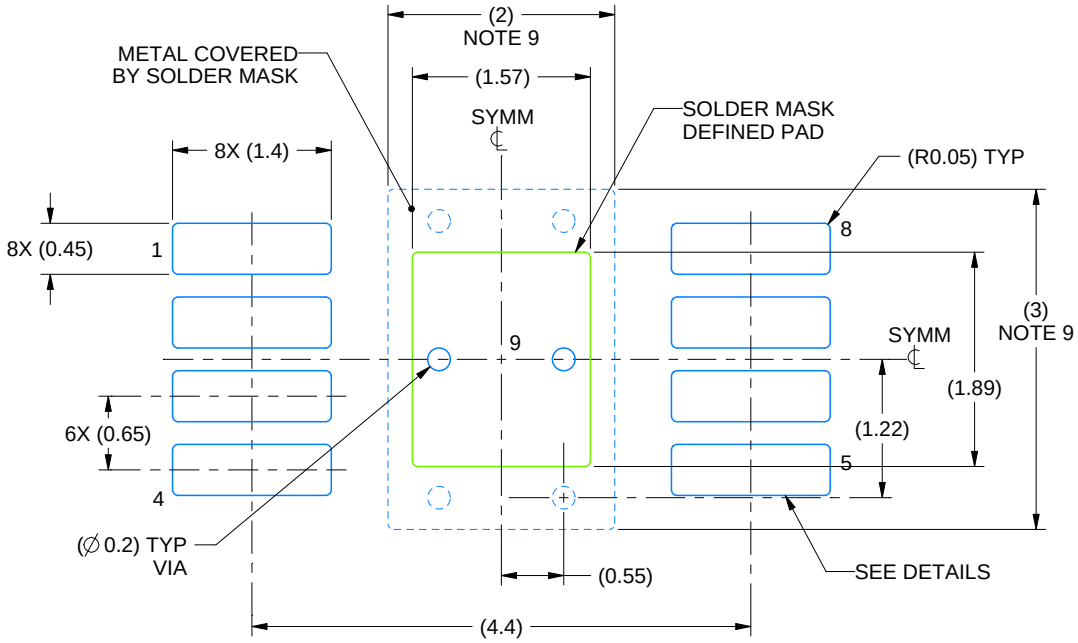
SMALL OUTLINE PACKAGE



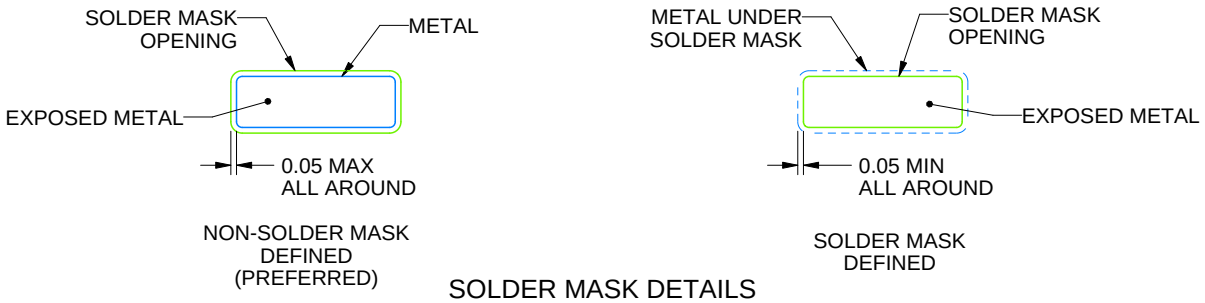
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

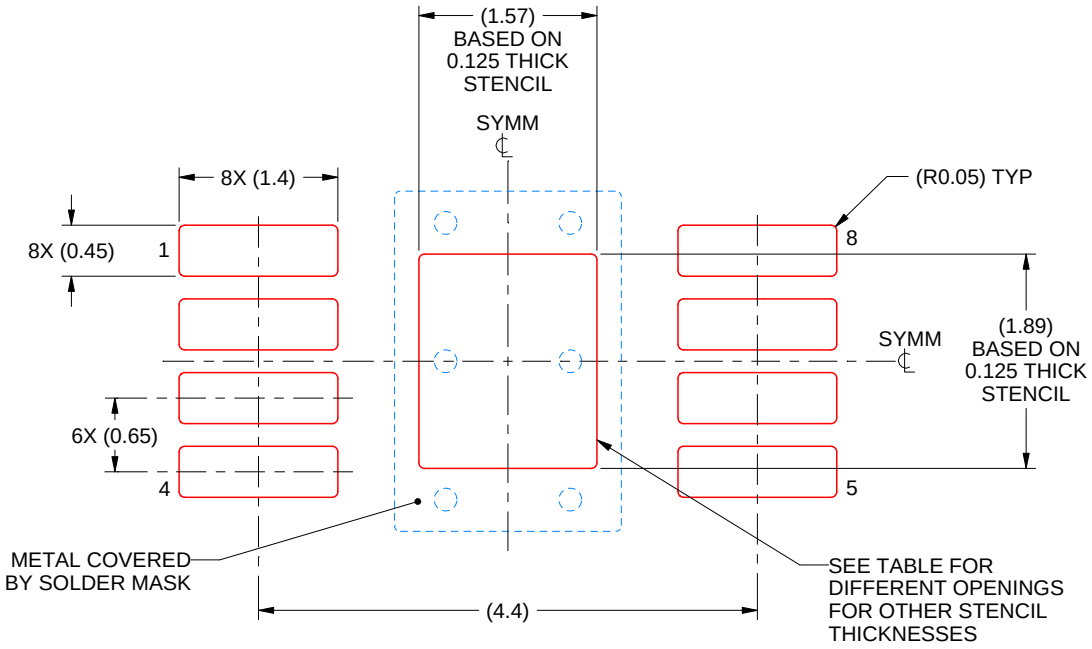


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

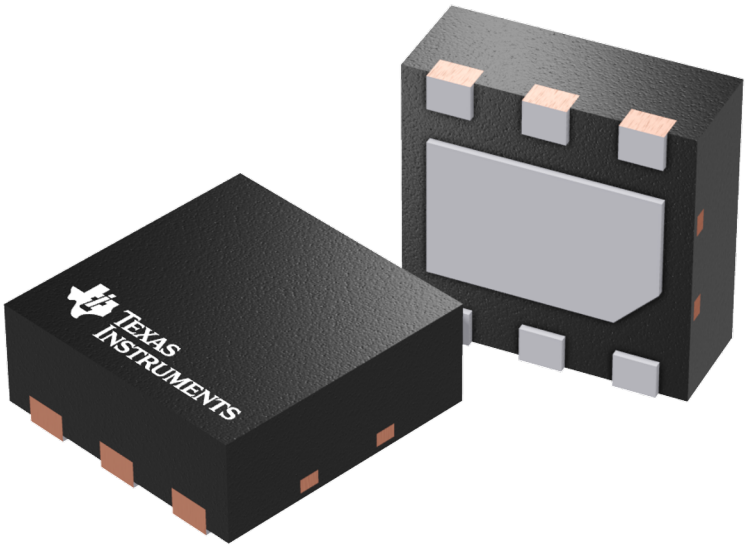
4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



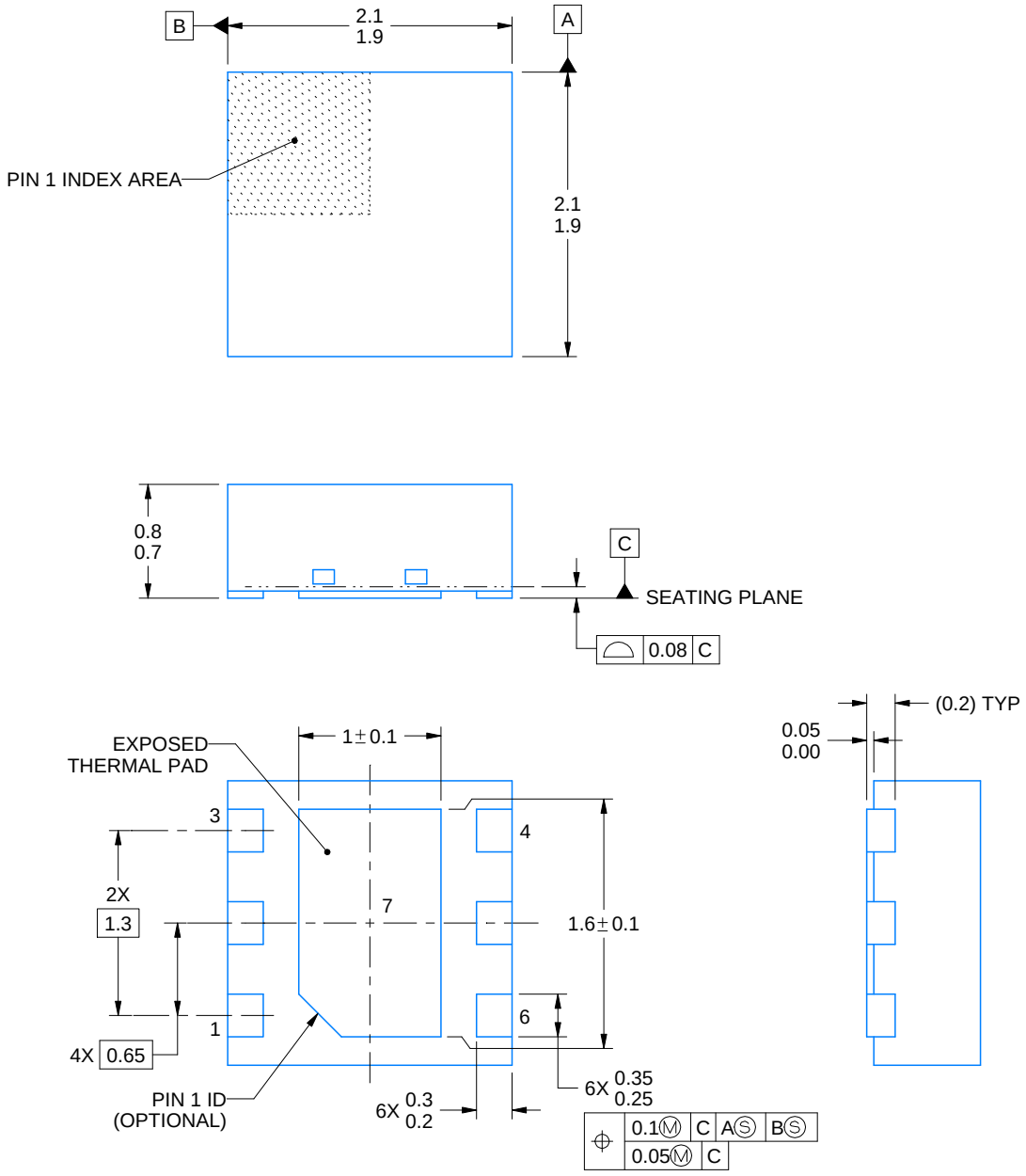
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

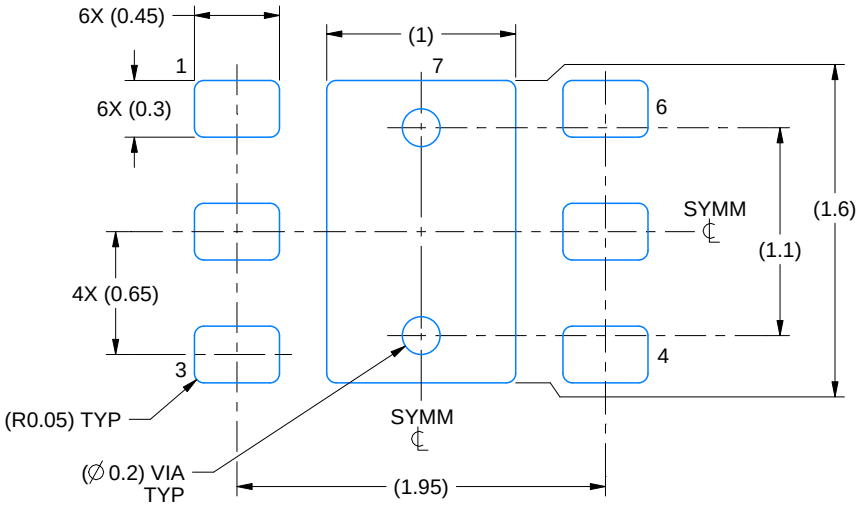
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

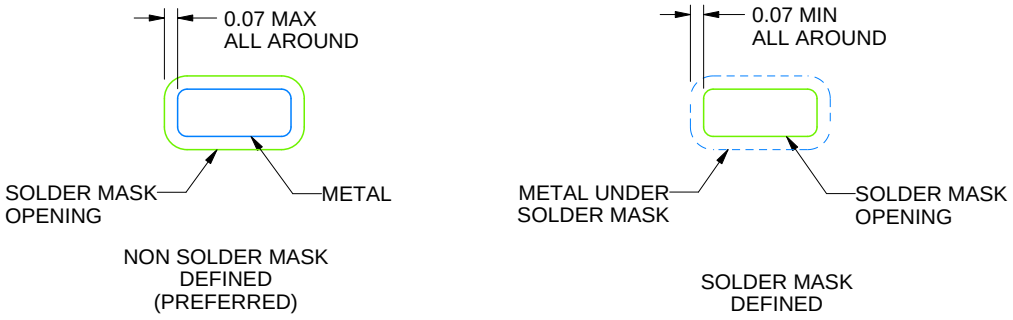


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

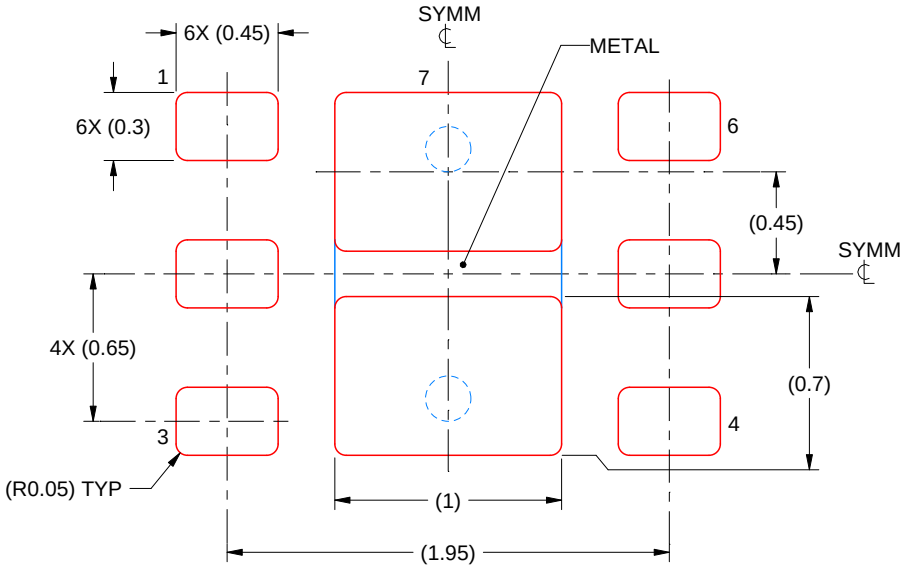
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

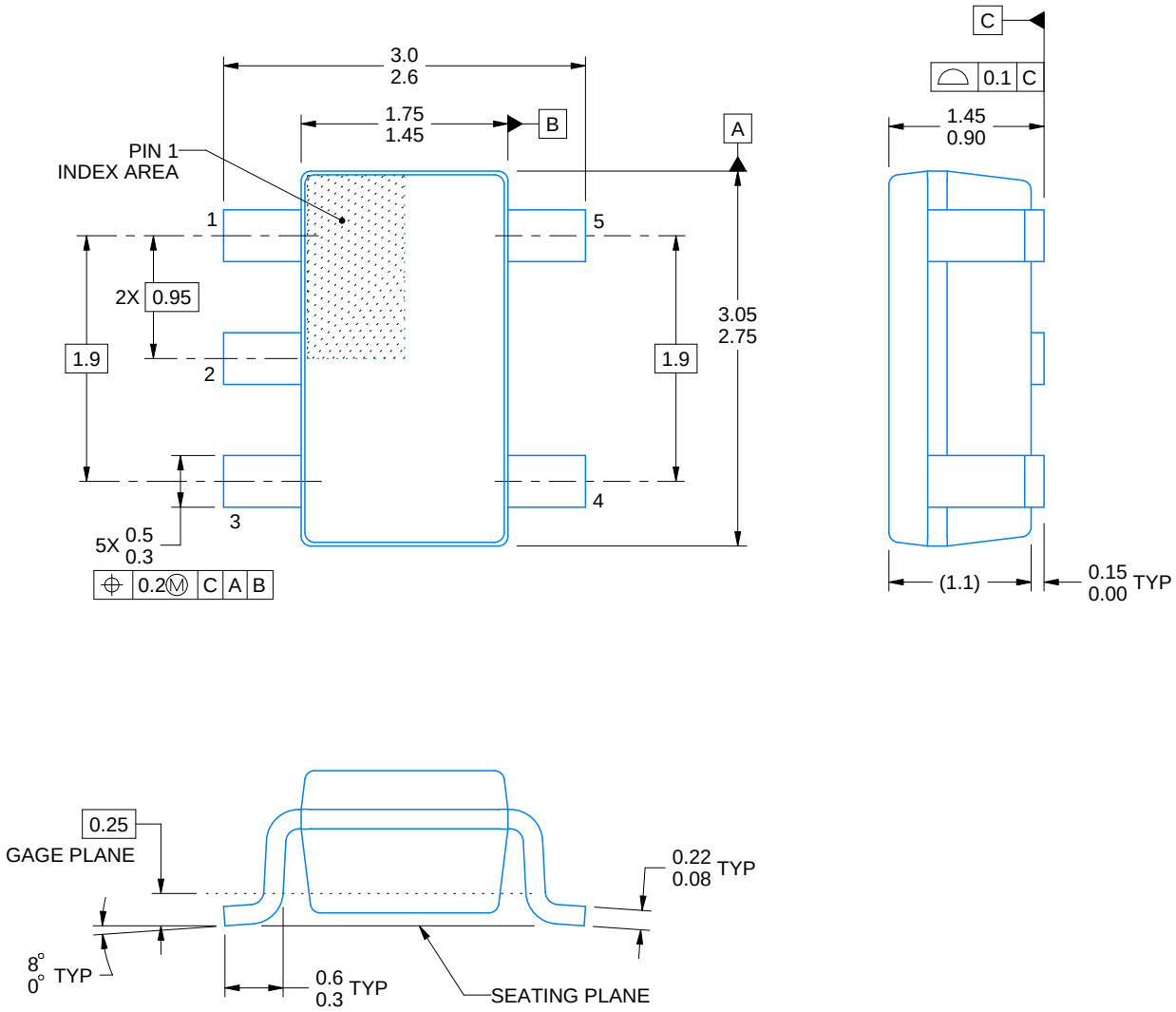
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

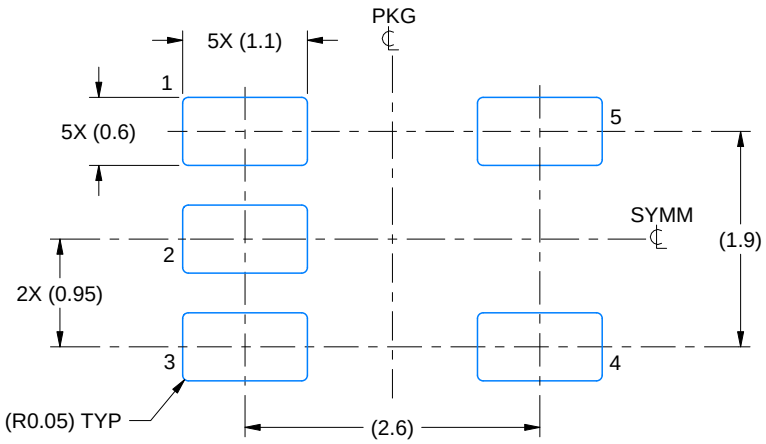
SMALL OUTLINE TRANSISTOR



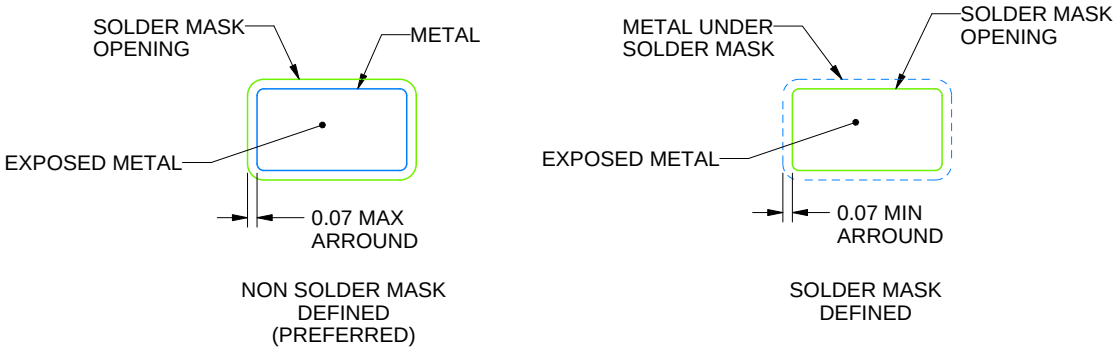
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

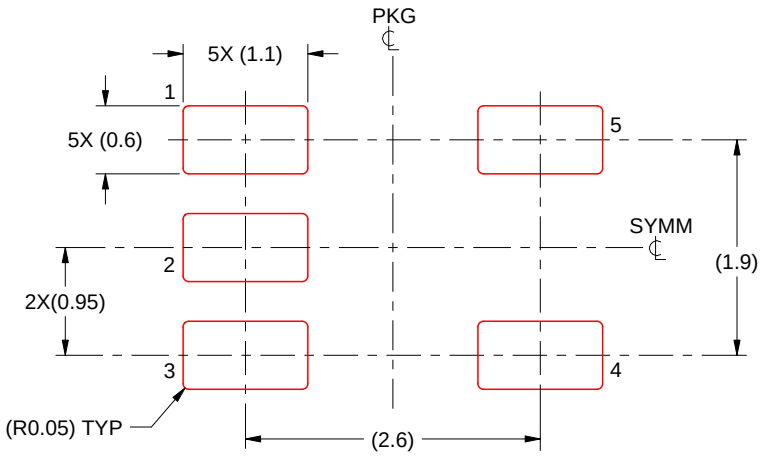


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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