TMS3705 应答器基站 IC

1 器件概述

1.1 特性

- 适用于 TI-RFid ™射频识别系统的基站 IC
- 驱动天线
- 向天线发送调制数据
- 检测并解调应答器响应 (FSK)
- 短路保护
- 诊断
- 睡眠模式电源电流：0.2mA
- 旨在满足汽车要求
- 16 引脚 SOIC (D) 封装

1.2 应用

- 汽车门禁
- 汽车防盗
- 楼宇门禁
- 牲畜信息读取器

1.3 说明

TMS3705 应答器基站 IC 用于驱动 TI-RFid 应答器系统的天线，以发送对天线信号调制的数据以及检测和解调应答器的响应。应答器的响应是一种移频键控 (FSK) 信号。高位和低位被编码到两个不同的高频率信号中（额定条件下，低位编码到 134.2kHz，高位编码到 123kHz）。应答器会根据内部存储的代码感应天线线圈中的这些信号。应答器发送数据时所需的能量存储在应答器的充电电容器中。天线场会在此前的充电阶段为此电容器充电。此 IC 有一个可连接外部微控制器的接口。

共有两种适用于微控制器和基站 IC 的时钟供应配置：

1. 为微控制器和基站 IC 供应的时钟信号只来源于一个谐振器：此谐振器与微控制器相连。为基站 IC 供应的时钟信号由微控制器的数字时钟输出驱动。时钟频率为 4MHz 或 2MHz，取决于所选的微控制器类型。
2. 微控制器和基站各有自己的谐振器。

基站 IC 具有一个片上 PLL，此 PLL 只会为内部时钟供给产生 16MHz 的时钟频率。建议只将 TMS3705DDRQ1 与 AES 应答器产品（例如 TRPWS21GTEA 或 RF430F5xxx）配合使用。建议将 TMS3705EDRQ1 与 DST40、DST80、MPT 应答器（例如 TMS37145TEAx、TMS37126xx、TMS37x128xx、TMS37x136xx、TMS37x158xx、RI-TRP-DR2B-xx、RI-TRP-BRHP-xx）配合使用以获得最佳性能，但不能将它与 AES 应答器产品配合使用。

器件信息(1)

器件型号	封装	封装尺寸(2)
TMS3705EDRQ1	SOIC (16)	9.9mm x 3.91mm
TMS3705DDRQ1	SOIC (16)	9.9mm x 3.91mm

(1) 要获得所有可用器件的最新部件、封装和订购信息，请参见*封装选项附录*（节 9）或浏览 TI 网站 www.ti.com.cn。
(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见*机械数据*（节 9）。

1.4 功能方框图

图 1-1 所示为功能方框图。

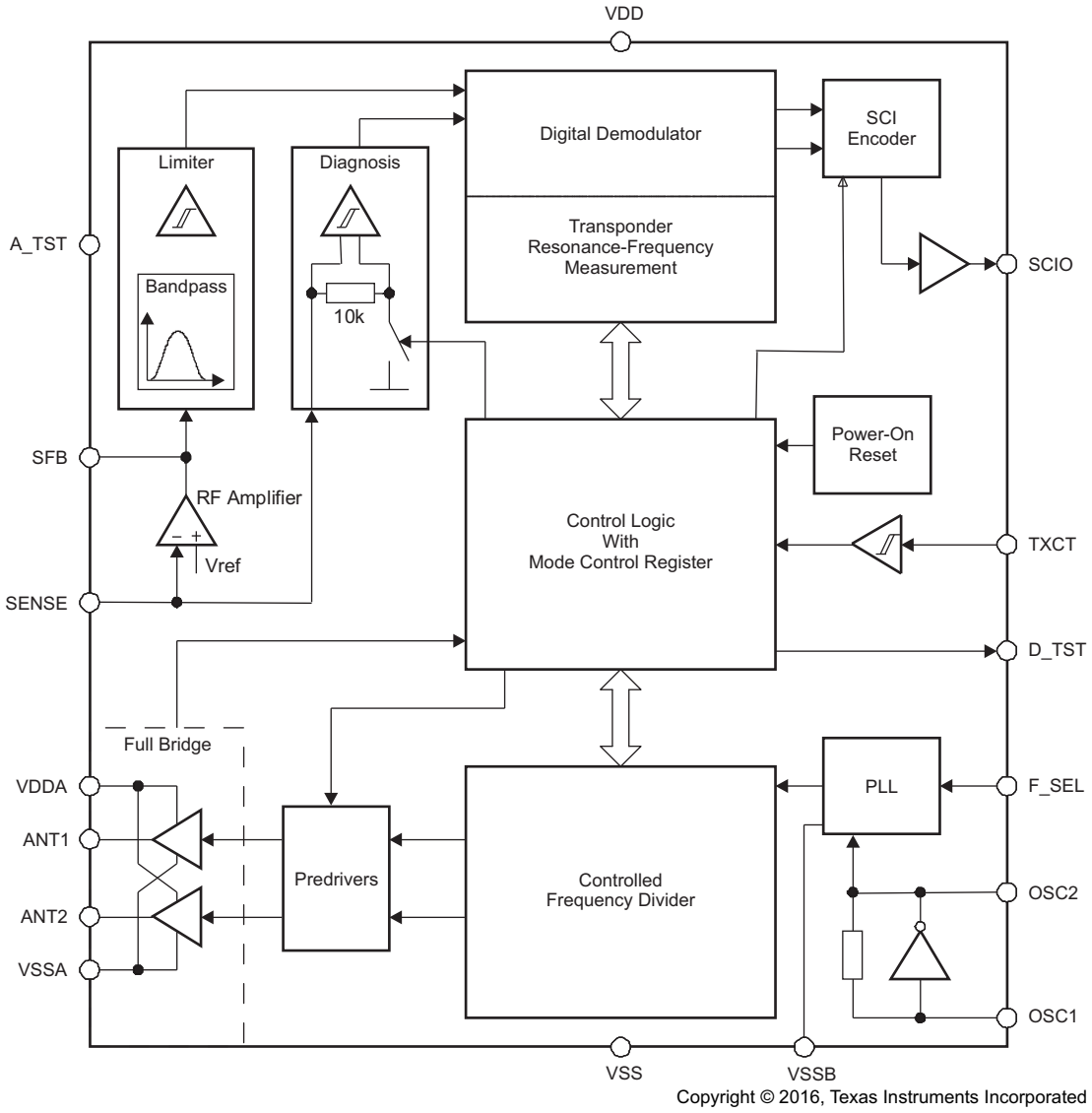


图 **1-1.** 功能方框图

内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from October 19, 2016 to October 31, 2018 **Page**

- 更新了“说明”部分节 1.3 *中从“基站 IC 具有一个片上 PLL...”开始的那个段落.* 1
- 删除了 TMS3705A1DRG4、TMS3705BDRG4 和 TMS3705CDRQ1，并在 *器件信息* 表中添加了 TMS3705EDRQ1 .. 1
- Replaced TMS3705A1DRG4 with TMS3705EDRQ1 in note (F) on Figure 6-1, *Operational State Diagram for the Control Logic* 15
- Changed the note "Setting not allowed for TMS3705DDRQ1" on Table 6-1, *Mode Control Register (7-Bit Register)* 16

3 Device Characteristics

Table 3-1 lists the characteristics of the TMS3705.

Table 3-1. Device Characteristics

Characteristic	TMS3705
Data rate (maximum)	8 kbps
Frequency	134.2 kHz
Required antenna inductance	100 to 1000 µH
Supply voltage	4.5 to 5.5 Vdc
Transmission principle	HDX, FSK

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for Wireless Connectivity Connect more – Industry's broadest wireless connectivity portfolio

Products for NFC / RFID Texas Instruments provides one of the industry's largest, most differentiated NFC product portfolios enabling lower power solutions to meet a broad range of RF connectivity needs.

Companion Products for TMS3705 Review products that are frequently purchased or used with this product.

Reference Designs The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pinout of the 16-pin D (SOIC) package.

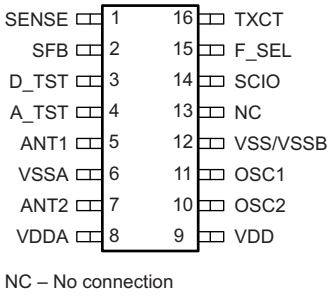


Figure 4-1. 16-Pin D Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the device signals.

Table 4-1. Signal Descriptions

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1	SENSE	Analog input	Input of the RF amplifier
2	SFB	Analog output	Output of the RF amplifier
3	D_TST	Digital output	Test output for digital signals
4	A_TST	Analog output	Test output for analog signals
5	ANT1	Driver output	Antenna output 1
6	VSSA	Supply input	Ground for the full bridge drivers
7	ANT2	Driver output	Antenna output 2
8	VDDA	Supply input	Voltage supply for the full bridge drivers
9	VDD	Supply input	Voltage supply for nonpower blocks
10	OSC2	Analog output	Oscillator output
11	OSC1	Analog input	Oscillator input
12	VSS/VSSB	Supply input	Ground for nonpower blocks and PLL
13	NC		Not connected
14	SCIO	Digital output	Data output to the microcontroller
15	F_SEL	Digital input	Control input for frequency selection (default value is high)
16	TXCT	Digital input	Control input from the microcontroller (default value is high)

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range	VDD, VSS/VSSB, VDDA, VSSA	–0.3	7	V
V_{OSC}	Voltage range	OSC1, OSC2	–0.3	V_{DD} + 0.3	V
V_{inout}	Voltage range	SCIO, TXCT, F_SEL, D_TST	–0.3	V_{DD} + 0.3	V
I_{inout}	Overload clamping current	SCIO, TXCT, F_SEL, D_TST	–5	5	mA
V_{ANT}	Output voltage	ANT1, ANT2	–0.3	V_{DD} + 0.3	V
I_{ANT}	Output peak current	ANT1, ANT2	–1.1	1.1	A
V_{analog}	Voltage range	SENSE, SFB, A_TST	–0.3	V_{DD} + 0.3	V
I_{SENSE}	SENSE input current	SENSE, SFB, A_TST	–5	5	mA
I_{SFB}	Input current in case of overvoltage	SFB	–5	5	mA
T_A	Operating ambient temperature		–40	85	°C
T_{stg}	Storage temperature		–55	150	°C
P_D	Total power dissipation at T_A = 85°C			0.5	W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	ESD protection (MIL STD 883)	±2000	V

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	VDD, VSS/VSSB, VDDA, VSSA	4.5	5	5.5	V
f_{osc}	Oscillator frequency	OSC1, OSC2		4		MHz
V_{IH}	High-level input voltage	F_SEL, TXCT, OSC1	0.7 V_{DD}			V
V_{IL}	Low-level input voltage	TXCT, OSC1			0.3 V_{DD}	V
		F_SEL			0.2 V_{DD}	
I_{OH}	High-level output current	SCIO, D_TST	–1			mA
I_{OL}	Low-level output current	SCIO, D_TST			1	mA

5.4 Electrical Characteristics

V_{DD} = 4.5 V to 5.5 V, f_{osc} = 4 MHz, F_SEL = high, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply (VDD, VSS/VSSB, VDDA, VSSA)						
I_{DD}	Supply current	Sum of supply currents in Charge phase, without antenna load		8	20	mA
I_{Sleep}	Supply current, Sleep state	Sum of supply currents in Sleep state, without I/O currents		0.015	0.2	mA
Oscillator (OSC1, OSC2)						
g_{osc}	Transconductance	f_{osc} = 4 MHz, 0.5 V_{pp} at OSC1	0.5	2	5	mA/V
C_{in}	Input capacitance at OSC1 (1)				10	pF
C_{out}	Output capacitance at OSC2 (1)				10	pF
Logic Inputs (TXCT, F_SEL, OSC1)						
R_{pullup}	Pullup resistance	TXCT	120		500	kΩ
		F_SEL	10		500	
Logic Outputs (SCIO, D_TST)						
V_{OH}	High-level output voltage		0.8 V_{DD}			V
V_{OL}	Low-level output voltage				0.2 V_{DD}	V
Full-Bridge Outputs (ANT1, ANT2)						
ΣR_{ds_on}	Sum of drain-source resistances	Full-bridge N-channel and P-channel MOSFETs at driver current I_{ant} = 50 mA		7	14	Ω
	Duty cycle	P-channel MOSFETs of full bridge	38%	40%	42%	
t_{on1}/t_{on2}	Symmetry of pulse durations for the P-channel MOSFETs of full bridge		96%		104.5%	
I_{oc}	Threshold for overcurrent protection		220		1100	mA
t_{oc}	Switch-off time of overcurrent protection	Short to ground with 3 Ω	0.25		10	µs
t_{doc}	Delay for switching on the full bridge after an overcurrent		2	2.05	2.1	ms
I_{leak}	Leakage current				1	µA
Analog Module (SENSE, SFB, A_TST)						
I_{SENSE}	Input current	SENSE, In charge phase	–2		2	mA
V_{DCREF}/V_{DD}	DC reference voltage of RF amplifier, related to VDD		9.25%	10%	11%	
GBW	Gain-bandwidth product of RF amplifier	At 500 kHz with external components to achieve a voltage gain of minimum 4-mV_{pp} and 5-mV_{pp} input signal	2			MHz
φ_O	Phase shift of RF amplifier	At 134 kHz with external components to achieve a voltage gain of 5-mV_{pp} and 20-mV_{pp} input signal			16	°
V_{sfb}	Peak-to-peak input voltage of band pass at which the limiter comparator should toggle (2)	At 134 kHz (corresponds to a minimal total gain of 1000)	5			mV
f_{low}	Lower cut-off frequency of band-pass filter (3)		24	60	100	kHz
f_{high}	Higher cut-off frequency of band-pass filter (3)		160	270	500	kHz
ΔV_{hys}	Hysteresis of limiter	A_TST pin used as input, D_TST pin as output, offset level determined by band-pass stage	25	50	135	mV
Diagnosis (SENSE)						
I_{diag}	Current threshold for operating antenna (4)		80		240	µA

(1) Specified by design
(2) Specified by design; functional test done for input voltage of 90 mV_{pp}.
(3) Band-pass filter tested at three different frequencies: f_{mid} = 134 kHz and gain > 30 dB; f_{low} = 24 kHz; f_{high} = 500 kHz. Attenuation < –3 dB (reference = measured gain at f_{mid} = 134 kHz).
(4) Internal resistance switched on and much lower than external SENSE resistance.

Electrical Characteristics *(continued)*

V_{DD} = 4.5 V to 5.5 V, f_{osc} = 4 MHz, F_SEL = high, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase-Locked Loop (D_TST)						
f_{pll}	PLL frequency		15.984	16	16.0166	MHz
$\Delta f/f_{pll}$	Jitter of the PLL frequency				6%	
Power-On Reset (POR)						
V_{por_r}	POR threshold voltage, rising	V_{DD} rising with low slope	1.9		3.5	V
V_{por_f}	POR threshold voltage, falling	V_{DD} falling with low slope	1.3		2.6	V

5.5 Thermal Resistance Characteristics for D (SOIC) Package

PARAMETER		VALUE	UNIT
$R_{\theta JA}$	Thermal resistance, junction to ambient(1)	130	°C/W

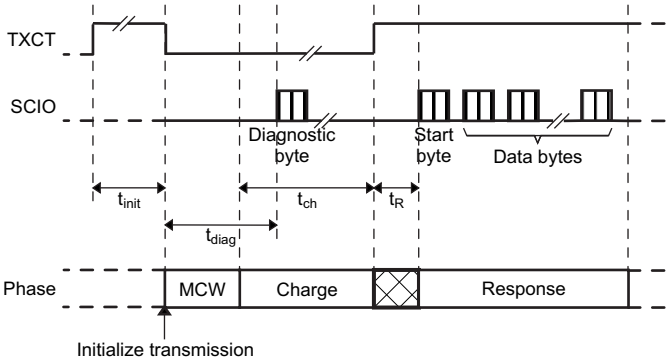
(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

5.6 Switching Characteristics

V_{DD} = 4.5 V to 5.5 V, f_{osc} = 4 MHz, F_SEL = high, over operating free-air temperature range (unless otherwise noted)

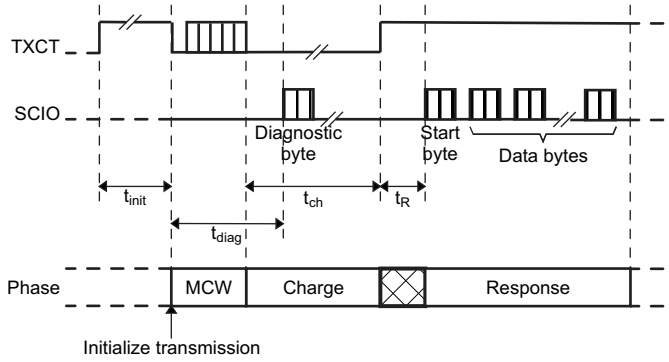
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{init\ min}$	Time for TXCT high to initialize a new transmission	From start of the oscillator after power on or waking up until reaching the Idle state (see Figure 5-1, Figure 5-2, Figure 5-3)	2	2.05	2.2	ms
t_{diag}	Delay between leaving Idle state and start of diagnosis byte at SCIO	Normal operation (see Figure 5-1, Figure 5-2, Figure 5-3)	2	2.12	2.2	ms
t_R	Delay between end of charge or end of program and start of transponder data transmit on SCIO	See Figure 5-1, Figure 5-2, Figure 5-3.		3		ms
t_{off}	Write pulse pause	See Figure 5-5.	0.1			ms
t_{dwrite}	Signal delay on TXCT for controlling the full bridge	Write mode	73	79	85	µs
t_{mcr}	NRZ bit duration for mode control register	See Figure 5-4.	121	128	135	µs
t_{sci}	NRZ bit duration on SCIO	Asynchronous mode (see Figure 5-6)	63	64	65	µs
t_{dstop}	Low signal delay on TXCT to stop	Synchronous mode	128		800	µs
t_{t_sync}	Total TXCT time for reading data on SCIO	Synchronous mode (see Figure 5-7)			900	µs
t_{sync}	TXCT period for shifting data on SCIO	Synchronous mode (seeFigure 5-7)	4	64	100	µs
t_{L_sync}	Low phase on TXCT	Synchronous mode (see Figure 5-7)	2	32	t_{sync} – 2	µs
t_{ready}	Data ready for output after SCIO goes high	Synchronous mode (see Figure 5-7)	1		127	µs

5.7 Timing Diagrams



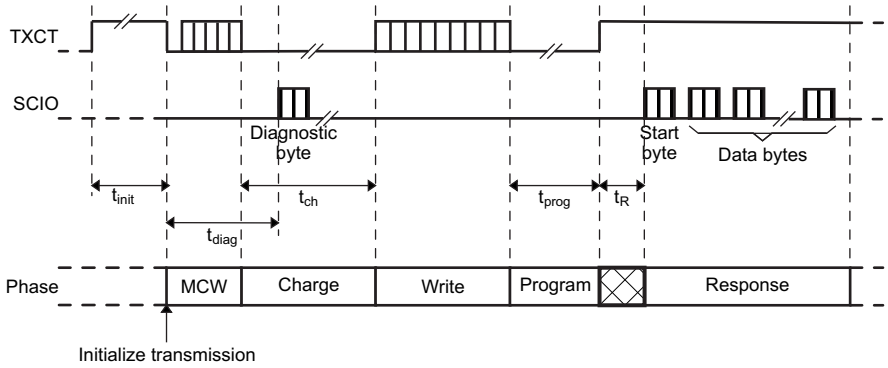
NOTE: MCW = Mode control write (to write into the mode control register)

Figure 5-1. Default Mode (Read Only, No Writing Into Mode Control Register)



NOTE: MCW = Mode control write (to write into the mode control register)

Figure 5-2. Read-Only Mode (Writing Into Mode Control Register)



NOTE: MCW = Mode control write (to write into the mode control register)

Figure 5-3. Write/Read Mode (Writing Into Mode Control Register)

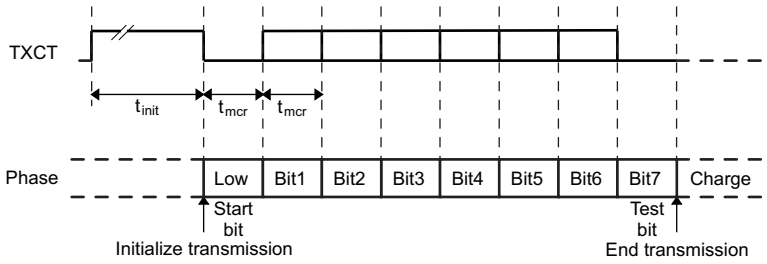


Figure 5-4. Mode Control Write Protocol (NRZ Coding)

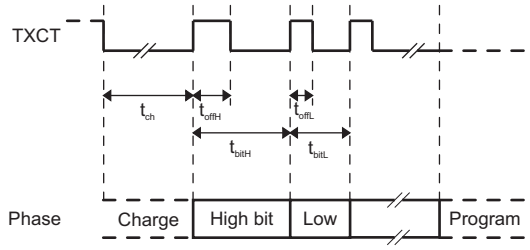


Figure 5-5. Transponder Write Protocol

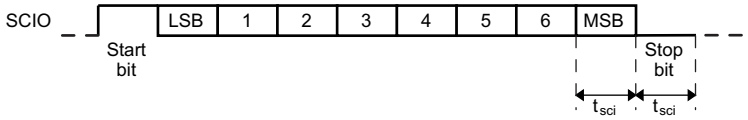


Figure 5-6. Transmission on SCIO in Asynchronous Mode (NRZ Coding)

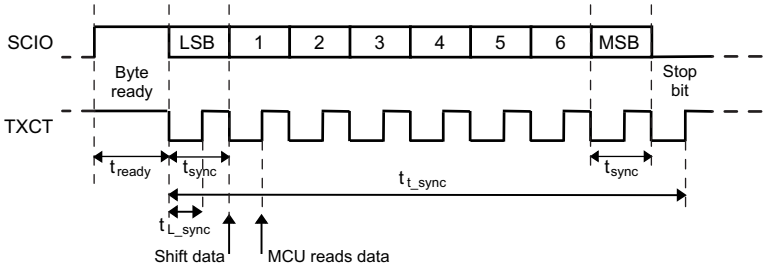


Figure 5-7. Transmission on SCIO in Synchronous Mode (NRZ Coding) (For Diagnosis Byte and Data Bytes)

6 Detailed Description

6.1 Power Supply

The device is supplied with 5 V by an external voltage regulator through two supply pins, one for providing the driver current for the antenna and the analog part in front of the digital demodulator and one for supplying the other blocks.

The power supply supplies a power-on reset that brings the control logic into Idle state as soon as the supply voltage drops under a certain value.

In Sleep state, the sum of both supply currents is reduced to 0.2 mA. The base station device falls into Sleep state 100 ms after TXCT has changed to high. When TXCT changes to low or is low, the base station IC immediately goes into and remains in normal operation.

6.2 Oscillator

The oscillator generates the clock of the base station IC of which all timing signals are derived. Between its input and output a crystal or ceramic resonator is connected that oscillates at a typical frequency of 4 MHz. If a digital clock signal with a frequency of 4 MHz or 2 MHz is supplied to pin OSC1, the signal can be used to generate the internal operation frequency of 16 MHz.

The oscillator block contains a PLL that generates the internal clock frequency of 16 MHz from the input clock signal. The PLL multiplies the input clock frequency depending on the logic state of the input pin F_SEL by a factor of 4 (F_SEL is high) or by a factor of 8 (F_SEL is low).

In the Sleep state, the oscillator is off.

6.3 Predrivers

The predrivers generate the signals for the four power transistors of the full bridge using the carrier frequency generated by the frequency divider. The gate signals of the P-channel power transistors (active low) have the same width (±1 cycle of the 16 MHz clock), the delay between one P-channel MOSFET being switched off and the other one being switched on is defined to be 12 cycles of the 16-MHz clock. In write mode the first activation of a gate signal after a bit pause is synchronized to the received transponder signal by a phase shift of 18°.

6.4 Full Bridge

The full bridge drives the antenna current at the carrier frequency during the charge phase and the active time of the write phase. The minimal load resistance the full bridge sees between its outputs in normal operation at the resonance frequency of the antenna is 43.3 Ω. When the full bridge is not active, the two driver outputs are switched to ground.

Both outputs of the full bridge are protected independently against short circuits to ground.

In case of an occurring short circuit, the full bridge is switched off in less than 10 µs to avoid a drop of the supply voltage. After a delay time of less than 10 ms the full bridge is switched on again to test if the short circuit is still there. An overcurrent due to a resistive short to ground that is higher than the maximum current in normal operation but lower than the current threshold for overcurrent protection does not need to be considered.

6.5 RF Amplifier

The RF amplifier is an operational amplifier with a fixed internal voltage reference and a voltage gain of 5 defined by external resistors. The RF amplifier has a high gain-bandwidth product of at least 2 MHz to show a phase shift of less than 16° for the desired signal and to give the possibility to use it as a low-pass filter by adapting additional external components.

The input signal of the RF amplifier is DC coupled to the antenna. The amplitude of the output signal of the RF amplifier is higher than 5 mV peak-to-peak.

6.6 Band-Pass Filter and Limiter

The band-pass filter provides amplification and filtering without external components. The lower cut-off frequency is approximately a factor of 2 lower than the average signal frequency of 130 kHz, the higher cut-off frequency is approximately a factor of 2 higher than 130 kHz.

The limiter converts the analog sine-wave signal to a digital signal. The limiter provides a hysteresis depending on the minimal amplitude of its input signal. The duty cycle of its digital output signal is between 40% and 60%. The band-pass filter and the limiter together have a high gain of at least 1000.

6.7 Diagnosis

The diagnosis is carried out during the charge phase to detect whether the full bridge and the antenna are working. When the full bridge drives the antenna, the voltage across the coil exceeds the supply voltage so that the voltage at the input of the RF amplifier is clamped by the ESD-protection diodes. For diagnosis, the SENSE pin is loaded on-chip with a switchable resistor to ground so that the internal switchable resistor and the external SENSE resistor form a voltage divider, while the internal resistor is switched off in read mode. When the voltage drop across the internal resistor exceeds a certain value, the diagnosis block passes the frequency of its input signal to the digital demodulator. The frequency of the diagnosis signal is accepted if eight subsequent times can be detected, all with their counter state within the range of 112 to 125, during the diagnosis time (at most 0.1 ms). The output signal is used only during the charge phase, otherwise it is ignored.

When the short-circuit protection switches off one of the full-bridge drivers, the diagnosis also indicates an improper operation of the antenna by sending the same diagnostic byte to the microcontroller as for the other failure mode.

During diagnosis, the antenna drivers are active. In synchronous mode the antenna drivers remain active up to 1 ms after the diagnosis is performed, without any respect to the logic state of the signal at TXCT (thus enabling the microcontroller to clock out the diagnosis byte).

6.8 Power-on Reset

The power-on reset generates an internal reset signal to allow the control logic to start up in the defined way.

6.9 Frequency Divider

The frequency divider is a programmable divider that generates the carrier frequency for the full-bridge antenna drivers. The default value for the division factor is the value 119 needed to provide the nominal carrier frequency of 134.45 kHz generated from 16 MHz. The resolution for programming the division factor is one divider step that corresponds to a frequency shift of approximately 1.1 kHz. The different division factors needed to cover the range of frequencies for meeting the resonance frequency of the transponder are 114 to 124.

6.10 Digital Demodulator

The input signal of the digital demodulator comes from the limiter and is frequency-coded according to the high- and low-bit sequence of the transmitted transponder code. The frequency of the input signal is measured by counting the oscillation clock for the time period of the input signal. As the high-bit and low-bit frequencies are specified with wide tolerances, the demodulator is designed to distinguish the high-bit and the low-bit frequency by the shift between the two frequencies and not by the absolute values. The threshold between the high-bit and the low-bit frequency is defined to be 6.5 kHz lower than the measured low-bit frequency and has a hysteresis of ±0.55 kHz.

The demodulator is controlled by the control logic. After the charge phase (that is during read or write phase) it measures the time period of its input signal and waits for the transponder resonance-frequency measurement to determine the counter state for the threshold between high-bit and low-bit frequency. Then the demodulator waits for the occurrence of the start bit. For that purpose, the results of the comparisons between the measured time periods and the threshold are shifted in a 12-bit shift register. The detection of the start bit comes into effect when the contents of the shift register matches a specific pattern, indicating 8 subsequent periods below the threshold immediately followed by 4 subsequent periods above the threshold. A 2-period digital filter is inserted in front of the 12-bit shift register to make a start bit detection possible in case of a nonmonotonous progression of the time periods during a transition from low- to high-bit frequency.

The bit stream detected by the input stage of the digital demodulator passes a digital filter before being evaluated. After demodulation, the serial bit flow received from the transponder is buffered byte-wise before being sent to the microcontroller by SCI encoding.

6.11 Transponder Resonance-Frequency Measurement

During the prebit reception phase, the bits the transponder transmits show the low-bit frequency, which is the resonance frequency of the transponder. The time periods of the prebits are evaluated by the demodulator counter. Based on the counter states, an algorithm is implemented that ensures a correct measurement of the resonance frequency of the transponder:

1. A time period of the low-bit frequency has a counter state between 112 and 125.
2. The measurement of the low-bit frequency (the average of eight subsequent counter states) is accepted during the write mode, when the eight time periods have counter states in the defined range. The measurement during write mode is started with the falling edge at TXCT using the fixed delay time at which end the full bridge is switched on again.
3. The counter state of the measured low-bit frequency results in the average counter state of an accepted measurement and can be used to update the register of the programmable frequency divider.
4. The measurement of the low-bit frequency (the average of eight subsequent counter states) is accepted during the read mode, when the eight time periods have counter states in the defined range. The start of the measurement during read mode is delayed to use a stable input signal for the measurement.
5. The threshold to distinguish between high-bit and low-bit frequency is calculated to be by a value of 5 or 7 (see hysteresis in threshold) higher than the counter state of the measured low-bit frequency.

6.12 SCI Encoder

An SCI encoder performs the data transmission to the microcontroller. As the transmission rate of the transponder is lower than the SCI transmission rate, the serial bit flow received from the transponder is buffered after demodulation and before SCI encoding.

The SCI encoder uses an 8-bit shift register to send the received data byte-wise (least significant bit first) to the microcontroller with a transmission rate of 15.625 kbaud (±1.5 %), 1 start bit (high), 1 stop bit (low), and no parity bit (asynchronous mode indicated by the SYNC bit of the Mode Control register is permanently low). The data bits at the SCIO output are inverted with respect to the corresponding bits sent by the transponder.

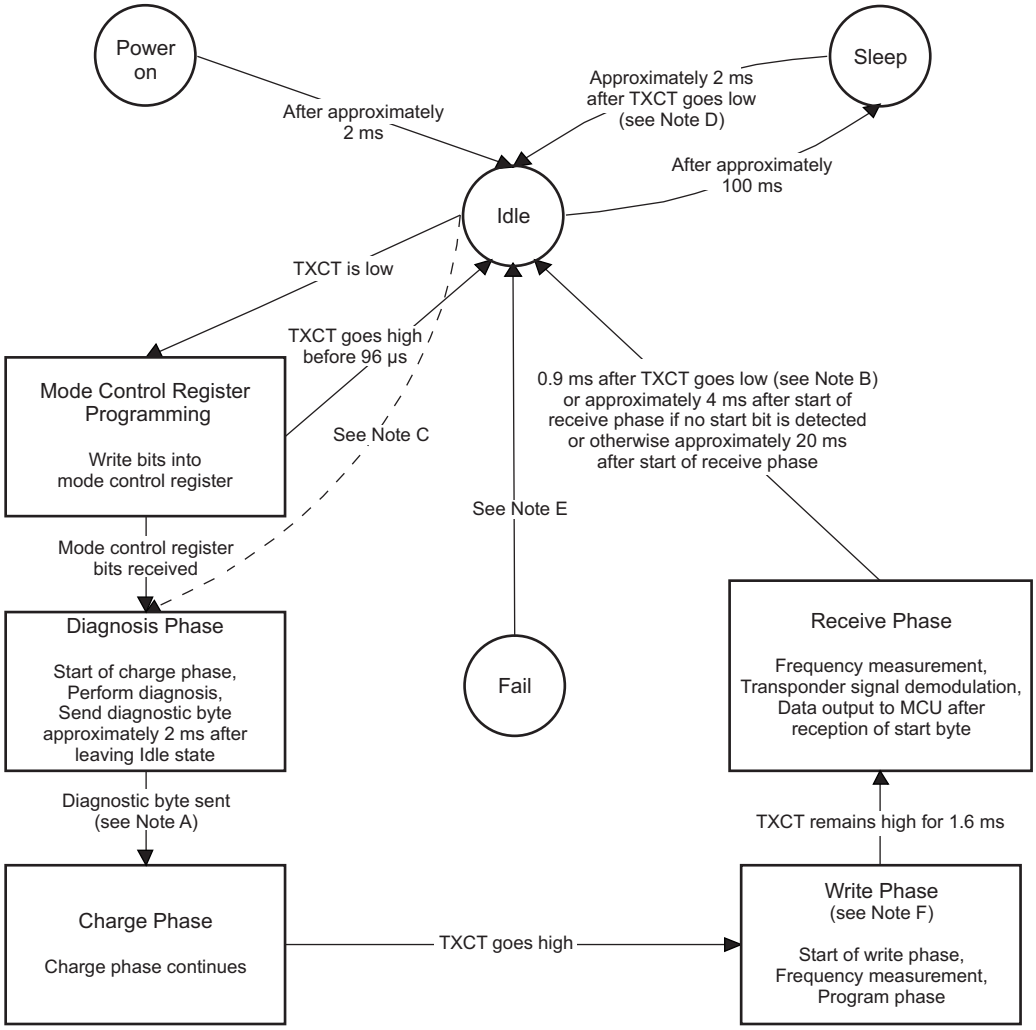
The transmission starts after the reception of the start bit. The start byte detection is initialized with the first rising edge. Typical values for the start byte are 81_H or 01_H (at SCIO). The start byte is the first byte to be sent to the microcontroller. The transmission stops and the base station returns to the Idle state when TXCT becomes low or 20 ms after the beginning of the read phase. TXCT remains low for at least 128 µs to stop the read phase and less than 900 µs to avoid starting the next transmission cycle.

The SCI encoder also sends the diagnostic byte 2 ms after beginning of the charge phase. In case of a normal operation of the antenna, the diagnostic byte AF_H is sent. If no antenna oscillation can be measured or if at least one of the full-bridge drivers is switched off due to a detected short circuit, the diagnostic byte FF_H is sent to indicate the failure mode.

The SCI encoder can be switched into a synchronous data transmission mode by setting the mode control register bit SYNC to high. In this mode, the output SCIO indicates by a high state that a new byte is ready to be transmitted. The microcontroller can receive the 8 bits at SCIO when sending the eight clock signals (falling edge means active) for the synchronous data transmission through pin TXCT to the SCI encoder.

6.13 Control Logic

The control logic is the core of the TMS3705 circuit. This circuit contains a sequencer or a state machine that controls the global operations of the base station (see Figure 6-1). This block has a default mode configuration but can also be controlled by the microcontroller through the TXCT serial input pin to change the configuration and to control the programmable frequency divider. For that purpose a mode control register is implemented in this module that can be written by the microcontroller.



A. In SCI synchronous mode, this transition always occurs approximately 3 ms after leaving Idle state. Diagnostic byte transmission is complete before the transition.

B. A falling edge on TXCT interrupts the receive phase after a delay of 0.9 ms. TXCT must remain low for at least 128 µs. If TXCT is still low after the 0.9-ms delay, the base station enters the Idle state and then the Diagnosis phase one clock cycle later (see the dotted line marked with "See Note C"). No mode control register can be written, and only the default mode is fully supported in this case. Otherwise, if TXCT returns high and remains high during the delay, the base station stays in Idle state and waits for TXCT to go low (which properly starts a new mode control register programming operation) or waits for 100 ms to enter the Sleep state.

C. This transition occurs only in a special case, as described in Note B.

D. A falling edge on TXCT interrupts the Sleep state. Only the default mode is fully supported when starting an operation from the Sleep state with only one falling edge on TXCT, because of the 2-ms delay. For proper mode control register programming, TXCT must return to high and remain high during this delay.

E. Idle state is the next state in case of undefined states (fail-safe state machine).

F. Frequency measurement is available for the TMS3705EDRQ1 only.

Figure 6-1. Operational State Diagram for the Control Logic

The default mode is a read-only mode that uses the default frequency as the carrier frequency for the full bridge. Therefore the mode control register does not need to be written (it is filled with low states), and the communication sequence between microcontroller and base station starts with TXCT being low for a fixed time to initiate the charge phase. When TXCT becomes high again, the module enters the read phase and the data transmission through the SCIO pin to the microcontroller starts.

There is another read-only mode that differs from the default mode only in the writing of the mode control register before the start of the charge phase. The method to fill the mode control register and the meaning of its contents is described in the following paragraphs.

The write-read mode starts with the programming of the mode control register. Then the charge phase starts with TXCT being low for a fixed time. When TXCT becomes high again, the write phase begins in which the data are transmitted from the microcontroller to the transponder through the TXCT pin, the control logic, the predrivers, and the full bridge by amplitude modulation of 100% with a fixed delay time. After the write phase TXCT goes low again to start another charge or program phase. When TXCT becomes high again, the read phase begins.

The contents of the mode control register (see Table 6-1) define the mode and the way that the carrier frequency generated by the frequency divider is selected to meet the transponder resonance frequency as closely as possible.

Table 6-1. Mode Control Register (7-Bit Register)

BIT		RESET VALUE	DESCRIPTION	
NAME	NO.			
START_BIT	Bit 0	0	START_BIT = 0	The start bit is always low and does not need to be stored.
DATA_BIT1	Bit 1	0	DATA_BIT[4:1] = 0000	Microcontroller selects division factor 119
			DATA_BIT[4:1] = 1111	Division factor is adapted automatically(1)
DATA_BIT2	Bit 2	0	DATA_BIT[4:1] = 0001	Microcontroller selects division factor 114
			DATA_BIT[4:1] = 0010	Microcontroller selects division factor 115
DATA_BIT3	Bit 3	0	...	...
			DATA_BIT[4:1] = 0110	Microcontroller selects division factor 119
DATA_BIT4	Bit 4	0	...	...
			DATA_BIT[4:1] = 1011	Microcontroller selects division factor 124
SCI_SYNC	Bit 5	0	SCI_SYNC = 0	Asynchronous data transmission to the microcontroller
			SCI_SYNC = 1	Synchronous data transmission to the microcontroller
RX_AFC	Bit 6	0	RX_AFC = 0	Demodulator threshold is adapted automatically
			RX_AFC = 1	Demodulator threshold is defined by DATA_BIT[4:1]
TEST_BIT	Bit 7	0	TEST_BIT = 0	No further test bytes
			TEST_BIT = 1	Further test byte follows for special test modes

(1) Setting is not allowed for TMS3705DDRQ1.

The TMS3705EDRQ1 can adjust the carrier frequency to the transponder resonance frequency automatically by giving the counter state of the transponder resonance-frequency measurement directly to the frequency divider by setting the first 4 bits in high state. The other combinations of the first 4 bits allow the microcontroller to select the default carrier frequency or to use another frequency. The division factor can be selected to be between 114 and 124.

Some bits are included for testability reasons. The default value of these test bits for normal operation is low. Bit 7 (TEST_BIT) is low for normal operation; otherwise, the base station may enter one of the test modes.

The control logic also controls the demodulator, the SCI encoder, the diagnosis, and the transmission of the diagnosis byte during the charge phase.

The state diagram in Figure 6-1 shows the general behavior of the state machine (the state blocks drawn can contain more than one state). All given times are measured from the moment when the state is entered if not specified otherwise.

6.14 Test Pins

The IC has an analog test pin A_TST for the analog part of the receiver. The digital output pin D_TST is used for testing the internal logic. Connecting both pins is not required.

7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Diagram

Figure 7-1 shows a typical application diagram.

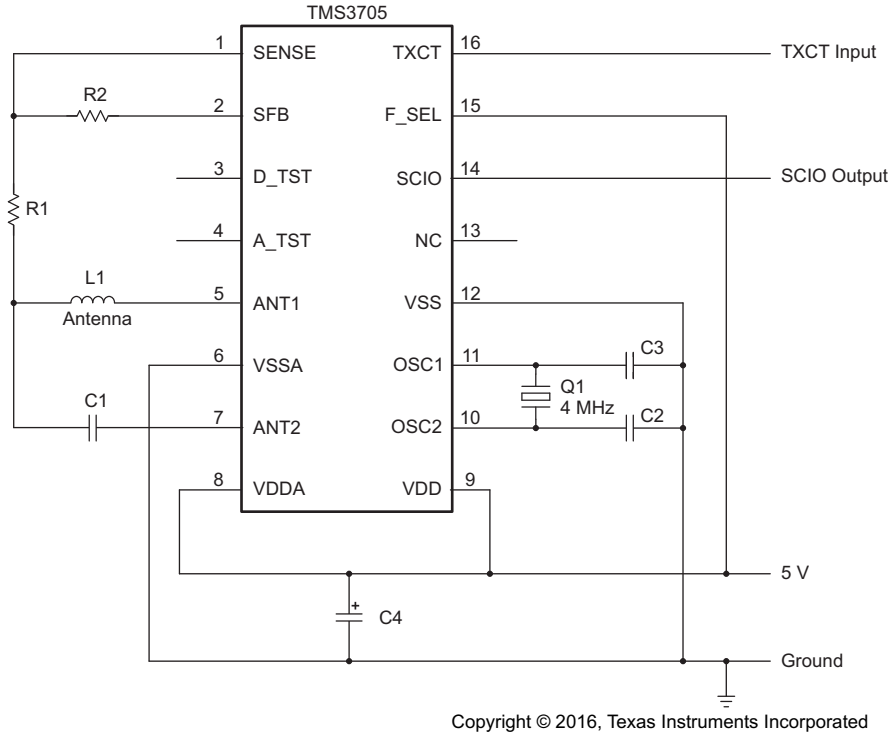


Figure 7-1. Application Diagram

Table 7-1 lists the bill of materials for the application in Figure 7-1.

Table 7-1. Bill of Materials (BOM)

COMPONENT	VALUE	COMMENTS
R1	47 kΩ	
R2	150 kΩ	
L1	422 µH at 134 kHz	Sumida part number: Vogt 581 05 042 40
C1	3 nF	NPO , COG (high Q types). Voltage rating must be 100 V or higher depending on Q factor.
C2	220 pF	NPO
C3	220 pF	NPO
C4	22 µF	Low ESR
Q1	4-MHz resonator	muRata part number: CSTCR4M00G55B-R0. See resonator data sheet (load capacitance is important).

8 器件和文档支持

8.1 入门和后续步骤

TI 的 RFID 产品可为各种 应用提供最终解决方案。TI RFID 采用 HDX 专利技术，可在读取范围、读取速率以及稳健性等方面提供无与伦比的性能。有关更多信息，请参阅 NFC/RFID 概述。

8.2 器件命名规则

为了标明产品开发周期的阶段，TI 为所有器件的部件号分配了前缀。每个器件都具有以下三个前缀之一：X、P 或无（无前缀）（例如 *TMS3705*）。

器件开发进化流程：

X 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

P 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

X 和 P 器件在供货时附带如下免责声明：

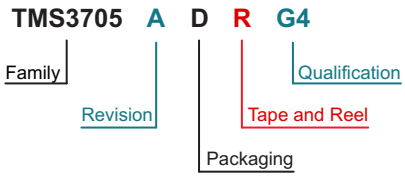
“开发中的产品用于内部评估之用。”

生产器件已进行完全特性化，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。由于这些器件的预计最终使用故障率尚不确定，德州仪器 (TI) 建议不要将它们用于任何生产系统。请仅使用合格的生产器件。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。这个后缀表示封装类型（例如 *D*）。图 8-1 提供了解读完整器件名称的图例。

要了解 *TMS3705* 器件（*D* 封装类型）的可订购部件号，请参阅*封装选项附录*（位于 节 9 中）、TI 网站，或者联系您的 TI 销售代表。



Family	TMS3705 = Transponder base station IC
Revision	A1, B, C, D = Silicon revision
Packaging	http://www.ti.com/packaging
Tape and Reel	R = Large reel
Qualification	G4 = Green (RoHS and no Sb, Br) Q1 = Q100 Qualified

图 **8-1.** 器件命名规则

8.3 工具和软件

设计套件与评估模块

低频演示读取器 ADR2 评估套件包含评估和操作 TI 汽车门禁产品所需的低频读取器。此套件含一块读取器基板、LF 天线和一个 USB-RS232 适配器。搭配使用可在线获取的 PC 软件，可以控制读取器的所有功能，所有汽车应答器、遥控无钥匙进入和被动门禁器件的问题也会迎刃而解。无需更换任何组件，即可使用该系统控制应答器的功能和进行被动门禁通信。

PaLFI、无源低频评估套件 TMS37157 PaLFI 评估套件包含评估和操作 TMS37157 所需的全部组件。此套件附带 eZ430 MSP430F1612 USB 开发记忆棒和 MSP430 目标板，包含 MSP430F2274 和 TMS37157 PaLFI。用于有源操作的电池板加上 RFID 基站读/写器一起为各种评估环境提供基础设施。

8.4 文档支持

以下文档介绍了应答器、相关外设和其他技术配套材料。

接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 TMS3705 产品文件夹。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

应用报告

谐振修整序列 本应用报告介绍了一种高效、精确的方法，通过配置只含几次迭代的修整阵列和测量谐振频率来获得所需的谐振频率。

使用 UCC27424-Q1 的 TMS3705 范围扩展器电源解决方案 本应用报告提供了关于与外部驱动器 IC 配合使用的 TI 134.2kHz RFID 基站 IC TMS3705x 的补充信息。特别值得一提的是，本文档介绍了一种成本低且易于实现的解决方案，扩大了事务处理器 (TRP) 与读取器装置之间的通信距离。

TMS3705 无源天线解决方案 TI 的低频应答器技术可以将简易的无源天线与任意长度的天线电缆配合使用。此解决方案可大大降低系统成本，原因在于可以将收发器的有源器件添加到现有的主机系统中，例如车辆的车身控制模块 (BCM)。

在低频读取器中集成了 TIRIS 射频模块 TMS3705A 简介 TIRIS 包含一个或多个应答器和一个读取器。本应用手册中介绍的读取器通常包含读取器天线、射频模块和控制模块。

更多文献

无线连接三合一套件概述 在 TI，我们致力于提供广泛的具有超低功耗且易于使用的无线连接解决方案产品系列。借助 TI 创新对您设计的支持，您能够 以无线方式 共享、监视和管理可穿戴设备、家庭和楼宇自动化、制造、智慧城市、医疗保健、汽车等应用的数据。

MSP430™ 超低功耗 MCU 和 TI-RFid 器件 TI 的 MSP430 微控制器和 TI-RFid 器件产品系列非常适合低功耗但功能强大的 RFID 读取器和应答器解决方案。将 MSP430 和 TI-RFid 器件配合使用时，可以帮助射频设计人员以极具竞争力的价格实现低功耗、一流的读取范围和可靠的性能。

8.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.6 商标

TI-RFid, MSP430, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.8 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS3705DDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TMS3705DQ1	Samples
TMS3705EDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TMS3705EQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

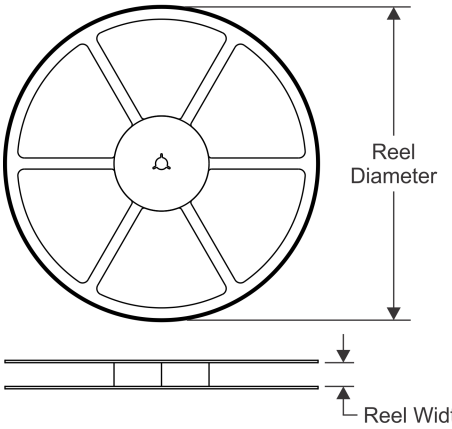
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

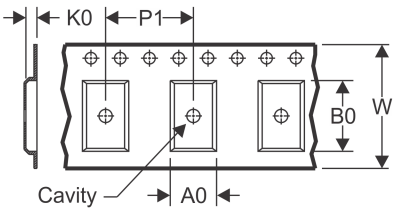
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

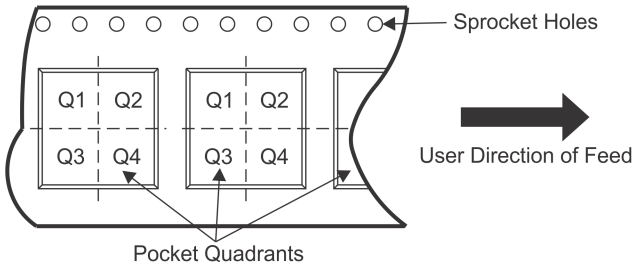


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

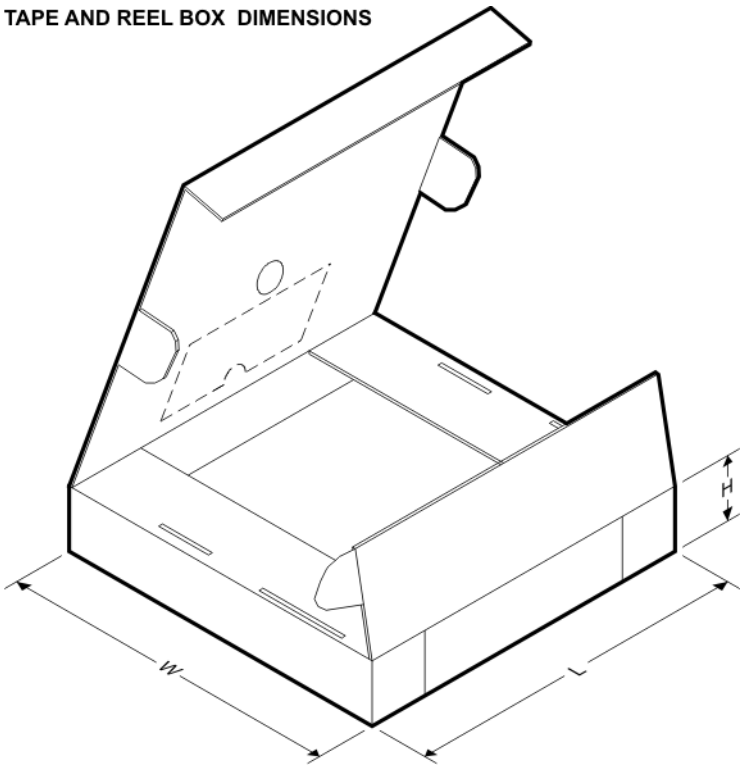
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMS3705DDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TMS3705EDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

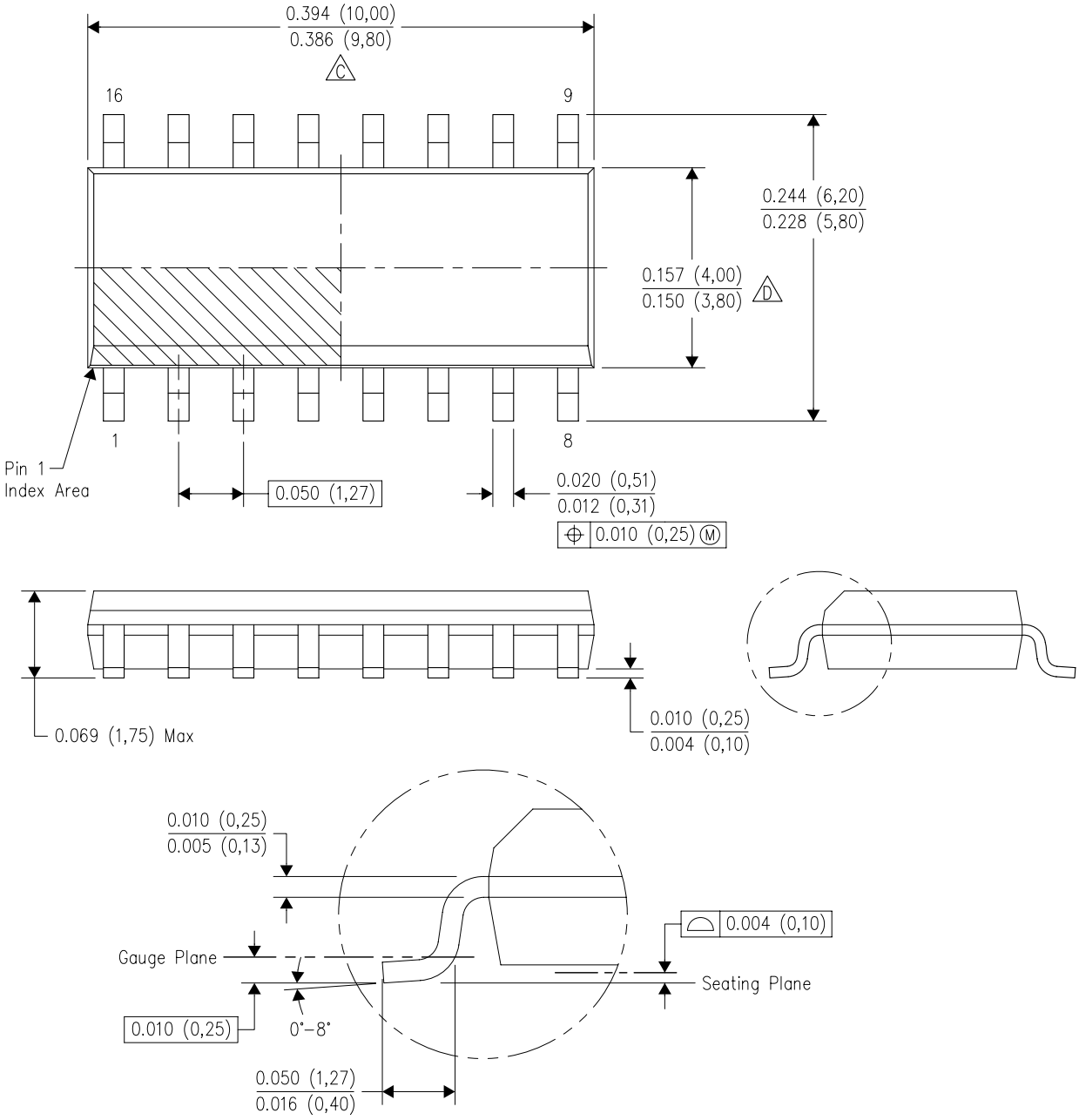
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

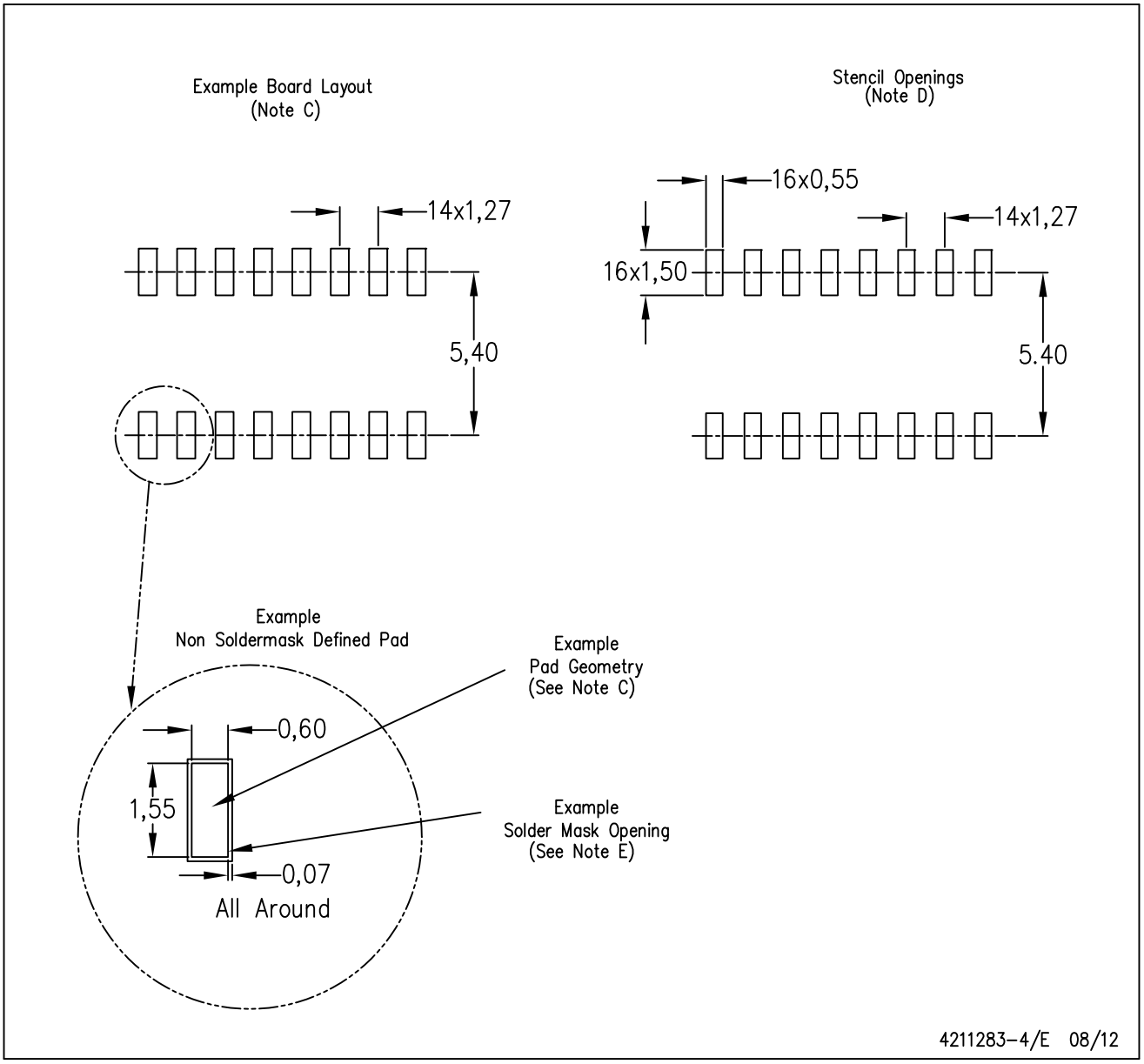
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMS3705DDRQ1	SOIC	D	16	2500	350.0	350.0	43.0
TMS3705EDRQ1	SOIC	D	16	2500	350.0	350.0	43.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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