TMUX1109 5V、±2.5V、低泄漏电流、4:1、2 通道精密多路复用器

1 特性

- 单电源范围：1.08V 至 5.5V
- 双电源范围：±2.75V
- 低泄漏电流：3pA
- 低电荷注入：1pC
- 低导通电阻：1.8Ω
- -40°C 至 +125°C 运行温度
- 兼容 1.8V 逻辑
- 失效防护逻辑
- 轨至轨运行
- 双向信号路径
- 先断后合开关
- ESD 保护 HBM：2000V

2 应用

- 超声波扫描仪
- 患者监护和诊断
- 光纤网络
- 光学测试设备
- 远程无线电单元
- 有线网络
- 自动测试设备 (ATE)
- 工厂自动化和工业控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- 声纳接收器
- 电机驱动器
- 伺服驱动器位置反馈

3 说明

TMUX1109 是精密互补金属氧化物半导体 (CMOS) 多路复用器 (MUX)。TMUX1109 提供差分 4:1 或双路 4:1 单端通道。1.08V 至 5.5V 的宽电源电压工作范围可支持 医疗设备到工业系统的大量应用。该器件可在源极 (Sx) 和漏极 (D) 引脚上支持从 GND 到 V_{DD} 范围的双向模拟和数字信号。所有逻辑输入均具有兼容 1.8V 逻辑的阈值，当器件在有效电源电压范围内运行时，这些阈值可确保 TTL 和 CMOS 逻辑兼容性。失效防护逻辑 电路允许在电源引脚之前的控制引脚上施加电压，从而保护器件免受潜在的损害。

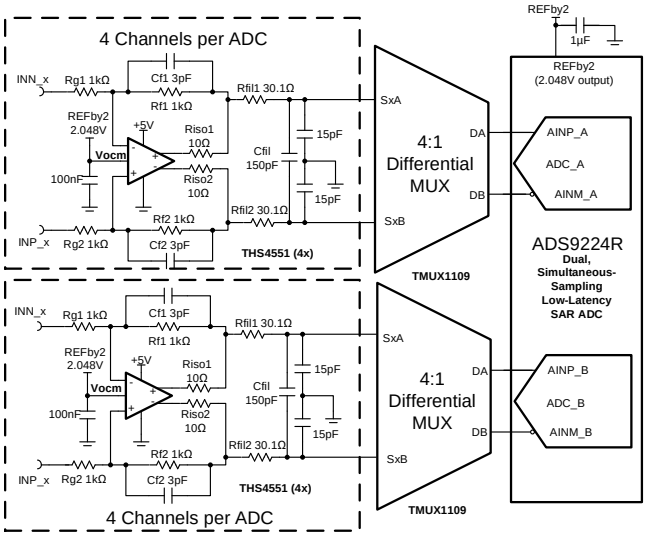
TMUX1109 是精密开关和多路复用器器件系列的一部分。这些器件具有非常低的导通和关断泄漏电流以及较低的电荷注入，因此可用于高精度测量 应用的需要。8nA 的低电源电流和小型封装选项使其可用于便携式应用。

器件信息(1)

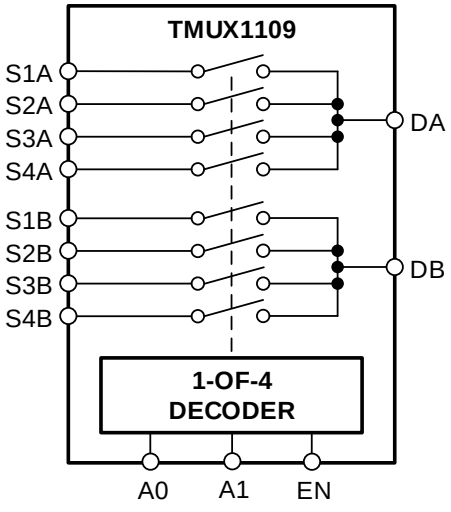
器件型号	封装	封装尺寸（标称值）
TMUX1109	TSSOP (16)	5.00mm × 4.40mm
	QFN (16)	2.60mm x 1.80mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

应用示例



方框图



目录

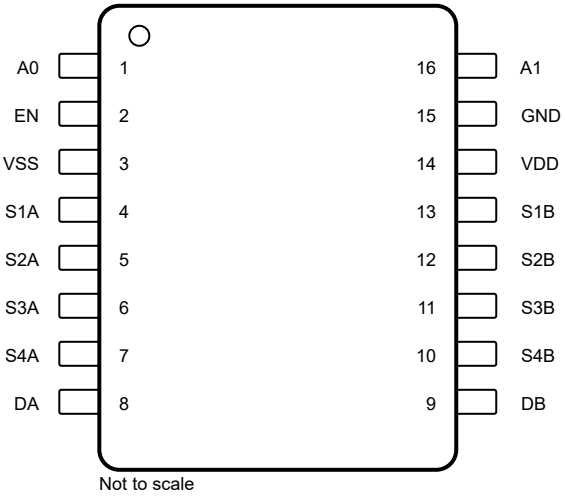
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2018 年 12 月	*	最初发布版本。

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



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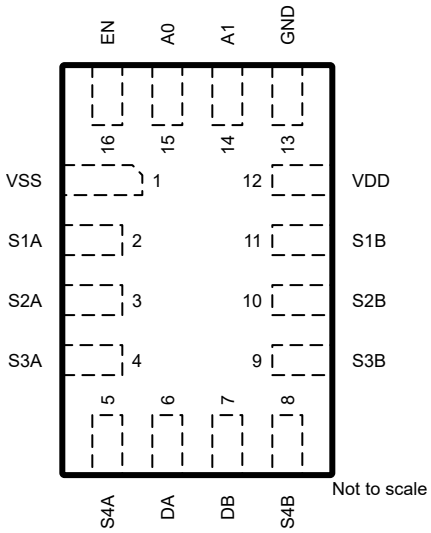
RSV Package
16-Pin QFN
Top View



Not to scale

Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	TSSOP	UQFN		
A0	1	15	I	Address line 0. Controls the switch configuration as shown in 表 1.
EN	2	16	I	Active high logic input. When this pin is low, all switches are turned off. When this pin is high, the A[1:0] address inputs determine which switch is turned on.
VSS	3	1	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND. V_{SS} can be connected to ground for single supply applications.
S1A	4	2	I/O	Source pin 1A. Can be an input or output.
S2A	5	3	I/O	Source pin 2A. Can be an input or output.
S3A	6	4	I/O	Source pin 3A. Can be an input or output.
S4A	7	5	I/O	Source pin 4A. Can be an input or output.
DA	8	6	I/O	Drain pin A. Can be an input or output.
DB	9	7	I/O	Drain pin B. Can be an input or output.
S4B	10	8	I/O	Source pin 4B. Can be an input or output.
S3B	11	9	I/O	Source pin 3B. Can be an input or output.
S2B	12	10	I/O	Source pin 2B. Can be an input or output.
S1B	13	11	I/O	Source pin 1B. Can be an input or output.
VDD	14	12	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	15	13	P	Ground (0 V) reference
A1	16	14	I	Address line 1. Controls the switch configuration as shown in 表 1.

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
V_{DD}–V_{SS}	Supply voltage	–0.5	6	V
V_{DD}		–0.5	6	V
V_{SS}		–3.0	0.3	V
V_{SEL} or V_{EN}	Logic control input pin voltage (EN, A0, A1)	–0.5	6	V
I_{SEL} or I_{EN}	Logic control input pin current (EN, A0, A1)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	–0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)	–30	30	mA
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive power supply voltage (single)	1.08		5.5	V
V_{SS}	Negative power supply voltage (dual)	-2.75		0	V
V_{DD} - V_{SS}	Supply rail voltage difference	1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, Dx)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Logic control input pin voltage	0		5.5	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMUX1109		UNIT
		PW (TSSOP)	RSV (QFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.9	134.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.3	74.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.2	62.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.6	4.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.6	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics (V_{DD} = 5 V ±10 %)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		1.8	4	Ω
			–40°C to +85°C			4.5	Ω
			–40°C to +125°C			4.9	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.18		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.85		Ω
			–40°C to +85°C			1.6	Ω
			–40°C to +125°C			1.6	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1.5 V V_S = 1.5 V / 4.5 V Refer to Off-Leakage Current	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1.5 V V_S = 1.5 V / 4.5 V Refer to Off-Leakage Current	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.75		0.75	nA
			–40°C to +125°C	–3.5		3.5	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 2.5 V Refer to On-Leakage Current	25°C	–0.025	±0.003	0.025	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.75		0.75	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 4.5 V / 1.5 V Refer to On-Leakage Current	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.75		0.75	nA
			–40°C to +125°C	–3		3	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		–40°C to +125°C	1.49		5.5	V
V_{IL}	Input logic low			0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.008		µA
			–40°C to +125°C			1	µA

(1) When V_S is 4.5 V, V_D is 1.5 V, and vice versa.

Electrical Characteristics (V_{DD} = 5 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		14		ns
			–40°C to +85°C			18	ns
			–40°C to +125°C			19	ns
t_{OPEN} (BBM)	Break before make time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		12		ns
			–40°C to +85°C			19	ns
			–40°C to +125°C			20	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		6		ns
			–40°C to +85°C			8	ns
			–40°C to +125°C			9	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–1		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–90		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–80		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		135		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7.5		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		32		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		38		pF

6.6 Electrical Characteristics (V_{DD} = 3.3 V ±10 %)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		4	8.75	Ω
			–40°C to +85°C			9.5	Ω
			–40°C to +125°C			9.75	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.13		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		1.9		Ω
			–40°C to +85°C		2		Ω
			–40°C to +125°C		2.2		Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Off-Leakage Current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Off-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3 V Switch On V_D = V_S = 3 V / 1 V Refer to On-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		–40°C to +125°C	1.35		5.5	V
V_{IL}	Input logic low			0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.006		µA
			–40°C to +125°C			1	µA

(1) When V_S is 3 V, V_D is 1 V, and vice versa.

Electrical Characteristics (V_{DD} = 3.3 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		15		ns
			–40°C to +85°C			23	ns
			–40°C to +125°C			23	ns
t_{OPEN} (BBM)	Break before make time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		9		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		14		ns
			–40°C to +85°C			25	ns
			–40°C to +125°C			25	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		7		ns
			–40°C to +85°C			12	ns
			–40°C to +125°C			12	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–1		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–90		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–80		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		135		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		32		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		38		pF

6.7 Electrical Characteristics (V_{DD} = 2.5 V ±10 %), (V_{SS} = –2.5 V ±10 %)

at T_A = 25°C, V_{DD} = +2.5 V, V_{SS} = –2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = V_{SS} to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		1.8	4	Ω
			–40°C to +85°C			4.5	Ω
			–40°C to +125°C			4.9	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = V_{SS} to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.18		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = V_{SS} to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.85		Ω
			–40°C to +85°C			1.6	Ω
			–40°C to +125°C			1.6	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = +2.5 V, V_{SS} = –2.5 V Switch Off V_D = +2 V / –1 V V_S = –1 V / +2 V Refer to Off-Leakage Current	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = +2.5 V, V_{SS} = –2.5 V Switch Off V_D = +2 V / –1 V V_S = –1 V / +2 V Refer to Off-Leakage Current	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.75		0.75	nA
			–40°C to +125°C	–3.5		3.5	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = +2.5 V, V_{SS} = –2.5 V Switch On V_D = V_S = +2 V / –1 V Refer to On-Leakage Current	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.75		0.75	nA
			–40°C to +125°C	–3		3	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		–40°C to +125°C	1.2		2.75	V
V_{IL}	Input logic low			0		0.73	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 2.75 V	25°C		0.008		µA
			–40°C to +125°C			1	µA
I_{SS}	V_{SS} supply current	Logic inputs = 0 V or 2.75 V	25°C		0.008		µA
			–40°C to +125°C			1	µA

(1) When V_S is positive, V_D is negative, and vice versa.

Electrical Characteristics (V_{DD} = 2.5 V ±10 %), (V_{SS} = –2.5 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = +2.5 V, V_{SS} = –2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1.5 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		14		ns
			–40°C to +85°C			21	ns
			–40°C to +125°C			21	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1.5 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 1.5 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		14		ns
			–40°C to +85°C			21	ns
			–40°C to +125°C			22	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 1.5 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		8		ns
			–40°C to +85°C			11	ns
			–40°C to +125°C			12	ns
Q_C	Charge Injection	V_S = –1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–1		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–90		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–80		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		135		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		32		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		38		pF

6.8 Electrical Characteristics (V_{DD} = 1.8 V ±10 %)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		40		Ω
			–40°C to +85°C			80	Ω
			–40°C to +125°C			80	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.98 V Switch Off V_D = 1.62 V / 1 V V_S = 1 V / 1.62 V Refer to Off-Leakage Current	25°C	–0.05	±0.003	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.98 V Switch Off V_D = 1.62 V / 1 V V_S = 1 V / 1.62 V Refer to Off-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98 V Switch On V_D = V_S = 1.62 V / 1 V Refer to On-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low			0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.001		µA
			–40°C to +125°C			0.85	µA

(1) When V_S is 1.62 V, V_D is 1 V, and vice versa.

Electrical Characteristics (V_{DD} = 1.8 V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		28		ns
			–40°C to +85°C			48	ns
			–40°C to +125°C			48	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		16		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		28		ns
			–40°C to +85°C			48	ns
			–40°C to +125°C			48	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		16		ns
			–40°C to +85°C			27	ns
			–40°C to +125°C			27	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–0.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–90		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–80		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		135		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		32		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		38		pF

6.9 Electrical Characteristics (V_{DD} = 1.2 V ±10 %)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1 V / 0.8 V V_S = 0.8 V / 1 V Refer to Off-Leakage Current	25°C	–0.05	±0.003	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1 V / 0.8 V V_S = 0.8 V / 1 V Refer to Off-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32 V Switch On V_D = V_S = 1 V / 0.8 V Refer to On-Leakage Current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		–40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low			0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.001		µA
			–40°C to +125°C			0.7	µA

(1) When V_S is 1 V, V_D is 0.8 V, and vice versa.

Electrical Characteristics (V_{DD} = 1.2 V ±10 %) (continued)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Transition Time	25°C		60		ns
			–40°C to +85°C			210	ns
			–40°C to +125°C			210	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Break-Before-Make	25°C		28		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		60		ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			190	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to $t_{ON(EN)}$ and $t_{OFF(EN)}$	25°C		45		ns
			–40°C to +85°C			150	ns
			–40°C to +125°C			150	ns
Q_C	Charge Injection	V_S = 1 V R_S = 0 Ω, C_L = 1 nF Refer to Charge Injection	25°C		–0.5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–90		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–80		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		135		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		32		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		38		pF

6.10 Typical Characteristics

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

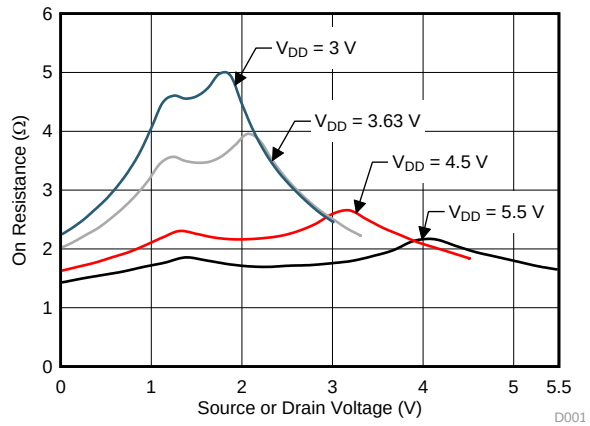


图 1. On-Resistance vs Source or Drain Voltage

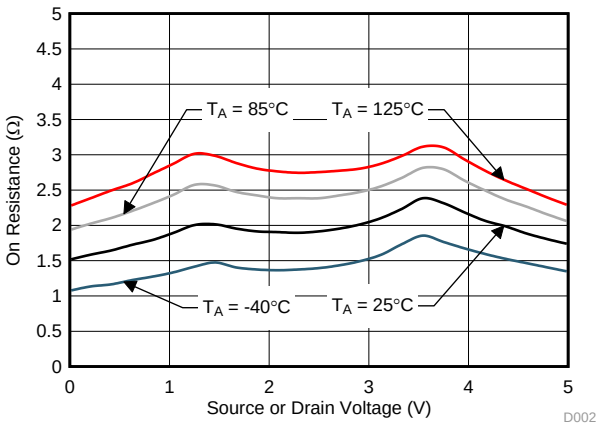


图 2. On-Resistance vs Temperature

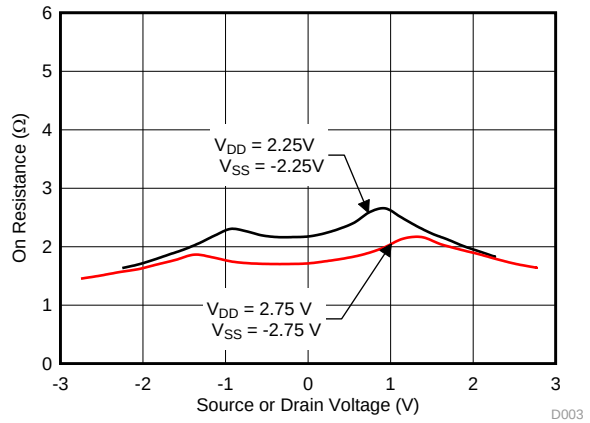


图 3. On-Resistance vs Source or Drain Voltage

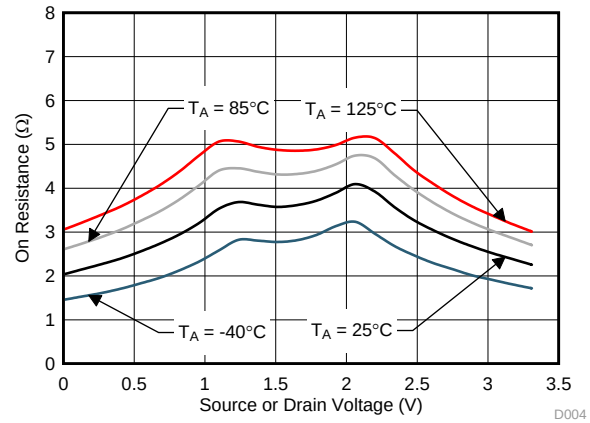


图 4. On-Resistance vs Temperature

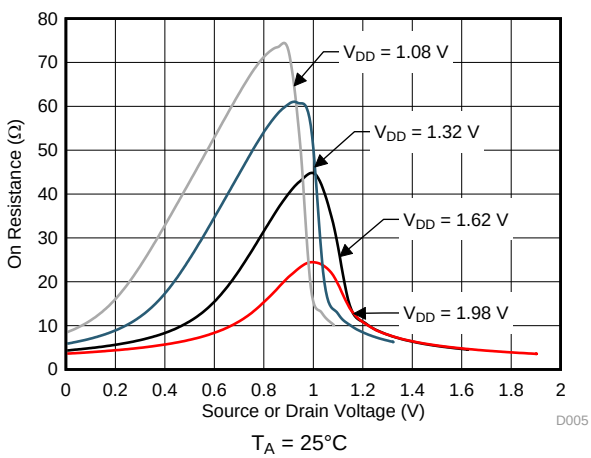


图 5. On-Resistance vs Source or Drain Voltage

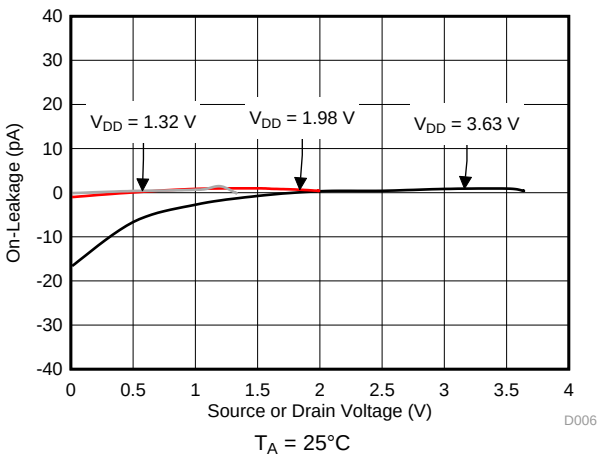
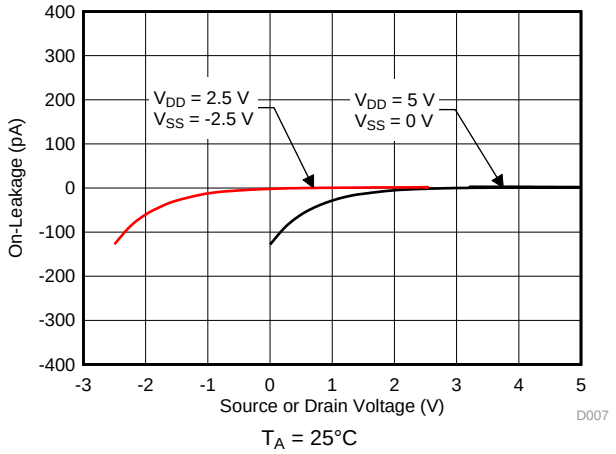


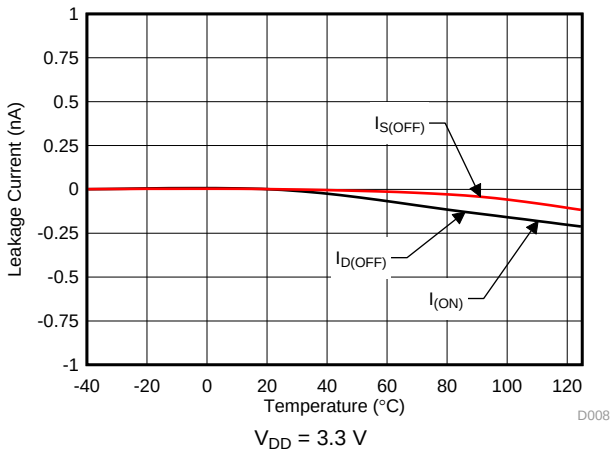
图 6. On-Leakage vs Source or Drain Voltage

Typical Characteristics (接下页)



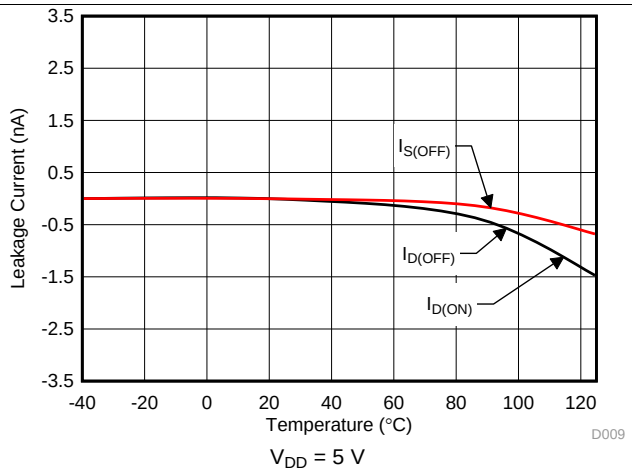
T_A = 25°C

图 7. On-Leakage vs Source or Drain Voltage



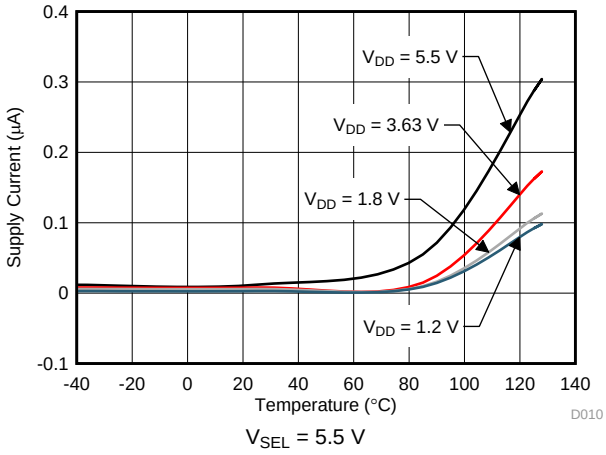
V_{DD} = 3.3 V

图 8. Leakage Current vs Temperature



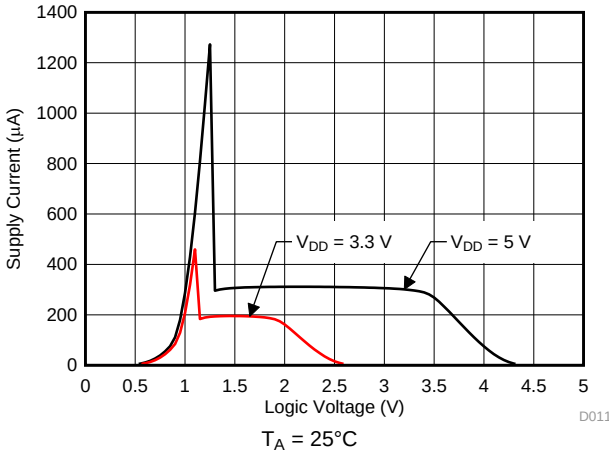
V_{DD} = 5 V

图 9. Leakage Current vs Temperature



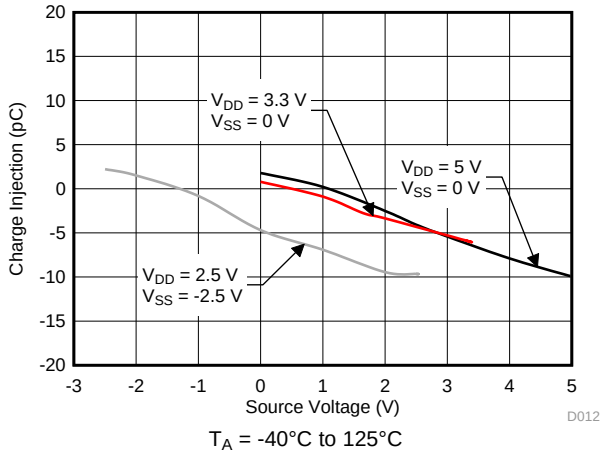
V_{SEL} = 5.5 V

图 10. Supply Current vs Temperature



T_A = 25°C

图 11. Supply Current vs Logic Voltage



T_A = -40°C to 125°C

图 12. Charge Injection vs Source or Drain Voltage

Typical Characteristics (接下页)

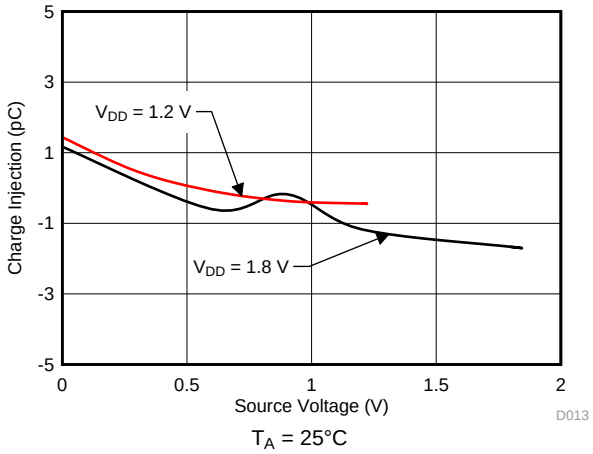


图 13. Charge Injection vs Source or Drain Voltage

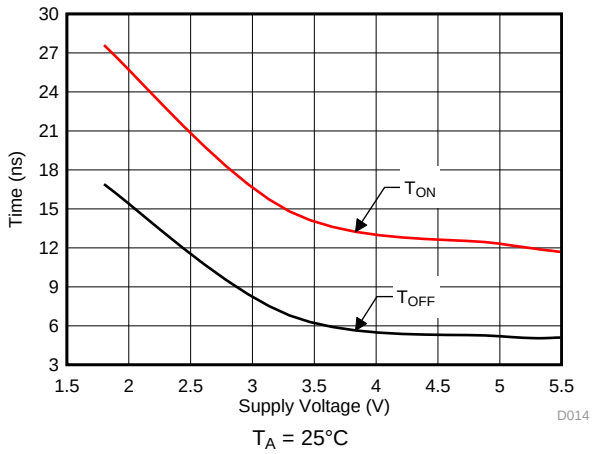


图 14. $T_{ON\ (EN)}$ and $T_{OFF\ (EN)}$ vs Supply Voltage

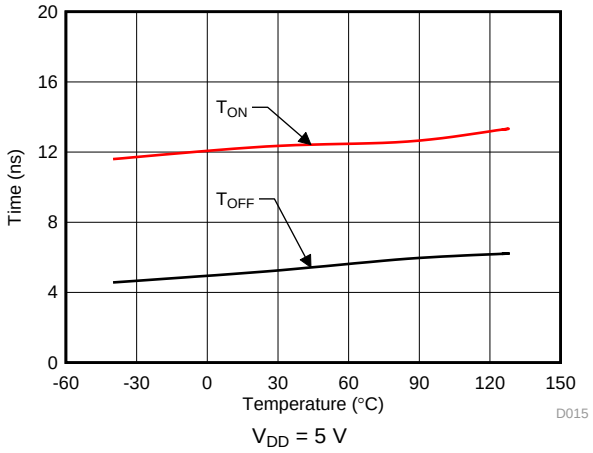


图 15. $T_{ON\ (EN)}$ and $T_{OFF\ (EN)}$ vs Temperature

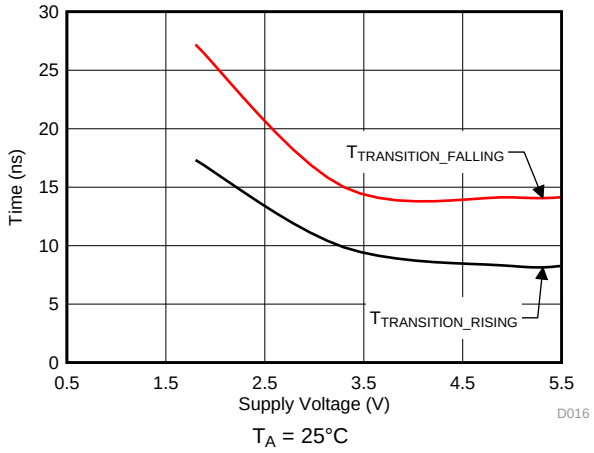


图 16. $T_{TRANSITION}$ vs Supply Voltage

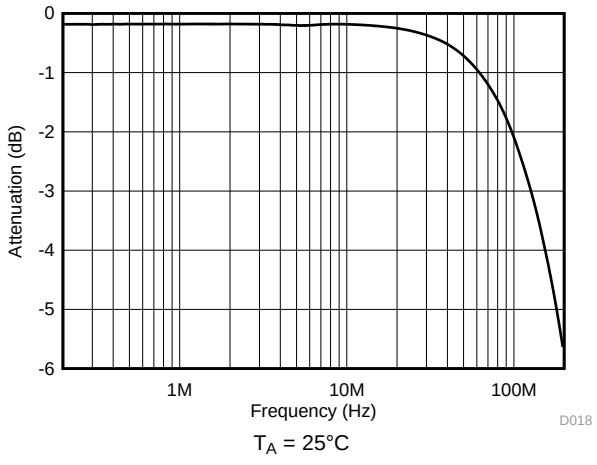


图 17. Frequency Response

7 Detailed Description

7.1 Overview

7.1.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 18. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

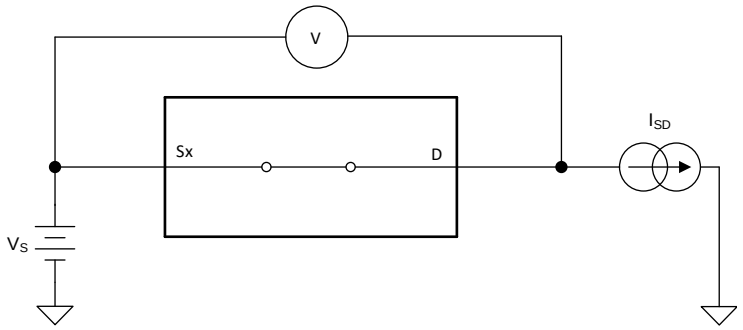


图 18. On-Resistance Measurement Setup

7.1.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 图 19.

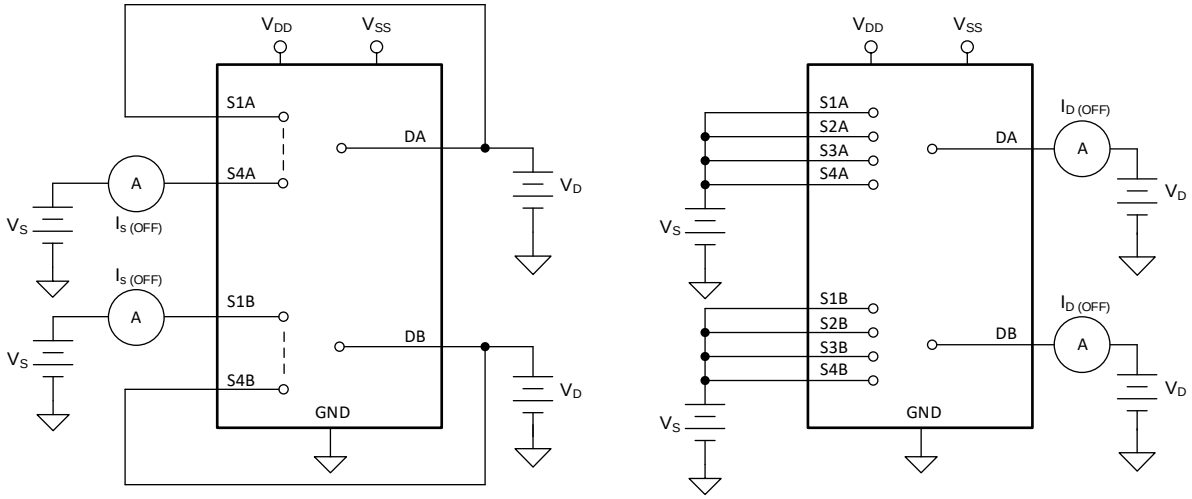


图 19. Off-Leakage Measurement Setup

Overview (接下页)

7.1.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 20 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

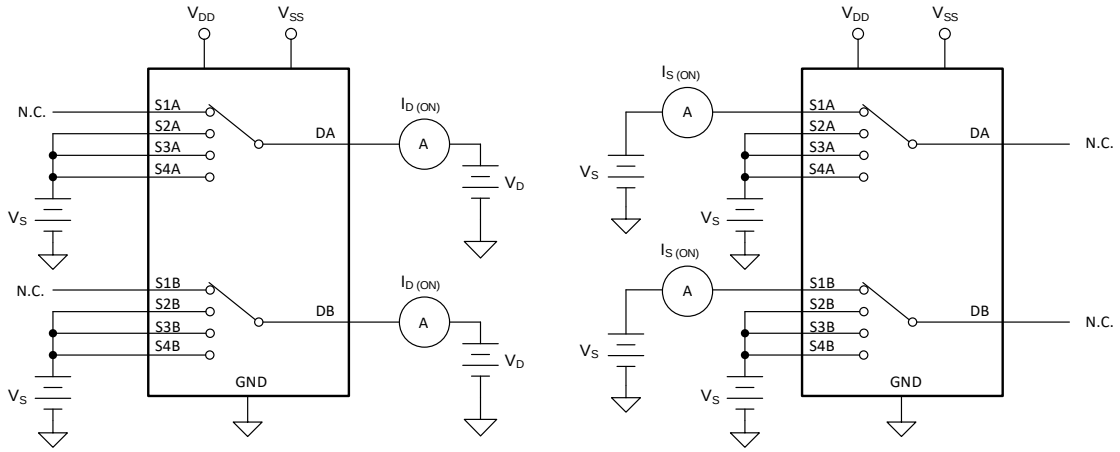


图 20. On-Leakage Measurement Setup

7.1.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. 图 21 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

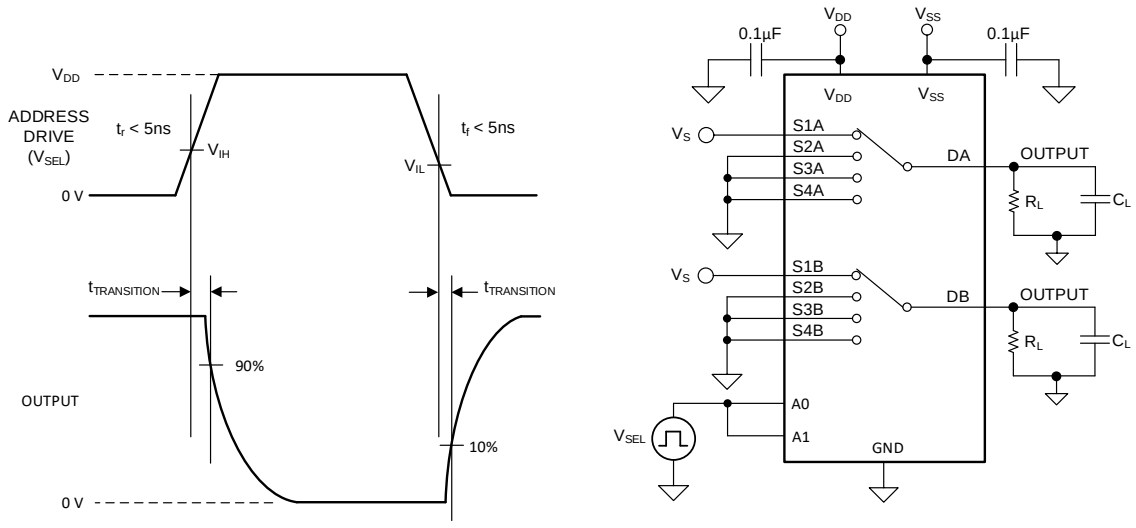


图 21. Transition-Time Measurement Setup

Overview (接下页)

7.1.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 22 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

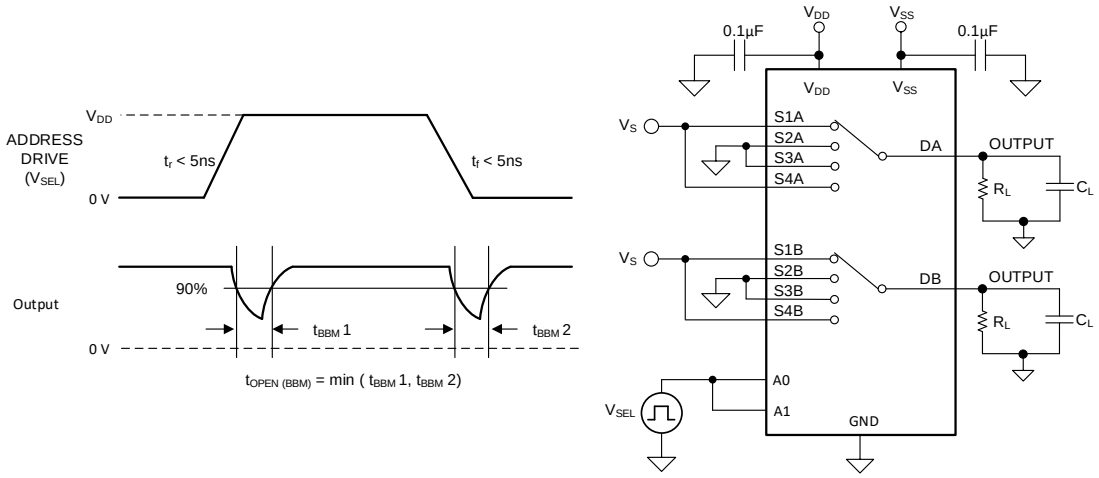


图 22. Break-Before-Make Delay Measurement Setup

7.1.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the logic threshold. The 10% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. 图 23 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the logic threshold. The 90% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. 图 23 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

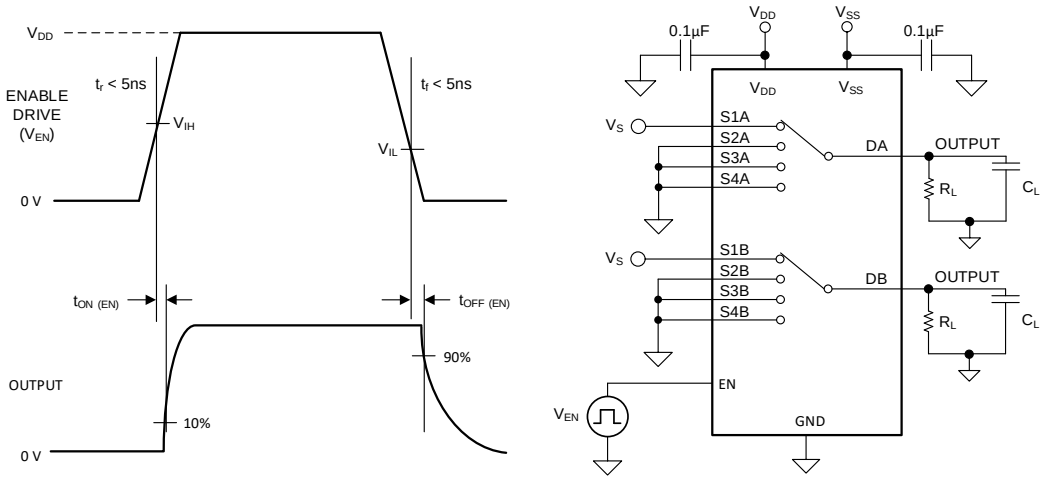


图 23. Turn-On and Turn-Off Time Measurement Setup

Overview (接下页)

7.1.7 Charge Injection

The TMUX1109 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 图 24 shows the setup used to measure charge injection from source (Sx) to drain (D).

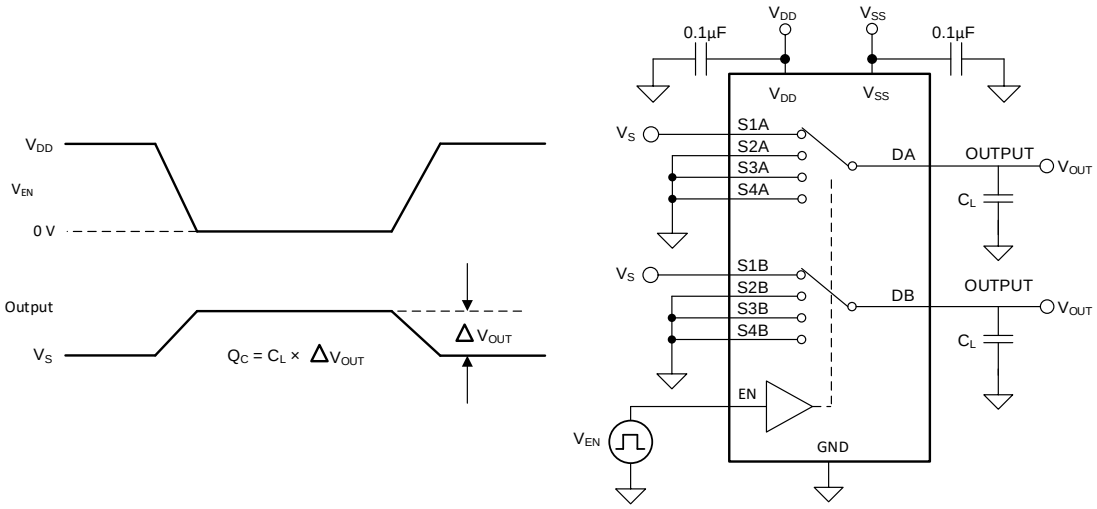


图 24. Charge-Injection Measurement Setup

7.1.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 25 shows the setup used to measure and the equation used to compute off isolation.

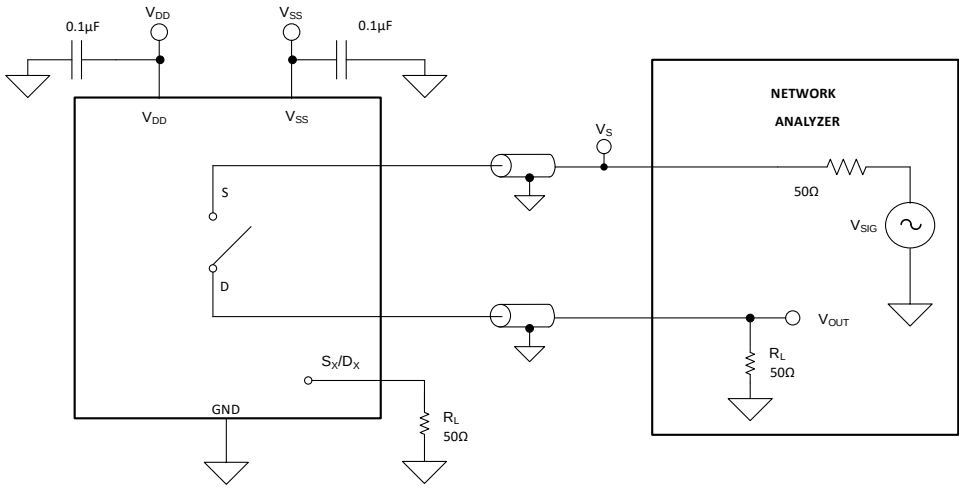


图 25. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

Overview (接下页)

7.1.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 26 shows the setup used to measure, and the equation used to compute crosstalk.

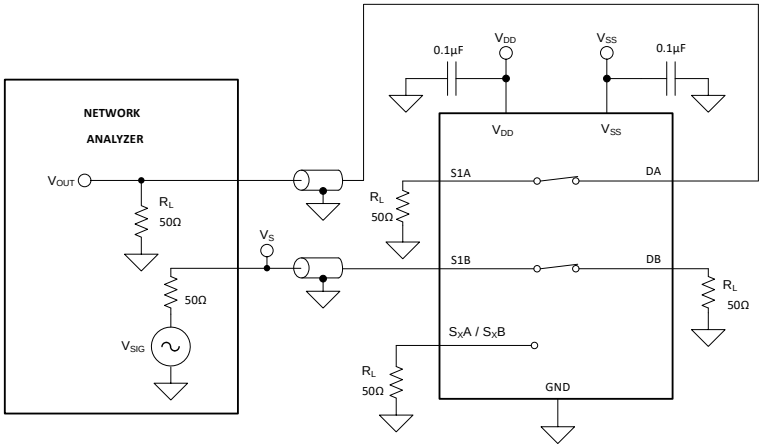


图 26. Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.1.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 27 shows the setup used to measure bandwidth.

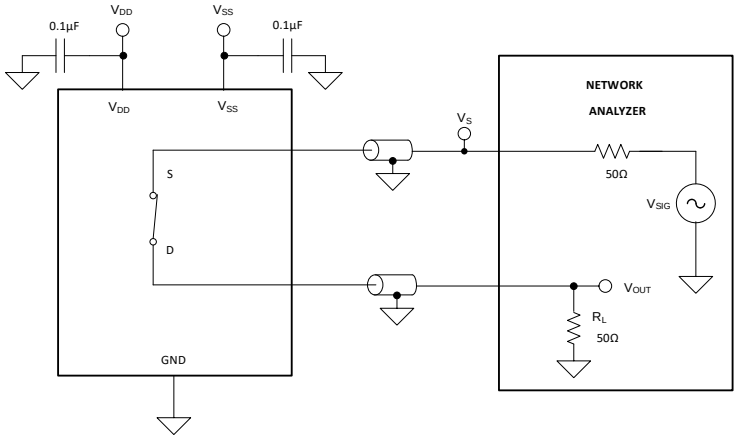


图 27. Bandwidth Measurement Setup

7.2 Functional Block Diagram

The TMUX1109 is an 4:1, differential (2-channel), multiplexer. Each switch is turned on or off based on the state of the address lines and enable pin.

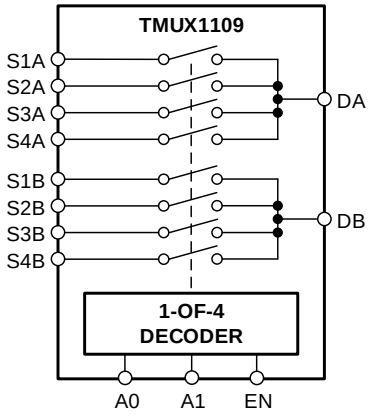


图 28. TMUX1109 Functional Block Diagram

7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX1109 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1109 ranges from V_{SS} to V_{DD}.

7.3.3 1.8 V Logic Compatible Inputs

The TMUX1109 has 1.8-V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allows the TMUX1109 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*

7.3.4 Fail-Safe Logic

The TMUX1109 supports Fail-Safe Logic on the control input pins (EN, A0, A1) allowing for operation up to 5.5 V above V_{SS}, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX1109 to be ramped to 5.5 V while V_{DD} = 0 V. Additionally, the feature enables operation of the TMUX1109 with V_{DD} = 1.2 V while allowing the select pins to interface with a logic level of another device up to 5.5 V.

Feature Description (接下页)

7.3.5 Ultra-low Leakage Current

The TMUX1109 provides extremely low on-leakage and off-leakage currents. The TMUX1109 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. 图 29 shows typical leakage currents of the TMUX1109 versus temperature.

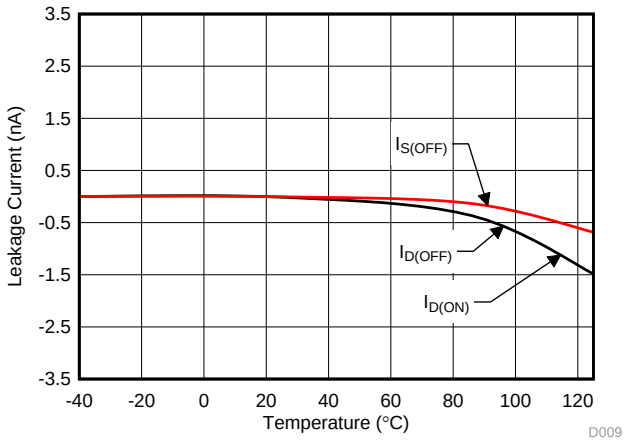


图 29. Leakage Current vs Temperature

7.3.6 Ultra-low Charge Injection

The TMUX1109 has a transmission gate topology, as shown in 图 30. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

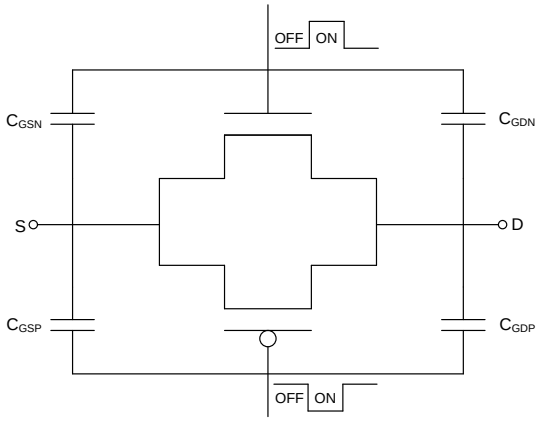


图 30. Transmission Gate Topology

The TMUX1109 has special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to as low as 1 pC at V_S = 1 V as shown in 图 31.

Feature Description (接下页)

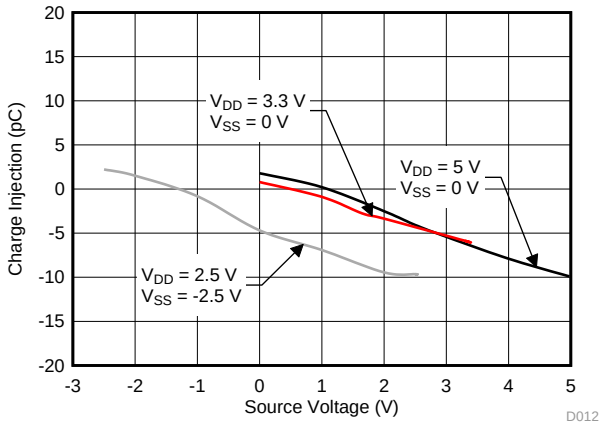


图 31. Charge Injection vs Source Voltage

7.4 Device Functional Modes

When the EN pin of the TMUX1109 is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state regardless of the state of the address lines.

7.4.1 Truth Tables

表 1. TMUX1109 Truth Table

EN	A1	A0	Selected Input Connected To Drain (DA, DB) Pins
0	X(1)	X(1)	All channels are off
1	0	0	S1A and S1B
1	0	1	S2A and S2B
1	1	0	S3A and S3B
1	1	1	S4A and S4B

(1) X denotes *don't care*.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMUX11xx family offers ulta-low input/output leakage currents and low charge injection. These devices operate up to 5.5 V, and offer true rail-to-rail input and output. The TMUX1109 has a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, robust, high-performance analog multiplexer for low-voltage applications.

8.2 Typical Application

图 32 shows a 16-bit, simultaneous-sampling data-acquisition system. This example is typical in industrial applications that require sampling simultaneous signals such as Optical Modules, Analog Input Modules, and Motor Drive circuits for position feedback. The circuit uses eight Fully Differential Amplifiers (FDAs), a 16-bit, 3-MSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a two differential precision multiplexers. Refer to *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* for more information.

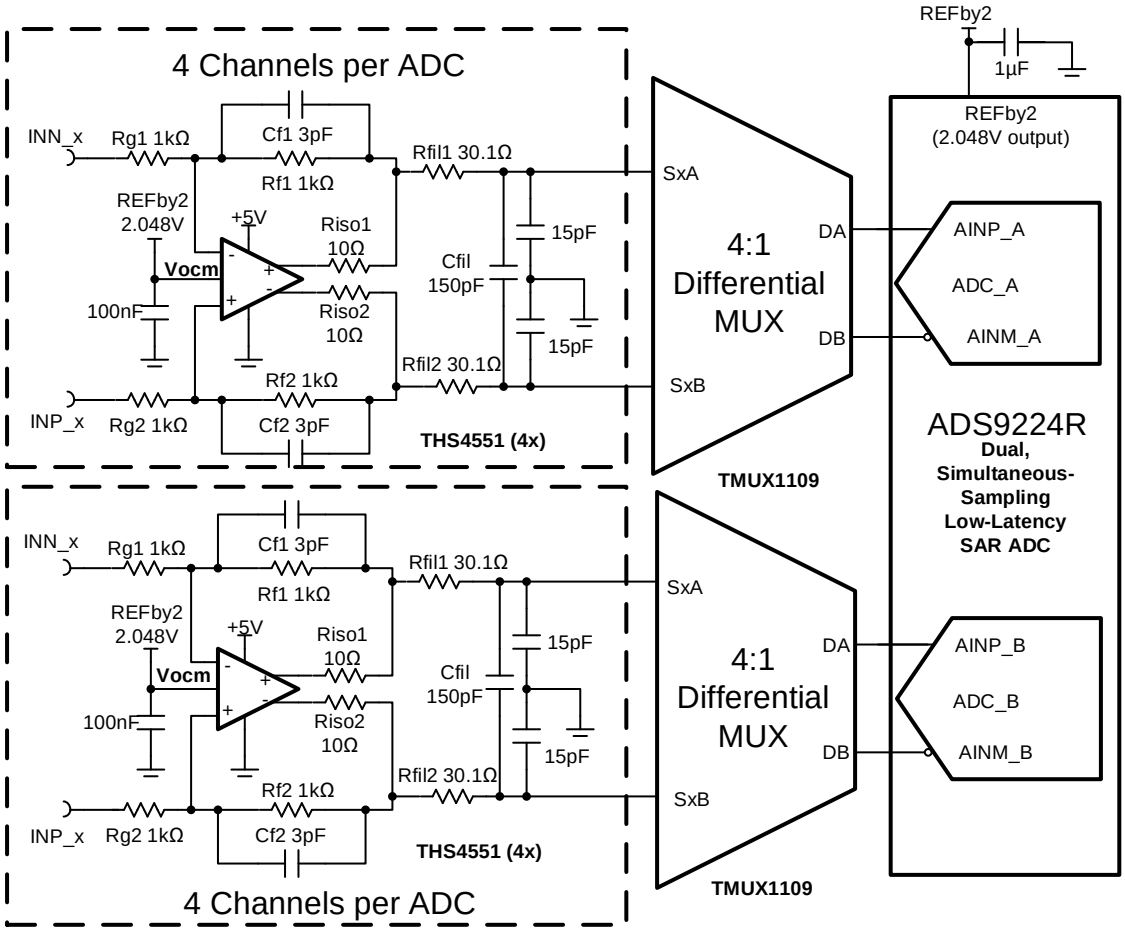


图 32. Simultaneous-Sampling ADC Circuit

8.3 Design Requirements

For this design example, use the parameters listed in 表 2.

表 2. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	5 V
Vref	4.096 V
Vocm	2.048 V
Max Differential Voltage	3.636 V
Control logic thresholds	1.8 V compatible

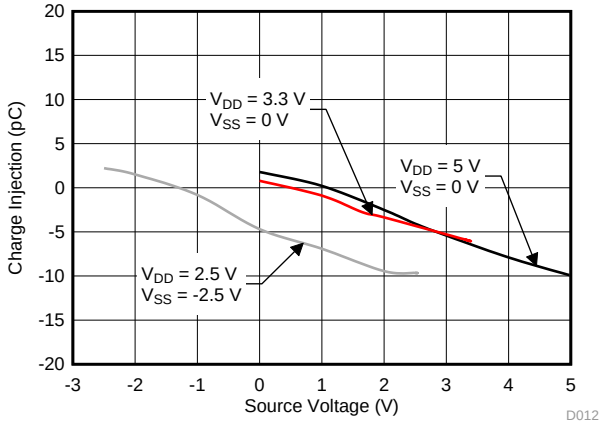
8.4 Detailed Design Procedure

The TMUX1109 can be operated without any external components except for the supply decoupling capacitors. If the device desired power-up state is disabled, the enable pin should have a weak pull-down resistor and be controlled by the MCU via GPIO. All inputs being muxed to the ADC must fall within the recommend operating conditions of the TMUX1109 including signal range and continuous current. System level design and component selection are made according to *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit*.

1. The ADS9224R was selected because of the dual simultaneous sampling and high throughput (3-MSPS).
2. The TMUX1109 4:1 (2x) multiplexer was selected to support 4 differential inputs for each ADC.
3. Find ADC full-scale range, resolution and common-mode range specifications.
4. Determine the linear range of the FDA (THS4551) based on common-mode and output swing specification.
5. Select COG capacitors for all filter capacitors at the ADC input to minimize distortion.
6. Select the FDA gain resistors RF1,2 , RG1,2. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift and to minimize distortion.
7. *Introduction to SAR ADC Front-End Component Selection* covers the methods for selecting the charge bucket circuit Rfil1, Rfil1 and Cfil. These component values are dependent on the amplifier bandwidth, data converter sampling rare, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected.
8. The THS4551 is commonly used in high-speed precision fully differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling, and multiplexer charge injection and provides the common-mode level shifting to the voltage range of the SAR ADC.
9. The TMUX1109 is used in high-speed precision fully differential SAR applications as it has sufficient bandwidth, low charge injection, and low on-resistance and capacitance. Low capacitance supports fast switching between channels and allows the system to settle within required precision in the specified timing.

8.5 Application Curve

Charge injection impacts system performance and settling characteristics of the charge bucket circuit. A multiplexer with low charge injection and a flat response across input voltage allows the system to settle to the required precision during the ADC acquisition period. 图 33 shows the flat charge injection of the TMUX1109 at multiple supply voltages.



T_A = 25°C

图 33. Charge Injection vs Source Voltage

9 Power Supply Recommendations

The TMUX1109 operates across a wide supply range of 1.08 V to 5.5 V, or ±2.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} and $_{SS}$ supplies to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} and V_{SS} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

10 Layout

10.1 Layout Guidelines

10.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.图 34 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

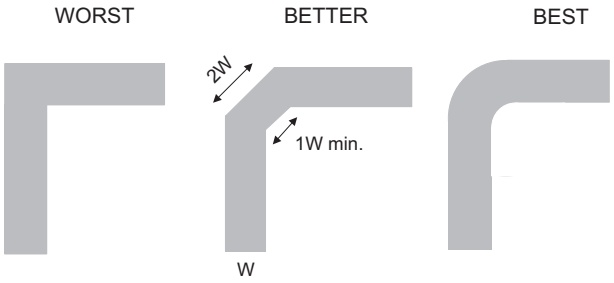


图 34. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 35 illustrates an example of a PCB layout with the TMUX1109. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

10.2 Layout Example

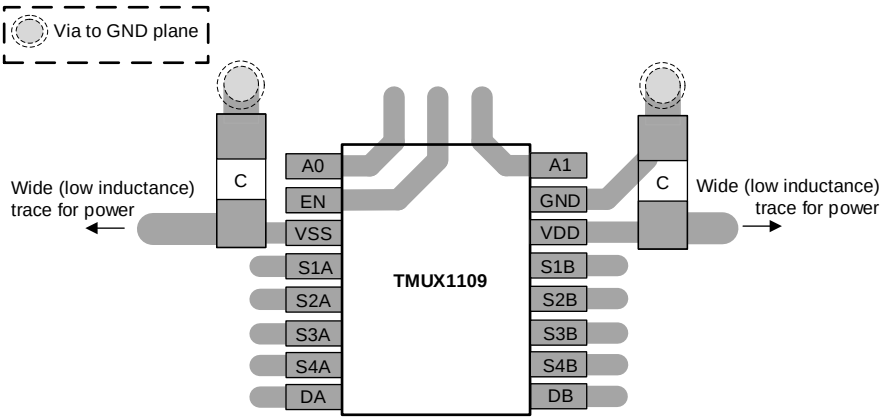


图 35. TMUX1109 Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

德州仪器 (TI)，*《真差分 4 x 2 多路复用器、模拟前端、同步采样 ADC 电路》*。

德州仪器 (TI)，*《使用低 CON 多路复用器改善稳定性问题》*。

德州仪器 (TI)，*《使用 1.8V 逻辑多路复用器和开关简化设计》*。

德州仪器 (TI)，*《利用关断保护信号开关消除电源排序》*。

德州仪器 (TI)，*《高电压模拟多路复用器的系统级保护》*。

德州仪器 (TI)，*《QFN/SON PCB 连接》*。

Texas Instruments, *《四方扁平封装无引线逻辑封装》*。

11.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

E2E is a trademark of Texas Instruments.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX1109PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM1109	Samples
TMUX1109RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1D1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

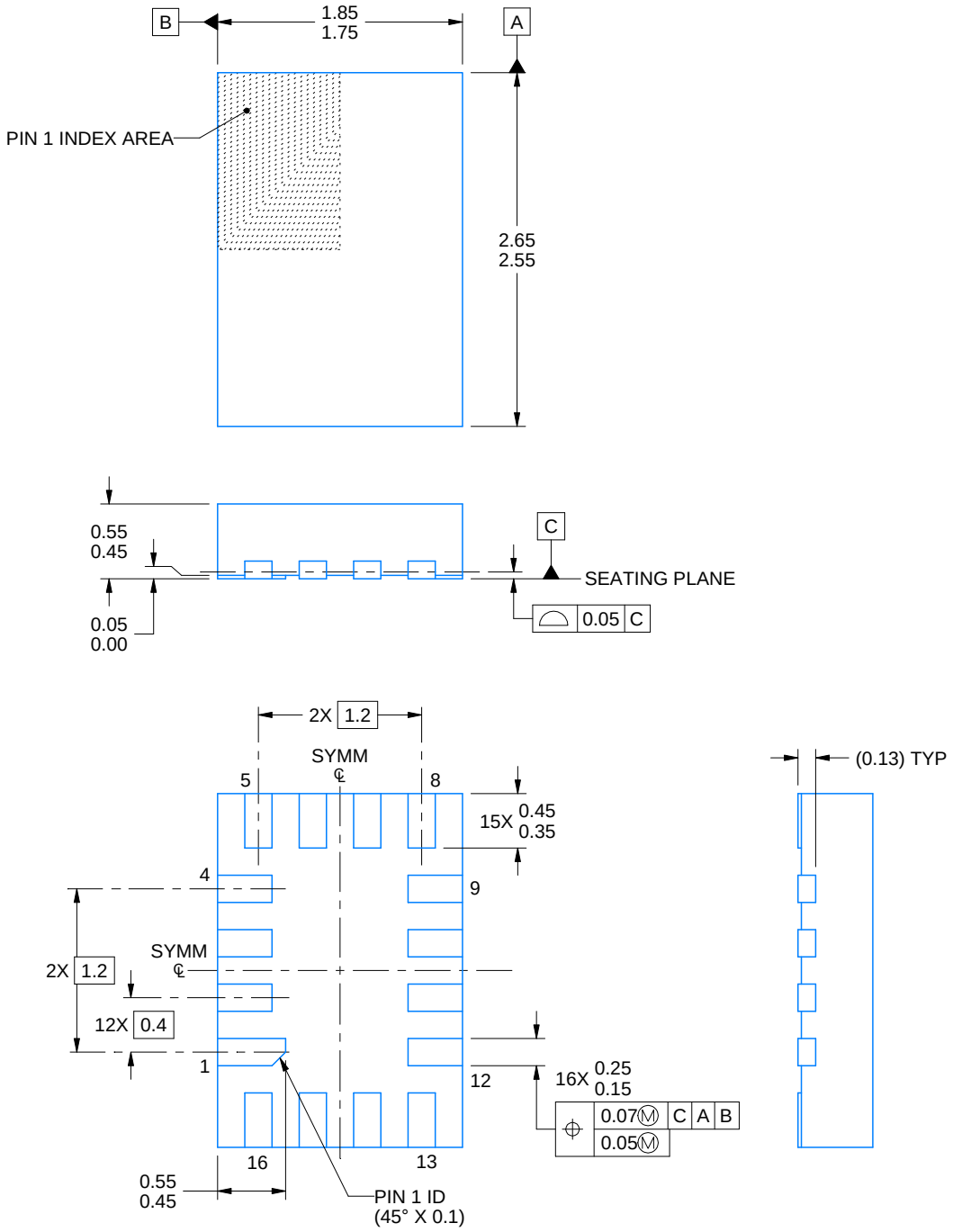
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RSV0016A

PACKAGE OUTLINE

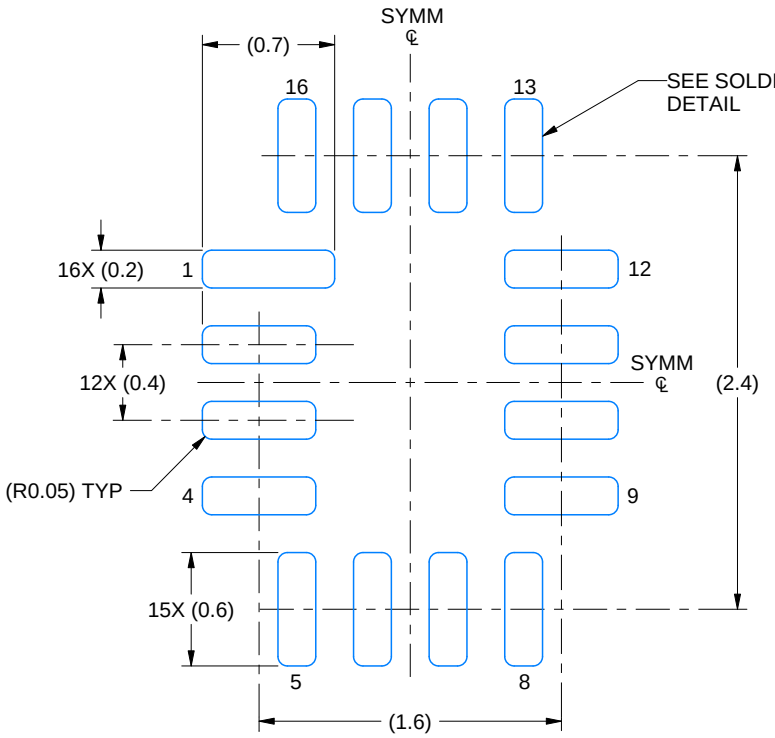
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

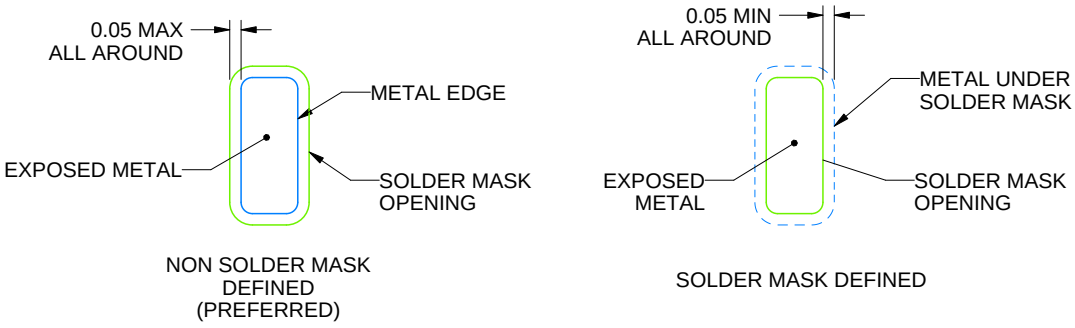


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

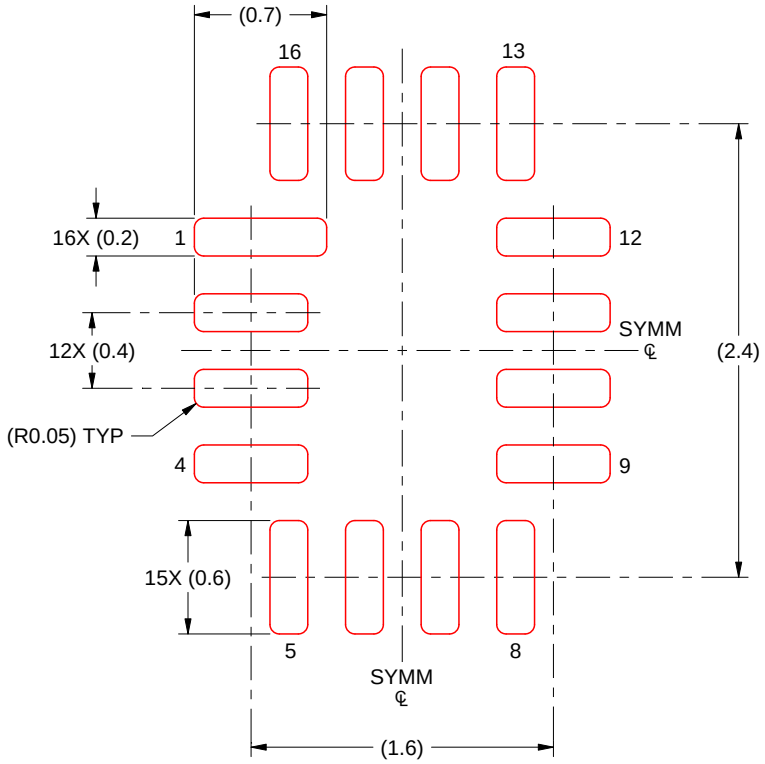


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

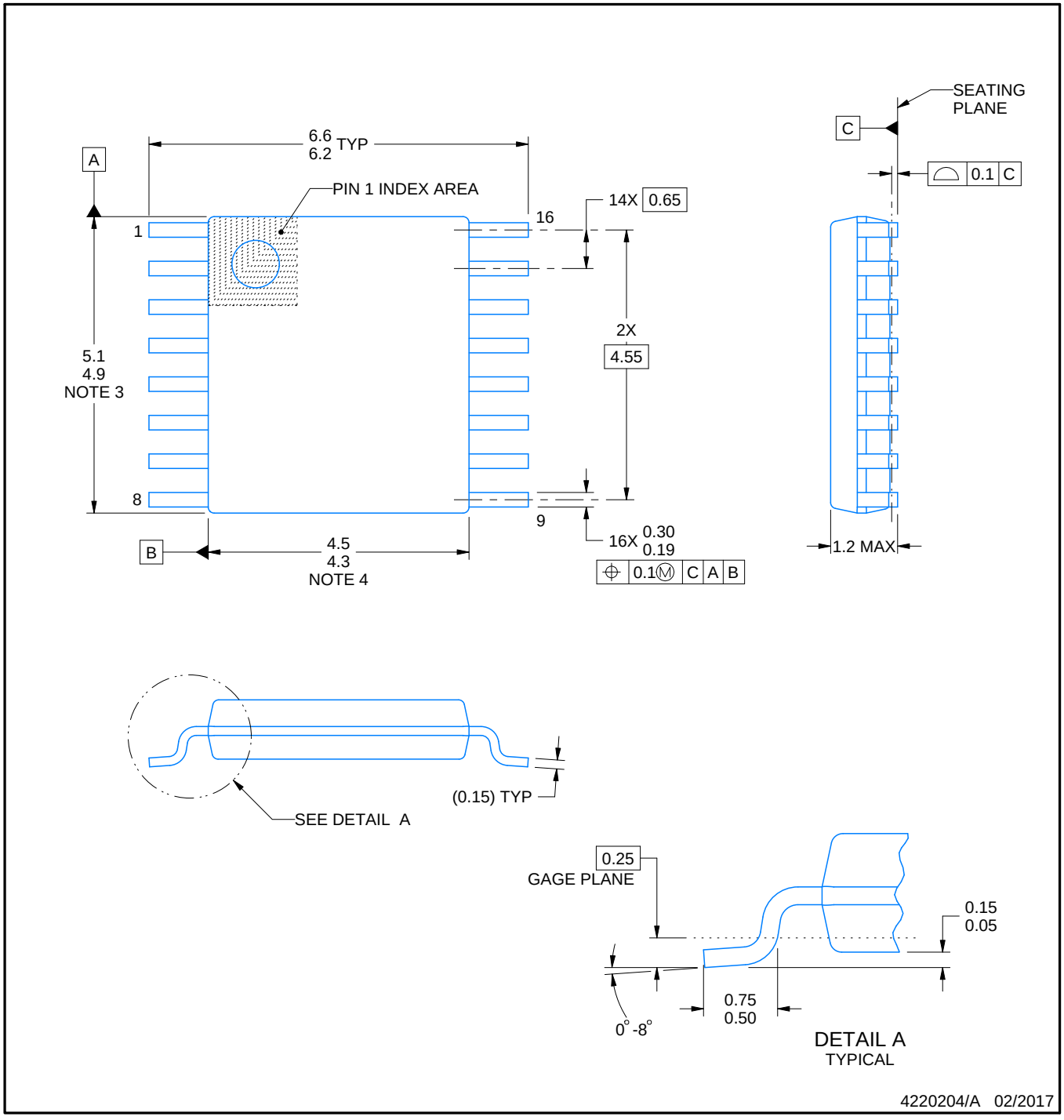
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

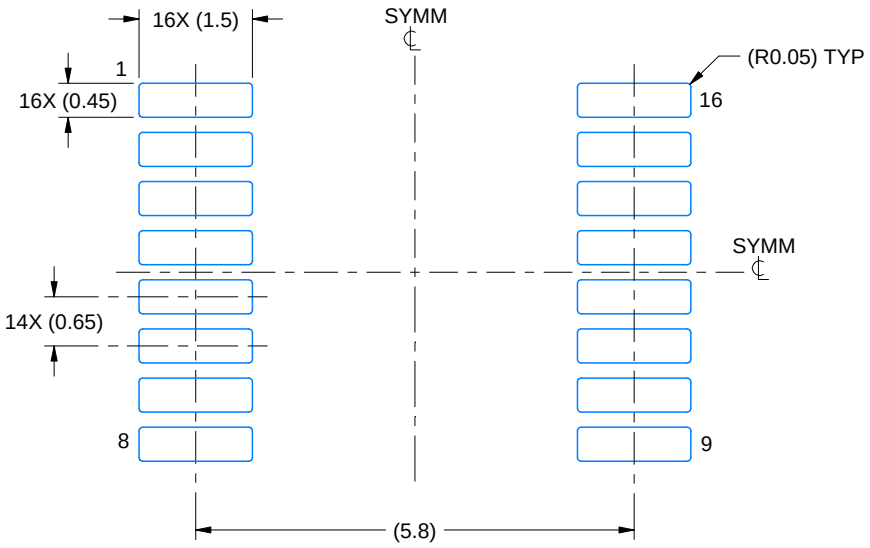
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

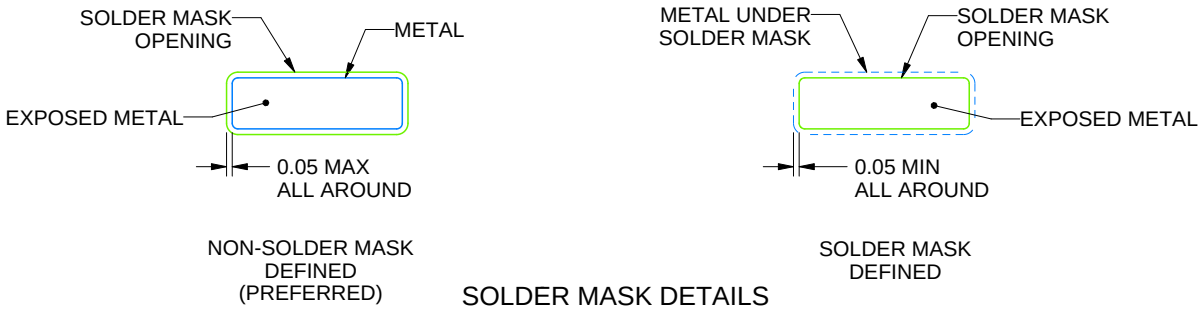


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

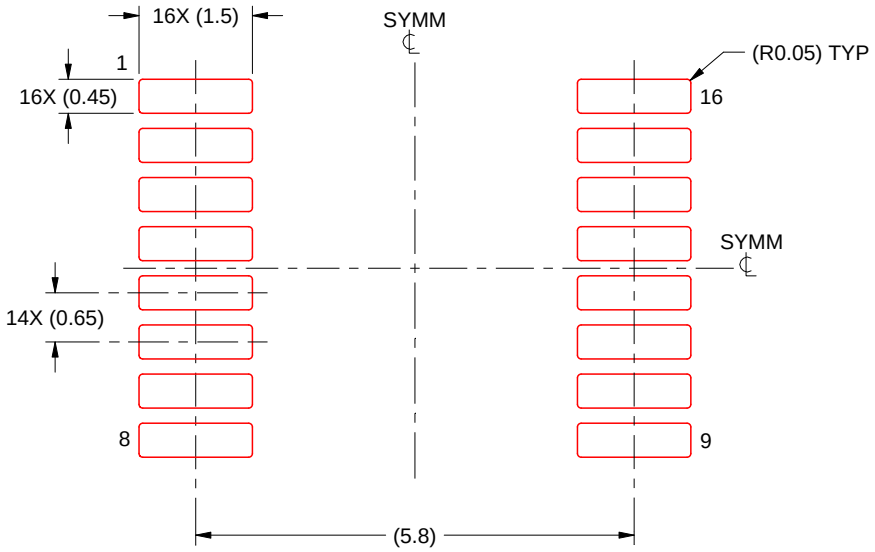


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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