TEXAS INSTRUMENTS

TMUX6136 ±16.5V、低电容、低漏电流、精密双路 SPDT 开关

1 特性

- 宽电源电压范围：±5V 至 ±16.5V（双电源）或 10V 至 16.5V（单电源）
- 所有引脚的闩锁性能都达到 100mA，符合 JESD78 II 类 A 级要求
- 低导通电容：5.5pF
- 低输入漏电流：0.5pA
- 低电荷注入：-0.4 pC
- 轨到轨运行
- 低导通电阻：120 Ω
- 快速转换时间：66ns
- 先断后合开关操作
- SELx 引脚可连接至带集成下拉电阻器的 V_{DD}
- 逻辑电平：2V 至 V_{DD}
- 低电源电流：17µA
- 人体放电模型 (HBM) ESD 保护：所有引脚上均为 ±2kV
- 业界通用 TSSOP 封装

2 应用

- 工厂自动化和工业过程控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- ATE 测试设备
- 数字万用表
- 电池监控系统

3 说明

TMUX6136 是一款具有两个独立可选 SPDT 开关的互补金属氧化物半导体 (CMOS) 模拟开关。该器件在双电源（±5V 至 ±16.5V）、单电源（10V 至 16.5V）或非对称电源供电时均能正常运行。数字选择引脚 (SELx) 具有兼容晶体管到晶体管逻辑 (TTL) 的阈值，这些阈值可确保 TTL/CMOS 逻辑兼容性。
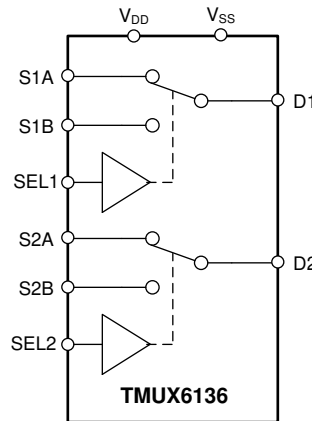
TMUX6136 会根据 SELx 引脚的状态将两个输入 (Sx) 之一切换为共模输出 (D)。每个开关在"ON"位置时在两个方向上表现得都很好，而且支持最高到电源的输入信号范围。在 OFF 状态下，则会阻止最高到电源的信号电平。所有开关都具有先断后合 (BBM) 开关操作。

TMUX6136 是德州仪器 (TI) 精密开关和多路复用器系列中的一款产品。该器件具有非常低的漏电流和电荷注入，因此可用于高精度测量应用。当开关处于 OFF 位置时，该器件还可通过阻断到达电源的信号电平来提供出色的隔离能力。17µA 的低电源电流使其可用于多种便携式应用。

封装信息[1]

器件型号	封装	封装尺寸（标称值）
TMUX6136	PW (TSSOP, 16)	5.00mm × 4.40mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

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简化版原理图

English Data Sheet: SCDS397

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

5 Pin Configuration and Functions
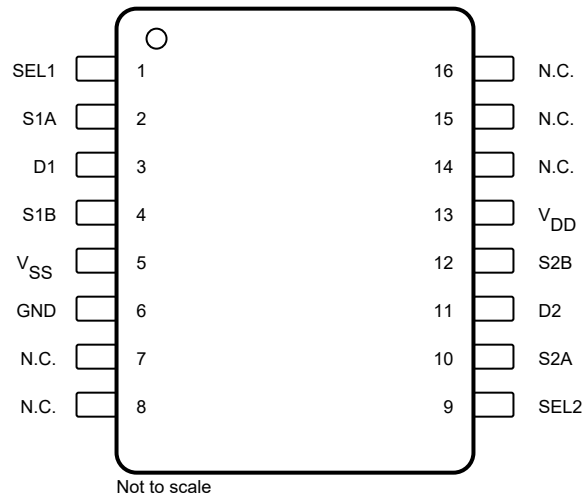
图 5-1. PW Package, 16-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SEL1	1	I	Select line 0
S1A	2	I/O	Source pin 1A. Can be an input or output.
D1	3	I/O	Drain pin D1. Can be an input or output.
S1B	4	I/O	Source pin 1B. Can be an input or output.
V_{SS}	5	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
GND	6		Ground (0 V) reference
N.C.	7, 8, 14, 15, 16	No Connect	No internal connection
SEL2	9	I	Select line 1
S2A	10	I/O	Source pin 2A. Can be an input or output.
D2	11	I/O	Drain pin D2. Can be an input or output.
S2B	12	I/O	Source pin 2B. Can be an input or output.
V_{DD}	13	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.

(1)   I = input, O = output, P = power

Product Folder Links: *TMUX6136*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		36	V
V_{DD} to GND		− 0.3	18	V
V_{SS} to GND		− 18	0.3	V
V_{DIG}	Digital input pin (SEL1, SEL2) voltage	GND − 0.3	V_{DD}+0.3	V
I_{DIG}	Digital input pin (SEL1, SEL2) current	− 30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	V_{SS} − 0.3	V_{DD}+0.3	V
I_{ANA_IN}	Analog input pin (Sx) current	− 30	30	mA
V_{ANA_OUT}	Analog output pin (D) voltage	V_{SS} − 0.3	V_{DD}+0.3	V
I_{ANA_OUT}	Analog output pin (D) current	− 30	30	mA
T_A	Ambient temperature	− 55	140	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	− 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

		TMUX6136	UNIT
	THERMAL METRIC[1]	PW (TSSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to V_{SS} [(1)]	Power supply voltage differential	10		33	V
V_{DD} to GND	Positive power supply voltage (singlle supply, V_{SS} = 0 V)	10		16.5	V
V_{DD} to GND	Positive power supply voltage (dual supply)	5		16.5	V
V_{SS} to GND	Negative power supply voltage (dual supply)	– 16.5		– 5	V
V_S [(1)]	Source pins voltage	V_{SS}		V_{DD}	V
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{DIG}	Digital input pin (SEL1, SEL2) voltage	0		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)	– 25		25	mA
T_A	Ambient temperature	– 40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 10 V $\leqslant$ (V_{DD} – V_{SS}) $\leqslant$ 33 V.

6.5 Electrical Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		T_A = – 40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_S = 1 mA			120	135	Ω
		V_S = ±10 V, I_S = 1 mA			140	160	Ω
			T_A = – 40°C to +85°C			210	Ω
			T_A = – 40°C to +125°C			245	Ω
$\triangle R_{ON}$	On-resistance mismatch between channels	V_S = ±10 V, I_S = 1 mA			2.5	6	Ω
			T_A = – 40°C to +85°C			9	Ω
			T_A = – 40°C to +125°C			11	Ω
R_{ON_FLAT}	On-resistance flatness	V_S = – 10 V, 0 V, +10 V, I_S = 1 mA			23	33	Ω
			T_A = – 40°C to +85°C			35	Ω
			T_A = – 40°C to +125°C			37	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.42		%/°C
$I_{S(OFF)}$	Source off leakage current[(1)]	Switch state is off, V_S = +10 V/ – 10 V, V_D = – 10 V/ + 10 V		– 0.05	0.005	0.05	nA
		Switch state is off, V_S = +10 V/ – 10 V, V_D = – 10 V/ + 10 V	T_A = – 40°C to +85°C	– 0.17		0.1	nA
		Switch state is off, V_S = +10 V/ – 10 V, V_D = – 10 V/ + 10 V	T_A = – 40°C to +125°C	– 1		0.25	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = +10 V/ – 10 V, V_D = – 10 V/ +10 V		– 0.06	0.008	0.06	nA
			T_A = – 40°C to +85°C	– 0.25		0.15	nA
			T_A = – 40°C to +125°C	– 1.6		0.4	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V

Product Folder Links: TMUX6136

6.5 Electrical Characteristics (Dual Supplies: ±15 V) (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{PD(SELx)}$	Pull-down resistance on SELx pins				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			17	21	µA
			T_A = − 40°C to +85°C			22	µA
			T_A = − 40°C to +125°C			23	µA
I_{SS}	V_{SS} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			8	10	µA
			T_A = − 40°C to +85°C			11	µA
			T_A = − 40°C to +125°C			12	µA

(1)   When V_S is positive, V_D is negative, and vice versa.

6.6 Switching Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF		66	78	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = − 40°C to +85°C			107	ns
		V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = − 40°C to +125°C			117	ns
tBBM	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = − 40°C to +125°C	20	40		ns
Q_J	Charge injection	V_S = 0 V, R_S = 0 Ω , C_L = 1 nF		− 0.4		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		− 85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz (Inter-channel: S1x and S2x)		− 105		dB
		R_L = 50 Ω , C_L = 5 pF, f = 1 MHz (Intra-channel: SxA and SxB)		− 92		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		− 7		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{DD}, f= 1 MHz		− 59		dB
		R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{SS}, f= 1 MHz		− 59		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		670		MHz
THD	Total harmonic distortion + noise	R_L = 10 kΩ , C_L = 5 pF, f= 20 Hz to 20 kHz		0.08		%
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.5		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 0 V, f = 1 MHz		2.4	3.3	pF
$C_{S(ON)},$ $C_{D(ON)}$	Source and drain on-capacitance	V_S = 0 V, f = 1 MHz		5.5	7.5	pF

6.7 Electrical Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range			V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_S = 1 mA			235	345	Ω
			T_A = −40°C to +85°C			400	Ω
			T_A = −40°C to +125°C			440	Ω
$\triangle R_{ON}$	On-resistance mismatch between channels	V_S = 10 V, I_S = 1 mA			4	12	Ω
			T_A = −40°C to +85°C			19	Ω
			T_A = −40°C to +125°C			23	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.47		%/°C
$I_{S(OFF)}$	Source off leakage current[1]	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		−0.03	0.005	0.03	nA
			T_A = −40°C to +85°C	−0.1		0.07	nA
			T_A = −40°C to +125°C	−0.8		0.2	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = floating, V_D = 1 V/ 10 V		−0.04	0.01	0.04	nA
			T_A = −40°C to +85°C	−0.16		0.09	nA
			T_A = −40°C to +125°C	−1.2		0.3	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(SELx)}$	Pull-down resistance on SELx pins					6	MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			13	16	µA
			T_A = −40°C to +85°C			17	µA
			T_A = −40°C to +125°C			18	µA

(1)   When V_S is positive, V_D is negative, and vice versa.

6.8 Switching Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF		72	84	ns
		V_S = 8 V, R_L = 300 Ω, C_L = 35 pF, T_A = −40°C to +85°C			117	ns
		V_S = 8 V, R_L = 300 Ω, C_L = 35 pF, T_A = −40°C to +125°C			128	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF, T_A = −40°C to +125°C	20	40		ns
Q_J	Charge injection	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF		−0.7		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		-85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz (Inter-channel: S1x and S2x)		−110		dB
		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz (Intra-channel: SxA and SxB)		−95		dB
I_L	Insertion loss	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		−13		dB

Product Folder Links: *TMUX6136*

6.8 Switching Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ, C_L = 5 pF, V_{PP} = 0.62 V, f = 1 MHz		-58		dB
BW	-3dB Bandwidth	R_L = 50 Ω, C_L = 5 pF		650		MHz
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.7		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 6 V, f = 1 MHz		2.6	3.7	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 6 V, f = 1 MHz		6.3	8.5	pF

Product Folder Links: *TMUX6136*

Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

Dual Supply Operation (T_A = 25°C)

图 6-1. On-Resistance vs Source or Drain Voltage

Single Supply Operation (T_A = 25°C)
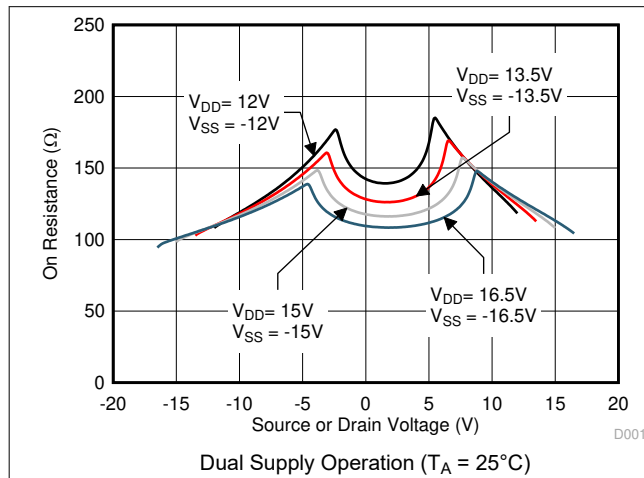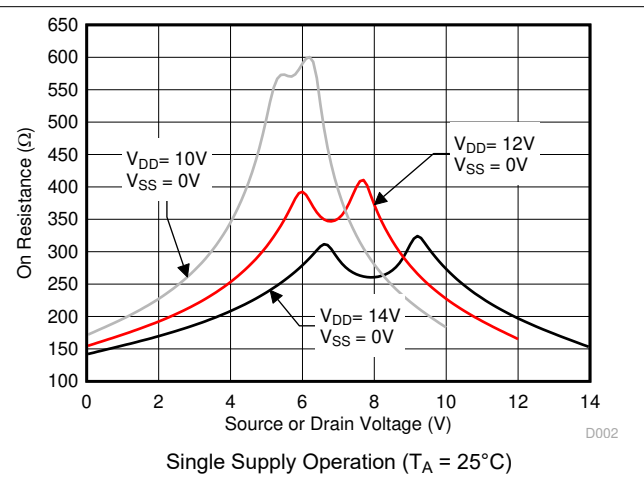
图 6-2. On-Resistance vs Source or Drain Voltage
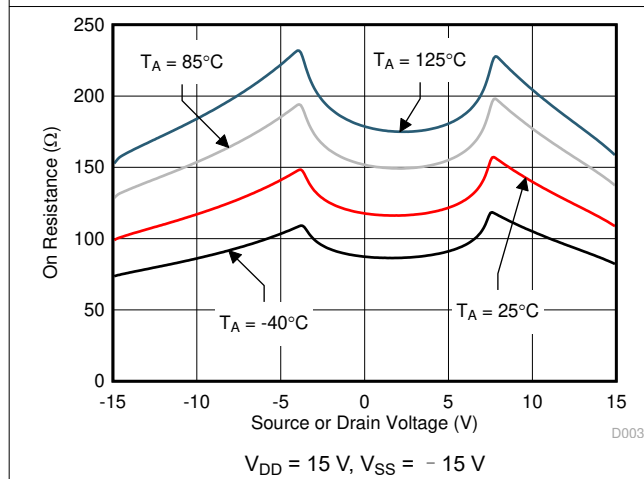
V_{DD} = 15 V, V_{SS} = –15 V

图 6-3. On-Resistance vs Source or Drain Voltage

V_{DD} = 12 V, V_{SS} = 0 V
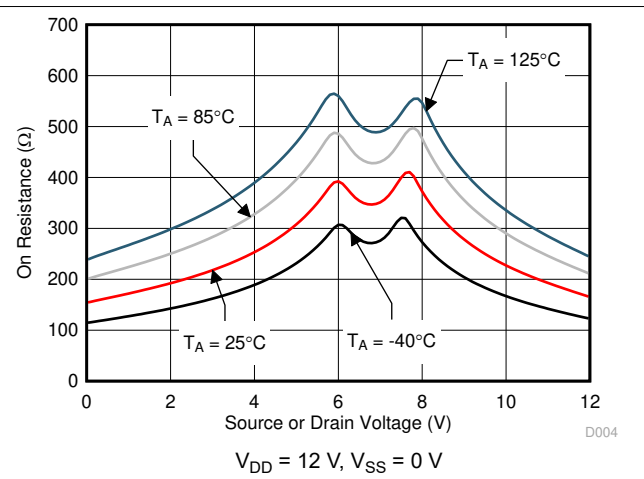
图 6-4. On-Resistance vs Source or Drain Voltage
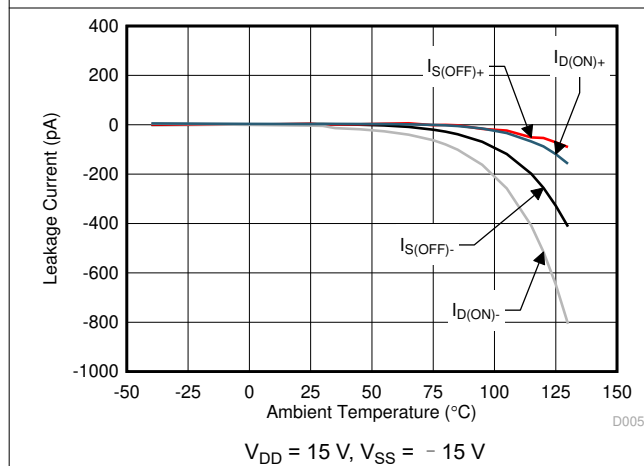
V_{DD} = 15 V, V_{SS} = –15 V

图 6-5. Leakage Current vs Temperature

V_{DD} = 12 V, V_{SS} = 0 V
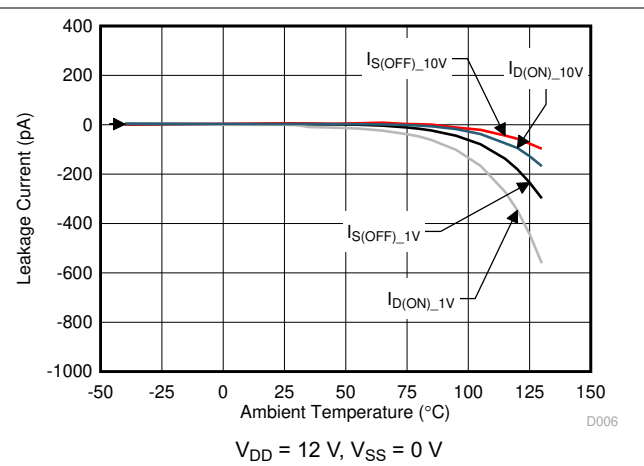
图 6-6. Leakage Current vs Temperature

Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = – 15 V (unless otherwise noted)
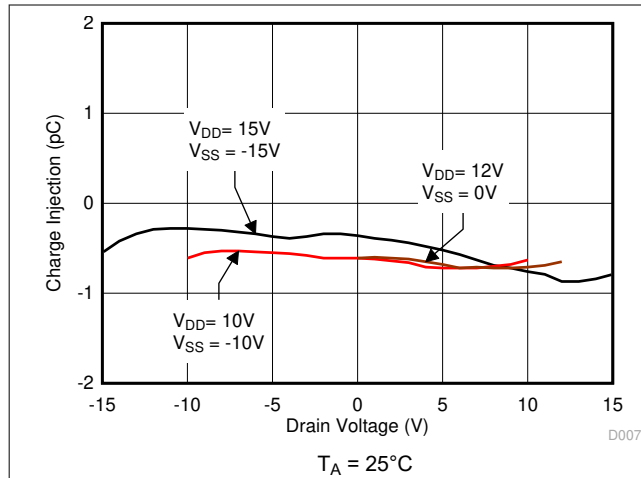

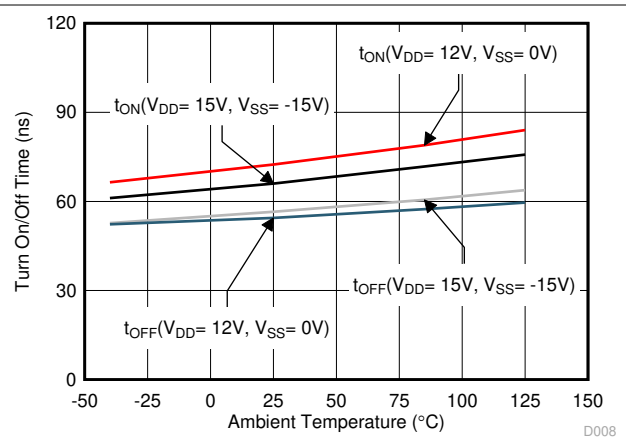图 6-7. Charge Injection vs Source Voltage

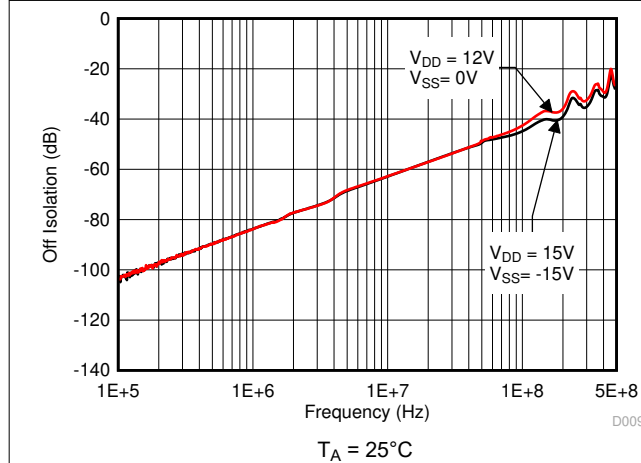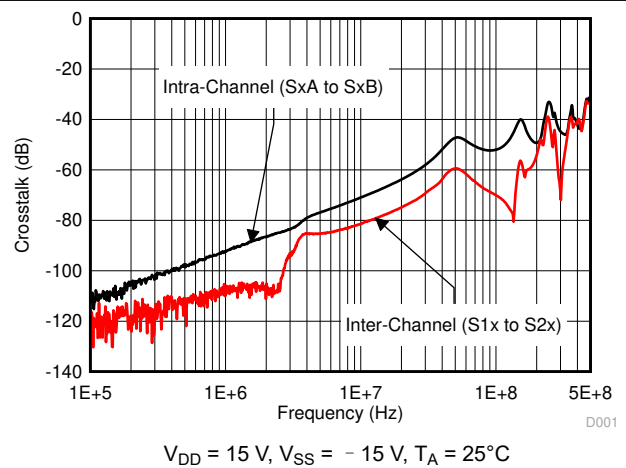图 6-8. Transition Times vs Temperature

图 6-9. Off Isolation vs Frequency

图 6-10. Crosstalk vs Frequency
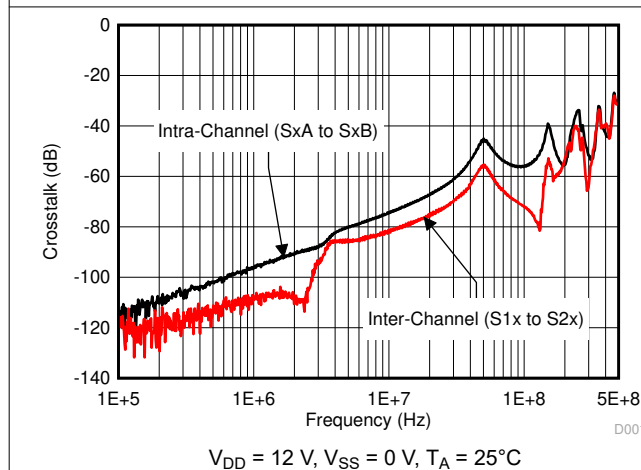
图 6-11. Crosstalk vs Frequency
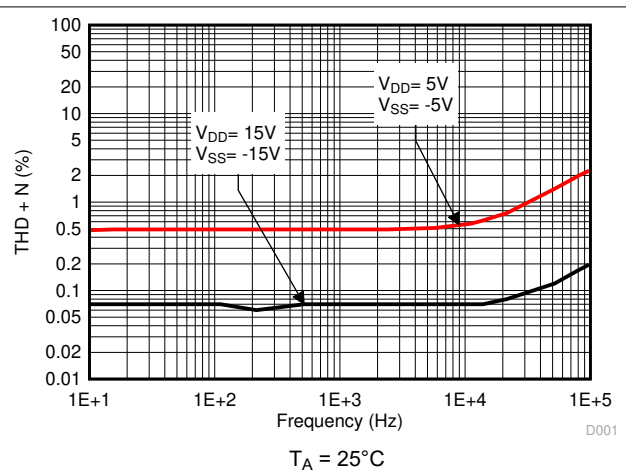
图 6-12. THD+N vs Frequency

Product Folder Links: *TMUX6136*

Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C
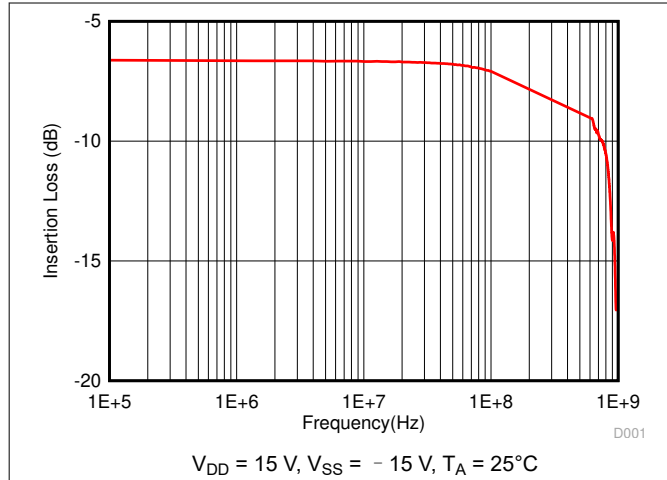
图 **6-13. On Response vs Frequency**

V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C
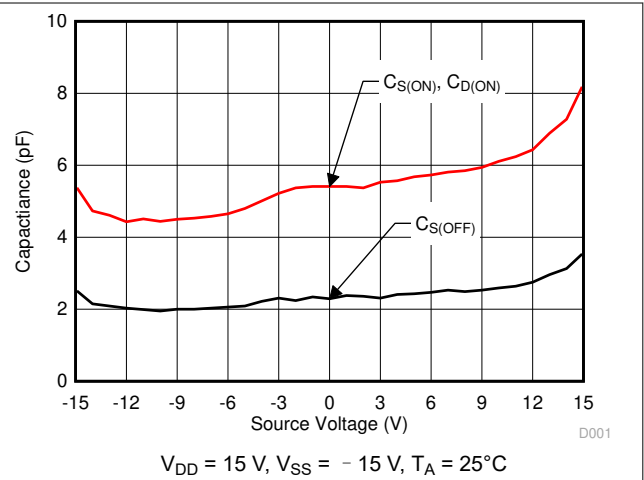
图 **6-14. Capacitance vs Source Voltage**

V_{DD} = 12 V, V_{SS} = 0 V, T_A = 25°C
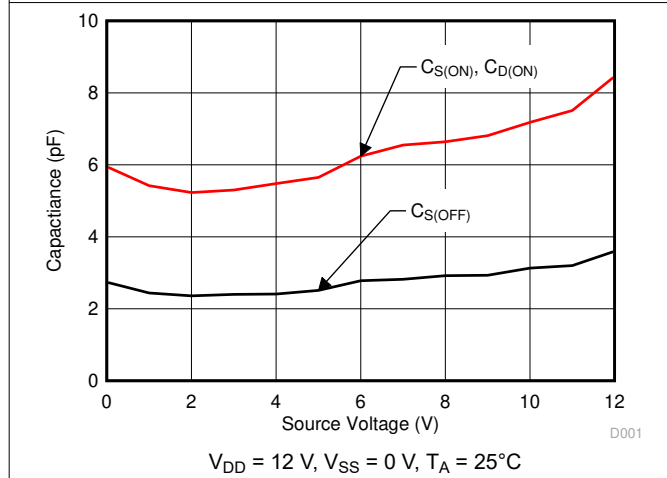
图 **6-15. Capacitance vs Source Voltage**

V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

图 **6-16. ACPSRR vs Frequency**

Product Folder Links: *TMUX6136*

7 Detailed Description

7.1 Overview

7.1.1 On-Resistance

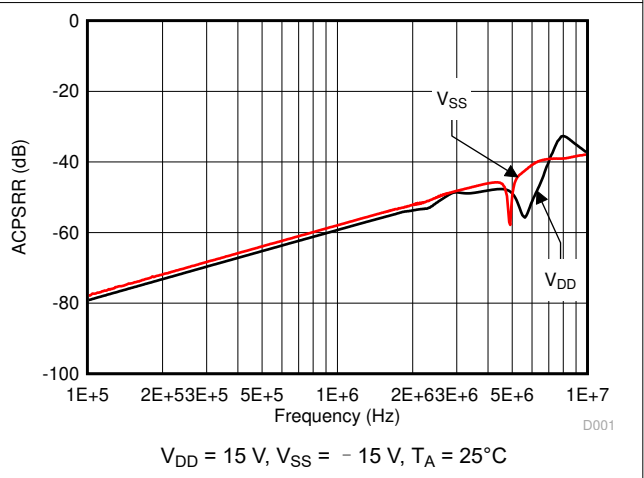The on-resistance of the TMUX6136 is the ohmic resistance across the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 7-1. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in 方程式 1.
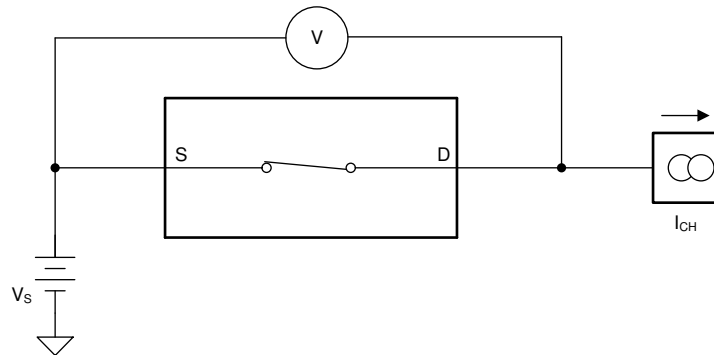

图 **7-1. On-Resistance Measurement Setup**

$$R_{ON} = V / I_{CH} \tag{1}$$

7.1.2 Off-Leakage Current

Source off-leakage current is defined as the leakage current that flows into or out of the source pin when the switch is in the off state. This current is denoted by the symbol $I_{S(OFF)}$. Drain off-leakage measurement is not characterization since the drain pin is always connected to one of the two source pins.

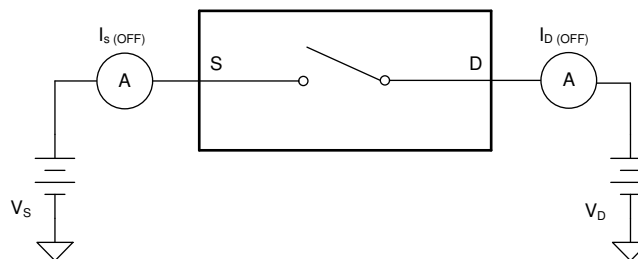The setup used to measure both off-leakage currents is shown in 图 7-2.

图 **7-2. Off-Leakage Measurement Setup**

Product Folder Links: *TMUX6136*

7.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. 图 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

图 7-3. On-Leakage Measurement Setup
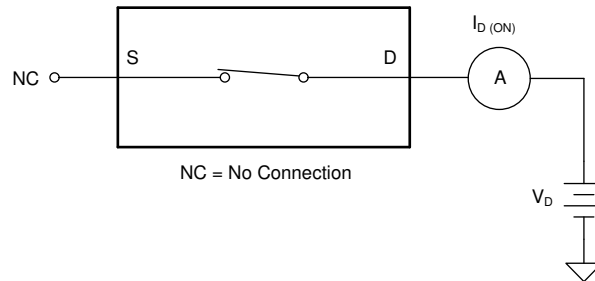
7.1.4 Transition Time

Transition time is defined as the time taken by the output of the TMUX6136 to rise or fall to 90% of the transition after the digital address signal has fallen or risen to 50% of the transition. 图 7-4 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.
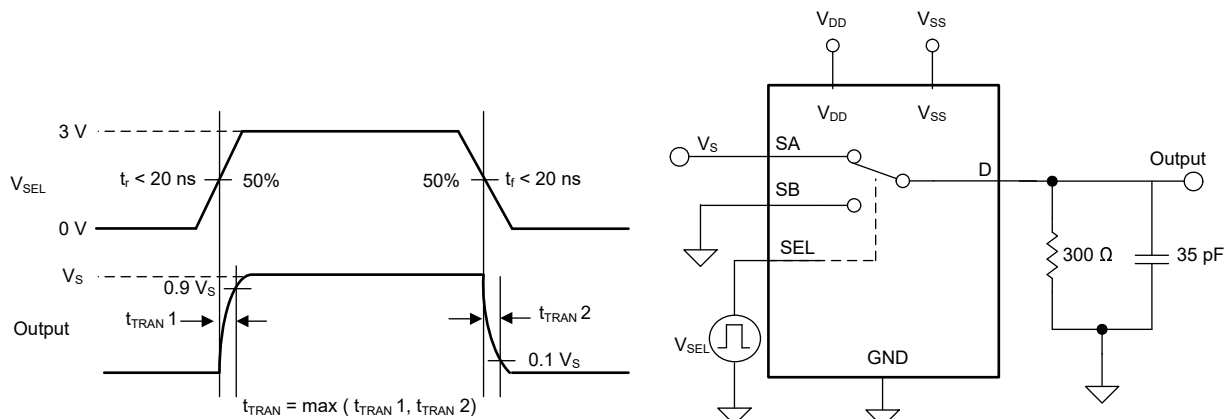

图 7-4. Transition-Time Measurement Setup

Product Folder Links: TMUX6136

7.1.5 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the TMUX6136 is switching. The TMUX6136 output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.
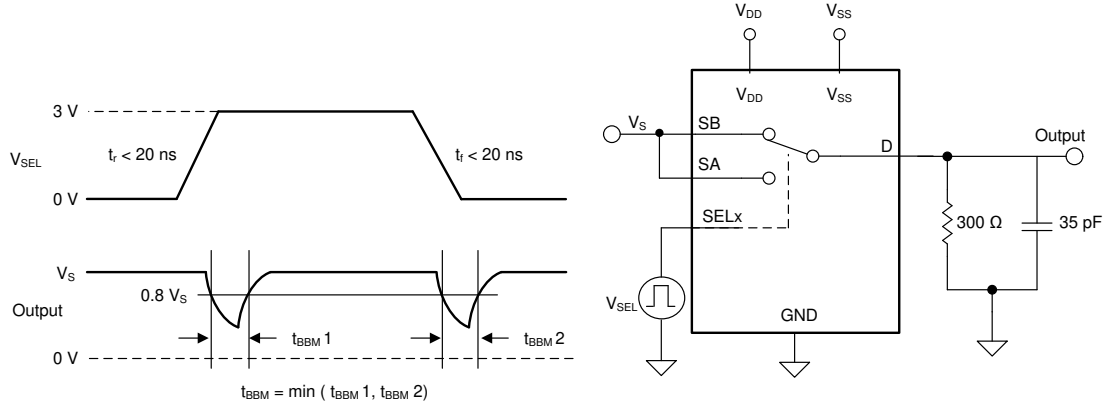

图 7-5. Break-Before-Make Delay Measurement Setup

7.1.6 Charge Injection

The TMUX6136 have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 图 7-6 shows the setup used to measure charge injection from drain (D) to source (Sx).
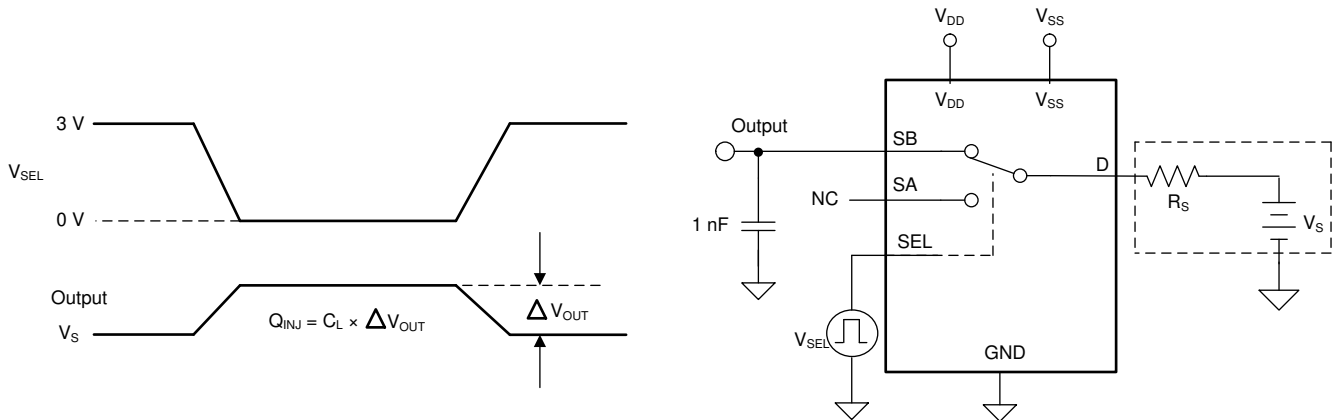

图 7-6. Charge-Injection Measurement Setup

7.1.7 Off Isolation

Off isolation is defined as the voltage at the drain pin (D) of the TMUX6136 when a 1-V_{RMS} signal is applied to the source pin (Sx) of an off-channel. 图 7-7 shows the setup used to measure off isolation. Use 方程式 2 to compute off isolation.

Product Folder Links: *TMUX6136*
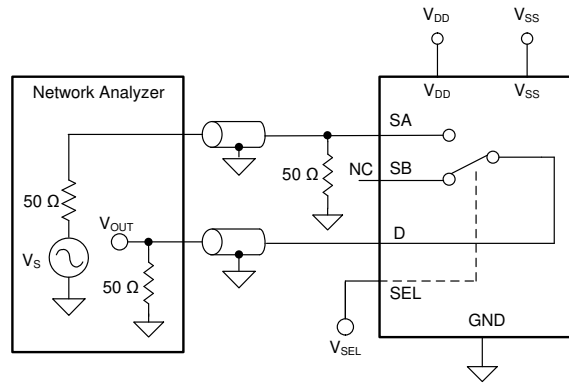
图 7-7. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right)$$

(2)

7.1.8 Channel-to-Channel Crosstalk

There are two types of crosstalk that can be defined for the TMUX6136:

1. Intra-channel crosstalk: the voltage at the source pin (Sx) of an off-switch input, when a 1-VRMS signal is applied at the source pin of an on-switch input in the same channel, as shown in 图 7-8.
2. Inter-channel crosstalk: the voltage at the source pin (Sx) of an on-switch input, when a 1-VRMS signal is applied at the source pin of an on-switch input in a different channel, as shown in 图 7-9.

图 7-8. Intra-Channel Crosstalk Measurement Setup
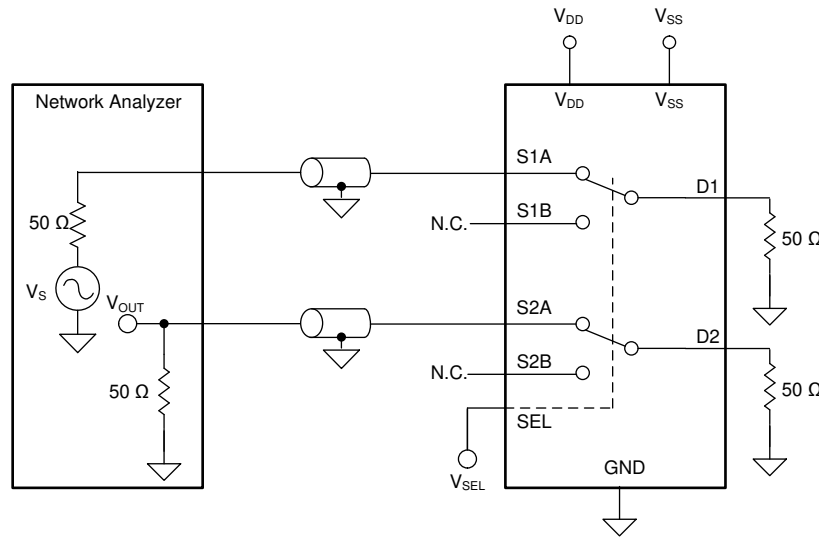
图 **7-9. Inter-Channel Crosstalk Measurement Setup**

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right)$$

(3)

7.1.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the TMUX6136. 图 7-10 shows the setup used to measure bandwidth of the mux. Use 方程式 4 to compute the attenuation.
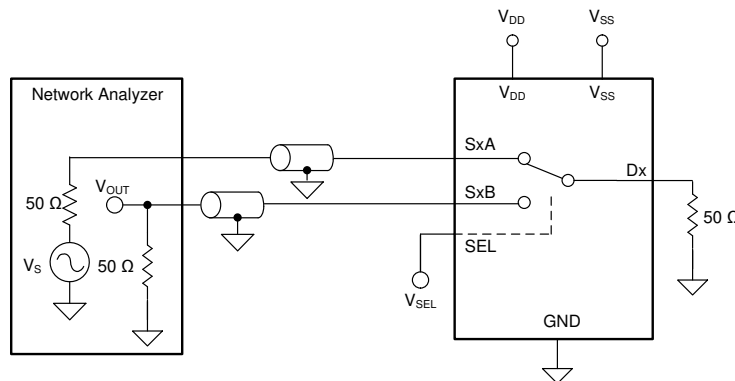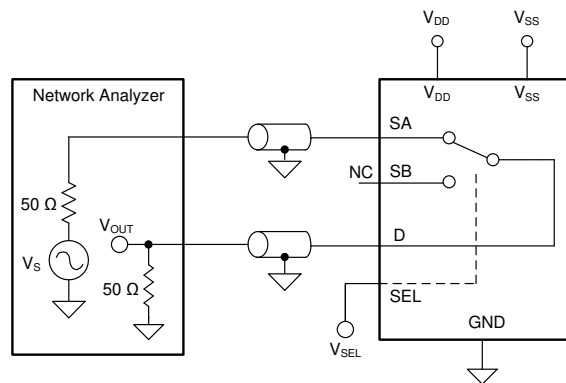

图 **7-10. Bandwidth Measurement Setup**

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right)$$

(4)

7.1.10 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX6136 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N.

Product Folder Links: *TMUX6136*
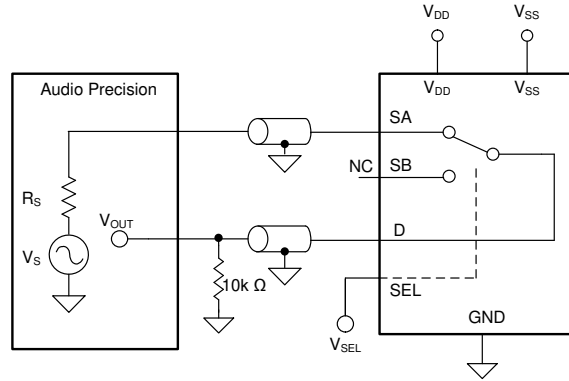
图 **7-11. THD+N Measurement Setup**

7.1.11 AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mV$_{PP}$. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

$V_{BIAS} = 0\ V$

$PSRR = 20 \times Log\ (V_{OUT}/\ V_{IN})$
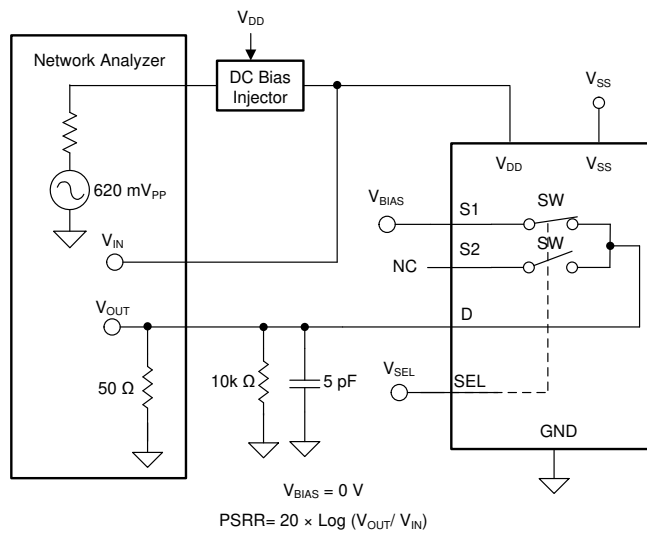
图 **7-12. AC PSRR Measurement Setup**

For a top-level block diagram of the TMUX6136, see 节 7.2. The TMUX6136 is a 4-channel, single-ended, analog multiplexer. Each channel is turned on or turned off based on the state of the address lines and enable pin.

Product Folder Links: *TMUX6136*

7.2 Functional Block Diagram
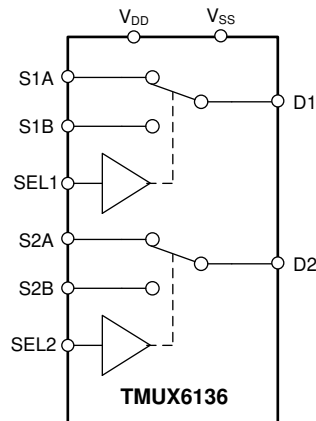
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7.3 Feature Description

7.3.1 Ultralow Leakage Current

The TMUX6136 provides extremely low on- and off-leakage currents. The TMUX6136 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. 图 7-13 shows typical leakage currents of the TMUX6136 versus temperature.
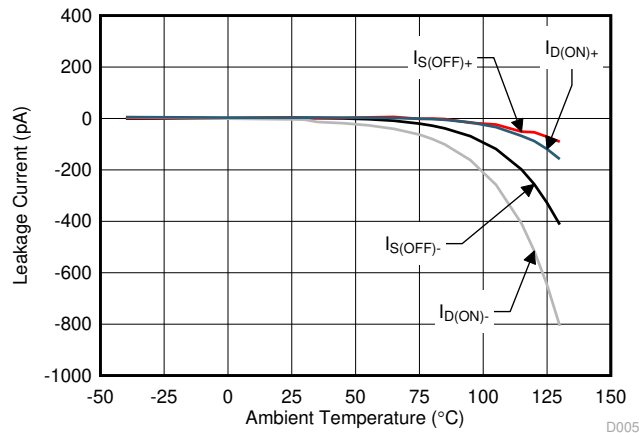
图 **7-13. Leakage Current vs Temperature**

7.3.2 Ultralow Charge Injection

The TMUX6136 is implemented with simple transmission gate topology, as shown in 图 7-14. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

Product Folder Links: *TMUX6136*
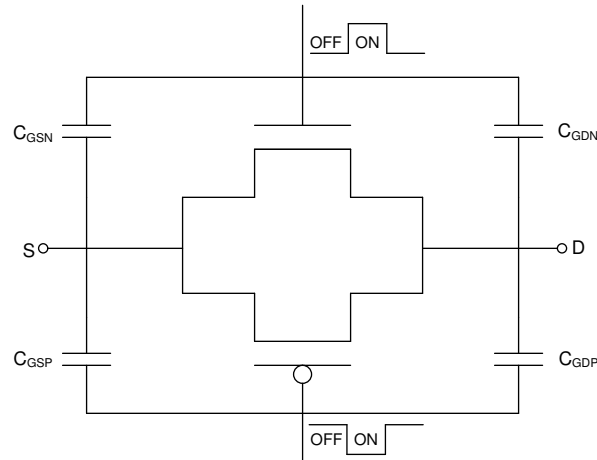
图 **7-14. Transmission Gate Topology**

The TMUX6136 utilizes special charge-injection cancellation circuitry that reduces the drain (D)-to-source (Sx) charge injection to as low as – 0.4 pC at V_S = 0 V, as shown in 图 7-15.
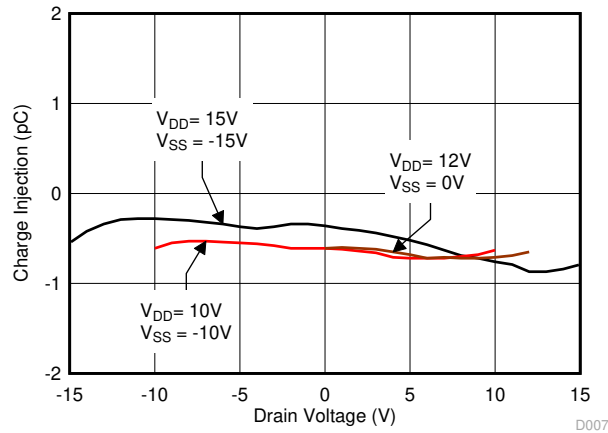
图 **7-15. Charge Injection vs Drain Voltage**

7.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX6136 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each TMUX6136 channel has very similar characteristics in both directions. The valid analog signal for TMUX6136 ranges from V_{SS} to V_{DD}. The input signal to the TMUX6136 swings from V_{SS} to V_{DD} without any significant degradation in performance.

7.4 Device Functional Modes

7.4.1 Truth Table

表 **7-1. TMUX6136 Truth Table**

SELx	Switch A (S1A to D1 or S2A to D2)	Switch B (S1B to D1 or S2B to D2)
0	OFF	ON
1	ON	OFF

Product Folder Links: *TMUX6136*

8 Application and Implementation

8.1 Application Information

The TMUX6136 offers outstanding input and output leakage currents and ultralow charge injection. The device operates up to 33 V (V_{DD} to V_{SS} dual supply) or 16.5 V (V_{DD} single supply), and offers true rail-to-rail input and output. The on-capacitance of the TMUX6136 is low. These features make the TMUX6136 a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

8.2 Typical Application

One example of the TMUX6136 precision performance to take advantage of is the implementation of parametric measurement unit (PMU) in the semiconductor automatic test equipment (ATE) application. The PMU is frequently used to characterize and measure the digital pin's DC characteristics of a device under test (DUT). Among all the PMU's capabilities, force voltage measure current (FVMC) and force current measure voltage (FCMV) are the two most typical configurations in DC characterizations.
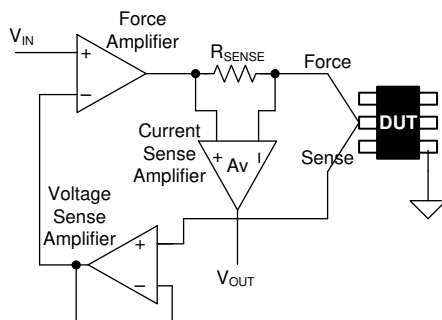
图 8-1. FVMC Measurement in PMU
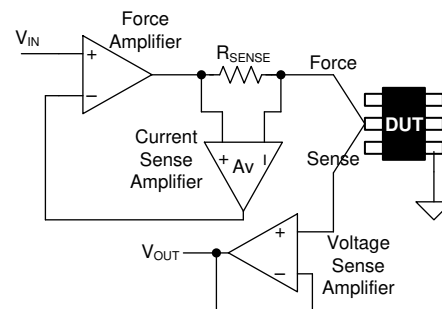
图 8-2. FCMV Measurement in PMU

图 8-1 shows a simplified diagram of the PMU in FVMC configuration. The control loop consists of the force amplifier with the voltage sense amplifier (unity gain in this example) making up the feedback path. Current flowing through the DUT is measured by sensing the current flowing through a sense resistor (R_{SENSE}) in series with the DUT. The current sense amplifier with a gain of Av generates a voltage (V_{OUT}) at its output and the voltage can then be measured by an ADC. The voltage produced at the DUT pin stays at the input voltage level (IN) as long as the force amplifier does not rail out (for example, I_{DUT} × R_{SENSE} x Av stays within the input voltage range of the force amplifier). Depending on the level of the DUT current to be measured, different gain settings need to be configured for the current sense amplifier.

图 8-2 shows a simplified diagram of the PMU in FCMV mode. The voltage V_{IN} is now converted to a current through the following relationship:

$$\text{Force Current} = V_{IN} / (R_{SENSE} \text{ x Av}) \tag{5}$$

The control loop consists of the force amplifier with the current sense amplifier making up the feedback path. The voltage at the DUT is sensed across the voltage sense amplifier (unity gain in this example) and presented at the output for sample.

8.2.1 Design Requirements

The goal of this design example is to simplify the FVMC and FCMV functions of a PMU design using a SPDT switch. The FVMC configuration is useful to test a device being used as a power supply, or in continuity or

leakage testing. In this configuration, the input voltage is directly applied to the DUT pin, and the current into or out of the DUT pin is converted to a voltage by a sense resistor and measured by an analog to digital converter (ADC). In the FCMV mode, an input current is forced to the DUT and the produced voltage on the DUT pin is directly measured. In this example, the PMU design is required to meet the following specifications:

- Force voltage range: –15 volts to +15 volts
- Force current range: ±5 µA to ±50 mA
- Measure voltage range: –15 volts to +15 volts
- Measure current range: ±5 µA to ±50 mA

In addition to the voltage and current requirements, fast throughput is also a key requirement in ATE because it relates directly to the cost of manufacturing the DUT.

8.2.2 Detailed Design Procedure
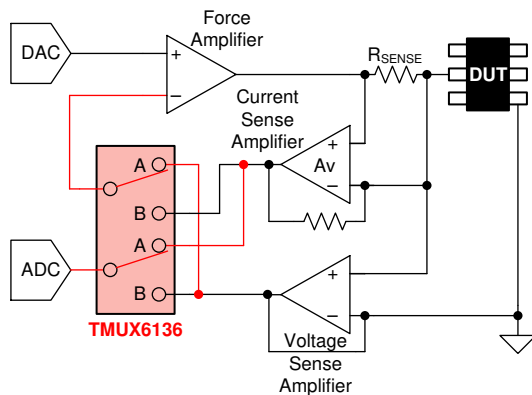
图 8-3. FVMC Implementation in PMU Using the TMUX6136
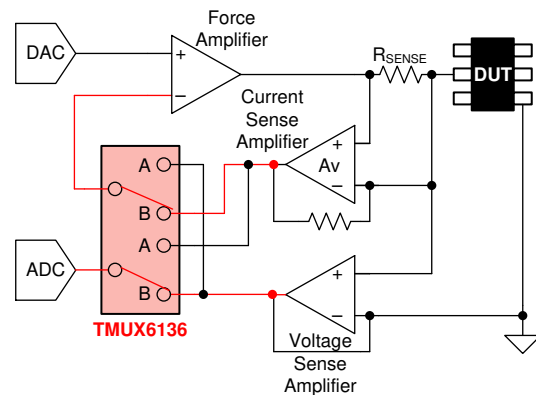
图 8-4. FCMV Implementation in PMU Using the TMUX6136

The implementation of the FVMC and FCMV modes can be combined with the use of a dual SPDT switch such as the TMUX6136. 图 8-3 and 图 8-4 shows simplified diagrams of such implementations. In the FVMC mode, the switch is toggled to position A and this allows the voltage sense amplifier to become part of the feedback loop and the voltage output of the current sense amplifier to be sampled by the ADC. In the FCMV mode, the switch is toggled to position B, and this allows the current sense amplifier to become part of the feedback loop and the voltage output of the voltage sense amplifier to be sampled by the ADC.

8.2.3 Application Curve

The fast transition time of the TMUX6136 and low input or output parasitic capacitance help minimize the settling time, making the TMUX6136 an excellent candidate to implement the FVMC and FCMV functions of the PMU. 图 8-5 shows the plot for the transition time versus temperature for the TMUX6136.
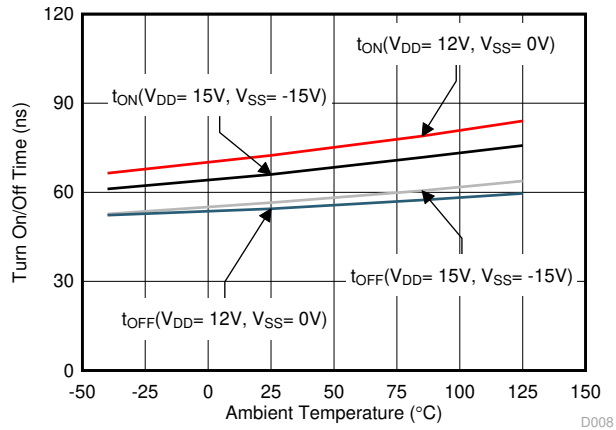
图 **8-5. Transition Time vs Temperature for TMUX6136**

9 Power Supply Recommendations

The TMUX6136 operates across a wide supply range of ±5 V to ±16.5 V (10 V to 16.5 V in single-supply mode). The device also performs well with unsymmetric supplies such as V_{DD} = 12 V and V_{SS}= – 5 V. For reliable operation, use a supply decoupling capacitor ranging between 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground.

10 Layout

10.1 Layout Guidelines

图 10-1 shows an example of a PCB layout with the TMUX6136.

Some key considerations are as follows:

1. Decouple the V_{DD} and V_{SS} pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

10.2 Layout Example

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图 **10-1. TMUX6136 Layout Example**

Product Folder Links: *TMUX6136*

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ADS8664 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges*
- Texas Instruments, *OPA192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-Trim™*
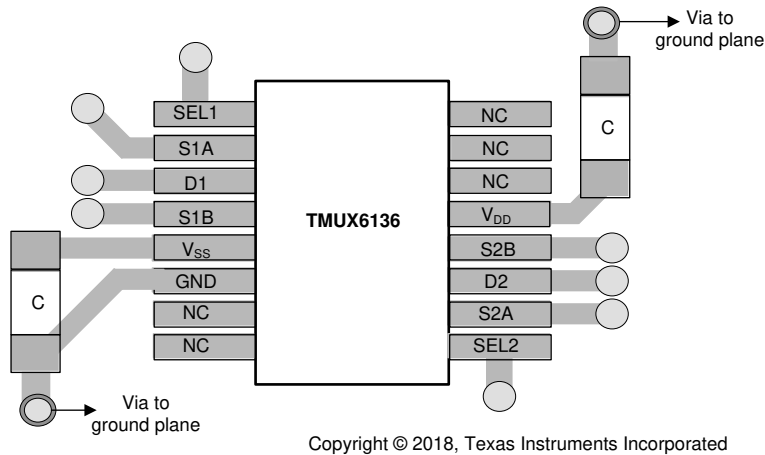
11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表   本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX6136PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6136	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX6136PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

![Texas Instruments]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX6136PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

A

6.6
6.2 TYP

PIN 1 INDEX AREA

14X 0.65

16

1

5.1
4.9
NOTE 3

2X

4.55

8

9

B

4.5
4.3
NOTE 4

16X 0.30
0.19

⊕ 0.1 Ⓜ C A B

SEATING
PLANE

C

◁ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL

4220204/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

(R0.05) TYP

1

16X (0.45)

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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