TPS272C45 45MΩ 双通道智能高侧开关，带诊断功能

1 特性

- 适用于 24V 工业应用的低 $R_{DS(on)}$（典型值 45mΩ）高侧开关
- 宽直流工作电压范围：6V 至 36V
- 24V 电源供电时具有低静态电流 (Iq)：0.5mA/通道（典型值）
- 固定 (5.8A) 及可调节（可通过外部电阻器调节为 0.7A 至 4A）电流限制
- 可驱动电感、容性和电阻性负载
  - 集成输出钳位支持电感负载放电
  - 容性负载驱动可通过双重阈值电流限制功能尽可能降低浪涌电流峰值
- 强大的输出保护
  - 热关断
  - 接地短路保护
  - 可配置故障处理
- 增强型诊断特性
  - 输出负载电流测量
  - 开路负载（关闭状态）检测
- 封装：24 引脚 QFN (5mm × 4mm)
- 提供功能安全
  - 有助于进行功能安全系统设计的文档

2 应用

- 工业 PLC 系统
  - 数字输出模块
  - IO-Link 主站端口
- 电机驱动器
- 楼宇自动化系统

3 说明

TPS272C45 是一款旨在满足工业控制系统要求的双通道智能高侧开关。低导通电阻（$R_{DS(on)}$ 为 45mΩ）可最大限度地降低器件功耗，实现 100mA 至 3A 的宽输出负载电流范围。该器件提供一个额外的低压电源（3.3V 至 5V）输入引脚，从而最大限度地降低空载功耗。该器件集成了多种保护功能，如热关断、输出钳位和过流限制。这些功能可在发生故障（如短路）时提高系统的稳健性。

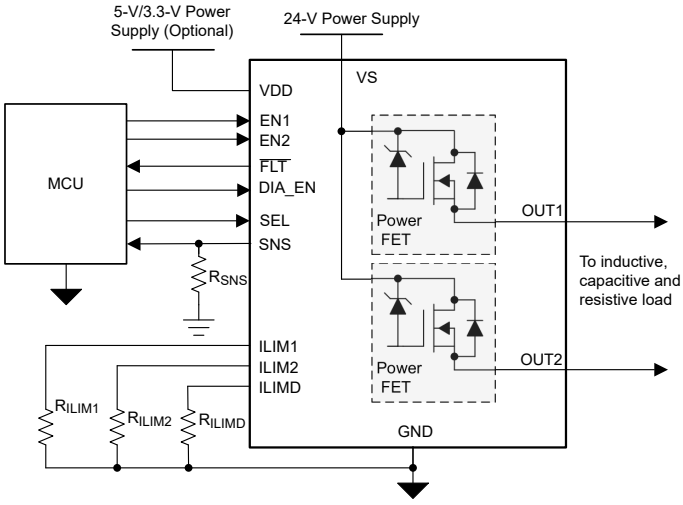
TPS272C45 器件采用可调阈值电流限制电路，通过减小驱动大容性负载时的浪涌电流并尽可能降低过载电流，提高了系统的可靠性。该器件还可配置浪涌电流持续时间，可通过较高的电流驱动高浪涌电流负载（如灯）或快速为容性负载充电。该器件还可提供精确的负载电流感测，以提高负载诊断功能，从而更好地进行预测性维护。

TPS272C45 器件采用引脚间距为 0.5mm 的 24 引脚 5mm × 4mm 小型 QFN 无引线封装，从而最大限度地减小 PCB 尺寸。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS272C45	QFN (24)	5.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2021) to Revision B (February 2022)	Page
• 删除了首页重复的功能方框图	1
• Deleted *Preview only* designation from all product variants in 节 5	3
• Deleted *Preview only* designation from 图 6-1	4
• Deleted *Preview only* designation from 图 6-2	4
• Corrected typographic error in Pin 10 label for 图 6-2	4

Changes from Revision * (December 2020) to Revision A (December 2021)	Page
• 将状态从“预告信息”更改为“量产数据”	1

5 Device Comparison Table

Device	Integrated Low Voltage Regulator	Integrated Clamp for Inductive Loads	Fault Diagnosis	Current Limit	Advantage
TPS272C45A	No	Yes	Single FLT pin, SNS pin provides per -ch fault	Dual level, inrush period	Lower device power dissipation with most of the quiescent current drawn from the lower voltage supply input – enables reduced total heat dissipation and thus smaller module sizes. Connect a 3.3V DC-DC regulator output to VDD pin. Single fault pin reduces IO count.
TPS272C45B	Yes	Yes	Single FLT pin, SNS pin provides per -ch fault	Dual level, inrush period	Lower system costs with a single power supply (cost of a low voltage regulator is avoided).
TPS272C45C	Yes	No	Single FLT pin, SNS pin provides per -ch fault	Dual level, inrush period	Enables usage of external TVS Clamp for high inductive loading. The device variant can be used with an external supply on VDD pin or using the internal 3.3-V regulation by GNDing the VDD pin.
TPS272C45D	Yes	Yes	Dual fault FLT1/ FLT2 pins	Single level	Dual FLT pins provides easier fault diagnosis. The device variant can be used with an external supply on VDD pin or using the internal 3.3-V regulation by GNDing the VDD pin.

6 Pin Configuration and Functions

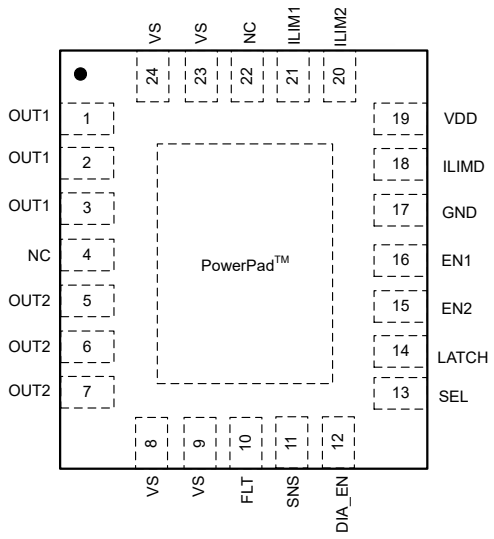


图 6-1. RHF Package, 24-Pin QFN (Top View) Version A and C

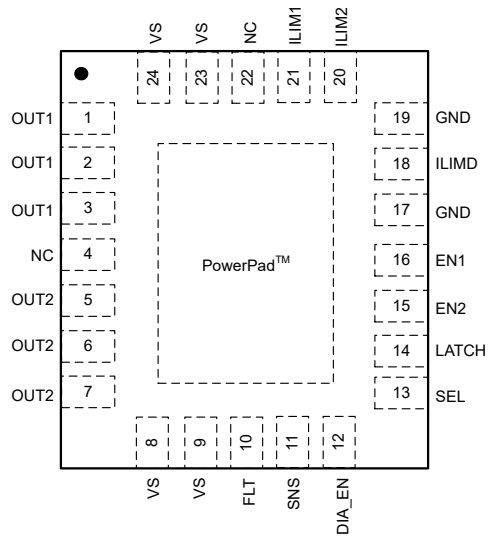


图 6-2. RHF Package, 24-Pin QFN (Top View) Version B

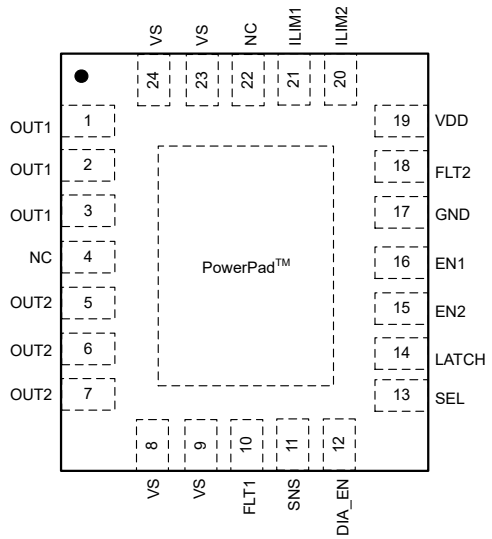


图 6-3. RHF Package, 24-Pin QFN (Top View) Version D

表 6-1. Pin Functions

PIN				I/O	DESCRIPTION
NAME	TPS272C45A, TPS272C45C	TPS272C45B	TPS272C45D		
DIA_EN	12	12	12	I	Enables diagnostic functionality
SEL	13	13	13	I	SEL = 0: SNS pin measures channel 1 load current or fault output SEL = 1: SNS pin measures channel 2 load current or fault output.
LATCH	14	14	14	I	Sets retry behavior. LATCH = 0: auto-retry after faults or LATCH = 1: latch off after faults.
EN2	15	15	15	I	Enables channel 2 output current
EN1	16	16	16	I	Enables channel 1 output current
GND	17	17, 19	17	GND	Device ground

表 6-1. Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	TPS272C45A, TPS272C45C	TPS272C45B	TPS272C45D		
ILIMD	18	18	—	O	Connect R_{ILIMD} to GND to set higher inrush current limit time duration.
$\overline{FLT2}$	—	—	18	O	Open drain output with pulldown to signal fault on Ch2 (active low signal).
ILIM2	20	20	20	O	Connect R_{ILIM2} to GND to set channel 2 current limit.
ILIM1	21	21	21	O	Connect R_{ILIM1} to GND to set channel 1 current limit.
PowerPad	Pad	Pad	Pad	—	Heat dissipation pad – connect to device GND. Maximize PCB copper area for the best heat dissipation.
VS	23, 24, 8, 9	23, 24, 8, 9	23, 24, 8, 9	I	Primary input supply, connect through vias down to a power plane to connect the two set of VS power pins.
VOUT1	1, 2, 3	1, 2, 3	1, 2, 3	O	Channel 1 output
NC	4, 22	4, 22	4, 22		No connect pin, leave unconnected
VOUT2	5, 6, 7	5, 6, 7	5, 6, 7	O	Channel 2 output
$\overline{FLT}$	10	10	—	O	Open drain output with pulldown to signal fault on either channel (active low signal).
$\overline{FLT1}$	—	—	10	O	Open drain output with pulldown to signal fault on Ch1 (active low signal).
SNS	11	11	11	O	Analog current output corresponding to load current – connect a resistor to GND to convert to voltage.
VDD	19	—	19	I	Version A: Connect low voltage supply input for lower power dissipation Version C, D: Optionally tie to gnd to use internal LDO or connect to external low voltage supply.

6.1 Recommended Connections for Unused Pins

The TPS272C45 is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins can be considered as optional.

表 6-2. Connections for Optional Pins

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
SNS	Ground through 1-kΩ resistor	Analog current sense is not available.
LATCH	GND pin of IC	With LATCH unused (pin grounded), the device auto-retries after a fault. If latched behavior is desired, but the system describes limited I/O, it is possible to use one microcontroller output to control the latch function of several high-side channels.
ILIMD	GND pin of IC	If ILIMD pin is connected to IC_GND, the current limit threshold is at a constant value determined by the ILIM1/ILIM2 resistor values (delay time of zero).
ILIM1/ILIM2	GND pin of IC	If either ILIMx pin is left floating or connected to IC_GND, the device is set to the default internal current-limit threshold.
$\overline{\text{FLT}}$ / $\overline{\text{FLTx}}$	GND pin of IC	If the $\overline{\text{FLT}}$ pin is unused, the system cannot read faults from the output.
SEL	GND pin of IC	With SEL unused, only channel one current sensing or Fault reporting is available from the SNS pin.
DIA_EN	GND pin of IC	With DIA_EN unused, the analog current sense, open-load and short-to-supply diagnostics are not available.
VDD	GND pin of IC	Version A: Connect to a 3.3-V or 5-V supply
		Version C, D: With VDD unused, all supply current is drawn from the primary supply VS.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum continuous supply voltage, Versions A, B, D: V_S		– 0.7	48	V
Maximum transient (< 100 us) voltage at the supply pin, Versions A, B, D : V_S		– 0.7	60	V
Maximum continuous supply voltage Version C, V_S		– 0.7	60	V
Maximum voltage across the VS and OUT pins (V_S - V_{OUT}) Version C,		– 0.7	71	V
Low voltage supply pin voltage, V_{DD}		– 1	5.5	V
Enable pin voltage, V_{EN1} and V_{EN2}		– 1	VS	V
LATCH pin voltage, V_{LATCH}		– 1	VS	V
Diagnostic Enable pin voltage, V_{DIA_EN}		– 1	VS	V
Sense pin voltage, V_{SNS}		– 1	VS	V
$\overline{FLT}$ pin voltage, Version A, B, C $V_{\overline{FLT}}$		– 1	VS	V
$\overline{FLTx}$ pin voltage, Version D, $V_{\overline{FLT1}}$,$V_{\overline{FLT2}}$		– 1	5.5	V
Select pin voltage, V_{SEL}		– 1	VS	V
Reverse ground current, I_{GND}	V_S < 0 V		– 50	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except VS and OUTx	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	VS and OUTx with respect to GND	±4000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), ANSI/ESDA/JEDEC JS-002(2)	All pins	±750	V
$V_{(surge)}$	Electrostatic discharge	Surge protection with 42 Ω, per IEC 61000-4-5; 1.2/50 μs (3)	OUTx pins	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested with application circuit and supply voltage (VS) of 24-V, ENx pins High (Output Enabled) and and EN pins Low (Outputs Disabled)

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{S_OPMAX}	Nominal supply voltage	4.5	36	V
V_{DD}	Low Voltage Supply Voltage	3.0	5.5	V
V_{EN1}, V_{EN2}	Enable voltage	– 1	36	V
V_{LATCH}	LATCH voltage	– 1	36	V
V_{DIA_EN}	Diagnostic Enable voltage	– 1	36	V

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{FLT}	$\overline{FLT}$ pin voltage (Versions A, B,C)	–1	36	V
$V_{FLT1, FLT2}$	$\overline{FLT1}$, $\overline{FLT2}$ pin voltage (Version D)	–1	5.5	V
V_{SEL}	Select pin voltage	–1	36	V
V_{SNS}	Sense pin voltage	–1	7	V
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND

7.4 Thermal Information

THERMAL METRIC(1) (2)		TPS272C45 RHF (QFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

7.5 Electrical Characteristics

V_S = 6 V to 36 V, V_{DD} = 3.0 V to 3.6 V, T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT						
$V_{DS,Clamp}$	V_{DS} clamp voltage	FET current = 10 mA, V_S = 24 V	49	53	61	V
$V_{S,OVPR}$	V_S overvoltage protection rising	Measured with respect to the GND pin of the device, ENx = HI	41.5	45.5	50	V
$V_{S,OVPRF}$	V_S overvoltage protection recovery falling	Measured with respect to the GND pin of the device, ENx = HI	40	43.5	48	V
$V_{S,OVPRD}$	V_S overvoltage protection deglitch time	Time from triggering the OVP fault to FET turn-off	30	72	85	µs
$V_{S,UVLOR}$	V_S undervoltage lockout rising	Measured with respect to the GND pin of the device	3.5	4.0	4.5	V
$V_{S,UVLOF}$	V_S undervoltage lockout falling	Measured with respect to the GND pin of the device	2.4	2.6	2.9	V
$V_{DD,UVLOF}$	V_{DD} undervoltage lockout falling	Measured with respect to the GND pin of the device	2.63	2.8	2.9	V
$V_{DD,UVLOR}$	V_{DD} undervoltage lockout rising	Measured with respect to the GND pin of the device	2.74	2.90	3.0	V
IL_{NOM}	Continuous load current, per channel	One channel enabled, T_{AMB} = 85°C		4.0		A
		Two channels enabled, T_{AMB} = 85°C		3.0		A
$I_{OUT(OFF)}$	Output leakage current (per channel)	VS <= 36 V, T_J = 85°C V_{ENx} = V_{DIA_EN} = 0 V, V_{OUT} = 0 V		0.5	3.0	µA
$I_{Q\_VS\_DS}$	VS quiescent current, Dual Supply input, both channels enabled, diagnostics disabled.	$V_S \leqslant$ 36 V, V_{DD} = 5 V V_{ENx} = HI V_{DIA_EN} = 0 V, I_{OUTx} = 0		1.05	1.4	mA

7.5 Electrical Characteristics (continued)

V_S = 6 V to 36 V, V_{DD} = 3.0 V to 3.6 V, T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q\_VDD\_DS}$	VDD quiescent current, both channels enabled, diagnostics disabled.	$V_S \leqslant$ 36 V, V_{DD} = 3.3 V V_{ENx} = 3.3 V V_{DIA_EN} = 0, I_{OUTx} = 0				2.0	mA
$I_{Q\_VDD\_DS}$	VDD quiescent current, both channels enabled, diagnostics disabled.	$V_S \leqslant$ 36 V, V_{DD} = 5 V V_{ENx} = 5 V V_{DIA_EN} = 0, I_{OUTx} = 0 A				2.1	mA
$I_{Q\_VS\_DIA\_DS}$	VS quiescent current, Dual Supply input, both channels diagnostics enabled	$V_S \leqslant$ 36 V, V_{DD} = 5 V V_{ENx} = V_{DIA_EN} = 5 V, I_{OUTx} = 0 A				2.8	mA
$I_{Q\_VS\_SS}$	VS quiescent current, single (VS only) supply input, both channels ON diagnostics disabled	V_{ENx} = HI V_{DIA_EN} = 0 V, I_{OUTx} = 0				4.4	mA
$I_{Q\_VS\_DIA\_SS}$	V_S quiescent current, single VS supply input, both channels ON diagnostics enabled	V_{ENx} = V_{DIA_EN} = HI, I_{OUTx} = 0				4.9	mA
RON CHARACTERISTICS							
R_{ON}	On-resistance (Includes MOSFET and package)	6 V $\leqslant V_S \leqslant$ 36 V, I_{OUTx} < 4 A	T_J = 25°C		45		mΩ
			T_J = 85°C			68	mΩ
			T_J = 125°C			78	mΩ
	On-resistance when channels are paralleled (Includes MOSFET and package)	6 V $\leqslant V_S \leqslant$ 36 V, I_{OUTx} < 4 A V_{EN1} tied to V_{EN2}, V_{OUT1} tied to V_{OUT2}	T_J = 25°C		23	27	mΩ
			T_J = 85°C			34	mΩ
			T_J = 125°C			39	mΩ
CURRENT SENSE CHARACTERISTICS							
K_{SNS}	Current sense ratio I_{OUTx} / I_{SNS}	I_{OUTX} = 1 A	I_{OUTX} = 1 A		1200		
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 4 A		3.33		mA
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 4 A	-4.4		4.4	%
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 2 A		1.67		mA
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 2 A	-4.4		4.4	%
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 1 A		0.83		mA
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 1 A	-4		4	%
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 500 mA		0.425		mA
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 500 mA	-6		6	%
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 200 mA		0.17		mA
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 200 mA	-10		10	%
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 100 mA		0.083		mA
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 100 mA	-18		18	%

7.5 Electrical Characteristics (continued)

V_S = 6 V to 36 V, V_{DD} = 3.0 V to 3.6 V, T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 50 mA		0.0416		mA
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V	I_{OUT} = 50 mA	-25		25	%
I_{SNSI} Paralleled	Paralleled channels current sense accuracy multiplier	V_{EN1} tied to V_{EN2}, V_{OUT1} tied to V_{OUT2} and I_Load > 1 A	Multiply percentage accuracy specification by this factor			1.2	times
SNS CHARACTERISTICS							
I_{SNSFH}	I_{SNS} fault high-level	V_{DIA_EN} = HI device in FLT state of CH selected, Vs>10 V	V_{DIA_EN} = HI, device in FLT state of CH selected, Vs>10 V	3.333	4.5	5.5	mA
I_{SNS_HR}	V_S - V_{SNS} headroom needed for current sense functionality	V_S = 6V, I_{SNS} = 3.4 mA				2.35	V
$I_{SNSleak}$	I_{SNS} leakage, with no load	V_{DIA_EN} = HI, V_{EN} = HI, I_L = 0 mA				10	µA
CURRENT LIMIT CHARACTERISTICS							
I_{CL}	Current limitation Level	Heavy overload or short circuit condition	R_{ILIMx} = GND, open, or out of range (< 4.3 kΩ, and > 80 kΩ)	4.3	5.8	6.95	A
I_{CL}	Current limitation Level	Heavy overload or short circuit condition	R_{ILIMx} = 5 kΩ, V_{VS}-V_{OUT} > 2 V	3.15	4.1	4.7	A
I_{CL_LINPK}	Overcurrent limit threshold(1)	Overload condition(1)	R_{ILIMx} = 5 kΩ V_{VS}-V_{VOUT} < 1V			4.78	A
I_{CL}	Current limitation Level	Heavy overload or short circuit condition	R_{ILIMx} = 10 kΩ, V_{VS}-V_{OUT} > 2 V	1.58	2.05	2.3	A
I_{CL_LINPK}	Overcurrent limit threshold(1)	Overload condition	R_{ILIMx} = 10 kΩ V_{VS}-V_{OUT} < 1V			2.42	A
I_{CL}	I_{CL} Current Limitation Level	Heavy overload or short circuit condition	R_{ILIMx} = 28.7 kΩ, V_{VS}-V_{VOUT} > 2 V	0.52	0.71	0.82	A
I_{CL_LINPK}	Overcurrent limit threshold(1)	Overload condition(1)	R_{ILIMx} = 28.7 kΩ, V_{VS}-V_{OUT} < 1 V			0.9	A
K_{CL}	Current Limit Ratio				20.5		A * kΩ
$I_{CL\_match12}$	I_{CL} Current Limitation Level - Matching between CH1 and CH2	Heavy overload or short circuit condition	R_{ILIMx} = 10 kΩ, V_{VS}-V_{OUT} = 24 V	-10		10	%
I_{CL_ENPS}	Peak current before regulation while enabling switch into 100 mohm load	R_{ILIMx} = 5 kΩ to 20 kΩ, VS = 24V				2.7 times I_{CL}	A
I_{CL}	Current limitation level during inrush delay period	Regulated current @ Short circuit when Enabled	R_{ILIMx} = 5 kΩ, RILIMD > 40 kΩ V_{VS}-V_{OUT}> 20 V	1.3	1.5	1.7	A
t_{DELAY}	Nominal Higher Inrush Current limit time delay range	Set by resistor on ILIMD pin in discrete steps		0		22	ms
t_{DELAY_VAR}	Variation in ILIMD pin set delay time			-250		250	µs
$I_{CL,PRLL}$	Paralled Channels Current Limitation Level - Multiplier compared to one channel	V_{EN1} tied to V_{EN2}, V_{OUT1} tied to V_{OUT2}	R_{ILIMx} = 5 kΩ to 20 kΩ		1.1		
FAULT CHARACTERISTICS							

7.5 Electrical Characteristics (continued)

V_S = 6 V to 36 V, V_{DD} = 3.0 V to 3.6 V, T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{pu_OL}	Open-load (OL, wire break) detection internal pull-up resistor	V_{ENx} = 0 V, V_{DIA_EN} = 5 V		125	150	180	kΩ
V_{OL_off}	Open-load (OL, wire break) detection voltage VS - VOUT	V_{ENx} = 0 V, V_{DIA_EN} = 5 V		1.4	2.0	2.5	V
t_{OL1}	Open Load (wire-break) indication-time from ENx falling	V_{ENx} HI to LO, V_{DIA_EN} = 5 V, V_{SEL} = X(2) I_{OUT} = 0 mA, Open load condition		170	300	440	µs
t_{OL2}	Open load (wire-break) indication-time from DIA_EN rising	V_{ENx} = 0 V, V_{DIA_EN} = LO to HI, V_{SEL} = X(2) I_{OUT} = 0 mA, Open Load Condition				650	µs
t_{OL3}	Open load (wire-break) indication-time from V_{OUT} rising beyond open load threshold	V_{ENx} = 0 V, V_{DIA_EN} = 5 V, V_{SEL} = X(2) I_{OUT} = 0 mA, V_S – V_{OUTx} = < 2 V				600	µs
T_{ABS}	Thermal shutdown			160	185	210	°C
T_{REL}	Relative thermal shutdown threshold			93	118	143	°C
T_{HYS}	Thermal shutdown hysteresis			18	24	30	°C
V_{ol_FLT}	Fault low-output voltage (Versions A, B, C)	I_{FLT} = 2 mA, sink current into the pin				0.4	V
V_{ol_FLTx}	Fault low-output voltage Version D	I_{FLT1} , I_{FLT2}= 2 mA, sink current into the pin				0.4	V
t_{RETRY}	Retry time	Time from fault shutdown until switch re-enable (thermal shutdown or current limit).		1	2	3	ms
EN1 AND EN2 PIN CHARACTERISTICS							
$V_{IL,\ ENx}$	Input voltage low-level					0.8	V
$V_{IH,\ ENx}$	Input voltage high-level			2			V
$V_{IHYS,\ ENx}$	Input voltage hysteresis				350		mV
R_{ENx}	Internal pulldown resistor			0.8	1.5	2.5	MΩ
$I_{IH,\ EN}$	Input current high-level	V_{EN} = 5 V			5		µA
DIA_EN PIN CHARACTERISTICS							
$V_{IL,\ DIA\_EN}$	Input voltage low-level					0.8	V
$V_{IH,\ DIA\_EN}$	Input voltage high-level			2			V
$V_{IHYS,\ DIA\_EN}$	Input voltage hysteresis			200	350	530	mV
R_{DIA_EN}	Internal pulldown resistor			0.8	1.5	2.5	MΩ
$I_{IH,\ DIA\_EN}$	Input current high-level	V_{DIA_EN} = 5 V		2.5	5.0	10.0	µA
SEL Characteristics							
$V_{IL,\ SEL}$	Input voltage low-level					0.8	V
$V_{IH,\ SEL}$	Input voltage high-level			2			V
$V_{IHYS,\ SEL}$	Input voltage hysteresis			200	350	530	mV
R_{SEL}	Internal pulldown resistor			0.8	1.5	2.5	MΩ
$I_{IH,\ SEL}$	Input current high-level	V_{DIA_EN} = 5 V	V_{DIA_EN} = 5 V	2.5	5.0	10.0	µA
LATCH PIN CHARACTERISTICS							
$V_{IL,\ LATCH}$	Input voltage low-level					0.8	V
$V_{IH,\ LATCH}$	Input voltage high-level			2			V

7.5 Electrical Characteristics (continued)

V_S = 6 V to 36 V, V_{DD} = 3.0 V to 3.6 V, T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IHYS, LATCH}$	Input voltage hysteresis			200	350	530	mV
R_{LATCH}	Internal pulldown resistor			0.8	1.5	2.5	MΩ
$I_{IH, LATCH}$	Input current high-level	V_{LATCH} = 5 V		2.5	5.0	10.0	µA

(1) The maximum current output under overload condition before current limiting occurs.
(2) SEL must be set to select the relevant channel. Diagnostics are performed on Channel 1 when SEL = 0 and diagnostics are performed on channel 2 when SEL =1

7.6 SNS Timing Characteristics

V_S = 6 V to 36 V, T_J = -40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIA_EN 50% of V_{DIA_EN} to 95% of settled ISNS	V_{ENx} = 5 V, V_{DIA_EN} = 0 V to 5 V R_{SNS} = 1 kΩ, I_L = 2 A			30	µs
$t_{SNSION1}$	Settling time from rising edge of DIA_EN 50% of V_{DIA_EN} to 95% of settled ISNS	V_{ENx} = 5 V, V_{DIA_EN} = 0 V to 5 V R_{SNS} = 1 kΩ, I_L = 100 mA			60	µs
$t_{SNSION2}$	Settling time from rising edge of EN and DIA_EN 50% of V_{DIA_EN} V_{EN} to 95% of settled I_{SNS}	V_{ENx} = V_{DIA_EN} = 0 V to 5 V V_S = 24 V, R_{SNS} = 1 kΩ, R_L = 12 Ω			85	µs
$t_{SNSION3}$	Settling time from rising edge of EN with DIA_EN HI; 50% of V_{DIA_EN} V_{EN} to 95% of settled I_{SNS}	VS=24V V_{ENx} = 0 V to 5 V, V_{DIA_EN} = 5 V R_{SNS} = 1 kΩ, I_L = 2A			85	µs
$t_{SNSIOFF1}$	Settling time from falling edge of DIA_EN	V_{ENx} = 5 V, V_{DIA_EN} = 5 V to 0 V R_{SNS} = 1 kΩ, I_L = 2 A			20	µs
$t_{SETTLEH}$	Settling time from rising edge of load step	V_{EN1} = 5 V, V_{DIA_EN} = 5 V R_{SNS} = 1 kΩ, I_{OUT} = 0.8 A to 2 A			20	µs
$t_{SETTLEL}$	Settling time from falling edge of load step	V_{ENx} = 5 V, V_{DIA_EN} = 5 V R_{SNS} = 1 kΩ, I_{OUT} = 2 A to 0.8 A			20	µs
SNS TIMING - MULTIPLEXER						
t_{MUX}	Settling time from current sense on CHx to CHy	V_{ENx} = 5V, V_{DIA_EN} = 5 V V_{SEL} = 0 V to 5 V R_{SNS} = 1 kΩ, I_{OUT1} = 0.2 A, I_{OUT2} = 2 A			20	µs

7.7 Switching Characteristics

V_S = 6 V to 36 V, T_J = -40°C to +125°C (unless otherwise noted)

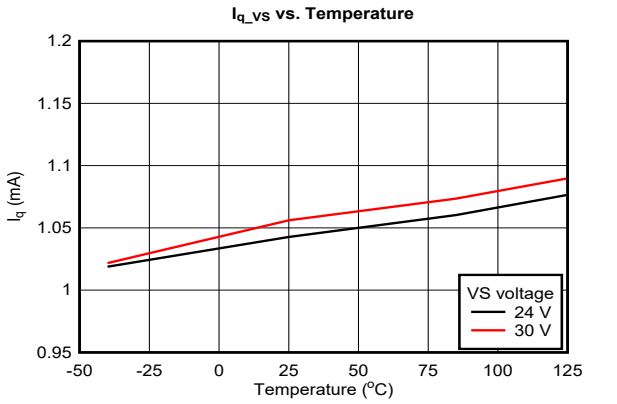
Parameter		Test Conditions	Min	Typ	Max	Unit
t_{DR}	CH1 and CH2 Turnon delay time	V_S = 24 V, R_L = 48 Ω 50% of EN to 10% of VOUT	10	15	25	µs
t_{DF}	CH1 and CH2 Turnoff delay time	V_S = 24 V, R_L = 48 Ω 50% of EN to 90% of VOUT	25	35	50	µs
$SR2_R$	VOUTx rising slew rate	V_S = 24 V, 25% to 75% of V_{OUT}, R_L = 48 Ω	0.45	0.65	1.05	V/µs
$SR2_F$	VOUTx falling slew rate	V_S = 24 V, 75% to 25% of V_{OUT}, R_L = 48 Ω	0.5	0.9	1.4	V/µs
f_{max}	Maximum PWM frequency				1	kHz
t_{ON}	CH1 and CH2 Turnon time	V_S = 24 V, R_L = 48 Ω 50% of EN to 90% of VOUT	25	40	65	µs

7.7 Switching Characteristics (continued)

V_S = 6 V to 36 V, T_J = -40°C to +125°C (unless otherwise noted)

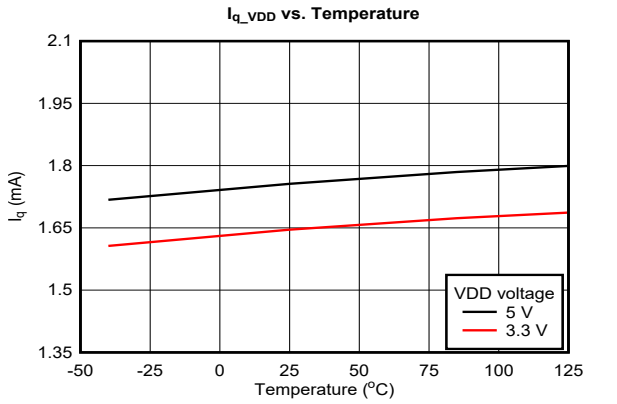
Parameter		Test Conditions	Min	Typ	Max	Unit
t_{OFF}	CH1 and CH2 Turnoff time	V_S = 24 V, R_L = 48 Ω 50% of EN to 10% of VOUT	40	50	80	µs
t_{ON} - t_{OFF}	CH1 and CH2 Turnon and off matching	1ms ON time switch enable pulse V_{BB} = 24 V, R_L = 48 Ω	– 25	0	25	µs
Δ_{PWM}	CH1 and CH2 PWM accuracy - average load current	200-µs enable pulse, V_S = 24 V, R_L = 48 Ω F = f_{max}	– 12.5	0	12.5	%
Δ_{PWM}	CH1 and CH2 PWM accuracy - average load current	100-µs enable pulse, V_S = 24 V, R_L = 48 Ω F = f_{max}	– 20		10	%
t_{ON} - t_{OFF}	CH1 Turnon and off timing matching	100-µs enable pulse, V_S = 24 V, R_L = 48 Ω F = f_{max}	– 40		10	µs
E_{ON}	Switching energy losses during turnon	V_S = 24 V, R_L = 8 Ω, 1 ms pulse, VOUT from 10% to 90% of VS voltage		0.3	0.4	mJ
E_{OFF}	Switching energy losses during turnoff	V_S = 24 V, R_L = 8 Ω, 1 ms pulse, VOUT from 10% to 90% of VS voltage		0.25	0.35	mJ

7.8 Typical Characteristics



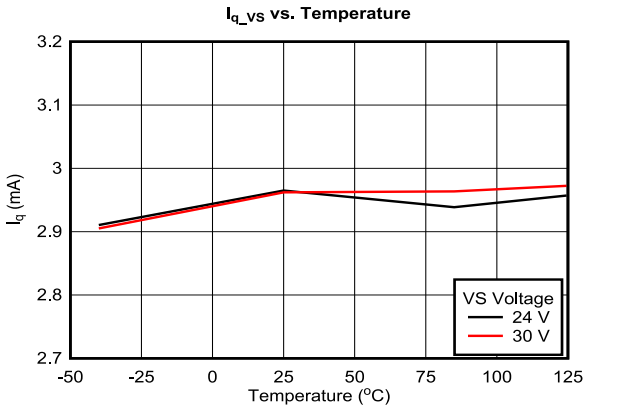
V_{DD} = 3.3 V V_{EN} = 3.3 V V_{DIA_EN} = 0 V
R_{OUT} = open

图 7-1. Quiescent Current ($I_{Q\_VS\_DS}$) From VS Input Supply vs Temperature



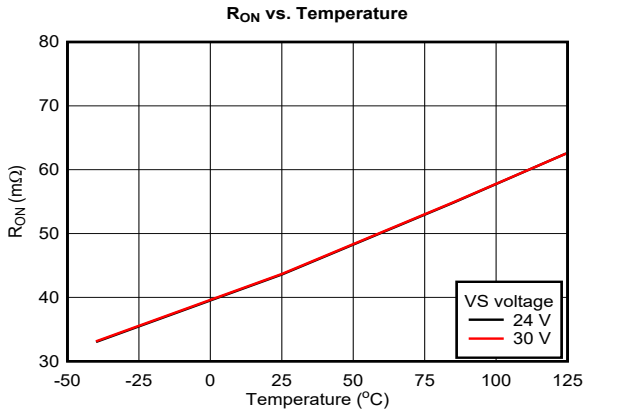
V_S = 24 V V_{EN} = 5 V V_{DIA_EN} = 0 V
R_{OUT} = open

图 7-2. Quiescent Current ($I_{Q\_VDD\_DS}$) From VDD Input Supply vs Temperature



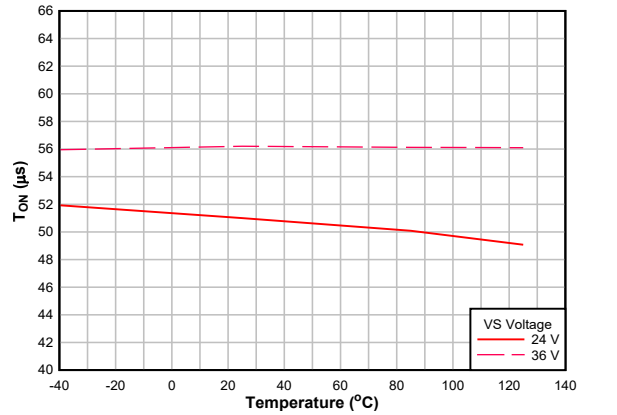
V_{DD} = 0 V V_{EN} = 5 V V_{DIA_EN} = 0 V
R_{OUT} = open

图 7-3. Quiescent Current ($I_{Q\_VS\_SS}$) From VS Input Supply vs Temperature



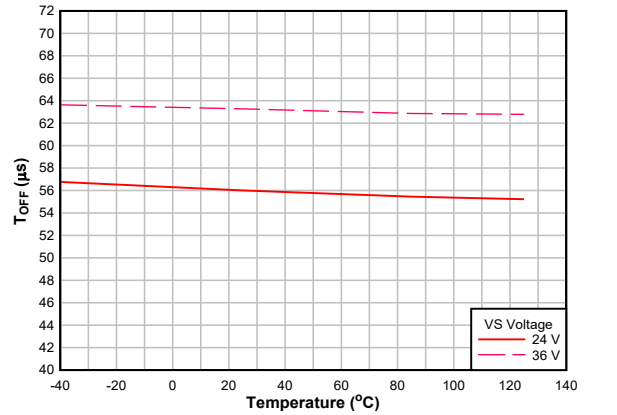
I_{OUT} = 200 mA V_{EN} = 5 V V_{DIA_EN} = 0 V

图 7-4. On Resistance (R_{ON}) vs Temperature



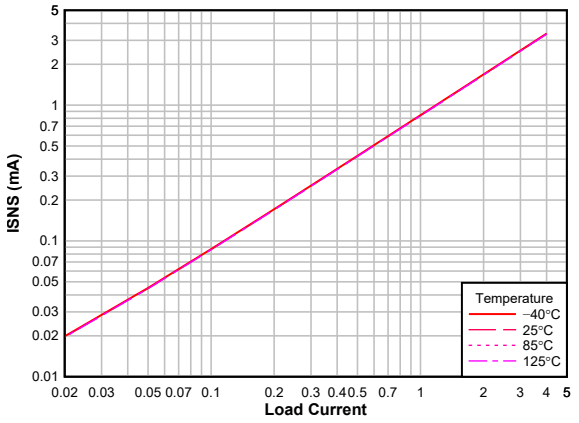
V_S = 24 V V_{EN} = 0 V to 5 V V_{DIA_EN} = 0 V
R_{OUT} = 48 Ω

图 7-5. Turn-on Time (t_{ON}) vs Temperature



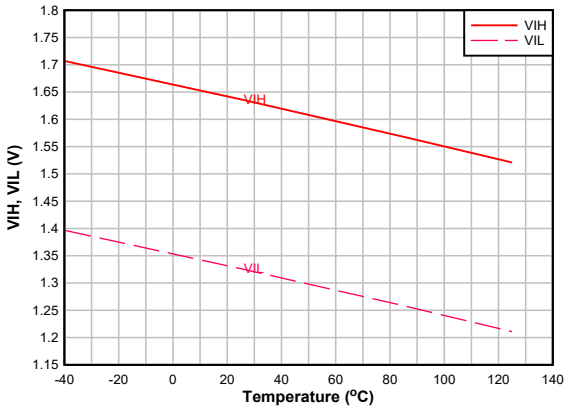
V_S = 24 V V_{EN} = 0 V to 5 V V_{DIA_EN} = 0 V
R_{OUT} = 48 Ω

图 7-6. Turn-off Time (t_{OFF}) vs Temperature



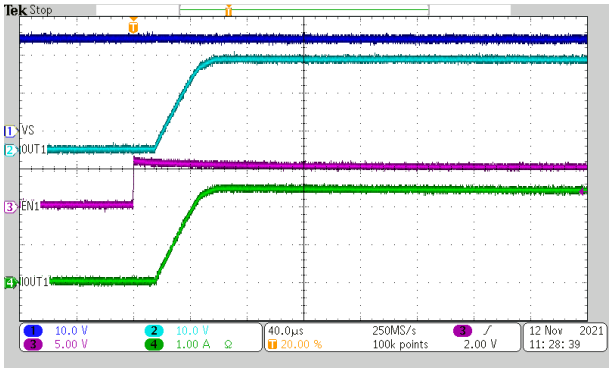
V_S = 24 V, 30 V V_{EN} = 5 V V_{DIA_EN} = 5 V
R_{SNS} = 1 kΩ

图 7-7. Current Sense Output Current (I_{SNSI}) vs Load Current (I_{OUT}) Across Temperature



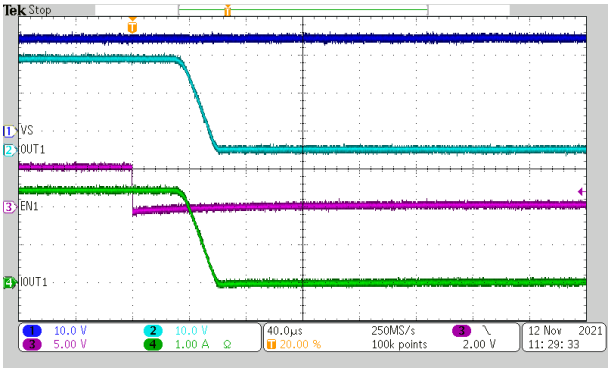
V_S = 24 V V_{DIA_EN} = 0 V R_{OUT} = 1 kΩ

图 7-8. VIH, V_{IL} vs Temperature



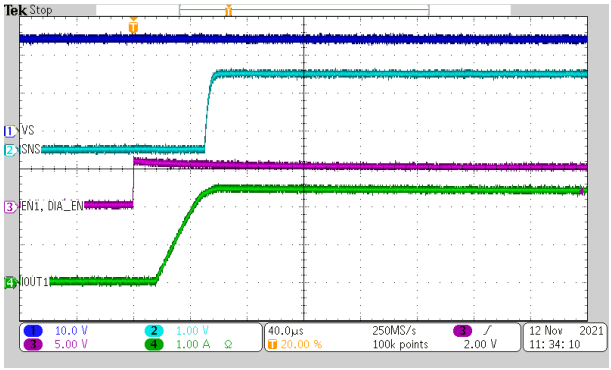
V_{EN} = 0 V to 5 V V_S = 24 V R_{OUT} = 10 Ω

图 7-9. Turn-on Time (T_{ON})



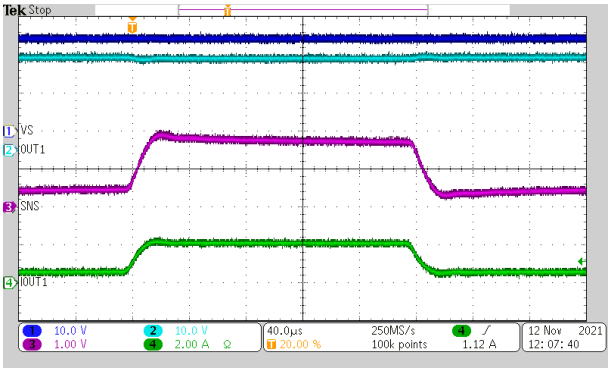
V_{EN} = 5 V to 0 V V_S = 24 V R_{OUT} = 10 Ω

图 7-10. Turn-off Time (T_{OFF})



V_{EN} = V_{DIAG_EN} = 0 V to 5 V V_S = 24 V R_{OUT} = 10 Ω

图 7-11. I_{SNS} Settling Time on DIA_EN Transition



V_{EN} = 5 V V_{DIAG_EN} = 5 V I_{OUT1} = 0.5 A to 2 A

图 7-12. I_{SNS} Settling Time on Rising Load Step

8 Parameter Measurement Information

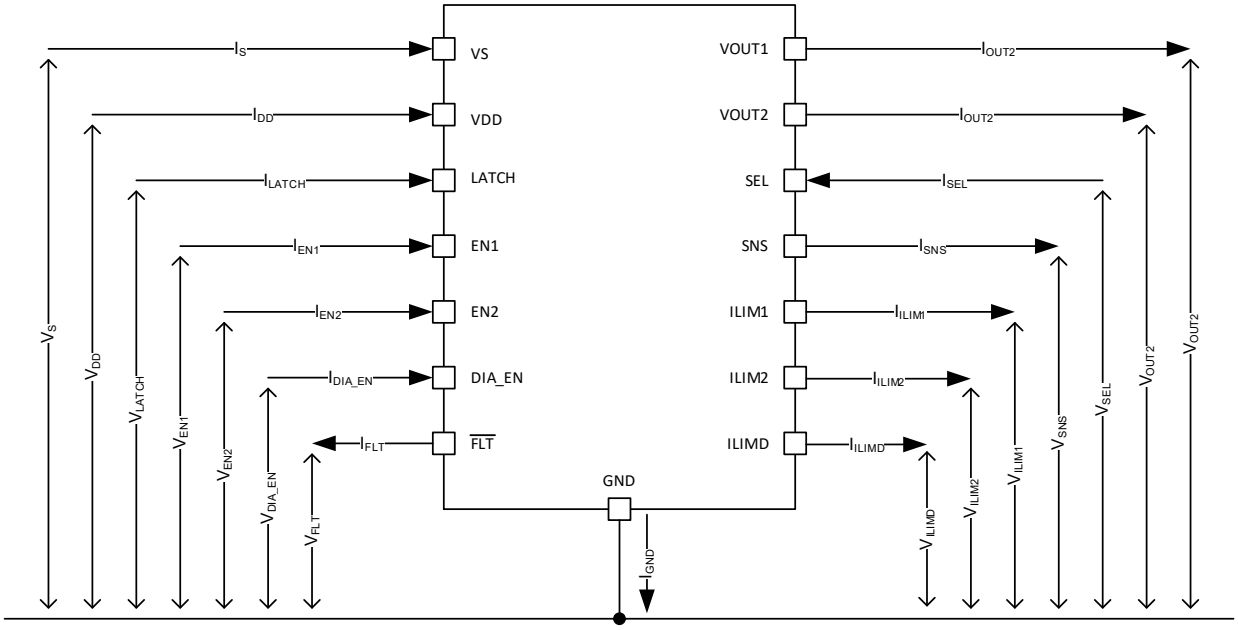
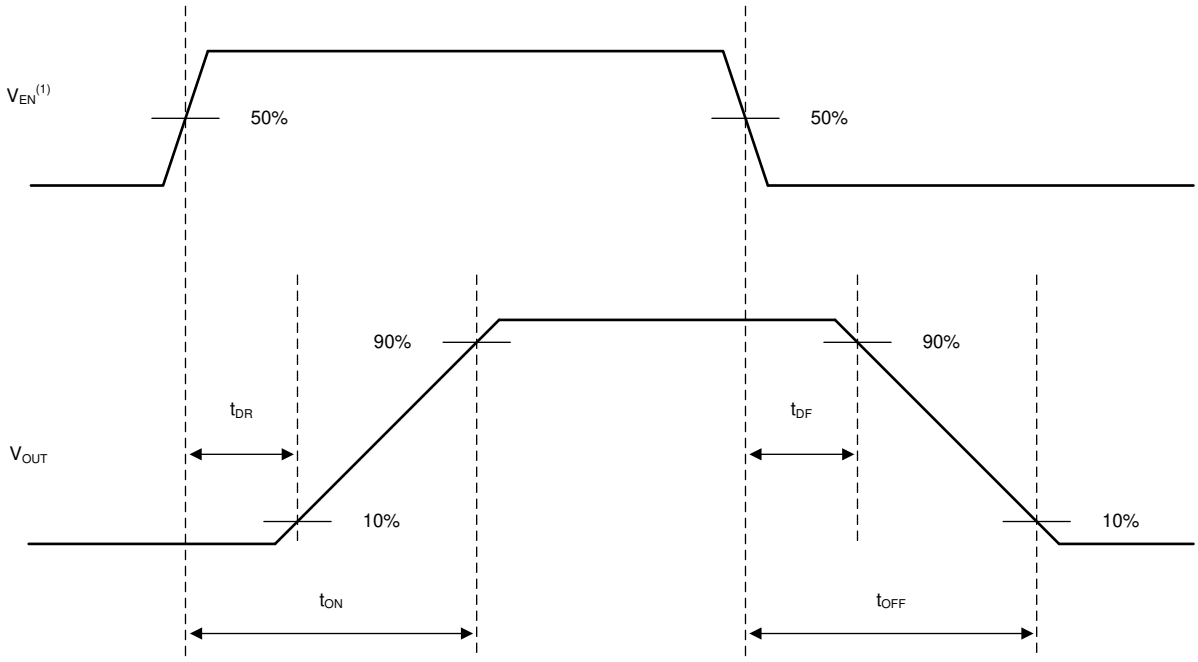
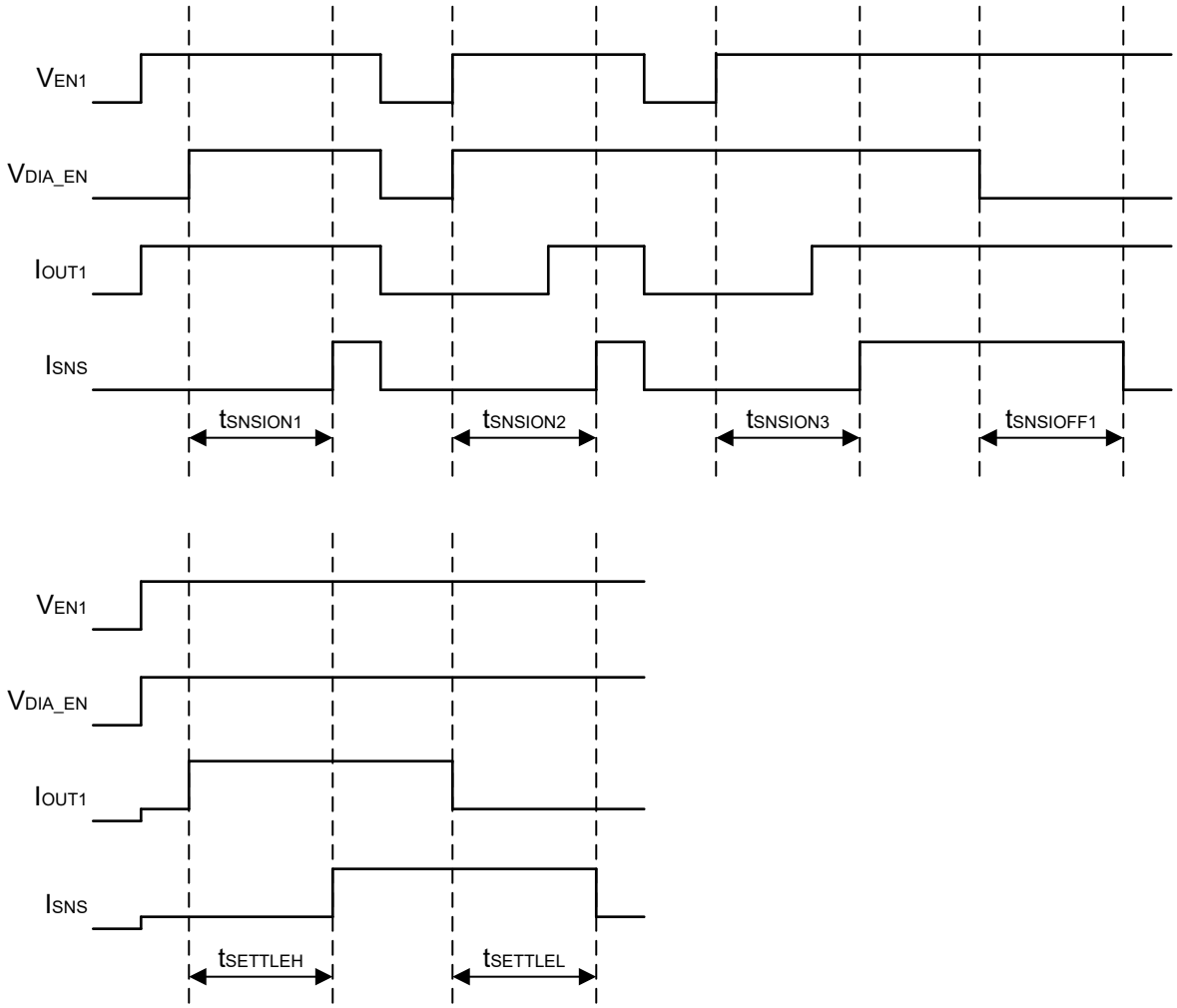


图 8-1. Parameter Definitions



A. Rise and fall time of V_{EN} is 100 ns.

图 8-2. Switching Characteristics Definitions



Rise and fall times of control signals are 100 ns. Control signals include: EN, DIA_EN, SEL
SEL pin must be set to the appropriate value.

图 8-3. SNS Timing Characteristics Definitions

9 Detailed Description

9.1 Overview

The TPS272C45 device is a dual channel 45-mΩ smart high-side switch that is intended to provide protection for output ports in 24-V Industrial systems. The device is designed to drive a variety of resistive, inductive and capacitive loads. The device integrates various protection features including overload protection through current limiting, thermal protection, and short-circuit protection. For more details on the protection features, refer to the *Feature Description* and *Application Information* sections of the document.

In addition, the device diagnostics features include the analog SNS output that is capable of providing a signal proportional to the load current flowing through the switch or constant high current as a fault indication. The high-accuracy load current sense allows for integration of load diagnostic features that can enable predictive maintenance for the system by watching for leading indicators of load failures. The device also integrates open load detection to enable protection against wire breaks. In addition, the device includes a single open drain $\overline{FLT}$ pin output (version A, B, C) and dual $\overline{FLT}$ pin outputs (version D) that indicate device fault states such as short to GND, short to supply, or overtemperature.

The TPS272C45 is one device in TI's industrial high side switch family. For each device, the part number indicates elements of the device behavior. 图 9-1 explains the device nomenclature.

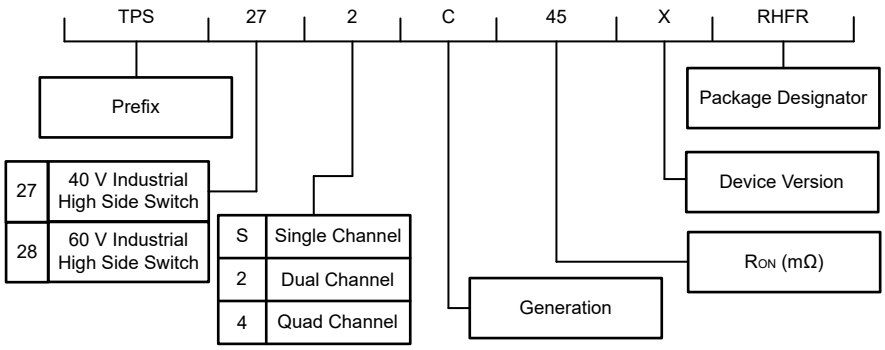
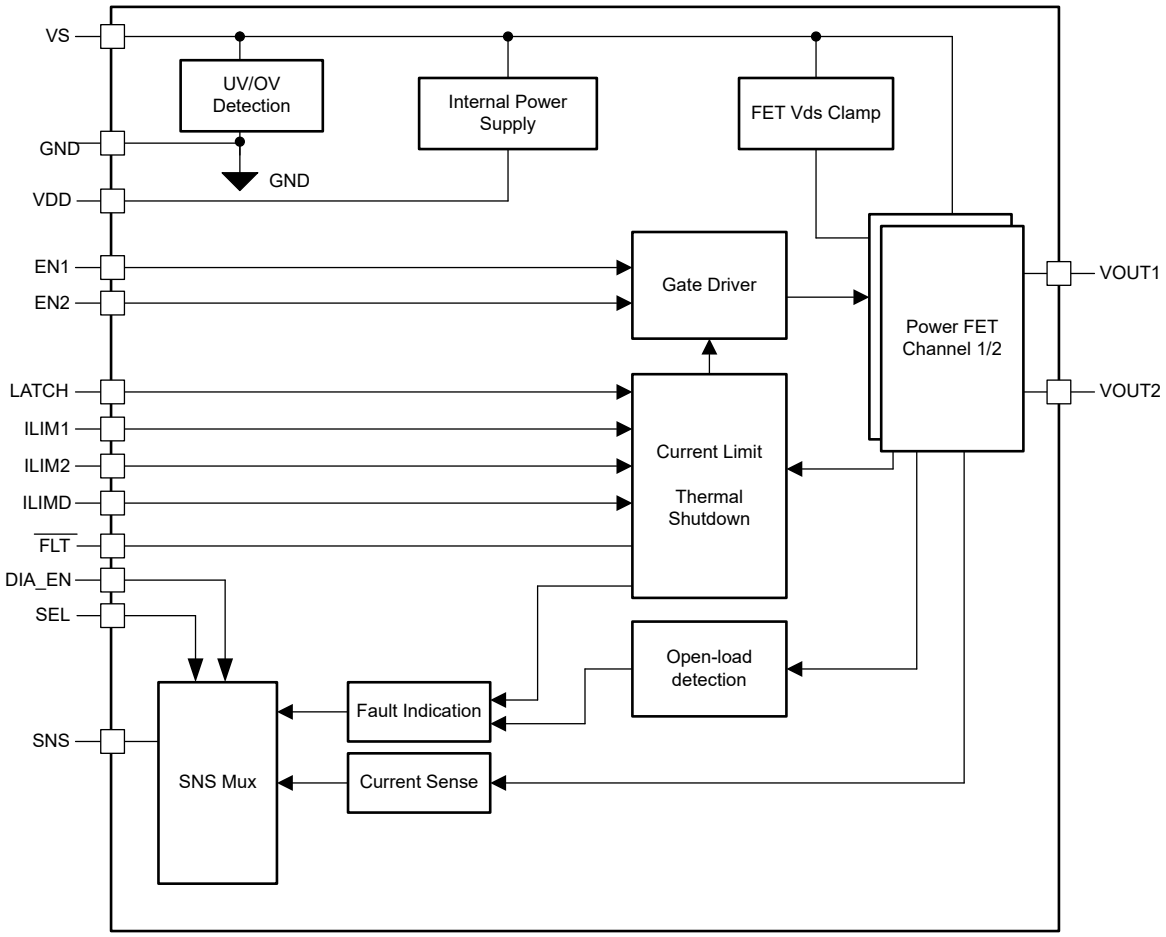


图 9-1. Naming Convention

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Programmable Current Limit

The TPS272C45 integrates a dual stage adjustable current limit. For the most efficient and reliable output protection, the current limit can be set as close to the DC current level as possible. Sometimes, systems require high inrush current handling as well (example incandescent lamp and capacitive loads). By integrating a dual stage current limit, the TPS272C45 enables robust DC current limiting while still allowing flexible inrush handling.

With the adjustable current limit feature, a lower current limit setting can reduce the fault energy and the output current during a load failure event such as a short-circuit or a partial load short (soft-short). By lowering fault energy and current, the overall system improves through:

- Reduced size and cost in current carrying components such as PCB traces and module connectors
- Less disturbance at the power supply (VS pin) during a short circuit event
- Less additional budget for the power supply to account for overload currents in one channel or more
- Improved protection of the downstream load

9.3.1.1 Inrush Current Handling

The TPS272C45 uses a resistor from the following pins to the IC GND to configure the current limit behavior: ILIM1, ILIM2, and ILIMD. The ILIM1 and ILIM2 pin resistors set the current limit thresholds for CH1 and CH2 respectively while ILIMD pin resistor sets a delay time for the device to operate in a higher or lower current limit during device start-up or output turn-on by retry after a fault (thermal) shutdown).

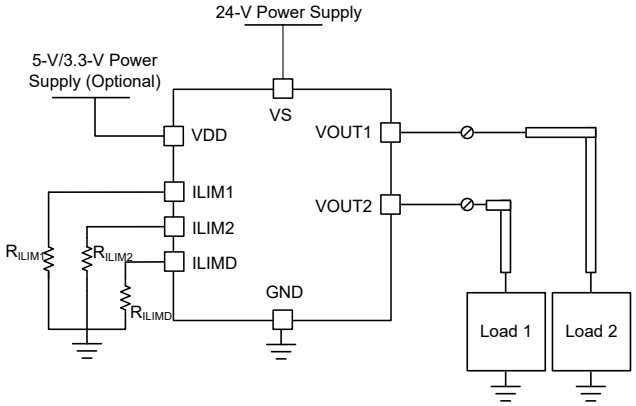


图 9-2. Current Limit Set Functionality

The ILIM1/ILIM2 thresholds and the ILIMD pin resistor controlled timing enable flexible inrush current control behavior. The following table shows the various options available.

表 9-1. Inrush Current Limit Options

Case Number	ILIMD Resistor Settings	Inrush Delay Time (ms)	Current Limit During Inrush Duration	Notes
1	Short to GND	0	At the level set by ILIM1/2 resistor	The device shows constant current limit threshold in each channel at all times set by the ILIM1/2 resistors.
2	Discrete resistor values (See table below)	Programmable in discrete steps 2- 18	Current limit at 2 times the level set by ILIM1/2 resistor	The current is set higher during the duration of the inrush delay to support high inrush current loads like incandescent lamps. See figure (case 1) showing current limit behavior enabling into a short circuit with ILIM1/2 threshold set at 2.2 A.
3	40.2 kΩ +/– 2%	Fixed 30	Current limit fixed at 1.5-A threshold for Vds > 16 V, or at the level set by ILIM1/2 resistor if Vds < 16 V	Additional feature to limit the current and power dissipation during initial phase of charging large power supply capacitor loads. The Vds dependence of current limit exists only during the duration set by the ILIMD resistor. If the ILIMD resistor is not connected (floating) or > 40.2 kΩ, the inrush current limit behavior defaults to Case 3.

表 9-2. Delay Resistor Values

ILIMD Resistor Value	Delay
3.48 kΩ	2 ms
7.15 kΩ	4 ms
12.1 kΩ	6 ms
17.8 kΩ	10 ms
24.9 kΩ	18 ms

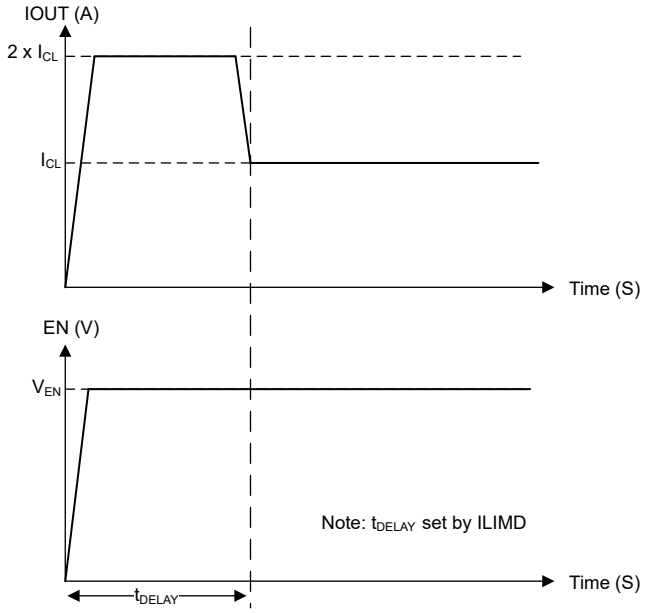


图 9-3. Inrush Current Control (Case 2) With a Shorted Load

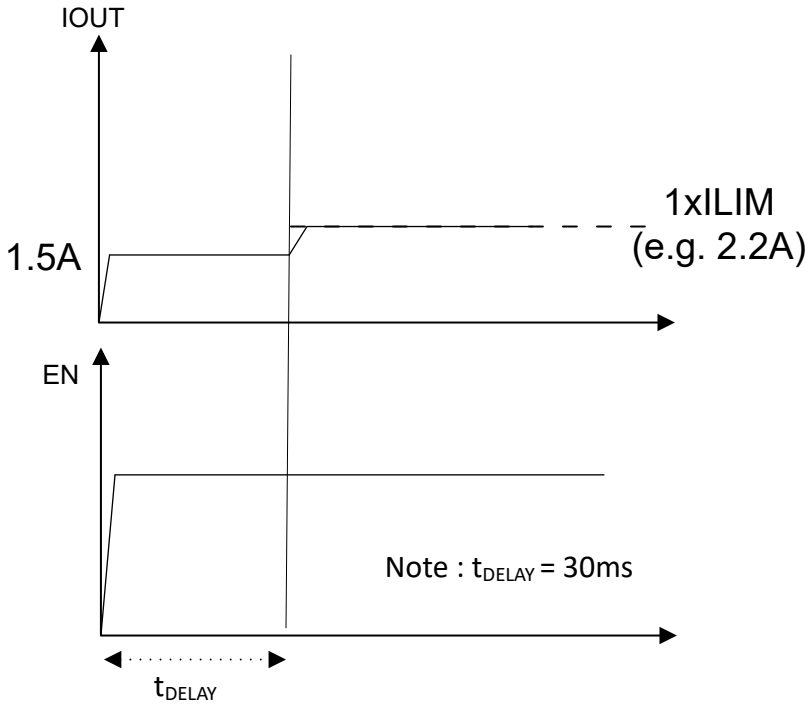


图 9-4. Inrush Current Control (Case 3) With a Shorted Load

For the Case 2, when the ENx pin goes high to turn on one of the channels (or the channel is turned on automatically to retry after a fault shutdwon), the device defaults to twice current limit threshold as determined by R_{ILIM1}/R_{ILIM2} or the maximum internal current limit level (whichever is lower). The internal current limit level is defined in the *Specifications* section of this document. After a T_{DELAY} period that is determined by R_{ILIMD}, the current limit changes to the threshold determined by R_{ILIM1}/R_{ILIM2}. The delay can be set in the range from 0 (the current limit threshold at all times set to that determined by R_{ILIM1}/R_{ILIM2}) to a maximum of 22 ms in dscrete steps.

Each channel operates independently with current limit thresholds controlled by R_{ILIM1} and R_{ILIM2}(so both channels can have separate current limit thresholds). If channel 2 is enabled after channel one, channel 2 has its own separate timing.

The initial inrush current period when the current limit is higher enables two different system advantages when driving loads

- Enables higher load current to be supported for a period of time of the order of milliseconds to drive high inrush current loads like incandescent bulb loads.
- Enables fast capacitive load charging. In some situations, it is ideal to charge capacitive loads at a higher current than the DC current to ensure quick supply bring up. This architecture allows a module to quickly charge a capacitive load using the initial higher inrush current limit and then use a lower current limit to reliably protect the module under overload or short circuit conditions.

While in current limiting mode, at any level, the device has a high power dissipation. If the FET temperature exceeds the over-temperature shutdown threshold, the device turns off just the channel that is overloaded. After cooling down, the device either latches off or re-tries, depending on the state of the LATCH pin. If the device is turning off prematurely on start-up, TI recommends to improve the PCB thermal layout, lower the current limit to lower power dissipation, or decrease the inrush current (capacitive loading).

9.3.1.2 Calculating R_{ILIMx}

To set the current limit thresholds, connect resistors from both ILIM1 and ILIM2 pins to GND. The current limit threshold for each channel is determined by Equation 1 (R_{ILIMx} in kΩ):

$$I_{CL} = K_{CL} / R_{ILIMx} \quad (1)$$

The nominal K_{CL} value to be used in the calculation is 20.5 A.kΩ. The allowed R_{ILIMx} range is between 5 kΩ and 28.2 kΩ. If either pin is floating, grounded, or outside of the range specified, the current limit defaults to an internal level that is defined in the *Specifications* section of this document.

9.3.1.3 Configuring ILIMx From an MCU

In many situations, modules like to allow the current limit to be set programmatically from an MCU. This action enables a module to set current limits to fit the load after determining what load is plugged in. As described, the TPS272C45 current limits are set by R_{ILIMx}. However, the R_{ILIMx} that is seen by the device can be configured through small external FETs as shown in 图 9-5.

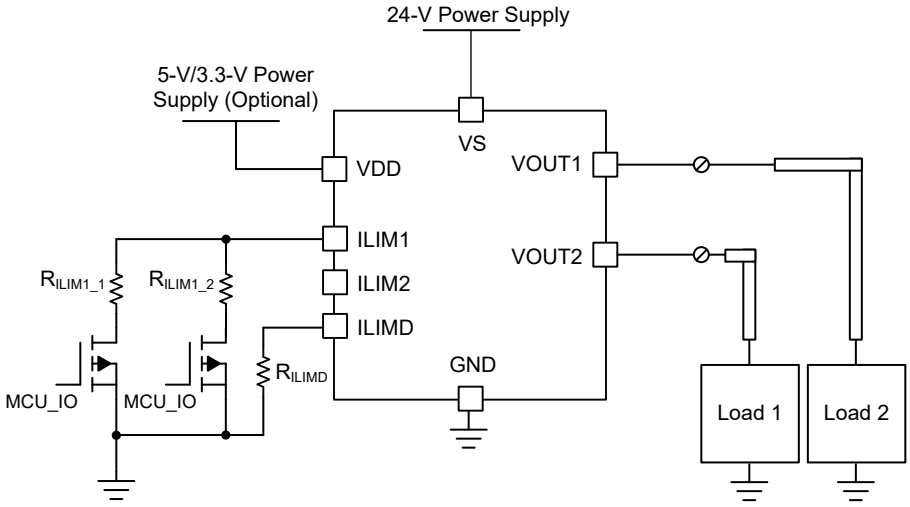


图 9-5. Dynamic ILIMx Control

For example, R_{ILIM1_1} can set the device to 500-mA ILIM while R_{ILIM1_2} can set the device at 2-A ILIM. After the MCU realizes how much current draw is required by the load, the MCU can drive one of the series FET's to set

the ILIM to be ideal for the specific load. The current limit (ILIM1 and ILIM2) thresholds can be changed dynamically, but the inrush current limit delay set with the ILIMD resistor cannot be changed after powerup.

The external FET switches used to dynamically adjust the current limit must be chosen with a minimum capacitance (Coss) from the drain the ground. The total capacitance to PCB ground at the ILMx pins including from traces must be limited to less than 100 pF.

9.3.2 Low Power Dissipation

There are two primary sources of power dissipation in the TPS272C45:

1. Resistive losses in the primary FET, which are calculated as $(I_{LOAD})^2 \times R_{ON}$
2. Controller losses due to quiescent operating current, which are calculated as $I_Q \times V_{SUPPLY}$

If I_{LOAD} is significantly more than 1 A, the resistive losses dominates the controller losses and they can be ignored. However, if I_{LOAD} is less than 1 A, the controller losses comprise a significant portion of the total device power dissipation. To lower the controller losses, version A of the TPS272C45 introduces a secondary low voltage supply on pin VDD that can power much of the device functionality. By lowering the controller supply voltage from 24 V to 3.3 V, the total controller losses decrease significantly. 表 9-3 shows the impact this second supply can make on the total device power dissipation calculated at a worst case supply voltage of 30 V, without diagnostics enabled. There is an additional contribution to power dissipation from the current sense circuitry as well as the sensed current out of the SNS pin when diagnostics are enabled. Savings of over 80 mW per channel in the IC is achieved by powering the device with a separate 3.3-V supply.

表 9-3. Power Dissipation Calculations

I_{LOAD}	Version	Resistive Losses (Maximum, 125°C)	Controller Losses (Maximum, 125°C)	Total P_{DISS} (Maximum, 125°C)
500 mA (both channels)	B	39 mW	211 mW	250 mW
	A	39 mW	50 mW	89 mW
2 A (both channels)	B	624 mW	211 mW	735 mW
	A	624 mW	50 mW	674 mW

By using version TPS272C45A and providing a 3.3-V supply to the VDD pin, for a 500-mA output module the worst case device total heating is cut from 250 mW to 89 mW, about a 30% decrease in per channel power dissipation. This lower power dissipation, in addition to the small size of the TPS272C45, enables modules that have many low current outputs to shrink the size of their casings without limiting output power distribution capability. To minimize power dissipation, the VDD supply must be powered by a small DC/DC providing the less than 5 mA per device. Multiple devices can use one DC/DC converter to limit system costs, as shown in 图 9-6.

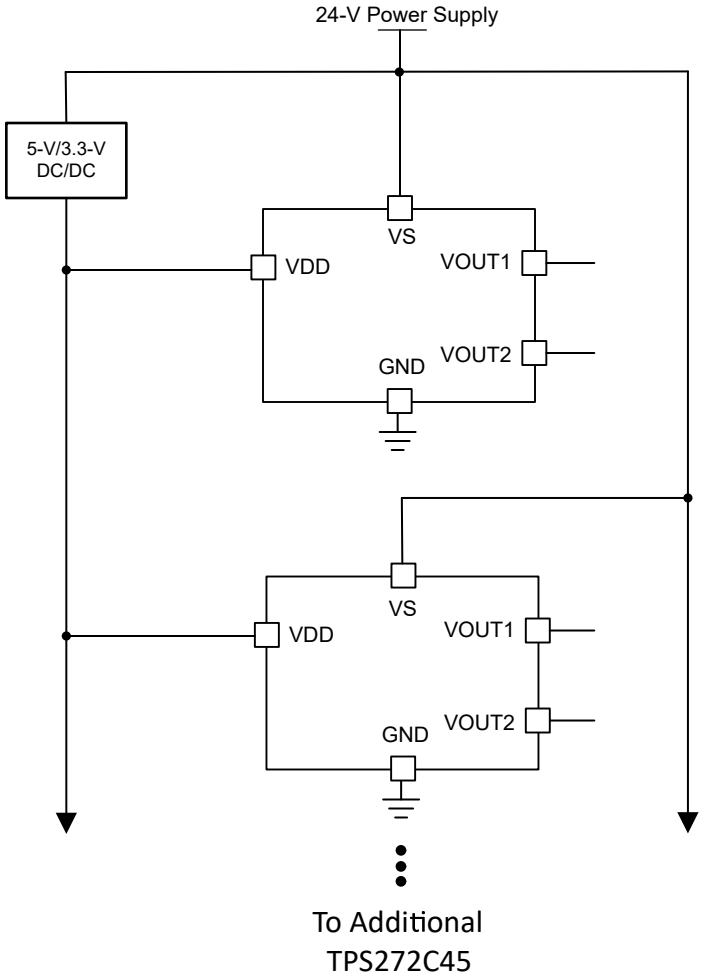


图 9-6. Secondary Low Voltage Supply Schematic

For higher current modules, the resistive losses dominate the total power dissipation and the impact of the secondary supply is less valuable. For example, 表 9-3 shows that for a 2-A output, providing the secondary supply lowers the total device dissipation by only 12%. In this case, to lower total system costs, versions with an internal regulator that need only single supply input can be used. If using versions C or D and the secondary supply is not useful or available, the VDD pin can be grounded and all current is drawn from the primary supply with no loss of functionality, but higher power dissipation.

9.3.3 Protection Mechanisms

The TPS272C45 protects the system against load fault events like short circuits, inductive load kickback, overload events, overvoltage and over-temperature events. This section describes the details for protecting against each of these fault cases.

There are a number of protection features which, if triggered, causes the switch to automatically disable:

- Current limit
- Thermal shutdown
- DC overvoltage on VS supply above the overvoltage protection threshold, V_{OVPR}

When one of these protections are triggered for either channel, the device enters the FAULT state. In the FAULT state, the fault indication is available on the $\overline{FLT}$ pin for an MCU to monitor and react to.

The fault indication is reset and the switch turns back on when all of the below conditions are met:

- LATCH pin is low

- t_{RETRY} has expired
- All faults are cleared (thermal shutdown, current limit, overvoltage)

9.3.3.1 Short-Circuit Protection

TPS272C45 provides output short-circuit protection to ensure that the device prevents current flow in the event of a low impedance path to GND, removing the risk of damage or significant supply droop. The device is specified to protect against short-circuit events regardless of the state of the ILIM pins and or supply voltages up to 36V and across the entire opeprating temperature range -40 °C 125°C.

图 9-7 shows the behavior of the TPS272C45 when the device is enabled into an overload condition and then recovers to a normal load.

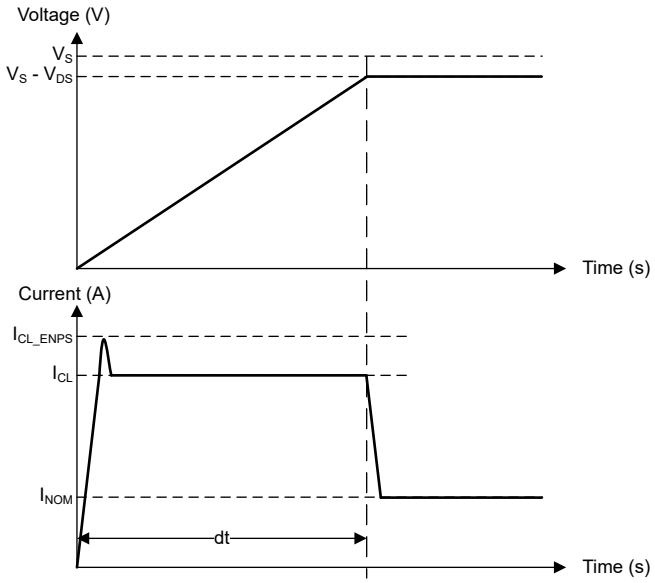


图 9-7. Enable into Short-Circuit Behavior

Due to the low impedance path, the output current rapidly increases until it hits the current limit threshold. Due to the response time of the current limiting circuit, the measured maximum current can temporarily exceed the I_{CL} value defined as I_{CL_ENPS}, before it settles to the current limit regulation value (I_{CL}).

In this state high power is dissipated in the FET, so eventually the internal thermal protection temperature for the FET is reached and the device safely shuts down. Then if LATCH pin is low the part waits t_{RETRY} amount of time and turns back on.

图 9-8 shows the behavior of the TPS272C45 when a short-circuit occurs when the device is in the on-state and already outputting current. When the internal pass FET is fully enabled, the current clamping settling time is slower so to ensure overshoot is limit, the device implements a fast trip turn-off at a high current threshold (approximately 40% higher than I_{CL}). When this fast trip threshold is hit, the device shuts off after a delay for a short period of time before quickly re-enabling and clamping the current to the regulation current limit level (I_{CL}) after a brief transient overshoot to the higher peak current level. The device then keeps the current clamped at the regulation current limit until the thermal shutdown temperature is hit and the device safely shuts off.

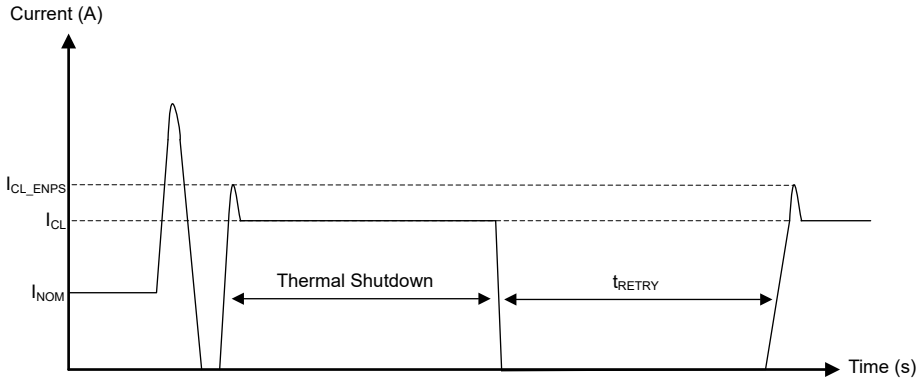


图 9-8. On-State Short-Circuit Behavior

Overload Behavior shows the behavior of the TPS272C45 when there is a small change in impedance that sends the load current above the I_{CL} threshold. The current rises to I_{CL_LIN} above the regulation level. Then the current limit regulation loop kicks in and the current drops to the I_{CL} value.

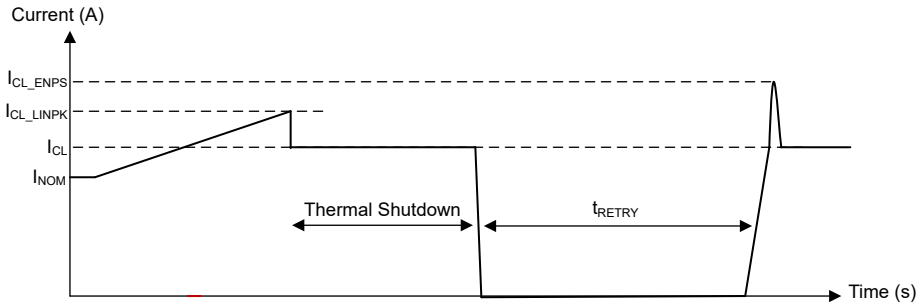


图 9-9. Overload Behavior

In all of these cases, the internal thermal shutdown is safe to hit repetitively. There is no device risk or lifetime reliability concerns from repeatedly hitting this thermal shutdown level.

9.3.3.1.1 V_S During Short-to-Ground

When V_{OUT} is shorted to ground, the module power supply (V_S) can see a transient decrease. This decrease is caused by the sudden increase in current flowing through the cable inductance. For ideal system behavior, TI recommends that the module maintain V_S > 3 V (above the maximum V_{UVLOF}) during V_{OUT} short-to-ground. This event is typically accomplished by placing bulk capacitance on the power supply node. If V_S goes below V_{UVLOF}, the device can sustain unexpected latch and timing behavior.

9.3.3.2 Inductive Load Demagnetization

When switching off an inductive load, the inductor can impose a negative voltage on the output of the switch. The TPS272C45 includes voltage clamps between V_S and V_{OUT} to limit the voltage across the FETs and demagnetize load inductance if there is any. The negative voltage applied at the OUT pin drives the discharge of inductor current. 图 9-10 shows the device discharging a 40-mH load.

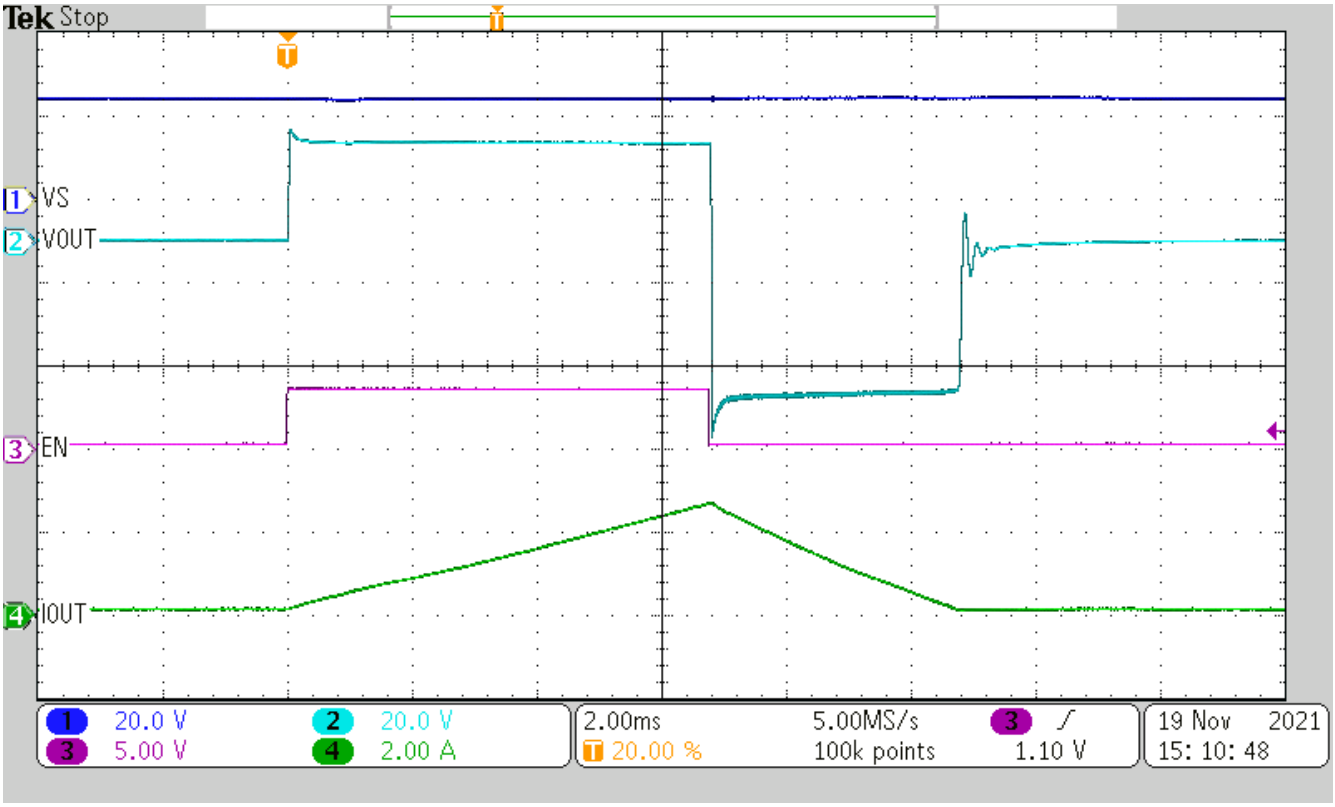


图 9-10. TPS272C45 Inductive Discharge (40 mH)

The maximum acceptable load inductance is a function of the energy dissipated in the device and therefore the load current and the inductive load. The maximum energy and the load inductance the device can withstand for one pulse inductive dissipation at 125°C is shown in 图 9-11.The device can withstand 50% of this energy for one million inductive repetitive pulses with a >4-Hz repetitive pulse. If the application parameters exceed this device limit, use a protection device like a freewheeling diode to dissipate the energy stored in the inductor.

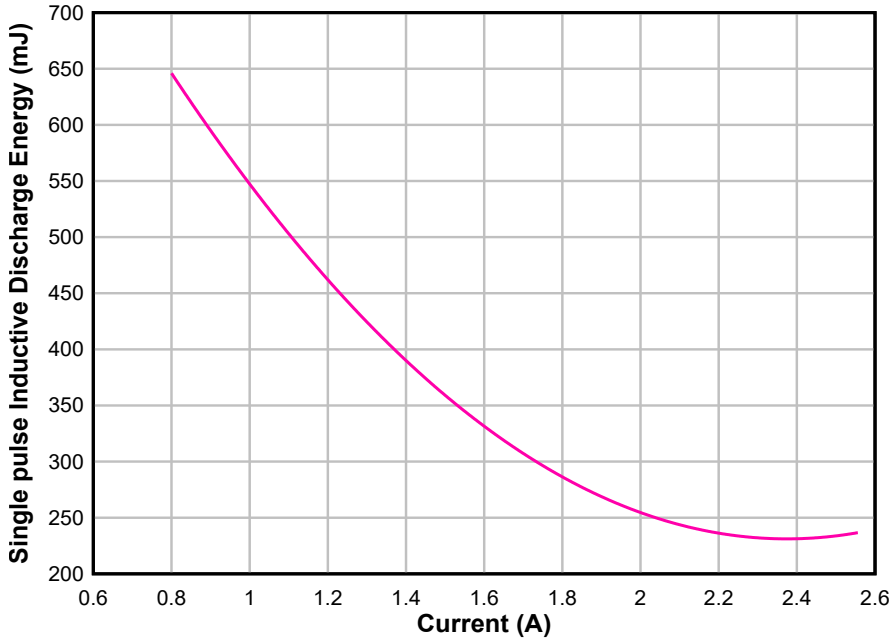


图 9-11. TPS272C45 Inductive Load Discharge Energy Capability at 125°C

For more information on driving inductive loads, refer to TI's *How to Drive Inductive, Capacitive, and Lighting Loads With Smart High-Side Switches* application report.

9.3.3.3 Thermal Shutdown

The TPS272C45 includes a temperature sensor on the power FET and also within the controller portion of the device. The device registers a thermal shutdown fault:

- $T_{J,FET} > T_{ABS}$
- $T_{J,FET} - T_{J,control} > T_{REL}$

After the fault is detected, the switch turns off. If $T_{J,FET}$ passes T_{ABS}, the fault is cleared when the switch temperature decreases by the hysteresis value, T_{HYS}. If instead the T_{REL} threshold is exceeded, the fault is cleared after T_{RETRY} passes.

Each channel shuts down independently in case of a thermal event, as each has its own temperature sensor and fault reporting.

9.3.3.4 Undervoltage Lockout on VS (UVLO)

The device monitors the supply voltage at the VS pin to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to V_{UVLOF}, the device enters the shut down state automatically. When the supply rises up to V_{UVLOR}, the device turns back on.

Fault is not indicated on the $\overline{FLT}$ pin during an UVLO event. During an initial ramp of V_{VS} from 0 V at a ramp rate slower than 1 V/ms, V_{ENx} pins must be held low until V_S is above the UVLO threshold. For best operation, ensure that V_S has risen above UVLO before setting the V_{ENx} pins to high.

9.3.3.5 Undervoltage Lockout on Low Voltage Supply (VDD_UVLO)

The device monitors the input supply voltage V_{VDD} (in versions A/C/D with external supply input) to prevent unpredictable behavior in the event that the supply voltage is too low. When the supply voltage falls down to V_{VDD_UVLOF}, the device switches operation to the VS (24 V) power supply, but results in increased current draw from the VS supply input.

9.3.3.6 Power-Up and Power-Down Behavior

All versions of the device power up from the OFF state only when the VS supply input exceeds the $V_{VSUVLOR}$ threshold (independent of the VDD supply input level). When VS supply is above the threshold, the internal regulators are enabled, the device version is recognized. The device then enters the standby state. With versions A, C, and D and using using an external supply on VDD pin - the device will use the internal regulators until the VDD voltage exceeds V_{VDD_UVLOR}.

In case the VDD power supply is enabled first and the VDD voltage exceeds V_{VDD_UVLOR} before the VS supply is up and the VS voltage exceeds VS_{UVLOR}, the device remains in the off-state.

The behavior of all versions of the device in case of brown-out or power loss in VS supply is as described in *Undervoltage Lockout on VS (UVLO)*. For versions A, C, and D if the VDD power supply is lost (VDD supply voltage falls below V_{VDD_UVLOR} threshold), the device switches over to the internal power supply, the switch outputs are disabled.

9.3.3.7 Overvoltage Protection (OVPR)

The device monitors the supply voltage V_{VS} to prevent higher voltages from appearing at the output than can be supported by the load, when the supply voltage is too high. When the supply voltage goes above V_{VS_OVPR}, the FET is shut down automatically after a deglitch time to prevent short transients or noise from triggering the protection. When the supply falls below V_{VS_OVPF}, the FET is allowed to turn back on.

9.3.4 Diagnostic Mechanisms

As systems demand more intelligence, it is becoming increasingly important to have robust diagnostics measuring the conditions of output power. The TPS272C45 integrates many diagnostic features that enable modules to provide predictive maintenance and intelligence power monitoring to the system.

9.3.4.1 Current Sense

The SNS output can be used to sense the load current through either channel. The SNS pin outputs a current that is proportional to the load current through either channel, depending on the state of the SEL pin. This current is sourced into an external resistor to create a voltage that is proportional to the load current. This voltage can be measured by an ADC or comparator and used to implement intelligent current monitoring for a system. To ensure accurate sensing measurement, R_{SNS} must be connected to the same ground potential as the μC ADC.

The SNS pin output is controlled by the SEL pin. If SEL pin is low, SNS outputs load current proportional to channel 1, whereas if SEL is high SNS outputs load current proportional to channel 2.

Equation 3 shows the transfer function for calculating the load current from the SNS pin current.

$$I_{SNSI} = I_{OUT} / K_{SNS} \quad (2)$$

K_{SNS} is defined in the *Specifications* section.

9.3.4.1.1 R_{SNS} Value

The following factors must be considered when selecting the R_{SNS} value:

- Current sense ratio (K_{SNS})
- Largest and smallest diagnosable load current required for application operation
- Full-scale voltage of the ADC
- Resolution of the ADC

For an example of selecting R_{SNS} value, reference *R_{ISNS} Calculation* in the applications section of this data sheet.

9.3.4.1.1.1 Current Sense Output Filter

To achieve the most accurate current sense value, TI recommends to filter the SNS output. There are two methods of filtering:

- Low-Pass RC filter between the SNS pin and the ADC input. This filter is illustrated in 图 10-1 with typical values for the resistor and capacitor. The designer must select a C_{SNS} capacitor value based on system requirements. A larger value provides improved filtering but a smaller value allows for faster transient response.
- The ADC and microcontroller can also be used for filtering. TI recommends that the ADC collects several measurements of the SNS output. The median value of this data set must be considered as the most accurate result. By performing this median calculation, the microcontroller can filter out any noise or outlier data.

9.3.4.2 Fault Indication

The following faults are registered on the $\overline{FLT}$x pin:

- FET thermal shutdown
- Active current regulation
- Thermal Shutdown caused by current limitation
- Open-load (FET OFF state only)

Open-load or short-to-supply are not indicated while the switch is enabled, although in on-state these conditions can still be detected through the sensed current (ISNS current). Hence, if there is a fault indication while the channel is enabled, then it must be either due to an overcurrent or overtemperature event. On the other hand, a fault indication while the output (FET) is disabled must be either due to an open load or output short-to-supply.

In versions A, B, C of the device, the open drain $\overline{FLT}$ pin output is a global fault output. $\overline{FLT}$ pin indicates a fault when one occurs in either channel. The $\overline{FLT}$ signal can be deactivated by toggling the EN input of the faulted channel and sequential toggling of ENx inputs can be used to determine the faulted channel. In versions A, B, C

of the device the SNS pin also indicates the fault status of the channel, provided the faulted channel is selected with the SEL pin.

In version D of the device, there are two ($\overline{FLT1}$ and $\overline{FLT2}$) pin outputs corresponding the presence of a fault in each channel. The independent $\overline{FLTx}$ signals can be used to easily determine the faulted channel. The $\overline{FLTx}$ signal is deactivated by toggling the EN input of the faulted channel. In version D of the device the SNS pin does not indicate the fault status of the channel, just the load current sense.

表 9-4 shows the states for both the SNS pin and the $\overline{FLT}$ pins based on the fault states and ENx/SEL pin state (applies to versions A, B, C). By looking at these pins, it is possible to detect where the fault has occurred. The method to identify the channel that caused the $\overline{FLT}$ signal is as follows when an MCU is monitoring the SNS pin output. If the SNS is signaling a fault (with I_{SNSFH} current output) while SEL=LO, then the fault is in channel 1, whereas with SEL=HI, the fault is in channel 2. If SNS pin signals fault with SEL at either LO or HI, then both channels are faulted. As discussed earlier, the type of faults (whether it is overcurrent, overtemperature or open-load) can be determined by the state of EN input in each channel. If the SNS pin output is not monitored, it is still possible to identify the channel that is faulted. To do this, the EN pin in each channel must be toggled (LO to HI or HI to LO as the case can be). If the fault indication on the $\overline{FLT}$ pin is removed by toggling the EN input in a channel, then the fault is in that channel. If the fault indication does not go away with toggling EN input of both channels, then the fault is in both. The time duration for toggling the EN input must be kept below 10 us to ensure that there is no impact on the actual output of the channels.

表 9-4. Device Fault Mux (Versions A, B, C)

INPUTS			OUTPUTS	
SEL	CH1 FAULT	CH2 FAULT	SNS	$\overline{FLT}$
0	0	0	CH1 load current	High
0	0	1	CH1 load current	Low
0	1	0	Corresponds to fault case(1)	Low
0	1	1	Corresponds to fault case(1)	Low
1	0	0	CH2 load current	High
1	0	1	Corresponds to fault case(1)	Low
1	1	0	CH2 load current	Low
1	1	1	Corresponds to fault case(1)	Low

(1) 表 9-5 describes this behavior

While typically the SNS pin output corresponds to I_{LOAD}, in a fault case the switch turns off and I_{LOAD} goes to zero so the SNS behavior is modified in a fault case. In the event of a fault cases where SEL is monitoring the proper channel, the SNS pin outputs a voltage level corresponding to the fault type to enable improved diagnosis as shown in 表 9-5.

By looking at the combination of the ENx condition, $\overline{FLT}$, and SNS pins, it is possible to distinguish between fault states. Each channel has independent fault states, so the table below applies to CH1 when SEL = LO and CH2 when SEL = HI.

表 9-5. Distinguishing Different Fault Cases (Versions A, B, C)

Channel State	Fault Case	SNS	$\overline{FLT}$
Enabled	Regulating current past the initial inrush delay set by ILIMD resistor	I_{SNSFH}	Low
	Short-to-supply/open-load	0	High
	T_J overtemperature	I_{SNSFH}	Low

表 9-5. Distinguishing Different Fault Cases (Versions A, B, C) (continued)

Channel State	Fault Case	SNS	$\overline{FLT}$
Disabled	Short-to-supply/open-load	I_{SNSFH}	Low
	T_J overtemperature	0	High

In version D of the device the fault table is shown in 表 9-6. By looking at these pins, it is possible to detect which channel the fault has occurred. As discussed earlier, the type of faults (whether it is overcurrent, overtemperature or open_load) can be determined by the state of EN input in each channel.

表 9-6. Device Fault Mux (Version D)

INPUTS		OUTPUTS	
CH1 FAULT	CH2 FAULT	$\overline{FLT1}$	$\overline{FLT2}$
0	0	High	High
0	1	High	Low
1	0	Low	High
1	1	Low	Low

9.3.4.2.1 Fault Event Diagrams

备注

All timing diagrams assume that the SEL pin is low to measure channel one behavior on the SNS pin. DIA_EN and SEL pins have no effect on the $\overline{FLT}$ (versions A, B, C) or $\overline{FLT1}$, $\overline{FLT2}$ (version D) pin output.

The LATCH, SEL, DIA_EN, and ENx pins are controlled by the user. The timing diagrams represent possible use-cases.

图 9-12 shows the device fault reporting behavior in the event of a fault in channel 2 (only) with LATCH and SEL pin set to LO. As shown, the fault signaling is deactivated when EN is toggled (in this case from HI to LO to HI). The faulted channel can be determined by toggling the EN pin with a short pulse (less than 10-us wide) that does not affect the output of the channel.

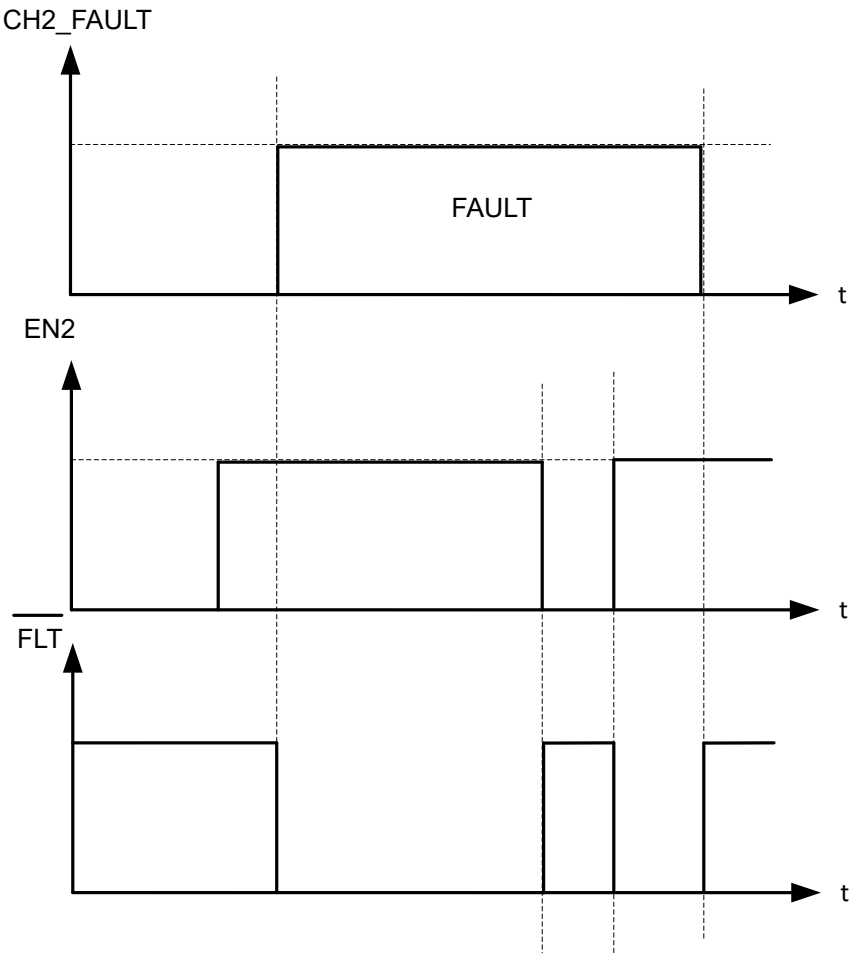


图 9-12. FLT Pin Behavior (Versions A, B, C)

图 9-13 shows the device fault reporting behavior in the event of an overcurrent fault when EN goes high. As shown, the fault signaling is active only after the initial inrush current limit phase is complete.

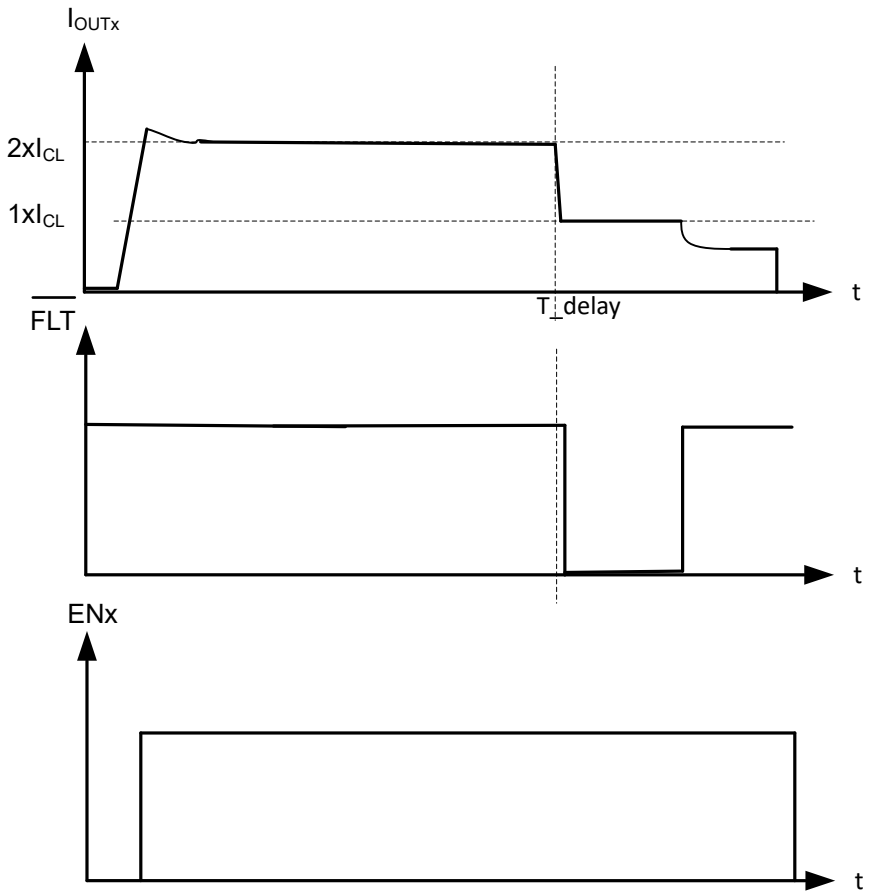


图 9-13. FLT Pin Behavior With an Overcurrent Event On Channel Enable (Versions A, B,C)

图 9-14 shows the device fault and retry behavior when there is a slow creep into an overcurrent event. As shown, the switch clamps the current until it hits thermal shutdown, and then the device remains latched off until the LATCH pin is low.

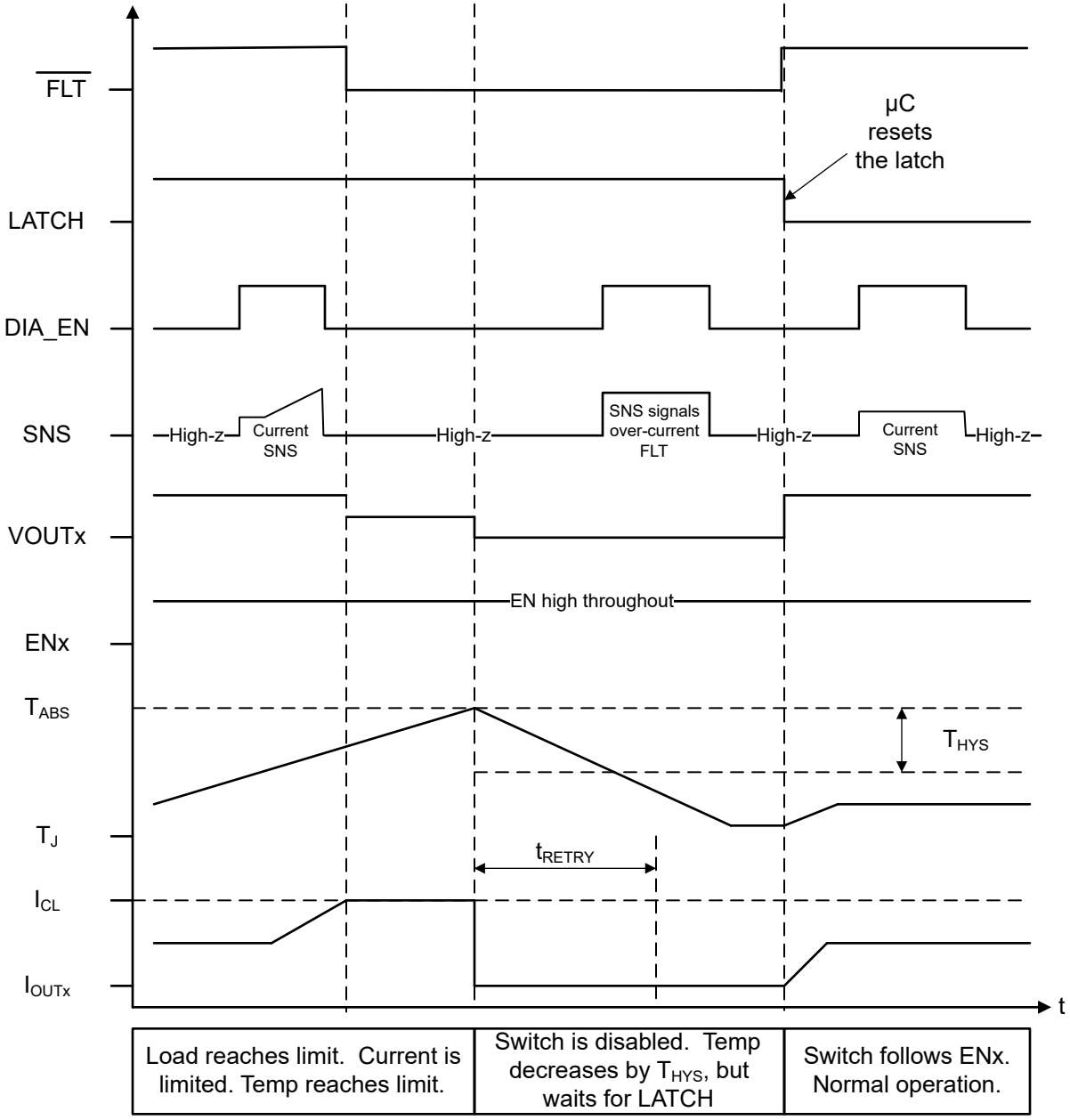


图 9-14. Current Limit – Latched Behavior

图 9-15 shows the behavior with LATCH tied to GND; hence, the switch retries after the fault is cleared and t_{RETRY} has expired.

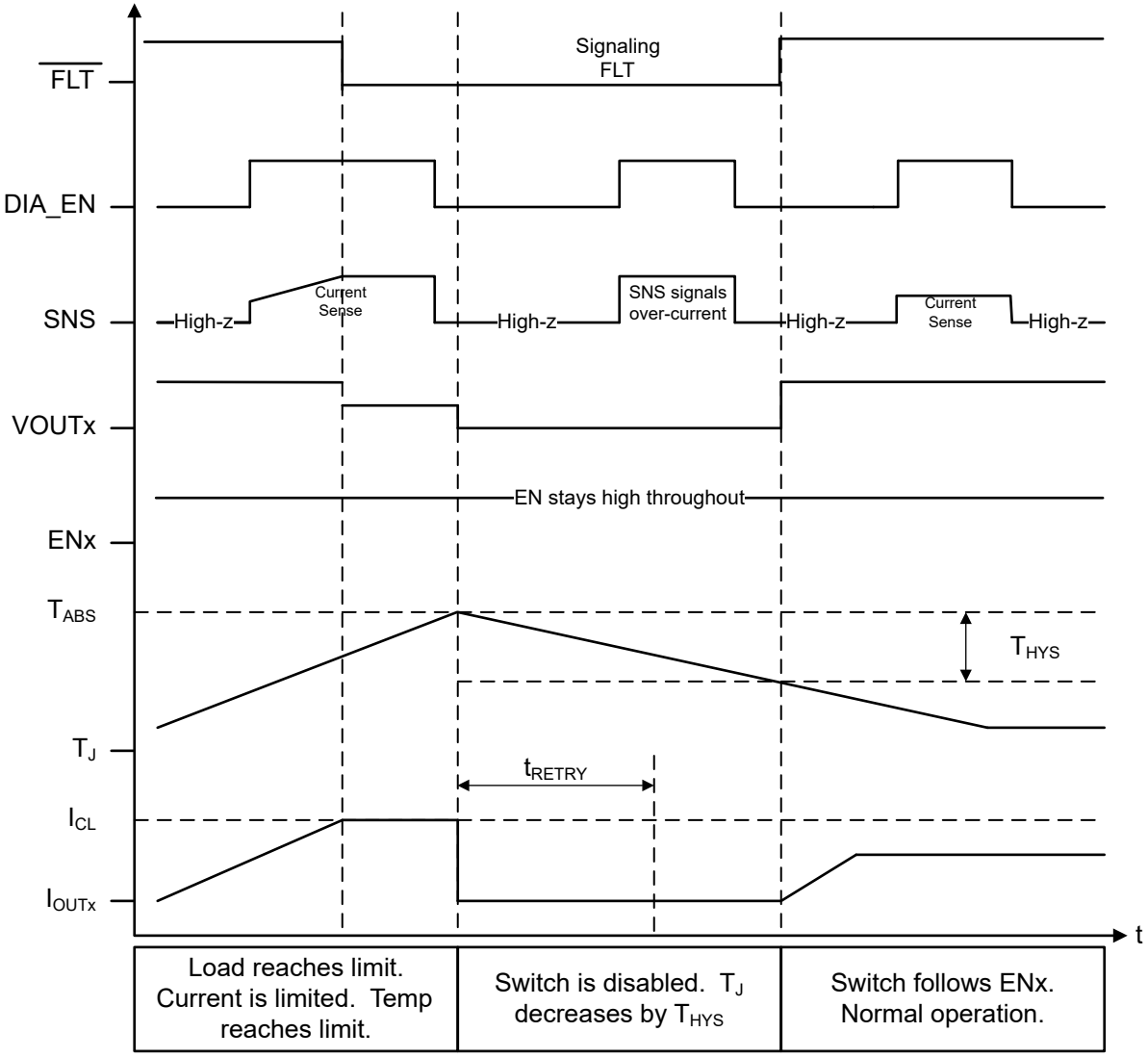


图 9-15. Current Limit – LATCH = 0

When the switch retries after a shutdown event, the fault indication remains until V_{OUTx} has risen to V_{VS} – 1.8 V. After V_{OUTx} has risen, the $\overline{FLT}$ output is reset and current sensing is available. If there is a short-to-ground and V_{OUT} is not able to rise, the SNS fault indication remains indefinitely. 图 9-16 illustrates auto-retry behavior and provides a zoomed-in view of the fault indication during retry.

备注

图 9-16 assumes that t_{RETRY} has expired by the time that T_J reaches the hysteresis threshold.

LATCH = LO and DIA_EN = HI

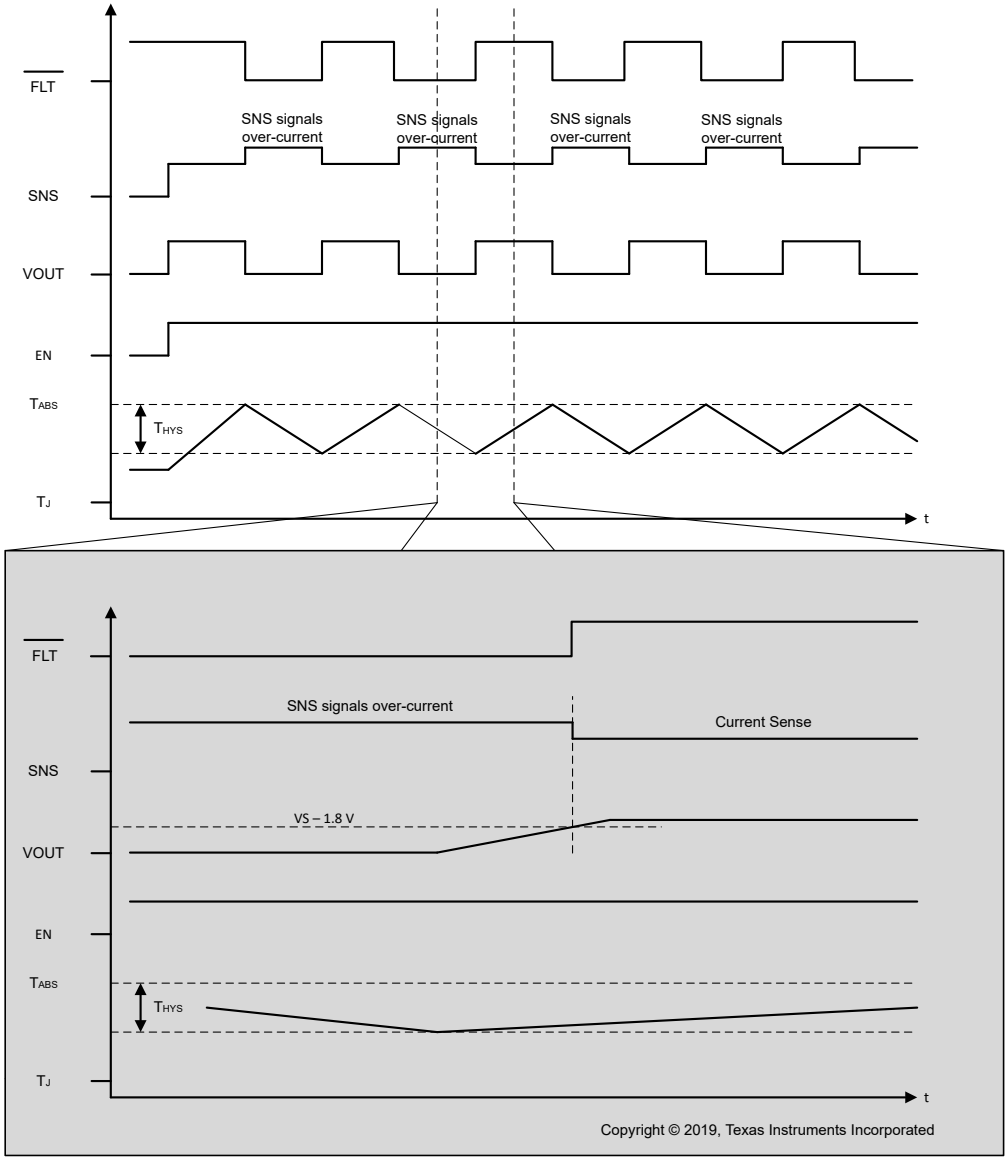


图 9-16. Fault Indication During Retry

9.3.4.3 Short-to-Supply or Open-Load Detection

The TPS272C45 is capable of detecting short-to-supply and open-load events regardless of whether the switch is turned on or off, however the two conditions use different methods to signify fault. This feature enables systems to recognize mis-wiring or wire-break events.

9.3.4.3.1 Detection With Switch Enabled

When the switch is enabled, the short-to-supply and open-load conditions are detected through the current sense feature. In both cases, the load current drops from the nominal value and instead be measured as close to zero. By measuring load current through the SNS pin, this state can be recognized.

9.3.4.3.2 Detection With Switch Disabled

While the switch is disabled and DIA_EN high, an internal comparator watches the condition of V_{OUT}. The TPS272C45 includes a nominally 150-kΩ pull-up resistor from OUT pin to VS pin in series with a switch controlled by the DIA_EN signal. So, if the load is disconnected (open load condition) or there is a short to supply the V_{OUT} voltage is pulled towards V_{VS}. In either of these events, the internal comparator measures V_{OUT} as higher than the open load threshold ($V_{OL,off}$) and a fault is indicated on the $\overline{FLT}$ pin (Version A) or $\overline{FLTx}$ pins (Version D) and on the SNS pin (only for versions A, B, C). No external component is required in most cases, however if there is a pull-down resistor to GND on V_{OUT}, an additional external pull-up resistor can be necessary to bias V_{OUT} appropriately.

Open load fault signaling on the SNS and the internal pull-up on OUT is enabled only if DIA_EN is set HI. To detect open-load threshold at higher pull-down load current, an external pull-up resistor (and potentially a switch) can be needed.

While the switch is disabled, the fault indication mechanisms continuously represent the present status. For example, if V_{OUT} decreases from greater than V_{OL_off} to less than V_{OL_off}, the fault indication is reset. Additionally, the fault indication is reset upon the falling edge of DIA_EN (for SNS pin) or the rising edge of EN.

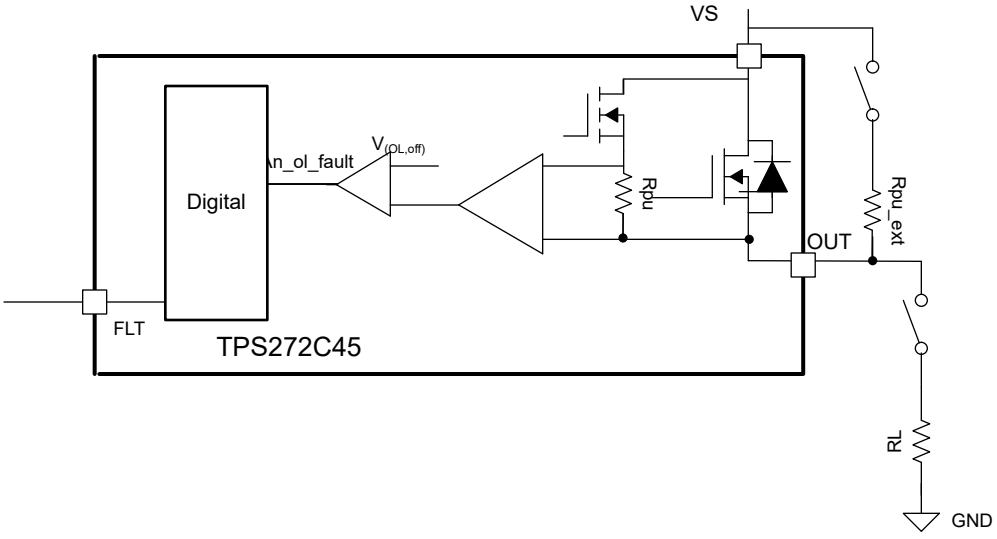


图 9-17. Open-Load Detection Circuit

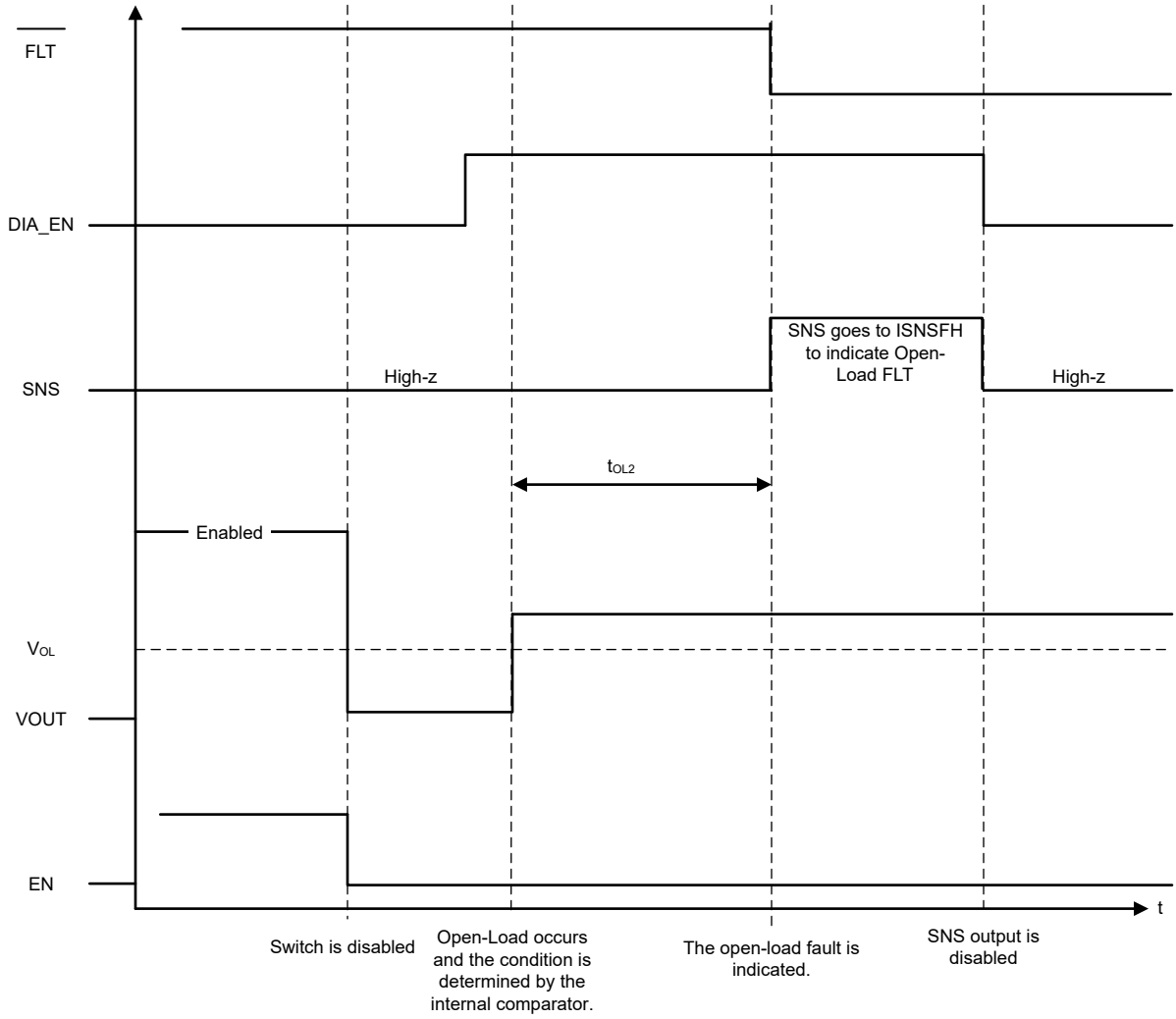


图 9-18. Open-Load Detection Timing

9.3.4.4 Current Sense Resistor Sharing

Multiple high-side devices can use the same R_{SNS} as shown in 图 9-19. This action reduces the total number of passive components in the system and the number of ADC terminals that are required of the microcontroller.

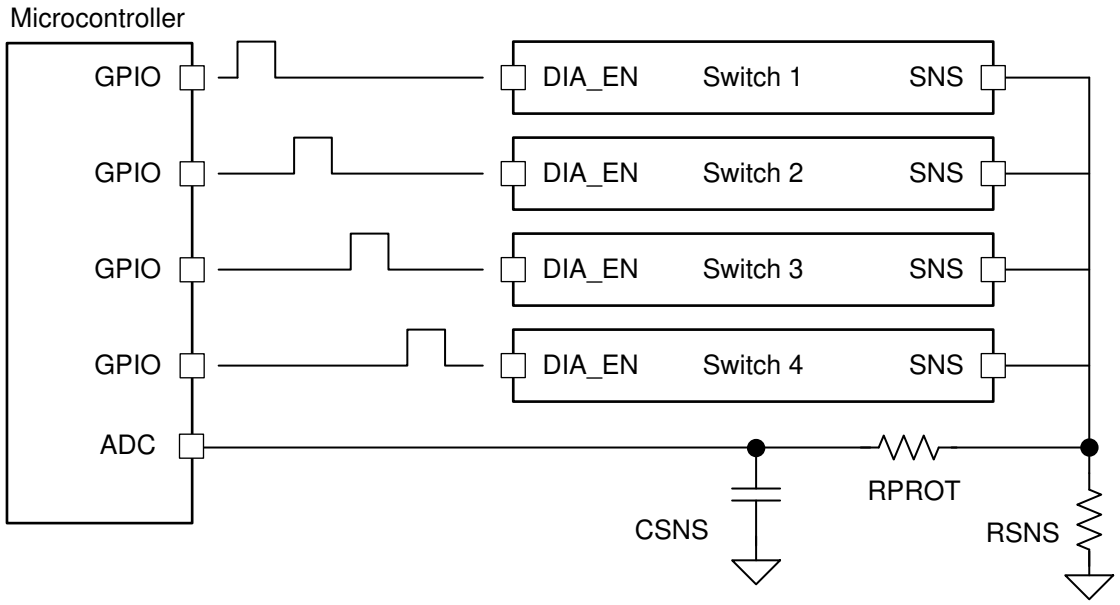


图 9-19. Sharing R_{SNS} Among Multiple Devices

9.4 Device Functional Modes

During typical operation, the TPS272C45 can operate in a number of states that are described below.

9.4.1 Off

OFF state occurs when the device is not powered.

9.4.2 Diagnostic

DIAGNOSTIC state occurs with DIA_EN is high but ENx are both low. The switch can be used to perform diagnostics like off-state open-load detection in this state.

9.4.3 Active

In ACTIVE state, the switch is enabled with ENx high. The diagnostic functions like current sense can be either on or off during ACTIVE state.

9.4.4 Fault

The FAULT state is entered if a fault shutdown occurs (thermal shutdown or current limit). After all faults are cleared, the LATCH pin is low, and the retry timer has expired, the device transitions out of FAULT state. If the EN pin is high, the switch re-enables. If the EN pin is low, the switch remains off.

10 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

图 10-1 shows the schematic of a typical application of the TPS272C45. The schematic includes all standard external components. This section of the data sheet discusses the considerations in implementing commonly required application functionality.

If reverse polarity can be applied to the VS supply voltage input, the ground network protection circuit must be added. The diode prevents the reverse current flow from the GND pin to supply. An additional resistor of 10 ohms or less is added to reduce the current flow if the VS to GND voltage rating is exceeded during any surge conditions. TI recommends the 1-K resistor in parallel to keep the GND potential close to the board GND under conditions where the ground network diode can be reverse biased.

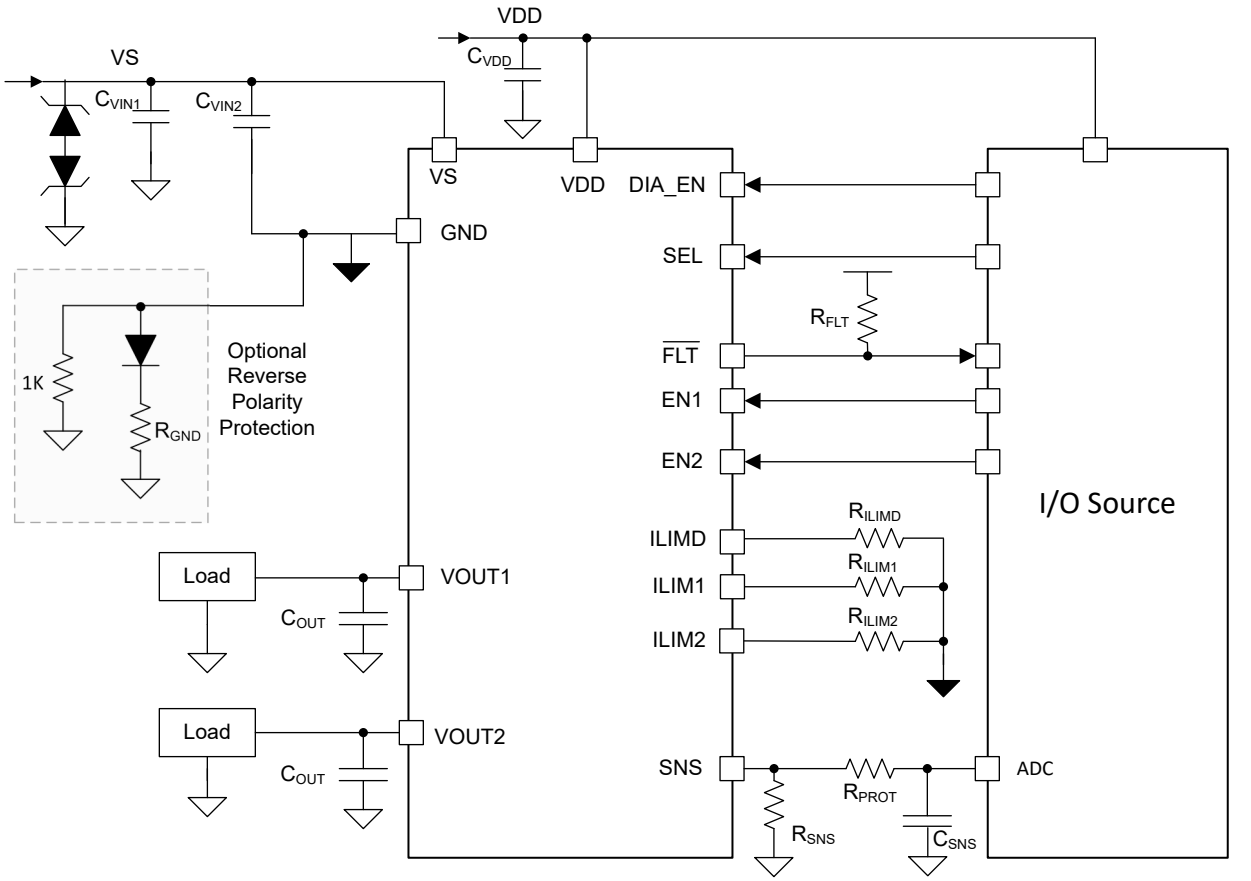


图 10-1. System Diagram

表 10-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{SNS}	1 kΩ	Translate the sense current into sense voltage.
R_{PROT}	10 kΩ	Low-pass RC filter resitance and protection for the ADC input.
C_{SNS}	100 pF	Low-pass filter capacitance for the ADC input.
R_{ILIMx}	5 kΩ to 40 kΩ	Set current limit threshold, connect from pin to IC GND.
C_{Vin1}	4.7 nF to Device GND	Filtering of voltage transients (for example, ESD, IEC 61000-4-5) and improved emissions.
C_{Vin2}	100 nF to Module GND	Stabilize the input supply and filter out low frequency noise.
C_{VDD}	2.2 uF to Module GND	Stabilize the input supply and limit supply excursions.
C_{OUT}	22 nF	Filtering of voltage transients (for example, ESD, RF transients)
Z_{TVS}	36-V TVS	Clamp surge voltages at the supply input.
D_{GND}, Z_{GND}	Diode + < 10 ohm from Device GND to Module GND	Optional for reverse polarity protection if needed.

10.1.1 IEC 61000-4-5 Surge

The TPS272C45 is designed to survive against IEC 61000-4-5 surge using external TVS clamps. The device is rated to 48 V ensuring that external TVS diodes can clamp below the rated maximum voltage of the TPS272C45. Above 48 V, the device includes V_{DS} clamps to help shunt current and ensure that the device survives the transient pulses. Depending on the class of the output, TI recommends that the system has a SMBJ36A or SMCJ36A between VS and module GND.

10.1.2 Inverse Current

Inverse current occurs when 0 V < V_{VS} < V_{OUT}. In this case, current can flow from VOUT to VS. Inverse current cannot be caused by a purely resistive load. However, a capacitive or inductive load can cause inverse current. For example, if there is a significant amount of load capacitance and the V_S node has a transient droop, V_{OUT} can be greater than V_S.

The TPS272C45 does not detect inverse current. When the switch is enabled, inverse current passes through the switch. When the switch is disabled, inverse current can pass through the MOSFET body diode. The device continues operating in the normal manner during an inverse current event.

10.1.3 Loss of GND

The ground connection can be lost either on the device level or on the module level. If the ground connection is lost, both the channel outputs are disabled irrespective of the EN input level. If the switch was already disabled when the ground connection was lost, the outputs remain disabled even when the channels are enabled. The steady state current from the output to the load that remains connected to the system ground is below the level specified in the *Specifications* section of this document. When the ground is reconnected, normal operation resumes.

10.1.4 Paralleling Channels

If an application requires lower power dissipation than is possible with a 45-mΩ switch, the TPS272C45 can have both channel outputs and ENx pins tied together to function as a single 22.5-mΩ high side switch. In this case, there is some decrease in I_{SNS} and I_{LIM} accuracy, however the device functions properly.

10.1.5 Thermal Information

When outputting current, the TPS272C45 heats up due to the power dissipation. The transient thermal impedance curve can be used to determine the device temperature during a pulse current of a given duration (time). This $Z_{\theta JA}$ value here corresponds to a JEDEC standard 2s2p thermal test PCB with no thermal vias.

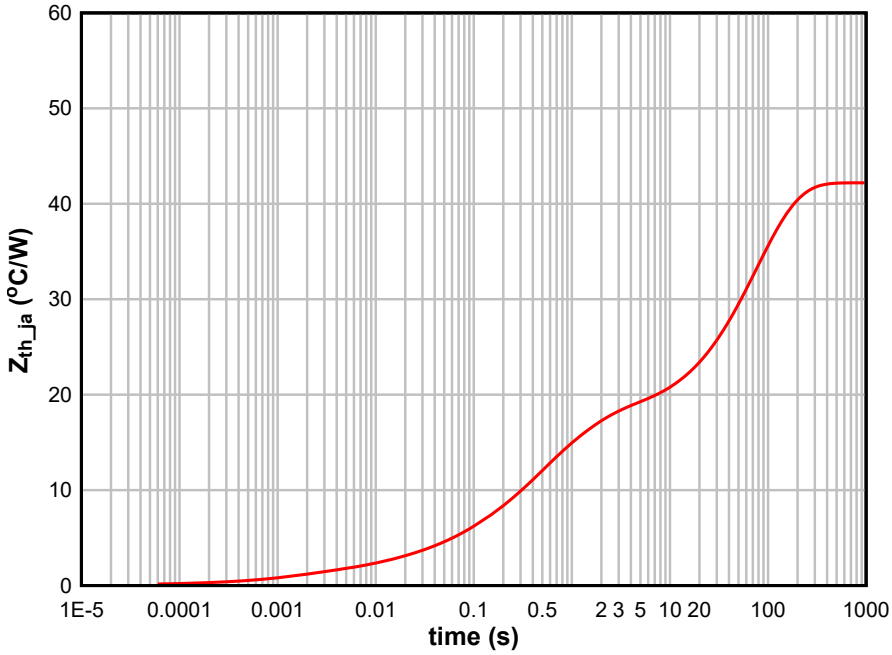


图 10-2. TPS272C45 Transient Thermal Impedance

10.2 Typical Application

This application example demonstrates how the TPS272C45 device can be used as output switches in a digital output module. In this example, consider an 8-channel module with a maximum output current capability of 2 A per channel.

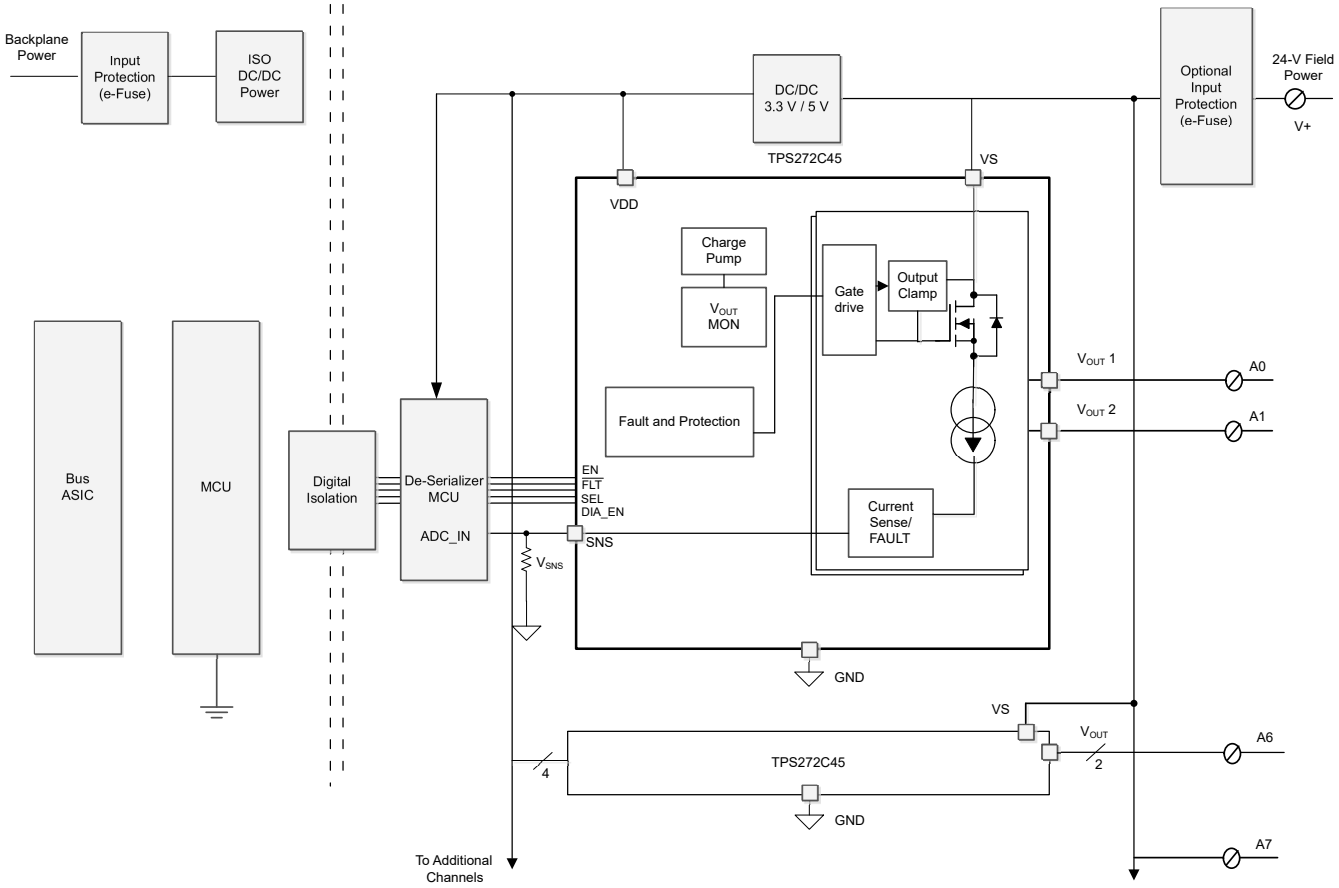


图 10-3. Block Diagram for PLC Digital Output Module

10.2.1 Design Requirements

For this design example, use the input parameters shown in 表 10-2.

表 10-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_S	24 V +/ – 20%
Load	2-A maximum DC
Load type	Resistive, Inductive, Capacitive
Load current sense	Maximum of 2.4 A
Regulation current limit (I_{LIM})	2.6-A typical
Ambient temperature	70°C
Device version	A

10.2.2 Detailed Design Procedure

10.2.2.1 R_{ILIM} Calculation

In this application, the TPS272C45 must allow for the maximum DC current with margin but minimize the energy in the switch and the load on the input supply during a fault condition by minimizing the current limit.

The nominal current limit must be set such that the worst case (lowest) current limit is higher than the maximum load current (2 A). Because the lower limit is 23% below the typical value, for this application, the best I_{LIM} set point is approximately 2.6 A for both channels. The below equation allows you to calculate the R_{ILIM} value that is placed from the I_{LIMx} pins to GND pin of the device. R_{ILIM} is calculated in kΩ.

$$R_{ILIM} = K_{CL} / I_{CL} \quad (3)$$

The K_{CL} value in the *Specifications* section is 20.5 A × kΩ. So the calculated value of R_{ILIM} closest 2% resistor is 7.87 kΩ.

10.2.2.2 Diagnostics

If the load is disconnected due a break in the connecting wire, an alert is desired. Open-load detection can be performed in the switch-enabled state with the current sense feature of the TPS272C45 device. Similarly in the off-state, a check for wire break can be performed. Under open load condition, with the DIA_EN set high, the current in the SNS pin is the fault current and the can be detected from the sense voltage measurement.

10.2.2.2.1 Selecting the R_{ISNS} Value

表 10-3 shows the requirements for the load current sense in this application. The K_{SNS} value is specified for the device and can be found in the *Specifications* section.

表 10-3. R_{SNS} Calculation Parameters

PARAMETER	EXAMPLE VALUE
Current sense ratio (K_{SNS})	1200
Largest diagnosable load current	2.4 A
Smallest diagnosable load current	50 mA
Full-scale ADC voltage	5 V
ADC resolution	10 bit

The load current measurement up to 2.4 A ensures that even in the event of a overcurrent but below the set current limit, the MCU can register and react by turning off the FET while the low level of 50 mA allows for accurate measurement of low load currents and enable the distinction open load faults from nominal load currents.

The R_{SNS} resistor value can be selected such that the largest diagnosable load current puts the SNS pin voltage (V_{SNS}) less than the ADC full-scale. With this design, any ADC value that shows full scale (FS) can be considered a fault. Additionally, the R_{SNS} resistor value must ensure that the smallest diagnosable load current does not cause V_{SNS} to fall below at a least a few LSB of the ADC. With the given example values, a 2.4-kΩ sense resistor satisfies both requirements shown in 表 10-4.

表 10-4. V_{SNS} Calculation

LOAD (A)	SENSE RATIO	I_{SNS} (mA)	R_{SNS} (Ω)	V_{SNS} (V)	% of 5-V ADC
2.4	1200	2.0	2400	4.8	96%
0.024	1200	0.02	2400	0.048	0.96% (9 LSB)

10.2.3 Application Curves

Upon enabling our device into a capacitive load, TPS272C45 defaults its current limit to 2x ICL for a period of time programmed set by ILIMD. In the figure below, you can see TPS272C45 charging a 1-mF capacitor using the inrush current handling feature. During the first 4 mS after enabling the device, IOUT1 is 2 times the icl programmed (4 A). After, the 4-mS period, the current folds back to the programmed icl (2 A).

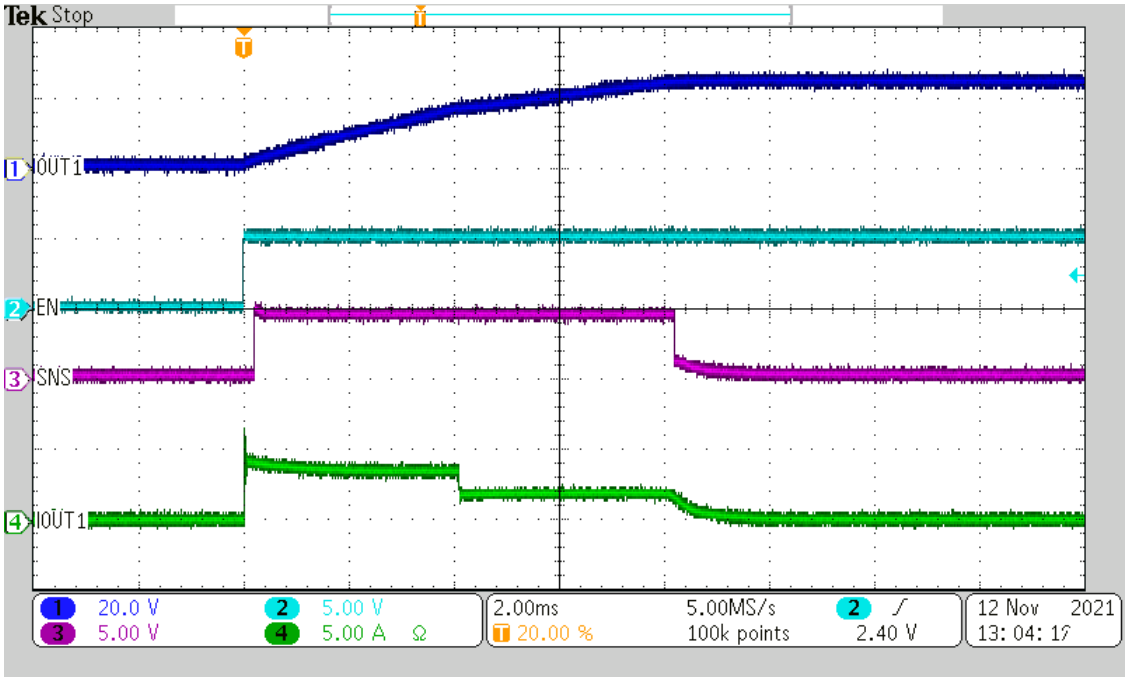


图 10-4. TPS272C45 Capacitor Charging

If the device has a no-load case due to an open load or wire-break, the device registers the fault even in an off-state if the DIA_EN pin is high. 图 10-5 shows the device behavior when an open load event is registered with EN low and DIAG_EN is raised. Systems can PWM DIA_EN to lower system power losses while still watching for open load events and the same timing applies.

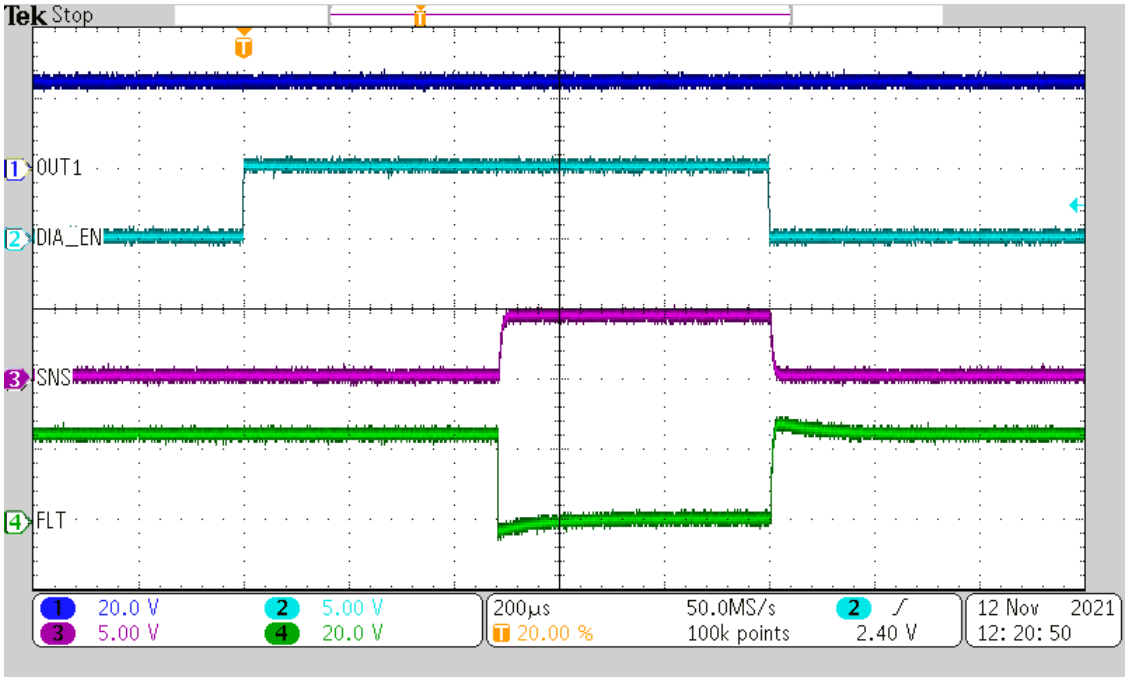


图 10-5. Open-Load (t_{OL}) Detection Time

If the output of the TPS272C45 is short-circuited, the device protects the system from failure. Depending on R_{ILIM}, the current limit set-point varies. The waveforms below show examples of the current limit behavior when the device is enabled into a short circuit.

In the Figure 10-6, the output is permanently shorted. Upon enabling the device, the current reaches the 2 times current limit is enabled for 6 mS set by ILIMD resistor. After the inrush current period, the current is reduced to the programmed current limit set by R_{ILIM}. In this case, because the power dissipation is low enough, the device is able to constantly act as a current source.

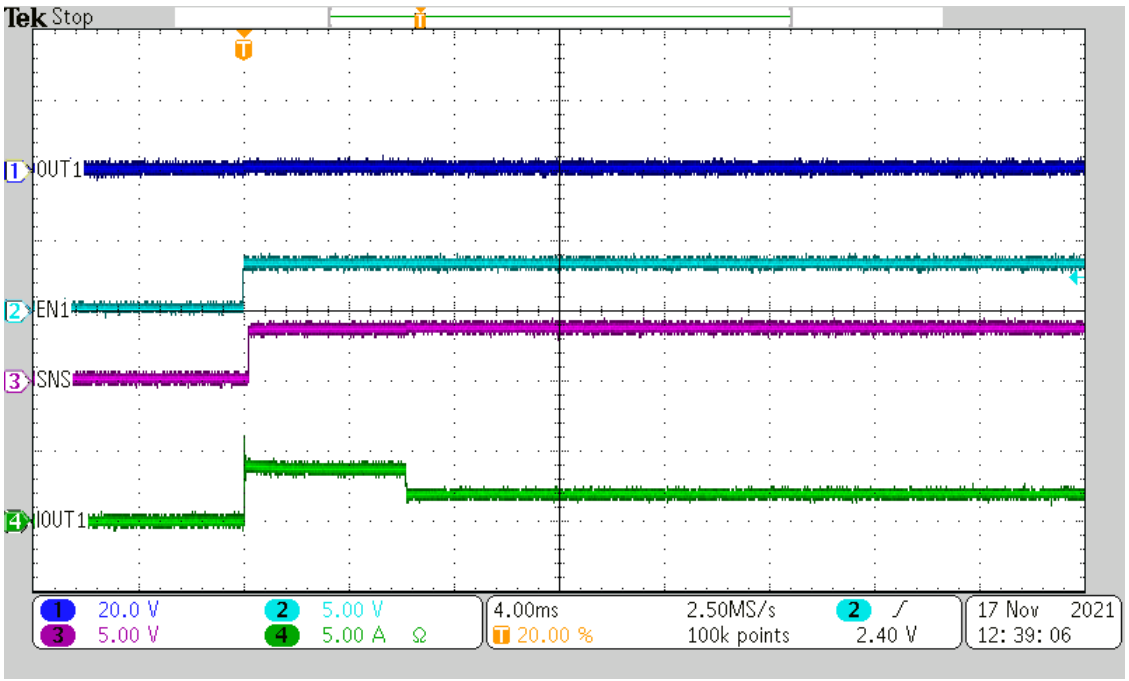


图 10-6. Enabling into Short (R_{ILIM} = 10 k , V_S = 6 V, Delay = 6 mS)

In Figure 10-7, the output is also permanently shorted. Upon enabling the device, the current reaches the 2 times current limit, however because the power dissipation is greater due to the higher input voltage at Vs the device reaches its thermal shutdown threshold and disables itself before reaching the programmed delay time.

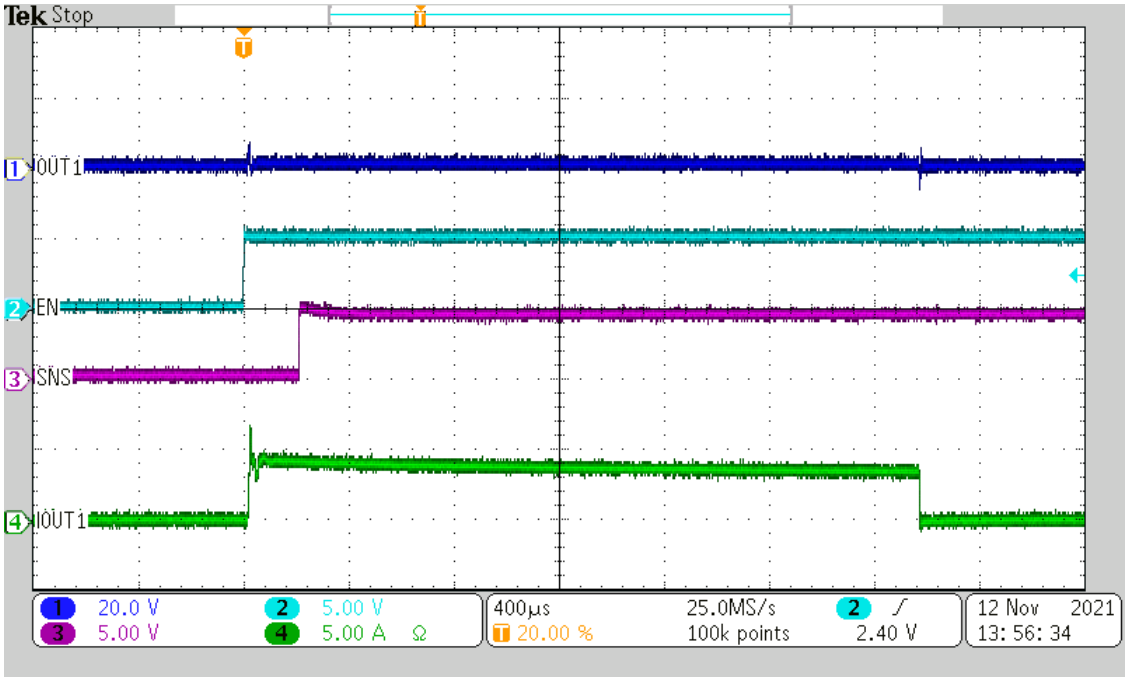


图 10-7. Enabling into Short (R_{ILIM} = 10 k , V_S = 24 V, Delay = 6 mS)

The Figure 10-8 shows that after the device has been enabled into a short and due to the high power dissipation, the device reaches its thermal shutdown threshold. The device then shuts down the FET for a period of tRETRY and re-enables the FET into the short. The capture shows the continuous retry cycle and protection because the short is permanently applied.

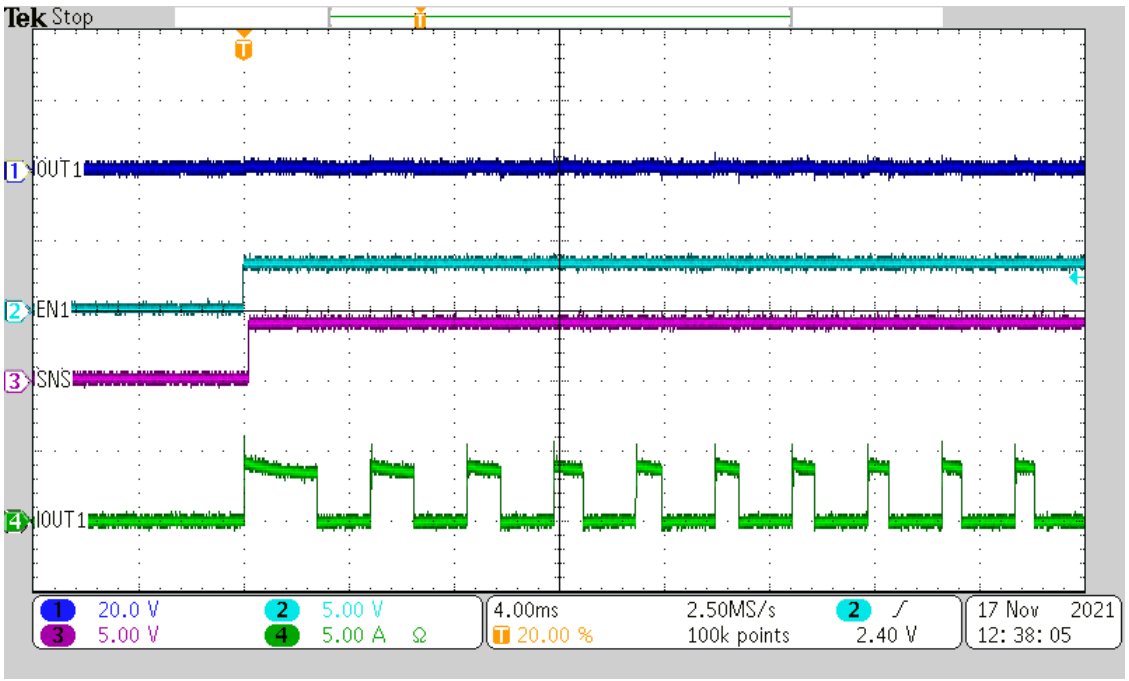


图 10-8. Permanent Short Behavior (R_{ILIM} = 10 k , V_S = 24 V, Delay = 6 mS)

In the event a short is applied to the output while a load is being driven, the device activates its fast trip comparator and shutdown the output to limit the inrush current. The device then immediately re-enables into the short and limit the current to the programmed current limit value. The figure below describes the described behavior.

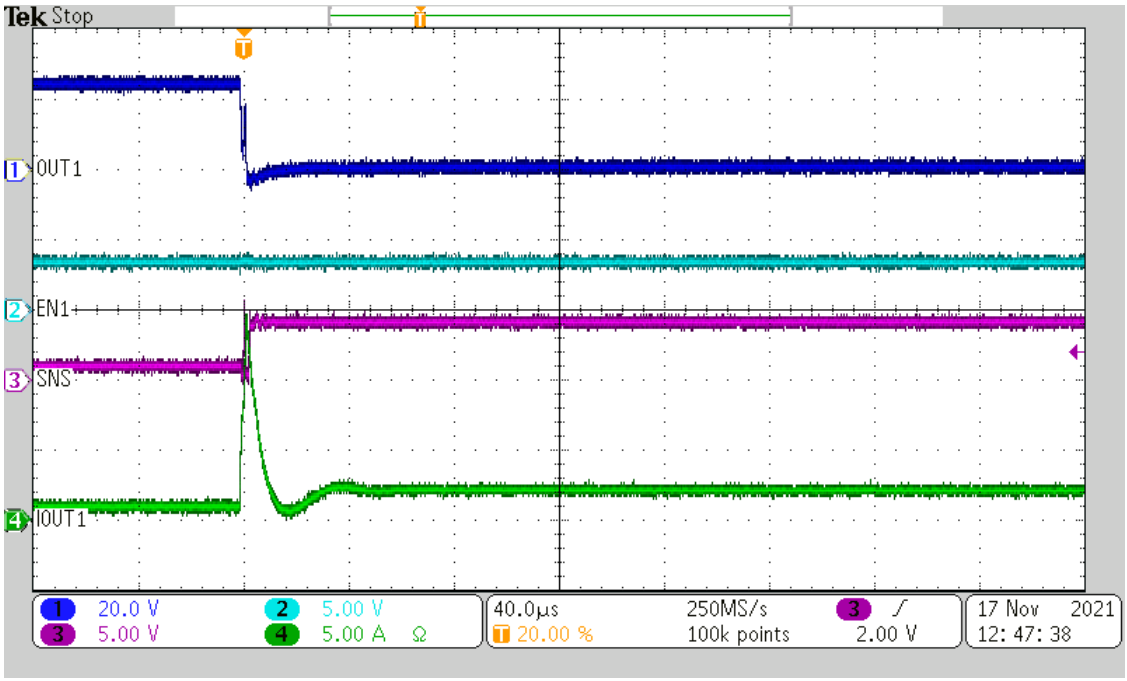


图 10-9. On-State Short circuit (R_{ILIM} = 10 k , V_S = 24 V)

11 Power Supply Recommendations

The TPS272C45 device is designed to operate in a 24-V industrial system. The allowed supply voltage range (VS pin) is 6 V to 36 V as measured at the VSpin with respect to the GND pin of the device. In this range the device meets full parametric specifications as listed in the *Electrical Characteristics* table. The maximum continuous operating voltage is 36 V. The device is also designed to withstand voltage transients beyond this range. The device version A requires an external power supply input in the range 3.0 V to 5.5 V. The C and D versions of the device have an secondary internal regulator (nominally 3.3 V) but an external supply can be optionally provided at the VDD pin to lower the power dissipation in the IC. Version B always use an internal 3.3V regulator, so a single 24V supply (VS pin) is sufficient.

表 11-1. Operating Voltage Range

Supply voltage pin	Input Supply Voltage Range	Note
VS	6 V to 36 V	Nominal supply voltage, all parametric specifications apply. The device is completely short-circuit protected up to 125°C.
VDD	3.0 to 5.5 V	Required for version A, and optional for versions C and D. A DC/DC converter supply reduces the overall power dissipation.

12 Layout

12.1 Layout Guidelines

To achieve optimal thermal performance, connect the exposed pad to a large copper pour. On the top PCB layer, the pour can extend beyond the package dimensions as shown in the example below. In addition to this, TI recommends to also have a GND plane either on one of the internal PCB layers or on the bottom layer.

Vias must connect this plane to the top GND pour.

Ensure that all external components are placed close to the pins. Device current limiting performance can be harmed if the R_{ILIM} is far from the pins and extra parasitics are introduced.

12.2 Layout Example

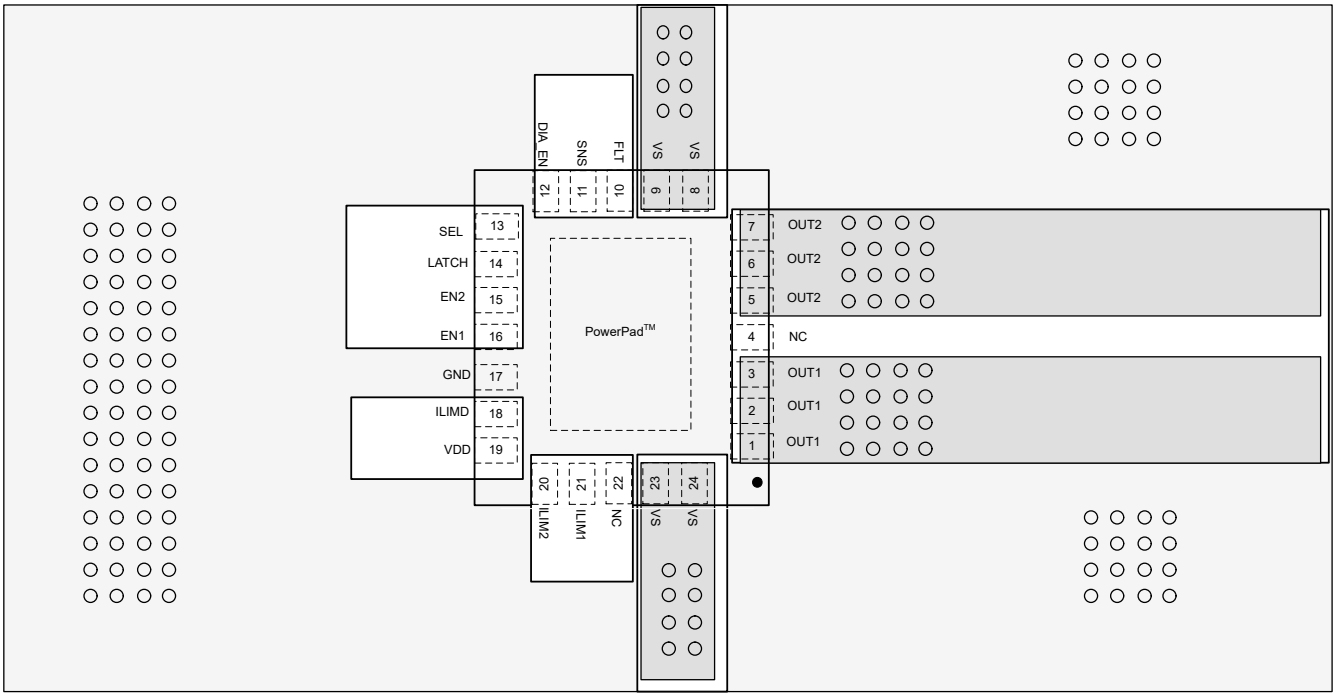


图 12-1. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

- Texas Instruments, *Adjustable Current Limit of Smart Power Switches* application report
- Texas Instruments, *How to Drive Inductive, Capacitive, and Lighting Loads With Smart High-Side Switches* application report

13.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS272C45ARHFR	ACTIVE	VQFN	RHF	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 272C45A	Samples
TPS272C45BRHFR	ACTIVE	VQFN	RHF	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 272C45B	Samples
TPS272C45CRHFR	ACTIVE	VQFN	RHF	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 272C45C	Samples
TPS272C45DRHFR	ACTIVE	VQFN	RHF	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 272C45D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

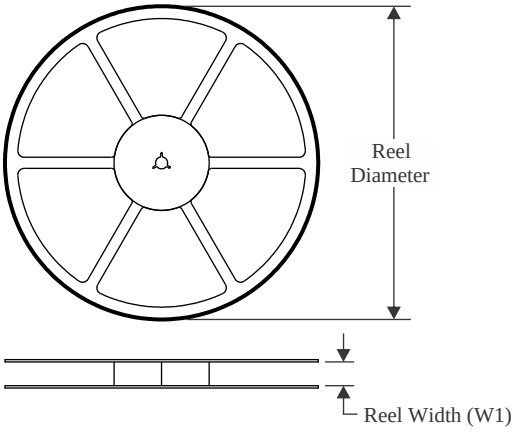
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

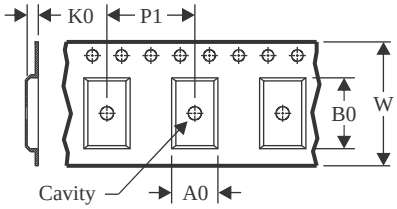
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

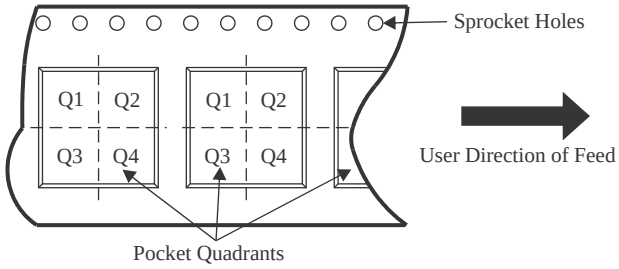


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

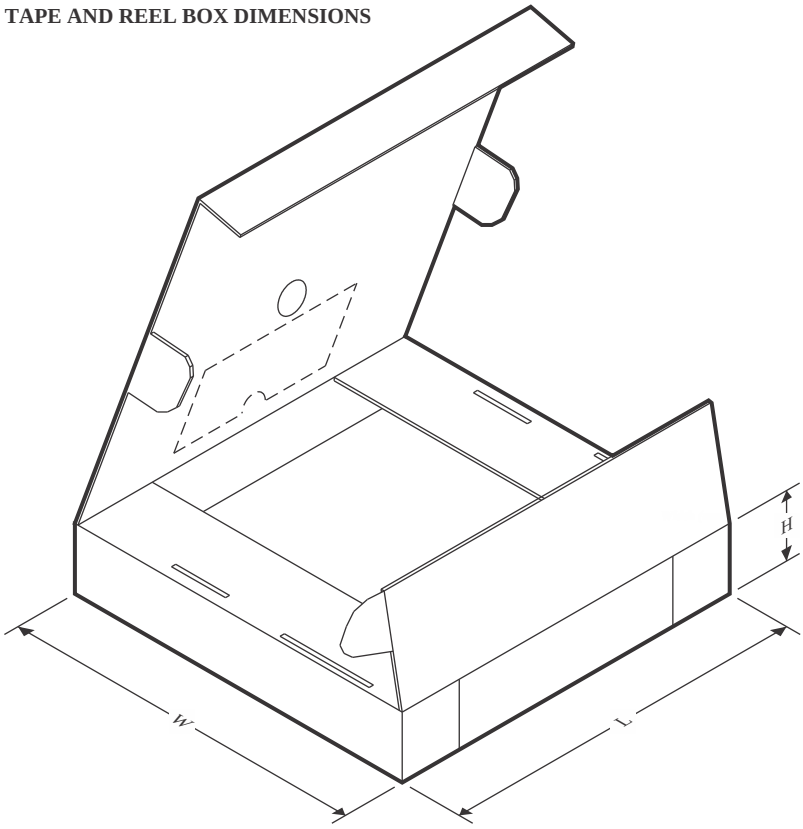
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS272C45ARHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS272C45BRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS272C45CRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS272C45DRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

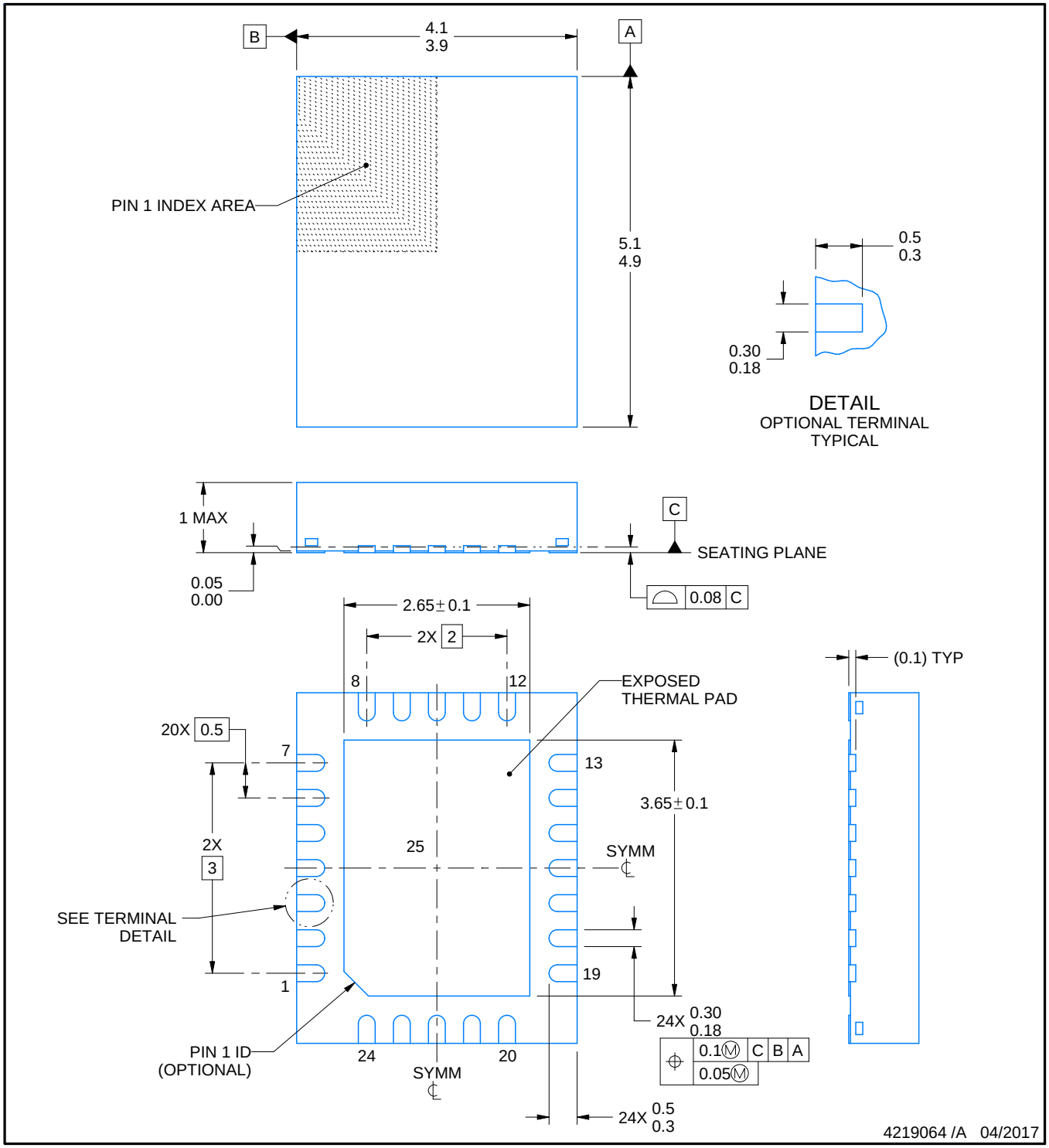
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS272C45ARHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
TPS272C45BRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
TPS272C45CRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
TPS272C45DRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

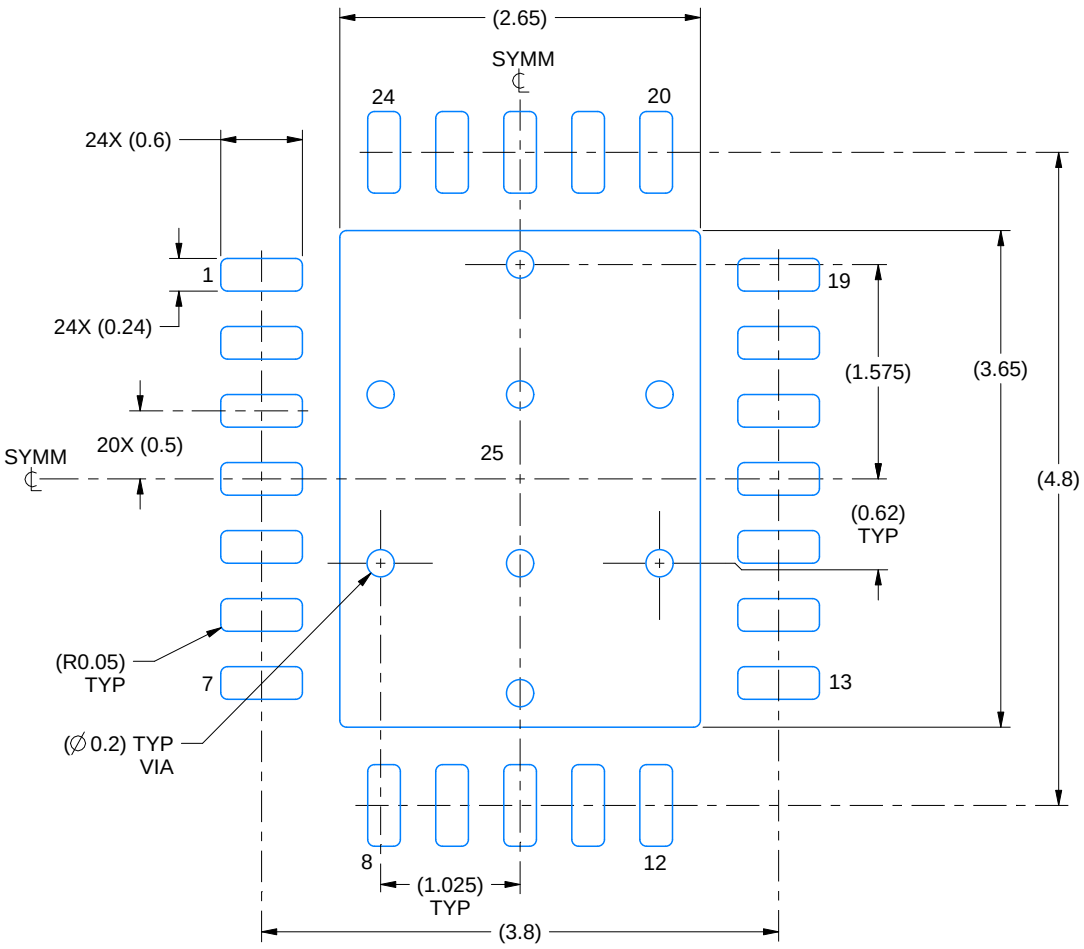
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

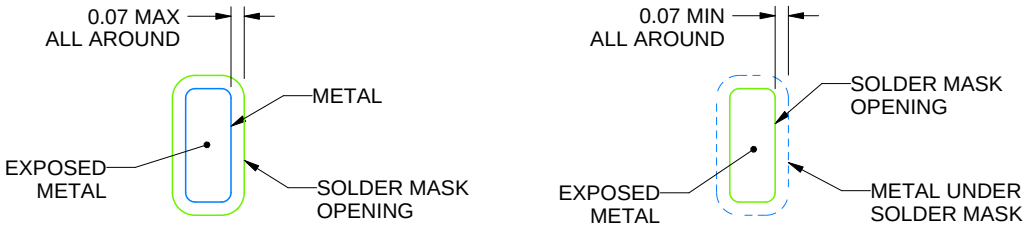
RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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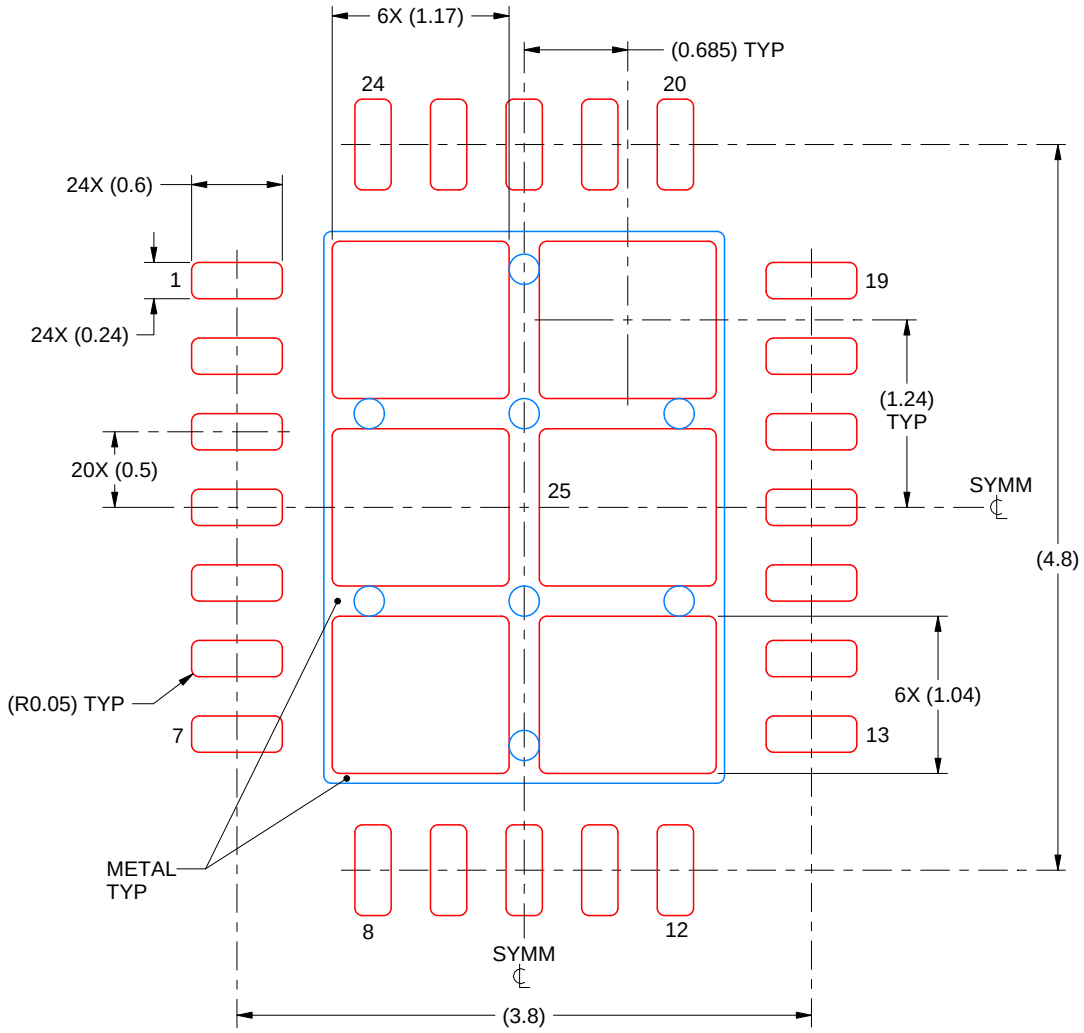
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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