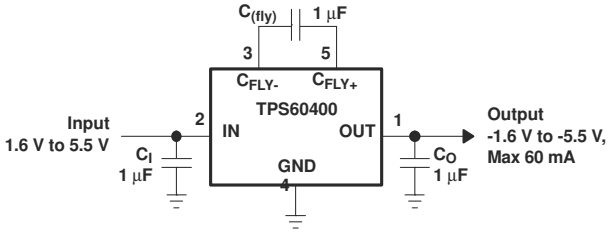
TPS6040x 非稳压 60mA 电荷泵电压逆变器

1 特性

- 反相输入电源电压
- 输出电流高达 60mA
- 只需要三个小型 1μF 陶瓷电容器
- 输入电压范围：1.6V 至 5.5V
- 用于改进低输出电流时效率的省电模式 (TPS60400)
- 器件静态电流典型值：65μA
- 用于启动至负载的集成式主动式肖特基二极管
- 小型 5 引脚 SOT-23 封装
- 提供评估模块 TPS60400EVM-178

2 应用

- LCD 偏置
- 射频功率放大器的 GaAs 偏置
- 便携式仪表中的传感器电源
- 双极放大器电源
- 医疗仪器
- 由电池供电的设备



典型应用

3 说明

TPS6040x 系列器件可在输入电压范围为 1.6V 至 5.5V 的情况下生成非稳压负输出电压。这些器件通常采用 5V 或 3.3V 的预稳压电源轨供电。由于输入电压范围很宽，两三节镍镉电池、镍氢电池或碱性电池，或者一节锂离子电池即可为其供电。

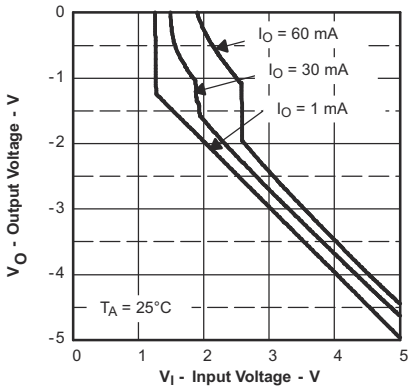
只需要三个 1μF 外部电容器就可以构建完整的直流/直流电荷泵逆变器。整个逆变器采用 5 引脚 SOT23 封装，可以构建在 50mm{1}2{2} 的电路板面积上。通过用集成电路取代启动至负载通常所需的肖特基二极管，可以进一步减小电路板面积并减少组件数。

TPS6040x 可以提供最大值为 60mA 的输出电流，在较宽输出电流范围内实现超过 90% 的典型转换效率。提供三个器件选项，分别为 20kHz、50kHz 和 250kHz 固定频率运行。TPS60400 具有可变的开关频率，可降低宽负载范围应用中的工作电流，并实现采用低值电容器的设计。

器件信息

器件型号	封装 (1)	封装尺寸（标称值）
TPS6040x	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



输出电压与输入电压间的关系

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (April 2015) to Revision C (October 2020)	Page
• 更新了整个文档的表、图和交叉参考的编号格式。	1

Changes from Revision A (November 2004) to Revision B (April 2015)	Page
• 添加了*处理额定值*表、*特性说明*部分、*器件功能模式*、*应用和实现*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分	1

5 Device Comparison Table

PART NUMBER(1)	MARKING DBV PACKAGE	TYPICAL FLYING CAPACITOR [µF]	FEATURE
TPS60400DBV	PFKI	1	Variable switching frequency 50 kHz-250 kHz
TPS60401DBV	PFLI	10	Fixed frequency 20 kHz
TPS60402DBV	PFMI	3.3	Fixed frequency 50 kHz
TPS60403DBV	PFNI	1	Fixed frequency 250 kHz

(1) The DBV package is available taped and reeled. Add R suffix to device type (for example, TPS60400DBVR) to order quantities of 3000 devices per reel. Add T suffix to device type (for example, TPS60400DBVT) to order quantities of 250 devices per reel.

6 Pin Configuration and Functions

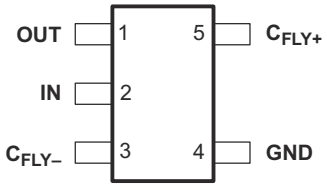


图 6-1. DBV Package 5 Pins Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C_{FLY+}	5		Positive terminal of the flying capacitor $C_{(fly)}$
C_{FLY-}	3		Negative terminal of the flying capacitor $C_{(fly)}$
GND	4		Ground
IN	2	I	Supply input. Connect to an input supply in the 1.6-V to 5.5-V range. Bypass IN to GND with a capacitor that has the same value as the flying capacitor.
OUT	1	O	Power output with $V_O = -V_I$ Bypass OUT to GND with the output filter capacitor C_O.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range	IN to GND	-0.3	5.5	V
	OUT to GND	-5.5	0.3	V
	C_{FLY-} to GND	0.3	V_O - 0.3	V
	C_{FLY+} to GND	-0.3 V	V_I + 0.3	V
Continuous power dissipation		See 节 9.2.1.2.5		
Continuous output current			80	mA
Maximum junction temperature, T_J			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-55°C	150°C	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	-1000	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	-500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Input voltage range, V_I	1.8		5.25	V
Output current range at OUT, I_O			60	mA
Input capacitor, C_I	0	$C_{(fly)}$		µF
Flying capacitor, $C_{(fly)}$		1		µF
Output capacitor, C_O		1	100	µF
Operating junction temperature, T_J	-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6040x DBV 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	221.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	
ψ_{JT}	Junction-to-top characterization parameter	3.3	
ψ_{JB}	Junction-to-board characterization parameter	38.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

$C_I = C_{(fly)} = C_O$ (according to Table 1), T_C = -40°C to 85°C, V_I = 5 V over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Supply voltage range		At T_C = -40°C to 85°C, R_L = 5 kΩ		1.8		5.25	V
			At $T_C \geq$ 0°C, R_L= 5 kΩ		1.6			
I_O	Maximum output current at V_O				60			mA
V_O	Output voltage					-V_I		V
V_{P-P}	Output voltage ripple	TPS60400	I_O = 5 mA	$C_{(fly)}$ = 1 µF, C_O = 2.2 µF		35		mV_{P-P}
		TPS60401		$C_{(fly)} = C_O$ = 10 µF		20		
		TPS60402		$C_{(fly)} = C_O$ = 3.3 µF		20		
		TPS60403		$C_{(fly)} = C_O$ = 1 µF		15		
I_Q	Quiescent current (no-load input current)	TPS60400	At V_I = 5 V			125	270	µA
		TPS60401				65	190	
		TPS60402				120	270	
		TPS60403				425	700	
		TPS60400	At T ≤ 60°C, V_I = 5 V				210	µA
		TPS60401					135	
		TPS60402					210	
		TPS60403					640	
f_{OSC}	Internal switching frequency	TPS60400	VCO version		30	50-250	350	kHz
		TPS60401			13	20	28	
		TPS60402			30	50	70	
		TPS60403			150	250	300	
	Impedance at 25°C, V_I = 5 V	TPS60400	$C_I = C_{(fly)} = C_O$ = 1 µF			12	15	Ω
		TPS60401	$C_I = C_{(fly)} = C_O$ = 10 µF			12	15	
		TPS60402	$C_I = C_{(fly)} = C_O$ = 3.3 µF			12	15	
		TPS60403	$C_I = C_{(fly)} = C_O$ = 1 µF			12	15	

7.6 Typical Characteristics

表 7-1. Table of Graphs

			FIGURE
η	Efficiency	vs Output current at 3.3 V, 5 V TPS60400, TPS60401, TPS60402, TPS60403	图 7-1, 图 7-2
I_I	Input current	vs Output current TPS60400, TPS60401, TPS60402, TPS60403	图 7-3, 图 7-4
I_S	Supply current	vs Input voltage TPS60400, TPS60401, TPS60402, TPS60403	图 7-5, 图 7-6
	Output resistance	vs Input voltage at -40°C, 0°C, 25°C, 85°C TPS60400, $C_I = C_{(fly)} = C_O$ = 1 µF TPS60401, $C_I = C_{(fly)} = C_O$ = 10 µF TPS60402 , $C_I = C_{(fly)} = C_O$ = 3.3 µF TPS60403, $C_I = C_{(fly)} = C_O$ = 1 µF	图 7-7, 图 7-8, 图 7-9, 图 7-10
V_O	Output voltage	vs Output current at 25°C, V_{IN}=1.8 V, 2.5 V, 3.3 V, 5 V TPS60400, $C_I = C_{(fly)} = C_O$ = 1 µF TPS60401, $C_I = C_{(fly)} = C_O$ = 10 µF TPS60402 , $C_I = C_{(fly)} = C_O$ = 3.3 µF TPS60403, $C_I = C_{(fly)} = C_O$ = 1 µF	图 7-11, 图 7-12, 图 7-13, 图 7-14

表 7-1. Table of Graphs (continued)

			FIGURE
f_{OSC}	Oscillator frequency	vs Temperature at V_I = 1.8 V, 2.5 V, 3.3 V, 5 V TPS60400, TPS60401, TPS60402, TPS60403	图 7-15, 图 7-16, 图 7-17, 图 7-18
f_{OSC}	Oscillator frequency	vs Output current TPS60400 at 2 V, 3.3 V, 5.0 V	图 7-19

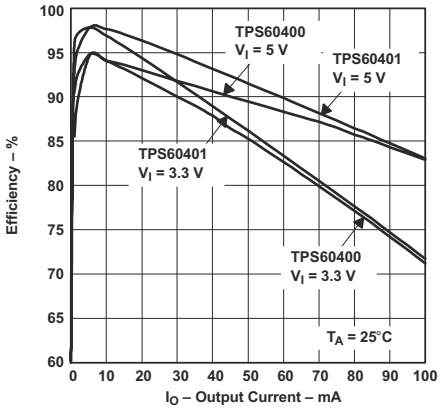


图 7-1. Efficiency vs Output Current

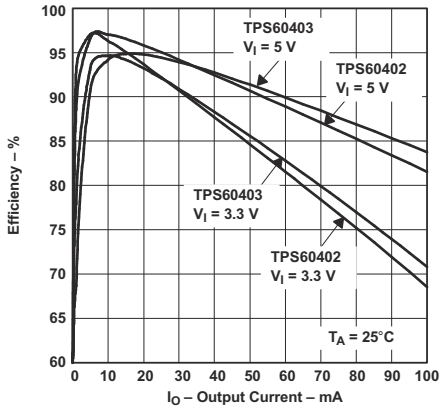


图 7-2. Efficiency vs Output Current

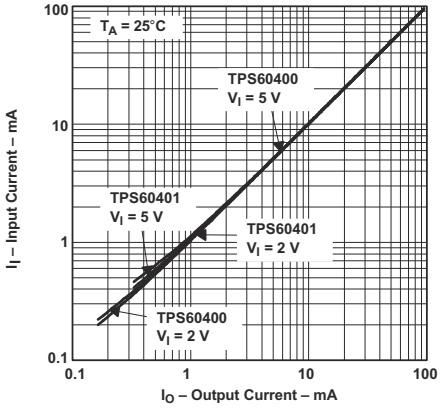


图 7-3. Input Current vs Output Current

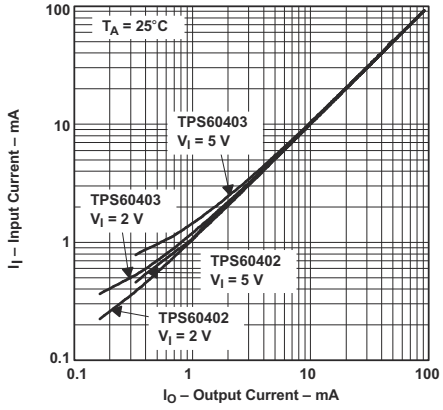


图 7-4. Input Current vs Output Current

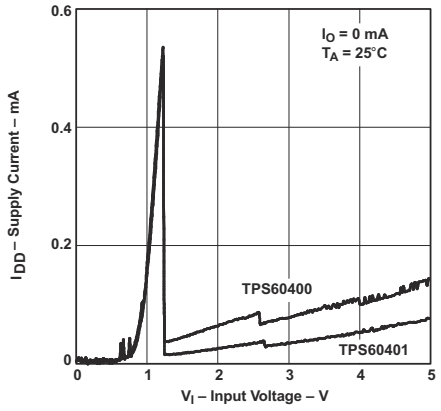


图 7-5. Supply Current vs Input Voltage

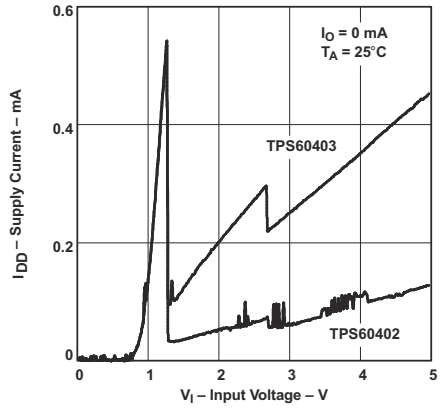


图 7-6. Supply Current vs Input Voltage

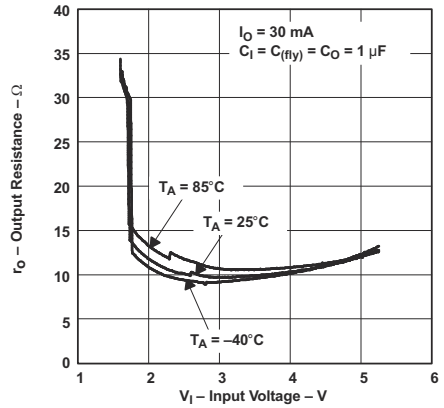


图 7-7. Output Resistance vs Input Voltage

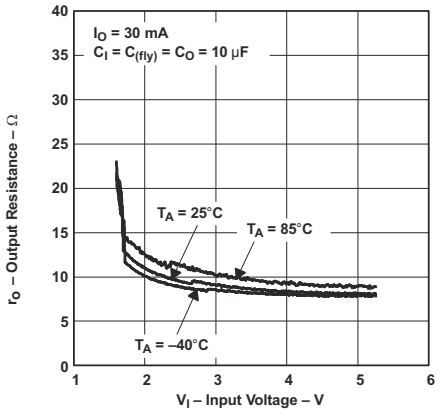


图 7-8. Output Resistance vs Input Voltage

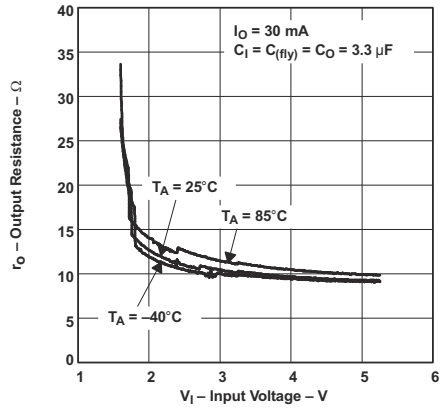


图 7-9. Output Resistance vs Input Voltage

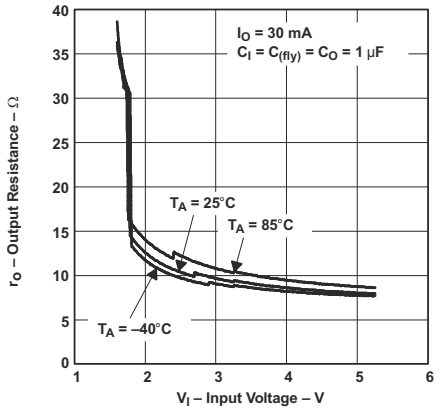


图 7-10. Output Resistance vs Input Voltage

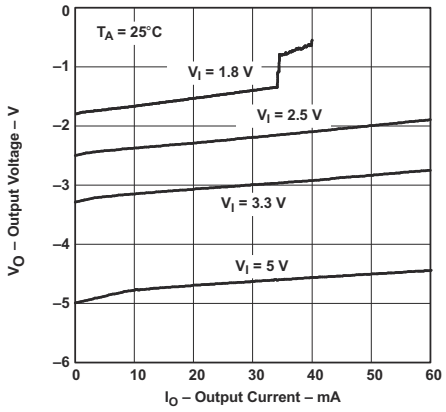


图 7-11. Output Voltage vs Output Current

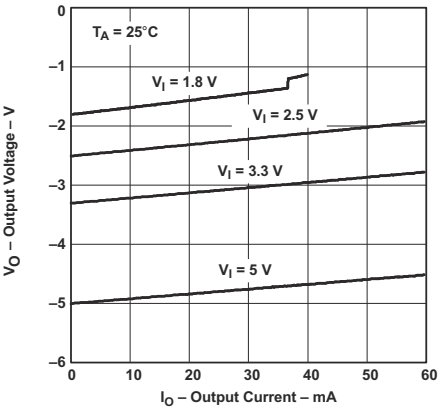


图 7-12. Output Voltage vs Output Current

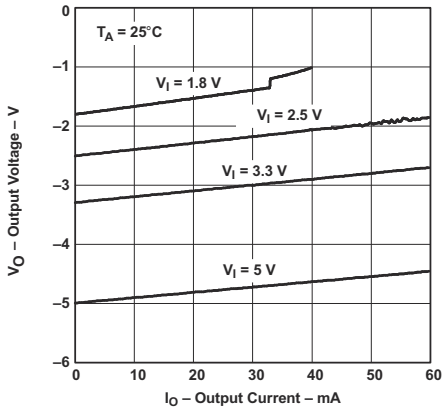


图 7-13. Output Voltage vs Output Current

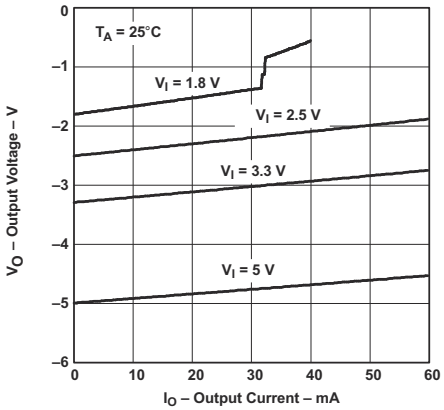


图 7-14. Output Voltage vs Output Current

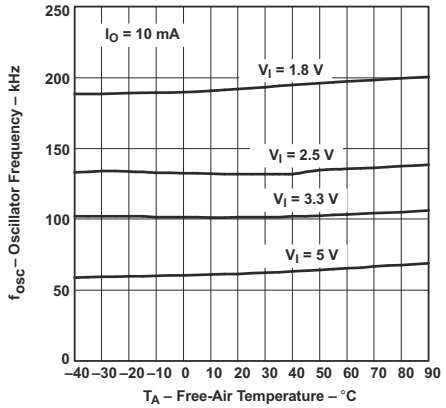


图 7-15. Oscillator Frequency vs Free-Air Temperature

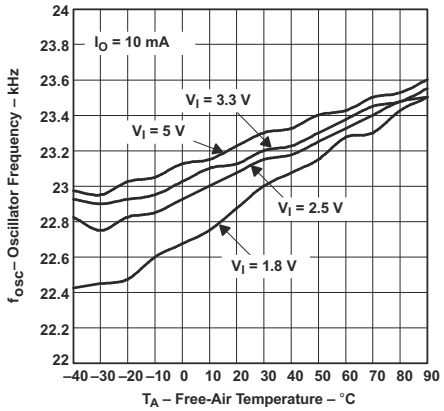


图 7-16. Oscillator Frequency vs Free-Air Temperature

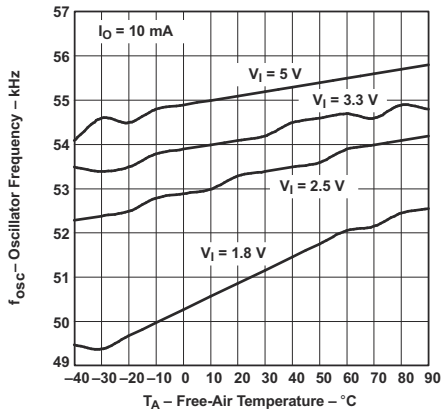


图 7-17. Oscillator Frequency vs Free-Air Temperature

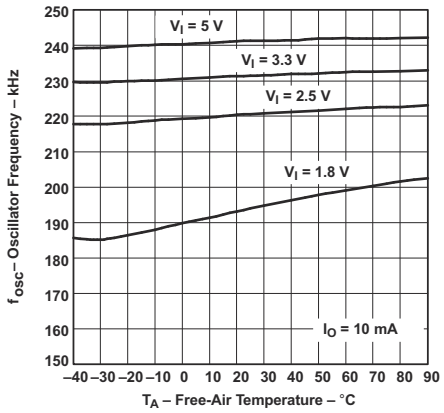


图 7-18. Oscillator Frequency vs Free-Air Temperature

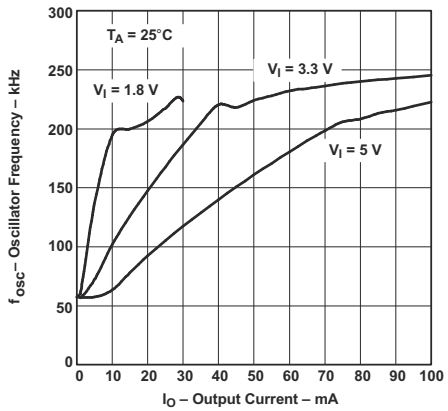


图 7-19. Oscillator Frequency vs Output Current

8 Detailed Description

8.1 Overview

The TPS60400, TPS60401 charge pumps invert the voltage applied to their input. For the highest performance, use low equivalent series resistance (ESR) capacitors (for example, ceramic). During the first half-cycle, switches S2 and S4 open, switches S1 and S3 close, and capacitor ($C_{(fly)}$) charges to the voltage at V_I. During the second half-cycle, S1 and S3 open, S2 and S4 close. This connects the positive terminal of $C_{(fly)}$ to GND and the negative to V_O. By connecting $C_{(fly)}$ in parallel, C_O is charged negative. The actual voltage at the output is more positive than $-V_I$, since switches S1-S4 have resistance and the load drains charge from C_O.

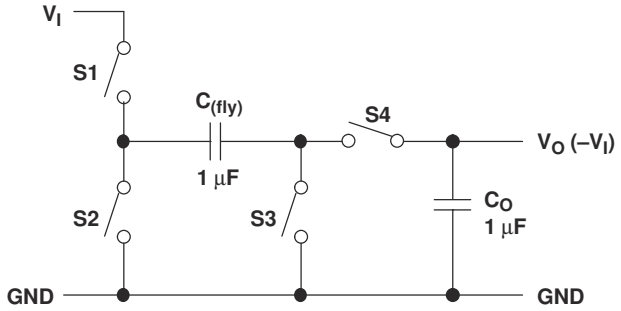
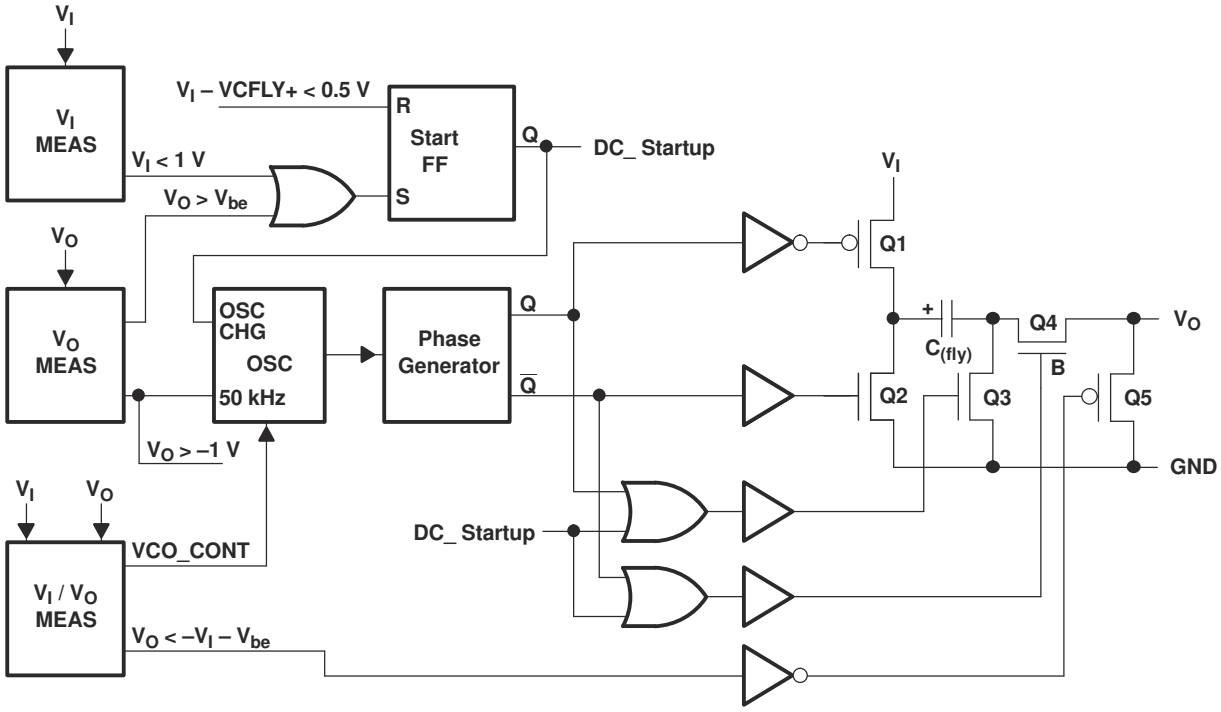


图 8-1. Operating Principle

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Charge-Pump Output Resistance

The TPS6040x devices are not voltage regulators. The charge pump's output source resistance is approximately 15 Ω at room temperature (with V_I = 5 V), and V_O approaches -5 V when lightly loaded. V_O droops toward GND as load current increases.

$$V_O = -(V_I - R_O \times I_O) \tag{1}$$

$$R_O \approx \frac{1}{f_{OSC} \times C_{(fly)}} + 4\left(2R_{SWITCH} + ESR_{CFLY}\right) + ESR_{CO} \tag{2}$$

R_O = output resistance of the converter

8.3.2 Efficiency Considerations

The power efficiency of a switched-capacitor voltage converter is affected by three factors: the internal losses in the converter IC, the resistive losses of the capacitors, and the conversion losses during charge transfer between the capacitors. The internal losses are associated with the internal functions of the IC, such as driving the switches, oscillator, and so forth. These losses are affected by operating conditions such as input voltage, temperature, and frequency. The next two losses are associated with the output resistance of the voltage converter circuit. Switch losses occur because of the on-resistance of the MOSFET switches in the IC. Charge-pump capacitor losses occur because of their ESR. The relationship between these losses and the output resistance is as follows:

$$P_{CAPACITOR\ LOSSES} + P_{CONVERSION\ LOSSES} = I_O^2 \times R_O \tag{3}$$

R_{SWITCH} = resistance of a single MOSFET-switch inside the converter
f_{OSC} = oscillator frequency

The first term is the effective resistance from an ideal switched-capacitor circuit. Conversion losses occur during the charge transfer between $C_{(fly)}$ and C_O when there is a voltage difference between them. The power loss is:

$$P_{CONV.LOSS} = \left[\frac{1}{2} \times C_{(fly)}\left(V_I^2 - V_O^2\right) + \frac{1}{2}C_O\left(V_{RIPPLE}^2 - 2V_O V_{RIPPLE}\right)\right] \times f_{osc} \tag{4}$$

The efficiency of the TPS6040x devices is dominated by their quiescent supply current at low output current and by their output impedance at higher current.

$$\eta \cong \frac{I_O}{I_O + I_Q}\left(1 - \frac{I_O \times R_O}{V_I}\right) \tag{5}$$

Where, I_Q = quiescent current.

8.4 Device Functional Modes

8.4.1 Active-Schottky Diode

For a short period of time, when the input voltage is applied, but the inverter is not yet working, the output capacitor is charged positive by the load. To prevent the output being pulled above GND, a Schottky diode must be added in parallel to the output. The function of this diode is integrated into the TPS6040x devices, which gives a defined startup performance and saves board space.

A current sink and a diode in series can approximate the behavior of a typical, modern operational amplifier. 图 8-2 shows the current into this typical load at a given voltage. The TPS6040x devices are optimized to start into these loads.

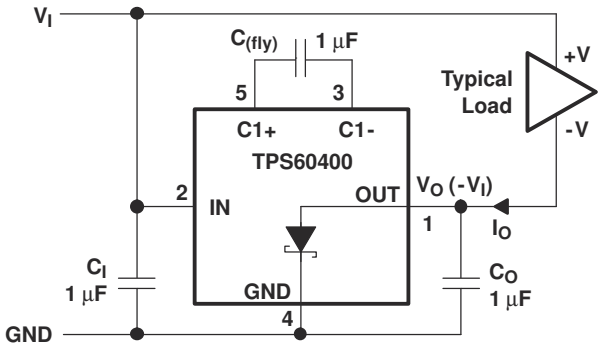


图 8-2. Typical Load

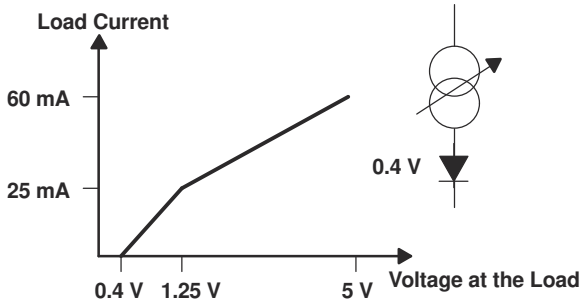


图 8-3. Maximum Start-Up Current

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6040x is a family of devices that generate an unregulated negative output voltage from an input voltage ranging from 1.6 V to 5.5 V.

9.2 Typical Application

9.2.1 Voltage Inverter

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

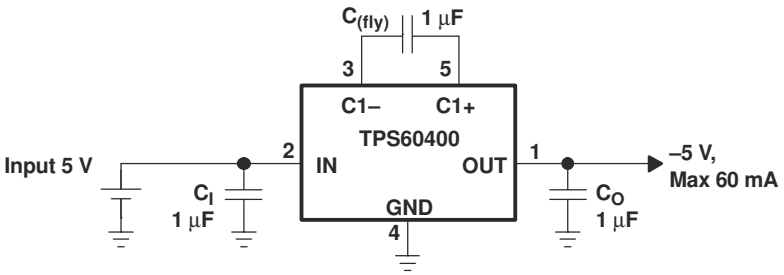


图 9-1. Typical Operating Circuit

9.2.1.1 Design Requirements

The TPS6040x is connected to generate a negative output voltage from a positive input.

9.2.1.2 Detailed Design Procedure

The most common application for these devices is a charge-pump voltage inverter (see 图 9-1). This application requires only two external components; capacitors $C_{(fly)}$ and C_O, plus a bypass capacitor, if necessary. Refer to the capacitor selection section for suggested capacitor types.

For the maximum output current and best performance, three ceramic capacitors of 1 µF (TPS60400, TPS60403) are recommended. For lower currents or higher allowed output voltage ripple, other capacitors can also be used. It is recommended that the output capacitors has a minimum value of 1 µF. With flying capacitors lower than 1 µF, the maximum output power decreases.

9.2.1.2.1 Capacitor Selection

To maintain the lowest output resistance, use capacitors with low ESR (see 表 9-1). The charge-pump output resistance is a function of $C_{(fly)}$'s and C_O's ESR. Therefore, minimizing the charge-pump capacitor's ESR minimizes the total output resistance. The capacitor values are closely linked to the required output current and the output noise and ripple requirements. It is possible to only use 1-µF capacitors of the same type.

9.2.1.2.2 Input Capacitor (C_I)

Bypass the incoming supply to reduce its ac impedance and the impact of the TPS6040x switching noise. The recommended bypassing depends on the circuit configuration and where the load is connected. When the inverter is loaded from OUT to GND, current from the supply switches between 2 x I_O and zero. Therefore, use a large bypass capacitor (for example, equal to the value of $C_{(fly)}$) if the supply has high ac impedance. When the inverter is loaded from IN to OUT, the circuit draws 2 × I_O constantly, except for short switching spikes. A 0.1-µF bypass capacitor is sufficient.

9.2.1.2.3 Flying Capacitor ($C_{(fly)}$)

Increasing the flying capacitor's size reduces the output resistance. Small values increases the output resistance. Above a certain point, increasing $C_{(fly)}$'s capacitance has a negligible effect, because the output resistance becomes dominated by the internal switch resistance and capacitor ESR.

9.2.1.2.4 Output Capacitor (C_O)

Increasing the output capacitor's size reduces the output ripple voltage. Decreasing its ESR reduces both output resistance and ripple. Smaller capacitance values can be used with light loads if higher output ripple can be tolerated. Use the following equation to calculate the peak-to-peak ripple.

$$V_{O(ripple)} = \frac{I_O}{f_{osc} \times C_O} + 2 \times I_O \times ESR_{CO} \quad (6)$$

表 9-1. Recommended Capacitor Values

DEVICE	V_I [V]	I_O [mA]	C_I [µF]	$C_{(fly)}$ [µF]	C_O [µF]
TPS60400	1.8···5.5	60	1	1	1
TPS60401	1.8···5.5	60	10	10	10
TPS60402	1.8···5.5	60	3.3	3.3	3.3
TPS60403	1.8···5.5	60	1	1	1

表 9-2. Recommended Capacitors

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	EMK212BJ474MG	0805	0.47 µF	Ceramic
	LMK212BJ105KG	0805	1 µF	Ceramic
	LMK212BJ225MG	0805	2.2 µF	Ceramic
	EMK316BJ225KL	1206	2.2 µF	Ceramic
	LMK316BJ475KL	1206	4.7 µF	Ceramic
	JMK316BJ106KL	1206	10 µF	Ceramic
TDK	C2012X5R1C105M	0805	1 µF	Ceramic
	C2012X5R1A225M	0805	2.2 µF	Ceramic
	C2012X5R1A335M	0805	3.3 µF	Ceramic

表 9-3 contains a list of manufacturers of the recommended capacitors. Ceramic capacitors will provide the lowest output voltage ripple because they typically have the lowest ESR-rating.

表 9-3. Recommended Capacitor Manufacturers

CAPACITOR TYPE	MANUFACTURER	WEB ADDRESS
X5R / X7R ceramic	Taiyo Yuden	www.t-yuden.com
X5R / X7R ceramic	TDK	www.component.tdk.com
X5R / X7R ceramic	Vishay	www.vishay.com
X5R / X7R ceramic	Kemet	www.kemet.com

9.2.1.2.5 Power Dissipation

As given in 节 7.4, the thermal resistance of TPS6040x is: $R_{\Theta JA}$ = 221°C/W.

The terminal resistance can be calculated using the following equation:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D} \tag{7}$$

where:

T_J is the junction temperature. T_A is the ambient temperature. P_D is the power that is dissipated by the device.

$$R_{\theta JA} = \frac{T_J - T_A}{P_D} \tag{8}$$

The maximum power dissipation can be calculated using the following equation:

$$P_D = V_I \times I_I - V_O \times I_O = V_{I(max)} \times (I_O + I_{(SUPPLY)}) - V_O \times I_O \tag{9}$$

The maximum power dissipation happens with maximum input voltage and maximum output current.

At maximum load the supply current is 0.7 mA maximum.

$$P_D = 5\ V \times (60\ mA + 0.7\ mA) - 4.4\ V \times 60\ mA = 40\ mW \tag{10}$$

With this maximum rating and the thermal resistance of the device on the EVM, the maximum temperature rise above ambient temperature can be calculated using the following equation:

$$\Delta T_J = R_{\Theta JA} \times P_D = 221°C/W \times 40\ mW = 8.8°C \tag{11}$$

This means that the internal dissipation increases T_J by <10°C.

The junction temperature of the device shall not exceed 125°C.

This means the IC can easily be used at ambient temperatures up to:

$$T_A = T_{J(max)} - \Delta T_J = 125°C/W - 10°C = 115°C \tag{12}$$

9.2.1.3 Application Curves

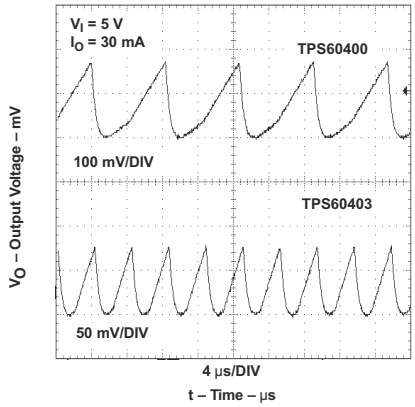


图 9-2. Output Voltage vs Time for TPS60400 and TPS60401

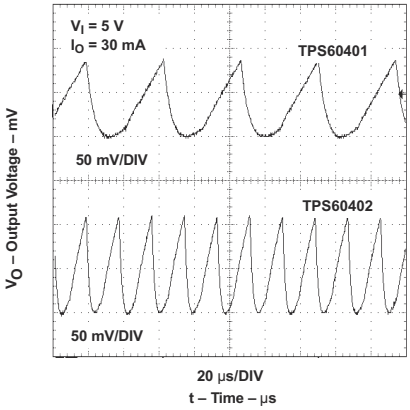


图 9-3. Output Voltage vs Time for TPS60401 and TPS60402

9.3 System Examples

To reduce the output voltage ripple, a RC post filter can be used.

An output filter can easily be formed with a resistor (R_P) and a capacitor (C_P). Cutoff frequency is given by:

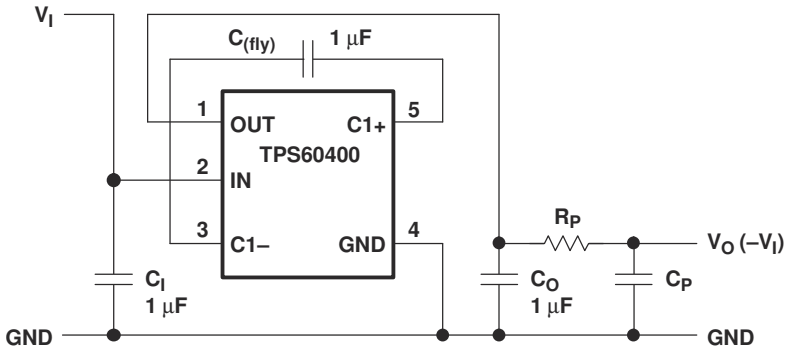


图 9-4. TPS60400 with RC-Post Filter

The equation refers only to the relation between output and input of the ac ripple voltages of the filter.

$$f_c = \frac{1}{2\pi R_P C_P} \quad (1)$$

and ratio V_O/V_{OUT} is:

$$\left|\frac{V_O}{V_{OUT}}\right| = \frac{1}{\sqrt{1 + \left(2\pi f R_P C_P\right)^2}} \quad (2)$$

with R_P = 50 Ω, C_P = 0.1 µF and f = 250 kHz: $\left|\frac{V_O}{V_{OUT}}\right| = 0.125$ (13)

To reduce the output voltage ripple, a LC post filter can be used.

图 9-5 shows a configuration with a LC-post filter to further reduce output ripple and noise.

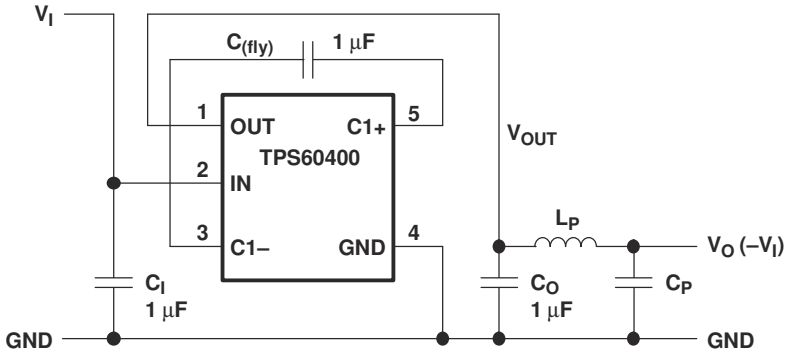


图 9-5. LC-Post Filter

The application allows to generate a voltage rail at a level of 1/2 of the input voltage.

A switched-capacitor voltage inverter can be configured as a high efficiency rail-splitter. This circuit provides a bipolar power supply that is useful in battery powered systems to supply dual-rail ICs, like operational amplifiers. Moreover, the SOT23-5 package and associated components require very little board space.

After power is applied, the flying capacitor ($C_{(fly)}$) connects alternately across the output capacitors C_3 and C_O. This equalizes the voltage on those capacitors and draws current from V_I to V_O as required to maintain the output at 1/2 V_I.

The maximum input voltage between V_I and GND in the schematic (or between IN and OUT at the device itself) must not exceed 6.5 V.

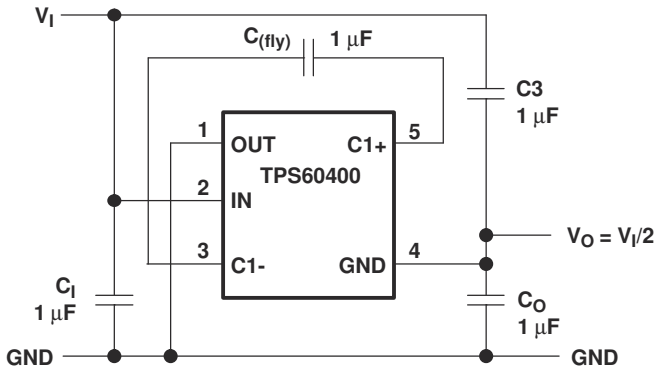


图 9-6. TPS60400 as a High-Efficiency Rail Splitter

The application allows to generate a voltage rail at a level of -Vi as well as 2 x Vi (V(pos)).

In the circuit of 图 9-7, capacitors C_I, $C_{(fly)}$, and C_O form the inverter, while C1 and C2 form the doubler. C1 and C $_{(fly)}$ are the flying capacitors; C_O and C2 are the output capacitors. Because both the inverter and doubler use part of the charge-pump circuit, loading either output causes both outputs to decline toward GND. Make sure the sum of the currents drawn from the two outputs does not exceed 60 mA. The maximum output current at $V_{(pos)}$ must not exceed 30 mA. If the negative output is loaded, this current must be further reduced.

$$I_I \approx -I_O + 2 \times I_{O(POS)}$$

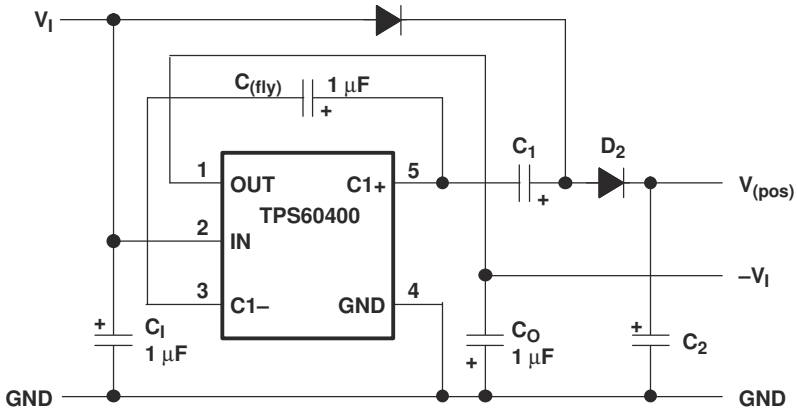


图 9-7. TPS60400 as Doubler/Inverter

The application generate a voltage rail at a level -2 x Vi.

Two devices can be cascaded to produce an even larger negative voltage (see 图 9-8). The unloaded output voltage is normally -2 × V_I, but this is reduced slightly by the output resistance of the first device multiplied by the quiescent current of the second. When cascading more than two devices, the output resistance rises dramatically.

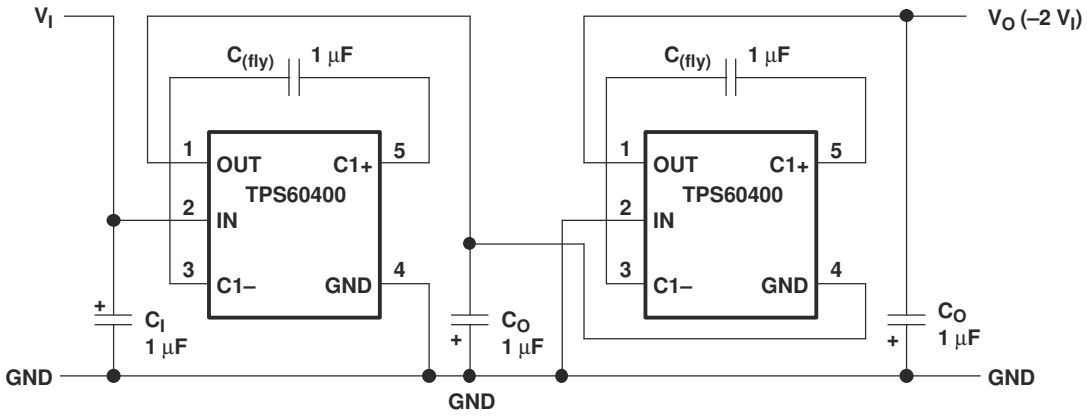


图 9-8. Doubling Inverter

The application allows to increase the output current by using two or more in parallel.

Paralleling multiple TPS6040xs reduces the output resistance. Each device requires its own flying capacitor ($C_{(fly)}$), but the output capacitor (C_O) serves all devices (see 图 9-9). Increase C_O's value by a factor of n, where n is the number of parallel devices. Equation 1 shows the equation for calculating output resistance.

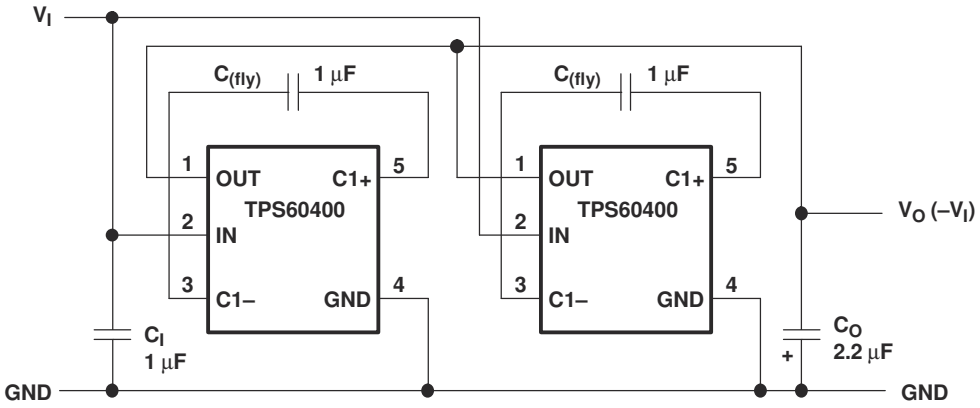


图 9-9. Paralleling Devices

The application adds a shutdown function.

If shutdown is necessary, use the circuit in 图 9-10. The output resistance of the TPS6040x typically is 15 Ω plus two times the output resistance of the buffer.

Connecting multiple buffers in parallel reduces the output resistance of the buffer driving the IN pin.

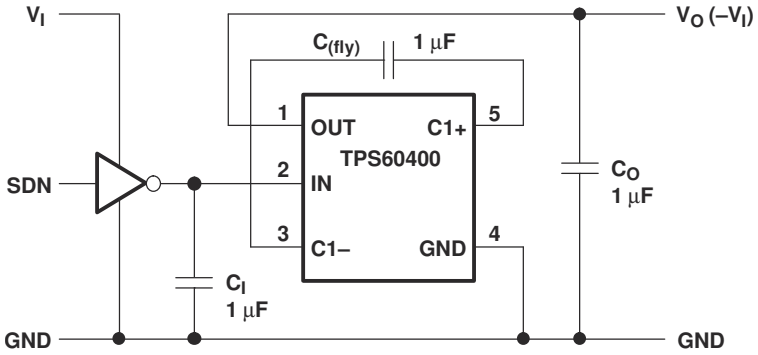


图 9-10. Shutdown Control

The application generates a regulated output voltage for a GaAs bias supply.

A solution for a -2.7-V/3-mA GaAs bias supply is proposed in 图 9-11. The input voltage of 3.3 V is first inverted with a TPS60403 and stabilized using a TLV431 low-voltage shunt regulator. Resistor R_P with capacitor C_P is used for filtering the output voltage.

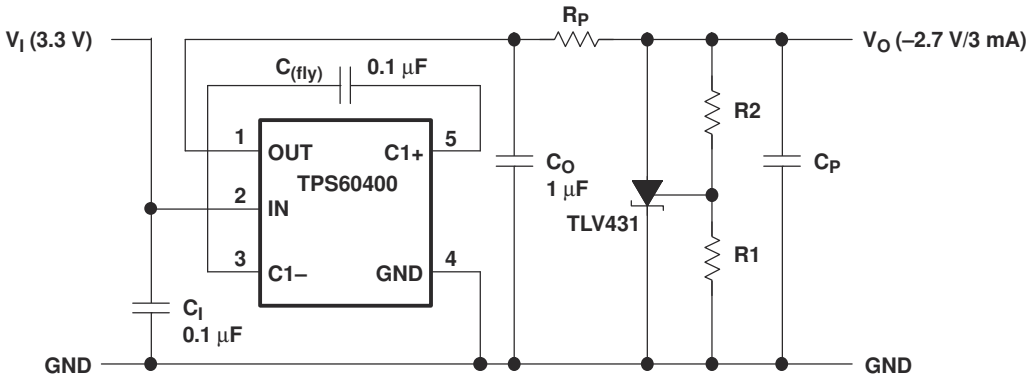


图 9-11. GaAs Supply

A 0.1-µF capacitor was selected for $C_{(fly)}$. By this, the output resistance of the inverter is about 52 Ω.

R_{PMAX} can be calculated using the following equation:

$$V_O = -\left(1 + \frac{R1}{R2}\right) \times V_{ref} - R1 \times I_{I(ref)} \tag{14}$$

A 100-Ω resistor was selected for R_P.

The reference voltage across R2 is 1.24 V typical. With 5-µA current for the voltage divider, R2 gets:

$$R_{PMAX} = \left(\frac{V_{CO} - V_O}{I_O} - R_O\right)$$

With: V_{CO} = –3.3 V; V_O = –2.7 V; I_O = –3 mA

R_{PMAX} = 200 Ω – 52 Ω = 148 Ω (15)

With C_P = 1 µF the ratio V_O/V_I of the RC post filter is:

$$R2 = \frac{1.24\ V}{5\ \mu A} \approx 250\ k\Omega$$

$$R1 = \frac{2.7 - 1.24\ V}{5\ \mu A} \approx 300\ k\Omega \tag{16}$$

$$\left|\frac{V_O}{V_I}\right| = \frac{1}{\sqrt{1 + (2\pi 125000Hz \times 100\Omega \times 1\ \mu F)^2}} \approx 0.01 \tag{17}$$

The application generates an output voltage of 1/2 of the input voltage.

By exchanging GND with OUT (connecting the GND pin with OUT and the OUT pin with GND), a step-down charge pump can easily be formed. In the first cycle S1 and S3 are closed, and $C_{(fly)}$ with C_O in series are charged. Assuming the same capacitance, the voltage across $C_{(fly)}$ and C_O is split equally between the capacitors. In the second cycle, S2 and S4 close and both capacitors with $V_I/2$ across are connected in parallel.

The maximum input voltage between V_I and GND in the schematic (or between IN and OUT at the device itself) must not exceed 6.5 V. For input voltages in the range of 6.5 V to 11 V, an additional Zener-diode is recommended (see 图 9-14).

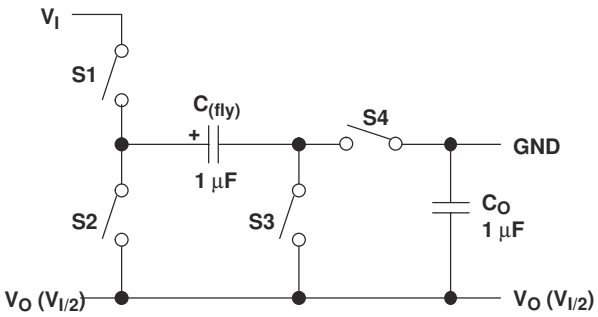


图 9-12. Step-Down Principle

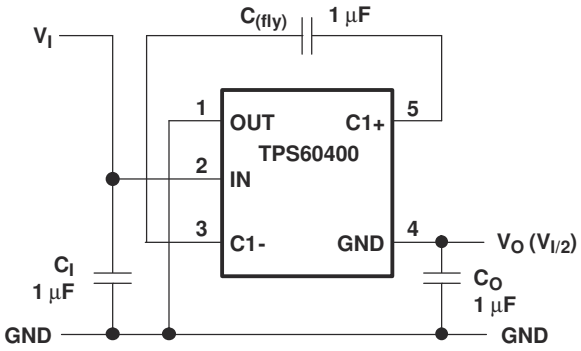


图 9-13. Step-Down Charge Pump Connection

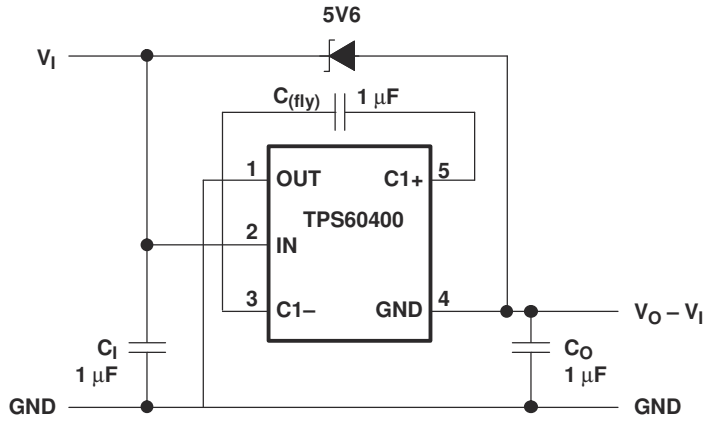


图 9-14. Step-Down Charge Pump Connection for Higher Input Voltages

10 Power Supply Recommendations

The TPS60400 device family has no special requirements for its power supply. The power supply output needs to be rated according to the supply voltage, output voltage and output current of the TPS6040x.

11 Layout

11.1 Layout Guidelines

All capacitors should be soldered as close as possible to the IC. A PCB layout proposal for a single-layer board is shown in 图 11-1. Care has been taken to connect all capacitors as close as possible to the circuit to achieve optimized output voltage ripple performance.

11.2 Layout Example

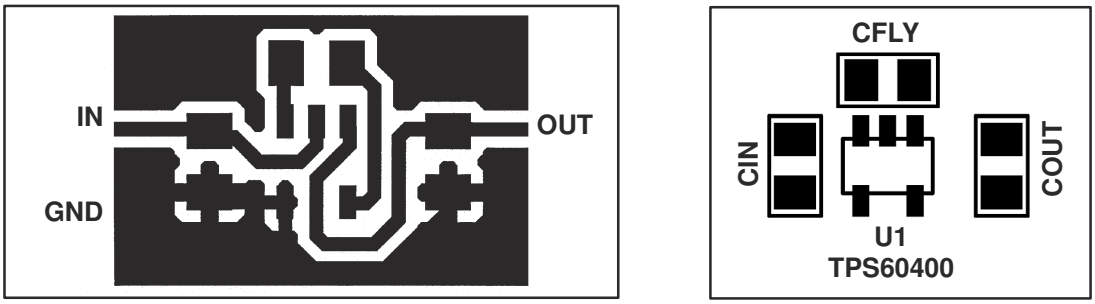


图 11-1. Recommended PCB Layout for TPS6040x (Top Layer)

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Device Family Products

Other inverting DC-DC converters from Texas Instruments are listed in 表 12-1.

表 12-1. Product Identification

PART NUMBER	DESCRIPTION
TPS6735	Fixed negative 5-V, 200-mA inverting dc-dc converter
TPS6755	Adjustable 1-W inverting dc-dc converter

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS60400	Click here	Click here	Click here	Click here	Click here
TPS60401	Click here	Click here	Click here	Click here	Click here
TPS60402	Click here	Click here	Click here	Click here	Click here
TPS60403	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60400DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFKI	Samples
TPS60400DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFKI	Samples
TPS60400DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFKI	Samples
TPS60400DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFKI	Samples
TPS60401DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFLI	Samples
TPS60401DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFLI	Samples
TPS60401DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFLI	Samples
TPS60401DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFLI	Samples
TPS60402DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFMI	Samples
TPS60402DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFMI	Samples
TPS60402DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFMI	Samples
TPS60402DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFMI	Samples
TPS60403DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFNI	Samples
TPS60403DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFNI	Samples
TPS60403DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFNI	Samples
TPS60403DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFNI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS60400, TPS60401, TPS60402, TPS60403 :

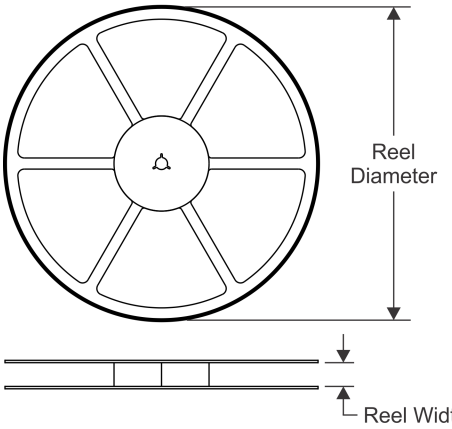
- Automotive : TPS60400-Q1, TPS60401-Q1, TPS60402-Q1, TPS60403-Q1

NOTE: Qualified Version Definitions:

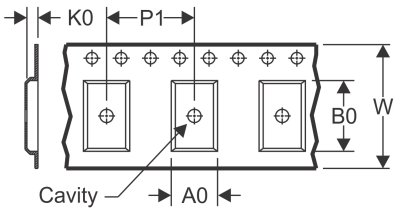
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

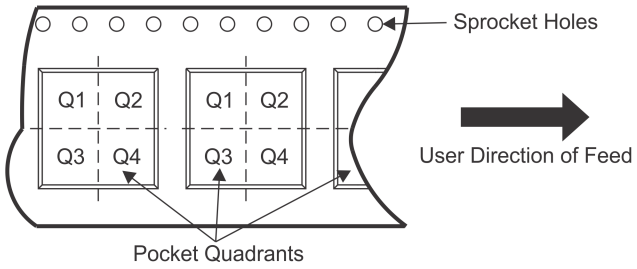


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

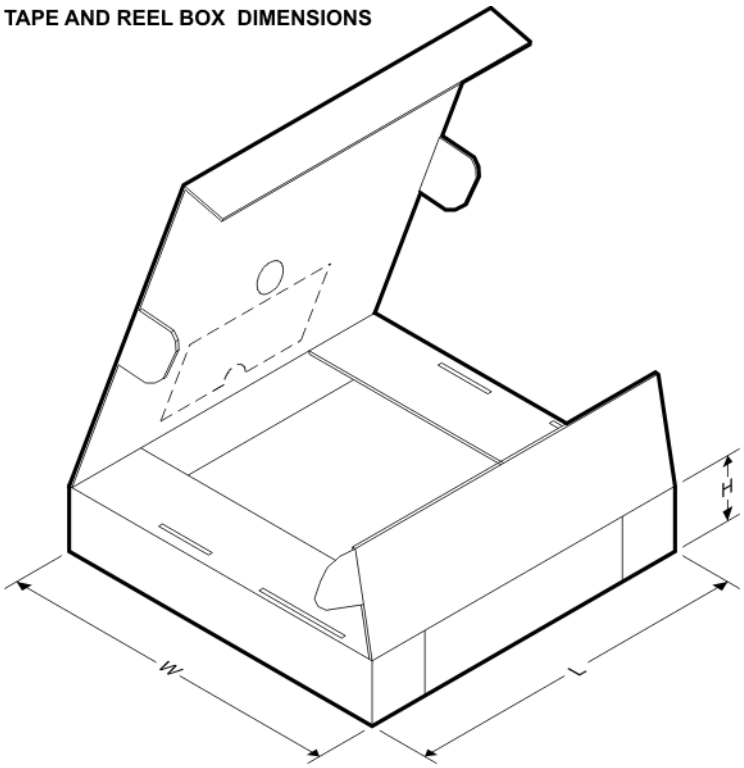
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60400DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS60400DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS60401DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS60401DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS60402DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS60402DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS60403DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS60403DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

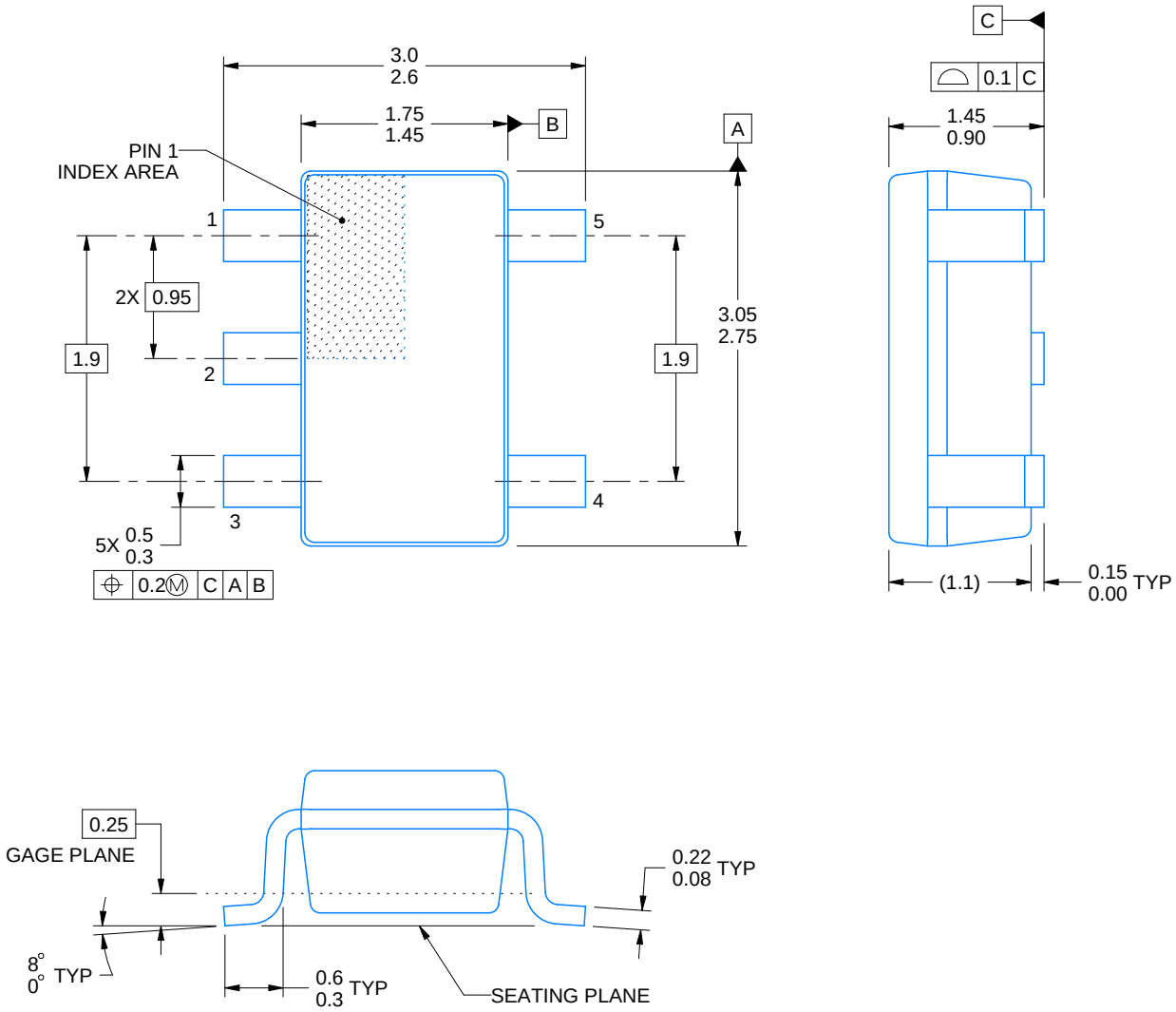
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60400DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS60400DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS60401DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS60401DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS60402DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS60402DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS60403DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS60403DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

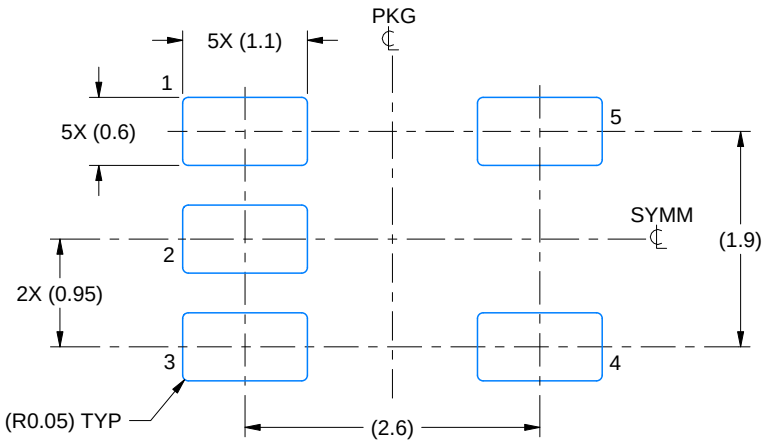
SMALL OUTLINE TRANSISTOR



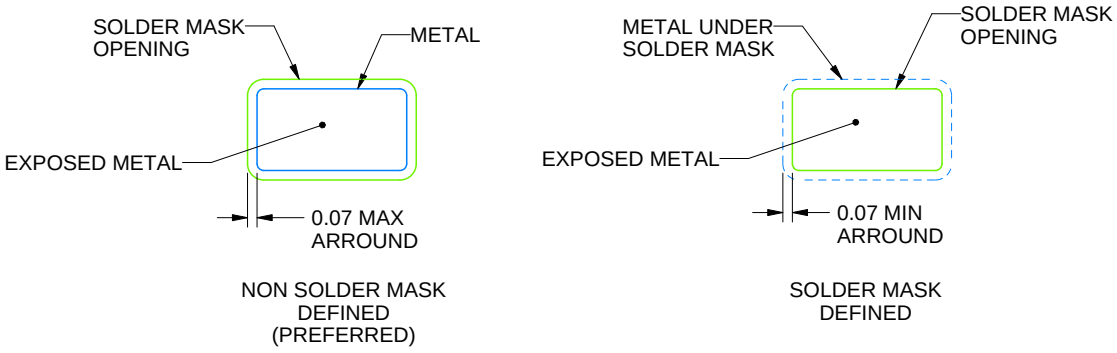
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

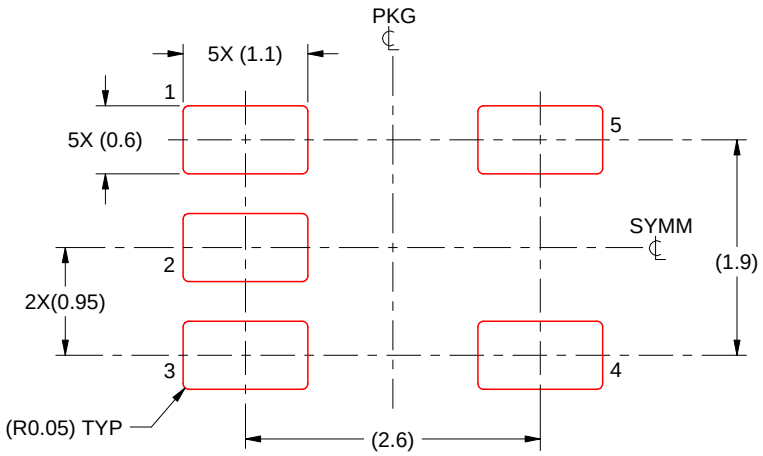


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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