TPS6040x-Q1 Unregulated 60-mA Charge Pump Voltage Inverter

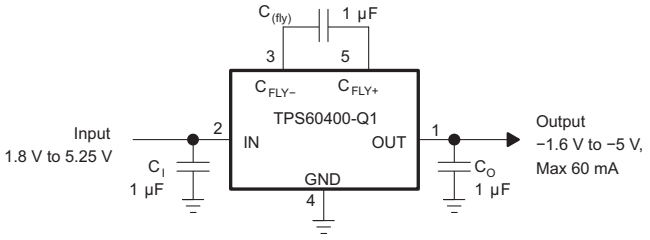
1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Inverts Input Supply Voltage
- Up to 60-mA Output Current
- Only Three Small 1-µF Ceramic Capacitors Needed
- Input Voltage Range From 1.8 V to 5.25 V
- PowerSave-Mode for Improved Efficiency at Low Output Currents (TPS60400-Q1)
- Device Quiescent Current Typical: 100 µA
- Integrated Active Schottky-Diode for Start-Up Into Load
- Small 5-Pin SOT23 Package
- Evaluation Module Available: TPS60400EVM-178

2 Applications

- Automotive Infotainment
- Automotive Cluster
- LCD Displays
- Negative Supply Voltages

Typical Application Circuit



3 Description

The TPS6040x-Q1 family of devices generate an unregulated negative output voltage from an input voltage ranging from 1.8 V to 5.25 V. The devices are typically supplied by a preregulated supply rail of 5 V or 3.3 V. Due to its wide-input voltage range, two or three NiCd, NiMH, or alkaline battery cells, as well as one Li-Ion cell, can also power them.

Only three external 1-µF capacitors are required to build a complete DC-DC charge pump inverter. Assembled in a 5-pin SOT-23 package, the complete converter can be built on a 50-mm^2 board area. Replacing the Schottky diode typically needed for start-up into load with integrated circuitry can achieve additional board area and component count reduction.

The TPS6040x-Q1 can deliver a maximum output current of 60 mA, with a typical conversion efficiency of greater than 90% over a wide output current range. Three device options TPS60401/2/3-Q1 with 20-kHz, 50-kHz, and 250-kHz fixed frequency operation are available. TPS60400-Q1 device comes with a variable switching frequency to reduce operating current in applications with a wide load range and enables the design with low-value capacitors.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6040x-Q1	SOT-23 (5)	2.80 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Output Voltage vs Input Voltage

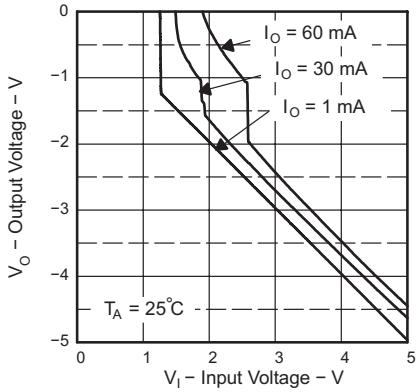


Table of Contents

4 Revision History

Changes from Revision A (June 2008) to Revision B **Page**

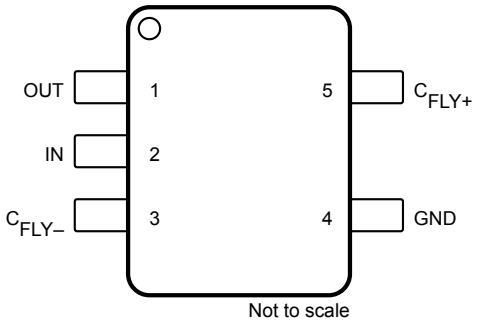
- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed TPS6040x to TPS6040x-Q1 throughout document ... 1
- Added AEC-Q100 Test Guidance bullets ... 1
- Changed Input voltage range throughout document to 1.8 V to 5.25 V ... 1
- Changed input voltage 5.5 V to 5.25 V. ... 1
- Added device options TPS60401/2/3-Q1 ... 1
- Deleted *Available Options* table and moved *device family products* section and renamed to *Device Comparison Table* ... 3
- Changed reference to *Thermal Information* ... 3
- Deleted Machine model (MM) from ESD Ratings table ... 4
- Added table note to reference values ... 4
- Deleted *Dissipation Ratings* section and replaced with *Thermal Information* table ... 5
- Changed Figure 1 and Figure 2 Output Current limit to 60 mA ... 6
- Split equation (1) into two separate numbered equations ... 11
- Moved equation definitions to corresponding equation ... 11
- Deleted *Voltage Inverter* title ... 13
- Deleted Table 4 and Table 5 manufacturer part information ... 13
- Moved Figure 21 and 22 to *Application Curves* section ... 15

5 Device Comparison Table

PART NUMBER	TYPICAL FLYING CAPACITOR (µF)	FEATURE
TPS60400-Q1	1	Variable switching frequency 50 kHz to 250 kHz
TPS60401-Q1	10	Fixed frequency 20 kHz
TPS60402-Q1	3.3	Fixed frequency 50 kHz
TPS60403-Q1	1	Fixed frequency 250 kHz

6 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C_{FLY+}	5	I	Positive terminal of the flying capacitor $C_{(fly)}$
C_{FLY-}	3	I	Negative terminal of the flying capacitor $C_{(fly)}$
GND	4	GND	Ground
IN	2	PWR	Supply input. Connect to an input supply in the 1.8-V to 5.25-V range. Bypass IN to GND with a capacitor that has the same value as the flying capacitor.
OUT	1	O	Power output with $V_O = -V_I$ Bypass OUT to GND with the output filter capacitor C_O.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range	IN to GND	–0.3	5.5	V
	OUT to GND	–5	0.3	
	C_{FLY-} to GND	0.3	V_O – 0.3	
	C_{FLY+} to GND	–0.3	V_I + 0.3	
Continuous power dissipation		See *Thermal Information*		
Continuous output current			80	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	1.8		5.25	V
I_O	Output current at OUT			60	mA
C_I	Input capacitor	0	$C_{(fly)}$ (1)		µF
$C_{(fly)}$	Flying capacitor		1		µF
C_O	Output capacitor		1	100	µF
T_J	Operating junction temperature	–40		125	°C

(1) Refer to *Device Comparison Table* for C_{fly} values

7.4 Thermal Information

THERMAL METRIC (1)		TPS6040x-Q1 DBV (SOT-25) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	221.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*.

7.5 Electrical Characteristics

$C_I = C_{(fly)} = C_O$ (according to Table 2), T_J = –40°C to 125°C, and V_I = 5 V over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Supply voltage range	At T_J = –40°C to 125°C, R_L = 5 kΩ		1.8		5.25	V
		At $T_C \geq$ 0°C, R_L = 5 kΩ		1.6			
I_O	Maximum output current at V_O			60			mA
V_O	Output voltage				$-V_I$		V
V_{P-P}	Output voltage ripple	I_O = 5 mA	TPS60400-Q1, $C_{(fly)}$ = 1 µF, C_O = 2.2 µF		35		mV_{P-P}
			TPS60401-Q1, $C_{(fly)}$ = C_O = 10 µF		20		
			TPS60402-Q1, $C_{(fly)}$ = C_O = 3.3 µF		20		
			TPS60403-Q1, $C_{(fly)}$ = C_O = 1 µF		15		

Electrical Characteristics (continued)

$C_I = C_{(fly)} = C_O$ (according to Table 2), T_J = –40°C to 125°C, and V_I = 5 V over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent current (no-load input current)	V_I = 5 V	TPS60400-Q1		125	270	µA
			TPS60401-Q1		65	190	
			TPS60402-Q1		120	270	
			TPS60403-Q1		425	700	
		T_J = 60°C, V_I = 5 V	TPS60400-Q1			210	
			TPS60401-Q1			135	
			TPS60402-Q1			210	
			TPS60403-Q1			640	
f_{OSC}	Internal switching frequency	TPS60400-Q1, VCO version		25	50 to 250	375	kHz
		TPS60401-Q1		10	20	30	
		TPS60402-Q1		25	50	75	
		TPS60403-Q1		115	250	325	
	Impedance at 25°C, V_I = 5 V	TPS60400-Q1, $C_I = C_{(fly)} = C_O$ = 1 µF			12	15	Ω
		TPS60401-Q1, $C_I = C_{(fly)} = C_O$ = 10 µF			12	15	
		TPS60402-Q1, $C_I = C_{(fly)} = C_O$ = 3.3 µF			12	15	
		TPS60403-Q1, $C_I = C_{(fly)} = C_O$ = 1 µF			12	15	

7.6 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
η	Efficiency	vs Output current at 3.3 V and 5 V (TPS6040x-Q1)	Figure 1, Figure 2
I_I	Input current	vs Output current (TPS6040x-Q1)	Figure 3, Figure 4
I_S	Supply current	vs Input voltage (TPS6040x-Q1)	Figure 5, Figure 6
	Output resistance	vs Input voltage at –40°C, 0°C, 25°C, 85°C $C_I = C_{(fly)} = C_O$ = 1 µF (TPS60400-Q1) $C_I = C_{(fly)} = C_O$ = 10 µF (TPS60401-Q1) $C_I = C_{(fly)} = C_O$ = 3.3 µF (TPS60402-Q1) $C_I = C_{(fly)} = C_O$ = 1 µF (TPS60403-Q1)	Figure 7, Figure 8, Figure 9, Figure 10
V_O	Output voltage	vs Output current at 25°C, V_{IN} = 1.8 V, 2.5 V, 3.3 V, 5 V $C_I = C_{(fly)} = C_O$ = 1 µF (TPS60400-Q1) $C_I = C_{(fly)} = C_O$ = 10 µF (TPS60401-Q1) $C_I = C_{(fly)} = C_O$ = 3.3 µF (TPS60402-Q1) $C_I = C_{(fly)} = C_O$ = 1 µF (TPS60403-Q1)	Figure 11, Figure 12, Figure 13, Figure 14
fOSC	Oscillator frequency	vs Temperature at V_I = 1.8 V, 2.5 V, 3.3 V, 5 V (TPS6040x-Q1)	Figure 15, Figure 16, Figure 17, Figure 18
		vs Output current TPS60400 at 2 V, 3.3 V, 5 V	Figure 19
	Output ripple and noise	V_I = 5 V, I_O = 30 mA, $C_I = C_{(fly)} = C_O$ = 1 µF (TPS60400-Q1) V_I = 5 V, I_O = 30 mA, $C_I = C_{(fly)} = C_O$ = 10 µF (TPS60401-Q1) V_I = 5 V, I_O = 30 mA, $C_I = C_{(fly)} = C_O$ = 3.3 µF (TPS60402-Q1) V_I = 5 V, I_O = 30 mA, $C_I = C_{(fly)} = C_O$ = 1 µF (TPS60403-Q1)	Figure 24, Figure 25

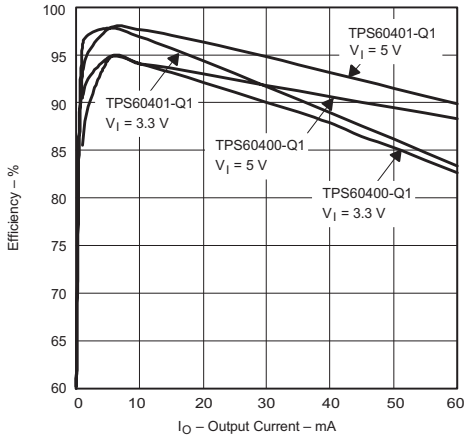


Figure 1. TPS60400-Q1, TPS60401-Q1 Efficiency vs Output Current

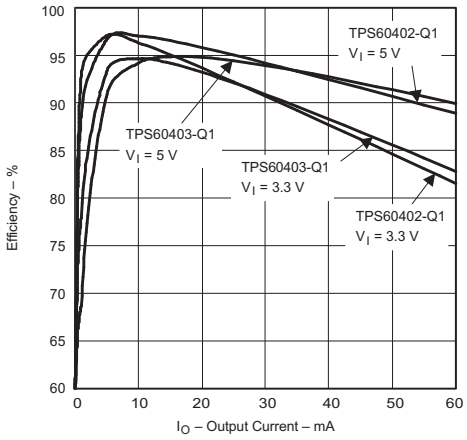


Figure 2. TPS60402-Q1, TPS60403-Q1 Efficiency vs Output Current

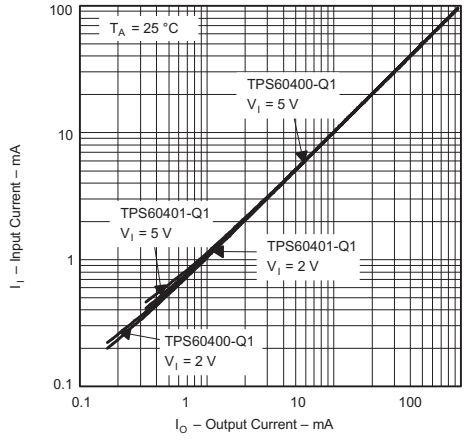


Figure 3. TPS60400-Q1, TPS60401-Q1 Input Current vs Output Current

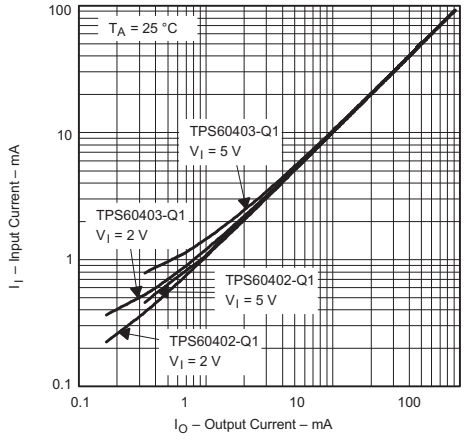


Figure 4. TPS60402-Q1, TPS60403-Q1 Input Current vs Output Current

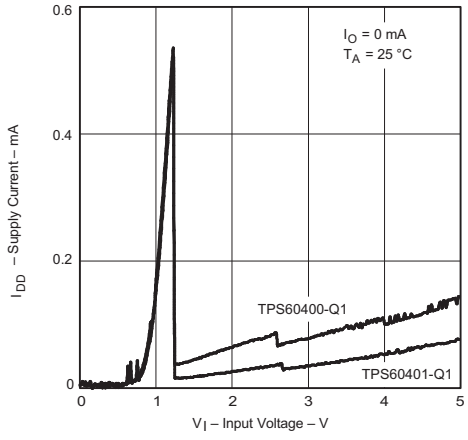


Figure 5. TPS60400-Q1, TPS60401-Q1 Supply Current vs Input Voltage

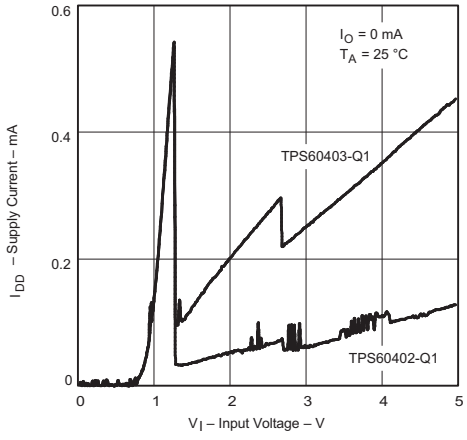


Figure 6. TPS60402-Q1, TPS60403-Q1 Supply Current vs Input Voltage

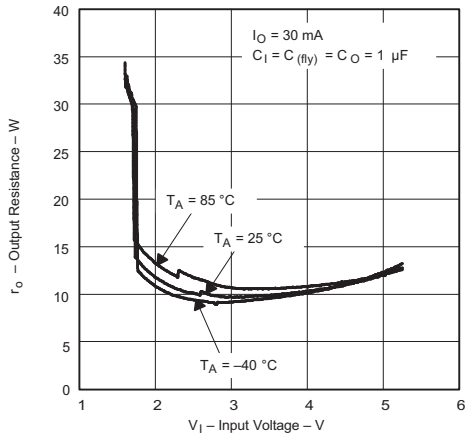


Figure 7. TPS60400-Q1 Output Resistance vs Input Voltage

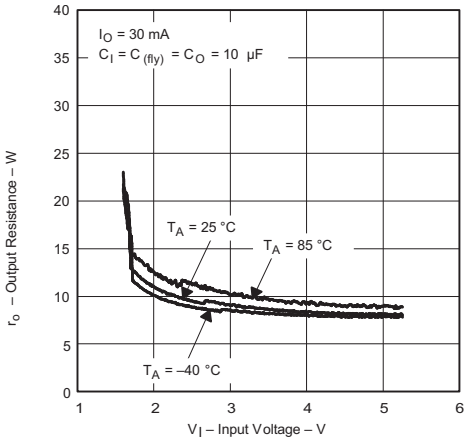


Figure 8. TPS60401-Q1 Output Resistance vs Input Voltage

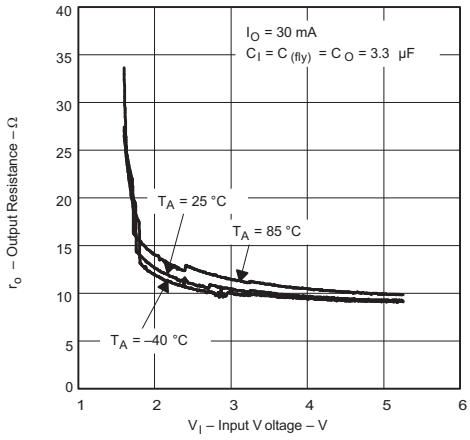


Figure 9. TPS60402-Q1 Output Resistance vs Input Voltage

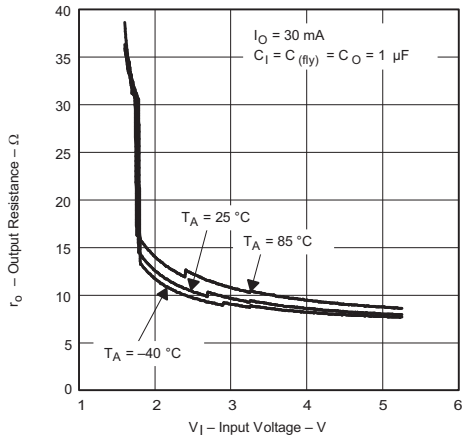


Figure 10. TPS60403-Q1 Output Resistance vs Input Voltage

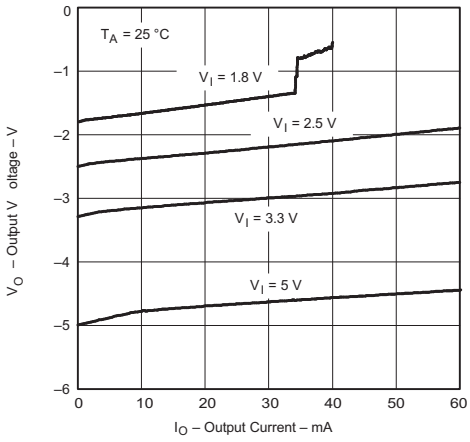


Figure 11. TPS60400-Q1 Output Voltage vs Output Current

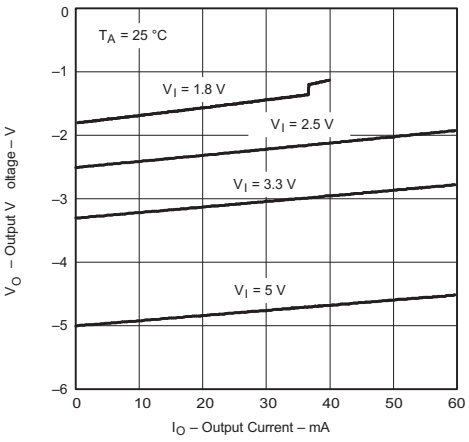


Figure 12. TPS60401-Q1 Output Voltage vs Output Current

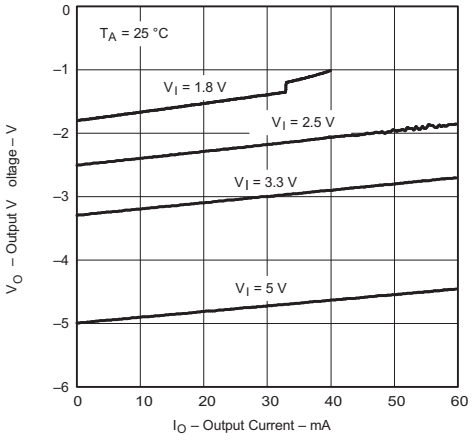


Figure 13. TPS60402-Q1 Output Voltage vs Output Current

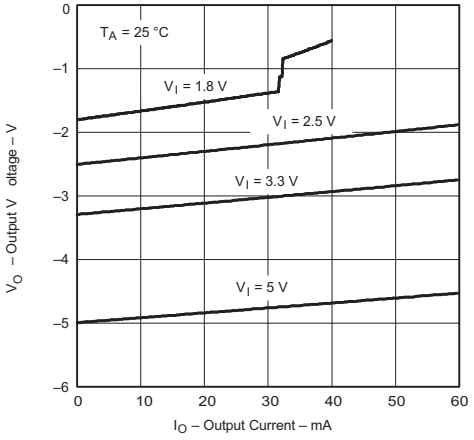


Figure 14. TPS60403-Q1 Output Voltage vs Output Current

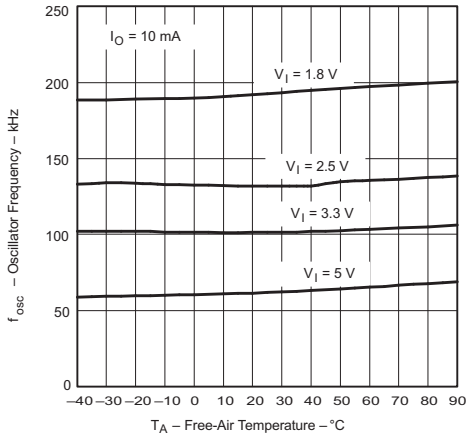


Figure 15. TPS60400-Q1 Oscillator Frequency vs Free-Air Temperature

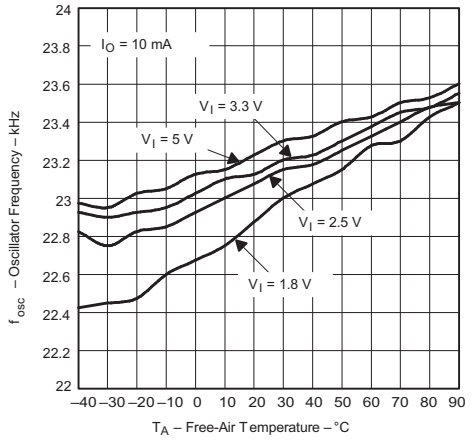


Figure 16. TPS60401-Q1 Oscillator Frequency vs Free-Air Temperature

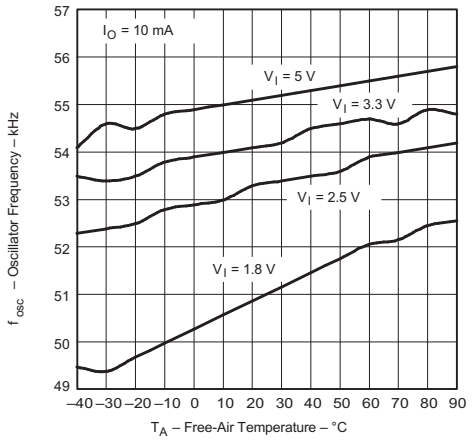


Figure 17. TPS60402-Q1 Oscillator Frequency vs Free-Air Temperature

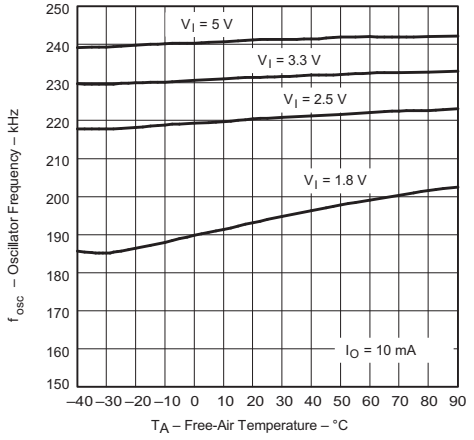


Figure 18. TPS60403-Q1 Oscillator Frequency vs Free-Air Temperature

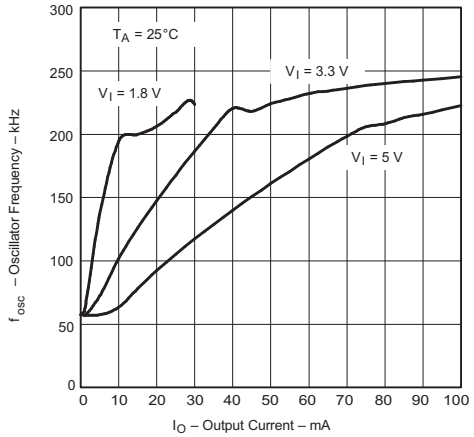


Figure 19. TPS60400-Q1 Oscillator Frequency vs Output Current

8 Detailed Description

8.1 Overview

The TPS6040x-Q1 charge pumps invert the voltage applied to their input. For the highest performance, use low equivalent series resistance (ESR) capacitors (for example, ceramic). During the first half-cycle, switches S2 and S4 open, switches S1 and S3 close, and capacitor ($C_{(fly)}$) charges to the voltage at V_I. During the second half-cycle, S1 and S3 open, and S2 and S4 close. This connects the positive terminal of $C_{(fly)}$ to GND and the negative to V_O. By connecting $C_{(fly)}$ in parallel, C_O is charged negative. The actual voltage at the output is more positive than $-V_I$, since switches S1–S4 have resistance and the load drains charge from C_O.

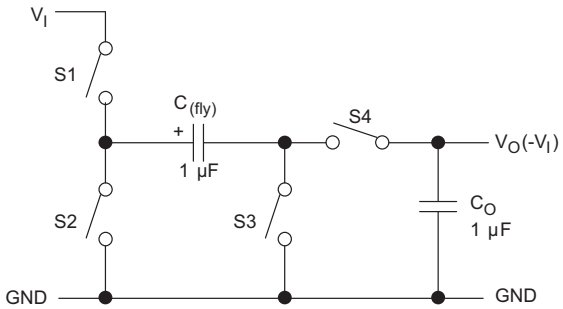
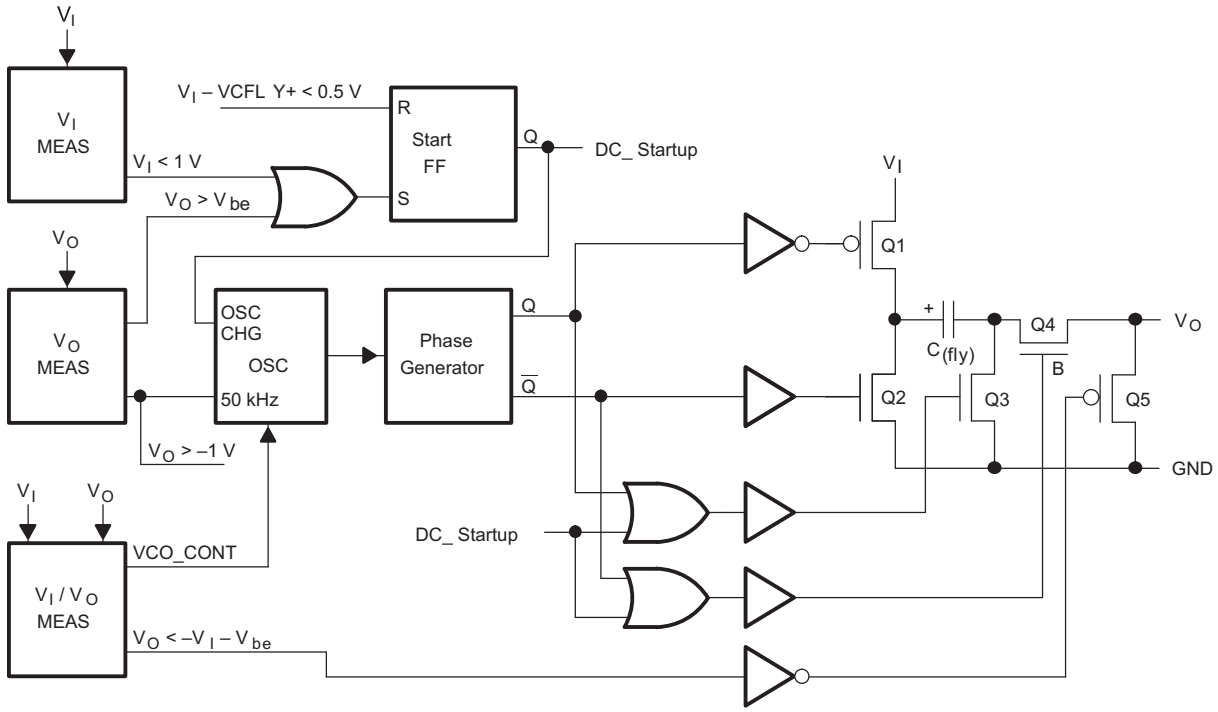


Figure 20. Operating Principle

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Charge-Pump Output Resistance

The TPS6040x-Q1 devices are not voltage regulators. The output source resistance of the charge pumps is approximately 15 Ω at room temperature (with V_I = 5 V), and V_O approaches –5 V when lightly loaded. V_O will droop toward GND as load current increases as seen in Equation 1.

$$V_O = -(V_I - R_O \times I_O) \tag{1}$$

$$R_O \approx \frac{1}{f\text{osc} \times C_{(fly)}} + 4\,(2 \times R_{SWITCH} + ESR_{CFLY}) + ESR_{CO} \tag{2}$$

where

- R_O = output resistance of the converter
- R_{SWITCH} = resistance of a single MOSFET-switch inside the converter
- f_{OSC} = oscillator frequency

8.3.2 Efficiency Considerations

The power efficiency of a switched-capacitor voltage converter is affected by three factors: the internal losses in the converter IC, the resistive losses of the capacitors, and the conversion losses during charge transfer between the capacitors. The internal losses are associated with the internal functions of the ICs, such as driving the switches, oscillator, and so forth. These losses are affected by operating conditions such as input voltage, temperature, and frequency. The next two losses are associated with the voltage converter circuit's output resistance. Switch losses occur because of the on-resistance of the MOSFET switches in the IC. Charge-pump capacitor losses occur because of their ESR. The relationship between these losses and the output resistance is Equation 3.

$$P_{CAPACITOR\ LOSSES} + P_{CONVERSION\ LOSSES} = I_O^2 \times R_O \tag{3}$$

The first term is the effective resistance from an ideal switched-capacitor circuit. Conversion losses occur during the charge transfer between $C_{(fly)}$ and C_O when there is a voltage difference between them. The power loss is Equation 4.

$$P_{CONV.LOSS} = \left[\frac{1}{2} \times C_{(flY)}(V_I^2 - V_O^2) + \frac{1}{2} C_O (V_{RIPPLE}^2 - 2V_O V_{RIPPLE})\right] \times f_{osc} \tag{4}$$

The efficiency of the TPS6040x-Q1 devices is dominated by their quiescent supply current at low output current and by their output impedance at higher current (see Equation 5).

$$\eta = \frac{I_O}{I_O + I_Q}\left(1 - \frac{I_O \times R_O}{V_I}\right) \tag{5}$$

where

- I_Q = quiescent current

8.4 Device Functional Modes

8.4.1 Active-Schottky Diode

For a short period of time, when the input voltage is applied, but the inverter is not yet working, the output capacitor is charged positive by the load. To prevent the output being pulled above GND, a Schottky diode must be added in parallel to the output. The function of this diode is integrated into the TPS6040x-Q1 devices, which gives a defined startup performance and saves board space.

A current sink and a diode in series can approximate the behavior of a typical, modern operational amplifier. Figure 21 shows the current into this typical load at a given voltage. The TPS6040x-Q1 devices are optimized to start into these loads.

Device Functional Modes (continued)

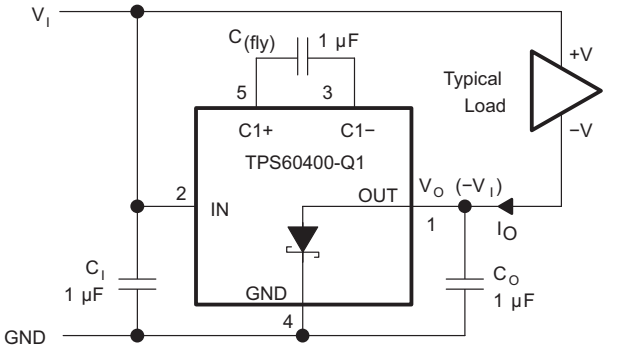


Figure 21. Typical Load

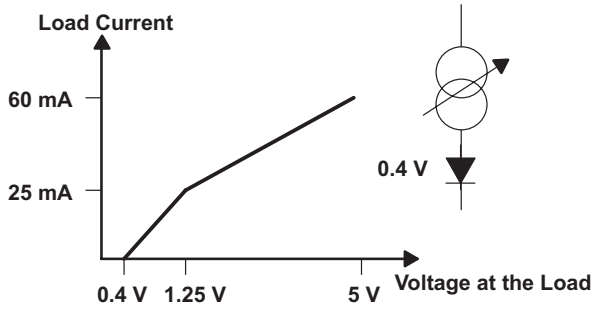


Figure 22. Maximum Start-Up Current

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6040x-Q1 family of devices generate an unregulated negative output voltage from an input voltage ranging from 1.8 V to 5.25 V.

9.2 Typical Applications

The most common application for these devices is a charge-pump voltage inverter (see Figure 23). This application requires only two external components; capacitors $C_{(fly)}$ and C_O, plus a bypass capacitor, if necessary. See *Capacitor Selection* for suggested capacitor types.

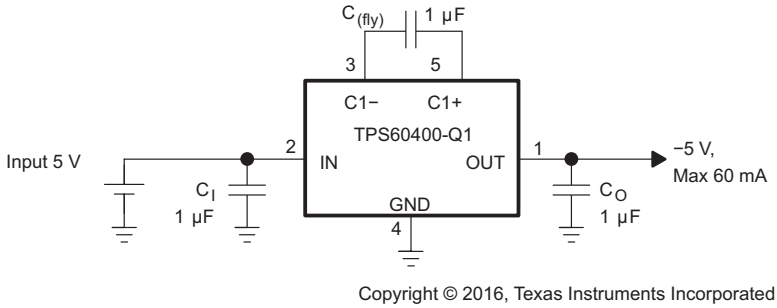


Figure 23. Typical Operating Circuit

9.2.1 Design Requirements

The TPS6040x-Q1 is connected to generate a negative output voltage with 60-mA maximum load, from a positive input voltage between 1.8 V and 5.25 V.

9.2.2 Detailed Design Procedure

For the maximum output current and best performance, three ceramic capacitors of 1 µF (TPS60400-Q1, TPS60403-Q1) are recommended. For lower currents or higher allowed output voltage ripple, other capacitors can also be used. TI recommends the output capacitors has a minimum value of 1 µF. With flying capacitors lower than 1 µF, the maximum output power will decrease.

9.2.2.1 Capacitor Selection

To maintain the lowest output resistance, use capacitors with low ESR (see Table 2). The charge-pump output resistance is a function of the ESR of $C_{(fly)}$ and C_O. Therefore, minimizing the ESR of the charge-pump capacitor minimizes the total output resistance. The capacitor values are closely linked to the required output current and the output noise and ripple requirements. It is possible to only use 1-µF capacitors of the same type. Ceramic capacitors will provide the lowest output voltage ripple because they typically have the lowest ESR-rating.

Table 2. Recommended Capacitor Values

DEVICE	V_I [V]	I_O [mA]	C_I [µF]	$C_{(fly)}$ [µF]	C_O [µF]
TPS60400	1.8 to 5.25	60	1	1	1
TPS60401	1.8 to 5.25	60	10	10	10
TPS60402	1.8 to 5.25	60	3.3	3.3	3.3
TPS60403	1.8 to 5.25	60	1	1	1

9.2.2.2 Input Capacitor (C_I)

Bypass the incoming supply to reduce AC impedance and the impact of the TPS6040x-Q1 switching noise. The recommended bypassing depends on the circuit configuration and where the load is connected. When the inverter is loaded from OUT to GND, current from the supply switches between 2 × I_O and zero. Therefore, use a large bypass capacitor (for example, equal to the value of $C_{(fly)}$) if the supply has high AC impedance. When the inverter is loaded from IN to OUT, the circuit draws 2 × I_O constantly, except for short switching spikes. A 0.1-µF bypass capacitor is sufficient.

9.2.2.3 Flying Capacitor ($C_{(fly)}$)

Increasing the flying capacitor's size reduces the output resistance. Small values increases the output resistance. Above a certain point, increasing the capacitance of $C_{(fly)}$ has a negligible effect, because the output resistance becomes dominated by the internal switch resistance and capacitor ESR.

9.2.2.4 Output Capacitor (C_O)

Increasing the output capacitor's size reduces the output ripple voltage. Decreasing its ESR reduces both output resistance and ripple. Smaller capacitance values can be used with light loads if higher output ripple can be tolerated. Use Equation 6 to calculate the peak-to-peak ripple.

$$V_{O(ripple)} = \frac{I_O}{f_{osc} \times C_O} + 2 \times I_O \times ESR_{CO} \tag{6}$$

9.2.2.5 Power Dissipation

As given in *Thermal Information*, the thermal resistance of the unsoldered package is $R_{\theta JA}$ = 221.2°C/W. Soldered on the EVM, a typical thermal resistance of $R_{\theta JA(EVM)}$ = 180°C/W was measured. The terminal resistance can be calculated using Equation 7.

$$R_{\theta JA} = \frac{T_J - T_A}{P_D} \tag{7}$$

where

- T_J is the junction temperature
- T_A is the ambient temperature
- P_D is the power that needs to be dissipated by the device

The maximum power dissipation can be calculated using Equation 8.

$$P_D = V_I \times I_I - V_O \times I_O = V_{I(max)} \times (I_O + I_{(SUPPLY)}) - V_O \times I_O \tag{8}$$

The maximum power dissipation happens with maximum input voltage and maximum output current.

At maximum load the supply current is 0.7 mA maximum (see Equation 9).

$$P_D = 5\ V \times (60\ mA + 0.7\ mA) - 4.4\ V \times 60\ mA = 40\ mW \tag{9}$$

With this maximum rating and the thermal resistance of the device on the EVM, the maximum temperature rise above ambient temperature can be calculated using Equation 10.

$$\Delta T_J = R_{\theta JA} \times P_D = 180°C/W \times 40\ mW = 7.2°C \tag{10}$$

This means that the internal dissipation increases T_J by < 10°C.

The junction temperature of the device shall not exceed 125°C.

This means the device can easily be used at ambient temperatures up to Equation 11.

$$T_A - T_{J(max)} - \Delta T_J - 125°C/W - 10°C = 115°C \tag{11}$$

9.2.3 Application Curves

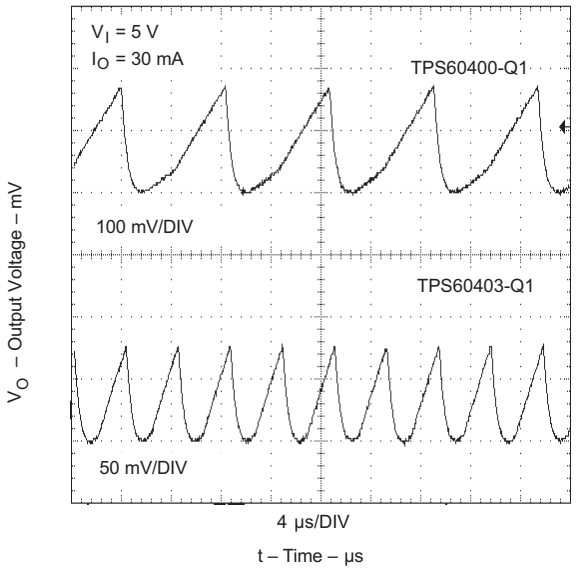


Figure 24. TPS60400-Q1, TPS60403-Q1 Output Voltage vs Time

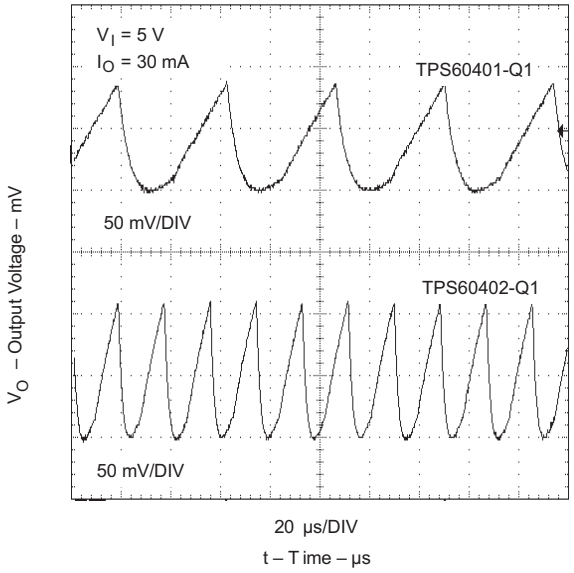


Figure 25. TPS60401-Q1, TPS60402-Q1 Output Voltage vs Time

9.3 System Examples

9.3.1 RC-Post Filter

To reduce the output voltage ripple a RC-post filter can be used (Figure 26).

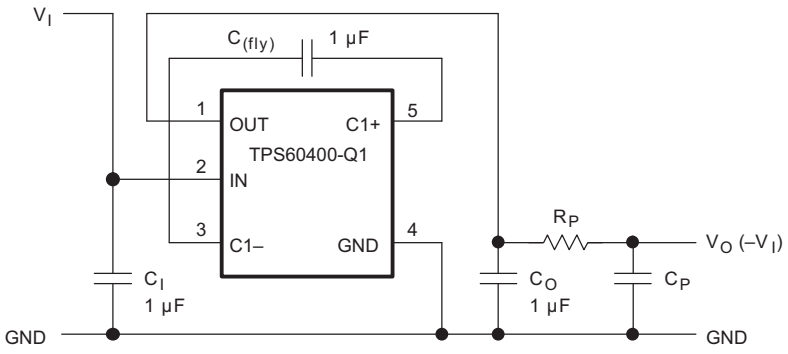


Figure 26. TPS60400 and TPS60401 With RC-Post Filter

An output filter can easily be formed with a resistor (R_P) and a capacitor (C_P). Cutoff frequency is given by Equation 12.

$$f_c = \frac{1}{2\pi R_P C_P} \quad (12)$$

The ratio V_O/V_{OUT} is determined by Equation 13.

System Examples (continued)

$$\left|\frac{V_O}{V_{OUT}}\right| = \frac{1}{\sqrt{1+(2\pi f R_P C_P)^2}}$$

$$\text{with } R_P = 50\ \Omega, C_P = 0.1\ \mu F \text{ and } f = 250\ kHz: \left|\frac{V_O}{V_{OUT}}\right| = 0.125 \quad (13)$$

The formula refers only to the relation between output and input of the ac ripple voltages of the filter.

9.3.2 LC-Post Filter

To reduce the output voltage ripple, an LC-post filter can be used.

Figure 27 shows a configuration with a LC-post filter to further reduce output ripple and noise.

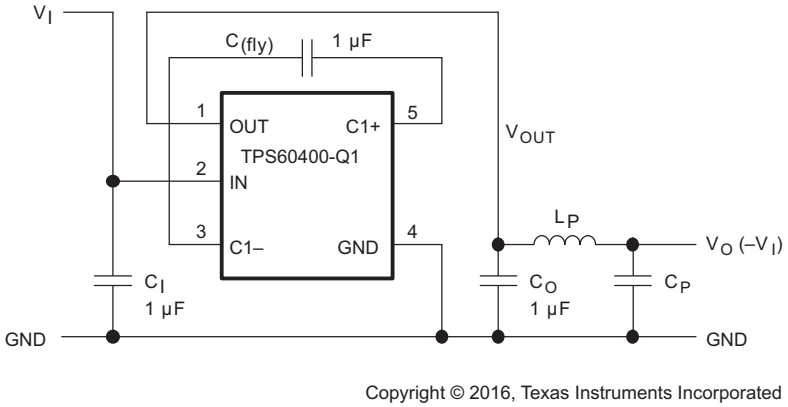


Figure 27. LC-Post Filter

Table 3 contains the typical measurement results using the TPS60400-Q1 device.

Table 3. Measurement Results on the TPS60400-Q1 (Typical)

V_I [V]	$I_{O(2)}$ [mA]	C_I [µF] CERAMIC	$C_{(fly)}$ [µF] CERAMIC	C_O [µF] CERAMIC	L_P [µH]	C_P [µF] CERAMIC	BW = 500 MHz V_{POUT} $V_{P–P}$ [mV]	BW = 20 MHz V_{POUT} $V_{P–P}$ [mV]	V_{POUT} VACeff [mV]
5	60	1	1	1			320	240	65
5	60	1	1	2.2			120	240	32
5	60	1	1	1		0.1 (X7R)	260	200	58
5	60	1	1	1	0.1	0.1 (X7R)	220	200	60
5	60	1	1	2.2	0.1	0.1 (X7R)	120	100	30
5	60	1	1	10	0.1	0.1 (X7R)	50	28	8

9.3.3 Rail Splitter

A switched-capacitor voltage inverter can be configured as a high efficiency rail-splitter. This circuit provides a bipolar power supply that is useful in battery powered systems to supply dual-rail ICs, like operational amplifiers. Moreover, the SOT23-5 package and associated components require very little board space.

The maximum input voltage between V_I and GND in Figure 28 (or between IN and OUT at the device itself) must not exceed 6.5 V.

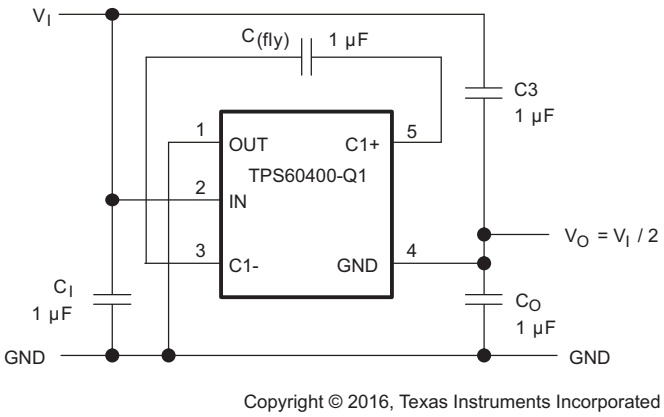


Figure 28. TPS60400 as a High-Efficiency Rail Splitter

After power is applied, the flying capacitor ($C_{(fly)}$) connects alternately across the output capacitors C_3 and C_O. This equalizes the voltage on those capacitors and draws current from V_I to V_O as required to maintain the output at 1/2 V_I.

9.3.4 Combined Doubler/Inverter

The application allows to generate a voltage rail at a level of -Vi as well as 2 x Vi (V(pos)).

In the circuit of Figure 29, capacitors C_I, $C_{(fly)}$, and C_O form the inverter, while C1 and C2 form the doubler. C1 and $C_{(fly)}$ are the flying capacitors; C_O and C2 are the output capacitors. Because both the inverter and doubler use part of the charge-pump circuit, loading either output causes both outputs to decline toward GND. Make sure the sum of the currents drawn from the two outputs does not exceed 60 mA. The maximum output current at $V_{(pos)}$ must not exceed 30 mA. If the negative output is loaded, this current must be further reduced.

$$I_I \approx -I_O + 2 \times I_{O(POS)}$$

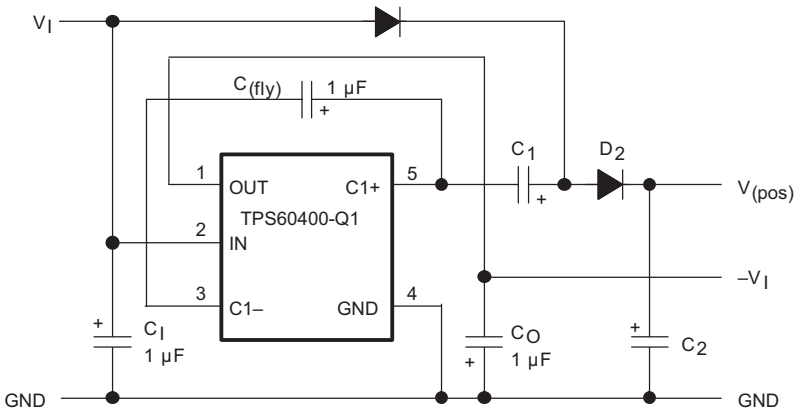


Figure 29. TPS60400-Q1 as Doubler/Inverter

9.3.5 Cascading Devices

Two devices can be cascaded to produce an even larger negative voltage (see Figure 30). The unloaded output voltage is normally −2 × V_I, but this is reduced slightly by the output resistance of the first device multiplied by the quiescent current of the second. When cascading more than two devices, the output resistance rises dramatically.

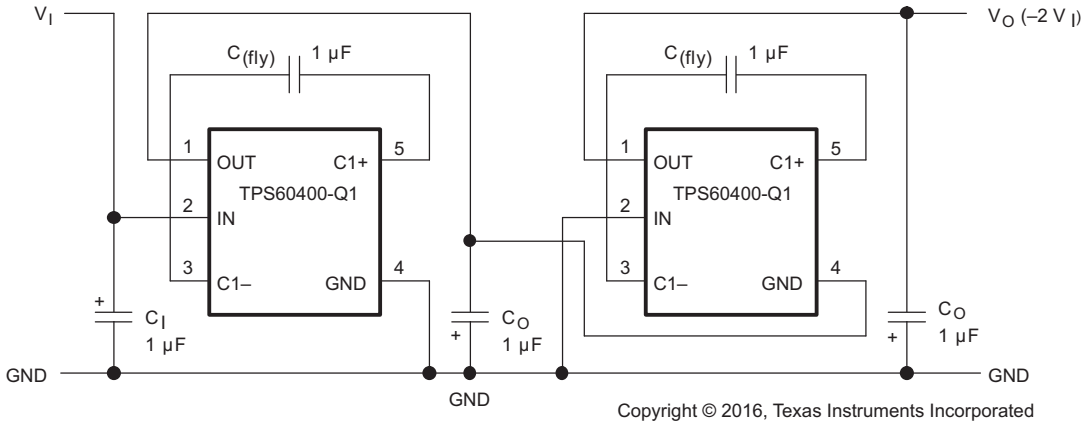


Figure 30. Doubling Inverter

9.3.6 Paralleling Devices

Paralleling multiple TPS6040x-Q1s reduces the output resistance. Each device requires its own flying capacitor ($C_{(fly)}$), but the output capacitor (C_O) serves all devices (see Figure 31). Increase C_O's value by a factor of n, where n is the number of parallel devices. Equation 2 shows the equation for calculating output resistance.

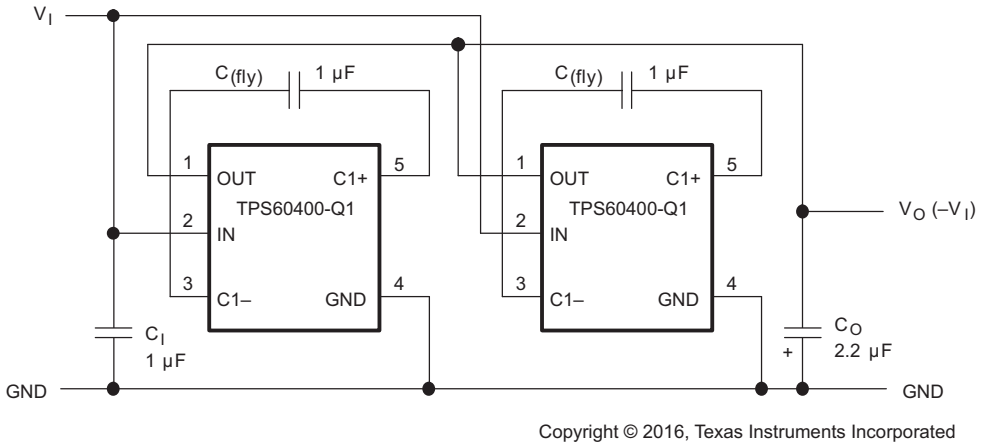


Figure 31. Paralleling Devices

9.3.7 Shutting Down the TPS6040x-Q1

If shutdown is necessary, use the circuit in Figure 32. The output resistance of the TPS6040x-Q1 will typically be 15 Ω plus two times the output resistance of the buffer.

Connecting multiple buffers in parallel can reduce the output resistance of the buffer driving the IN pin.

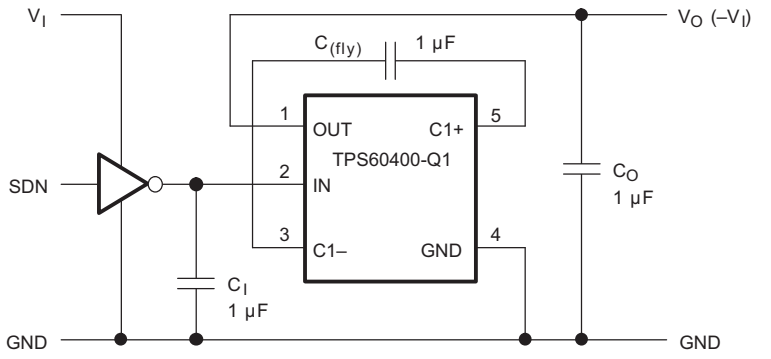


Figure 32. Shutdown Control

9.3.8 GaAs Supply

A solution for a –2.7-V/3-mA GaAs bias supply is proposed in Figure 33. The input voltage of 3.3 V is first inverted with a TPS60403-Q1 and stabilized using a TLV431 low-voltage shunt regulator. Resistor R_P with capacitor C_P is used for filtering the output voltage.

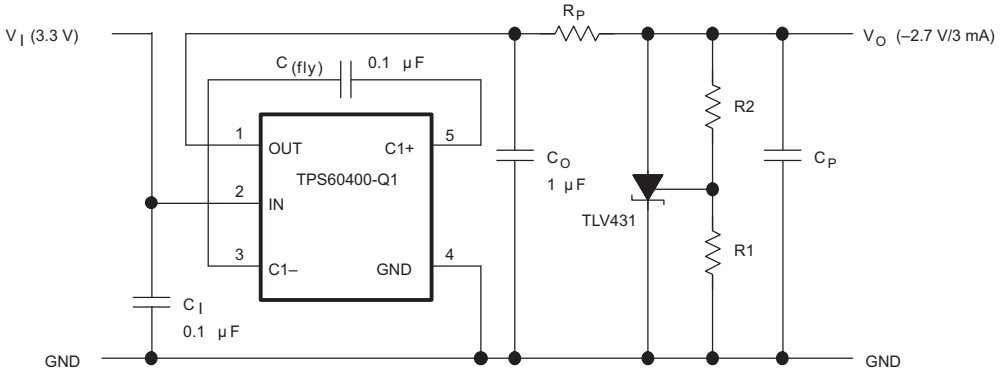


Figure 33. GaAs Supply

A 0.1-µF capacitor was selected for $C_{(fly)}$. By this, the output resistance of the inverter is about 52 Ω.

R_{PMAX} can be calculated using Equation 14.

$$V_O = -\left(1 + \frac{R1}{R2}\right) \times V_{ref} - R1 \times I_{I(ref)} \quad (14)$$

A 100-Ω resistor was selected for R_P.

The reference voltage across R2 is 1.24 V typical. With 5-µA current for the voltage divider, R2 gets Equation 16 to Equation 17.

(15)

$$R_{PMAX} = \left(\frac{V_{CO} - V_O}{I_O} - R_O\right) \quad (16)$$

With: V_{CO} = −3.3 V; V_O = −2.7 V; I_O = −3 mA

R_{PMAX} = 200 Ω − 52 Ω = 148 Ω

With C_P = 1 µF the ratio V_O/V_I of the RC post filter is Equation 18.

$$R2 = \frac{1.24\ V}{5\ \mu A} \approx 250\ k\Omega$$

$$R1 = \frac{2.7 - 1.24\ V}{5\ \mu A} \approx 300\ k\Omega \quad (17)$$

$$\left|\frac{V_O}{V_I}\right| = \frac{1}{\sqrt{1 + (2\pi 125000Hz \times 100\Omega \times 1\mu F)^2}} \approx 0.01 \quad (18)$$

9.3.9 Step-Down Charge Pump

The application generates an output voltage of 1/2 of the input voltage.

By exchanging GND with OUT (connecting the GND pin with OUT and the OUT pin with GND), a step-down charge pump can easily be formed. In the first cycle S1 and S3 are closed, and $C_{(fly)}$ with C_O in series are charged. Assuming the same capacitance, the voltage across $C_{(fly)}$ and C_O is split equally between the capacitors. In the second cycle, S2 and S4 close and both capacitors with $V_I/2$ across are connected in parallel.

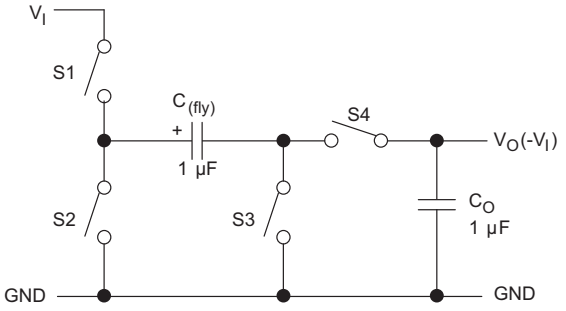


Figure 34. Step-Down Principle

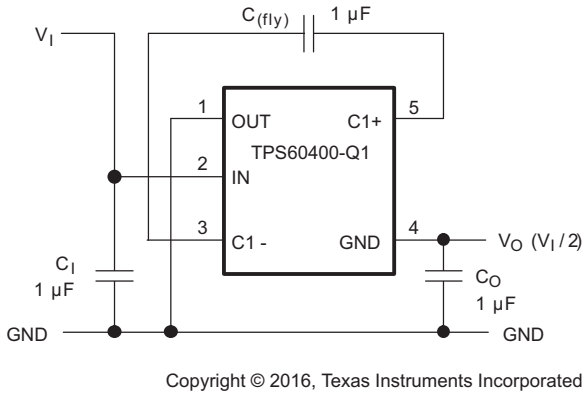


Figure 35. Step-Down Charge Pump Connection

The maximum input voltage between V_I and GND in the schematic (or between IN and OUT at the device itself) must not exceed 5.5 V. For input voltages in the range of 5.5 V to 11 V, an additional Zener-diode is recommended (see Figure 36).

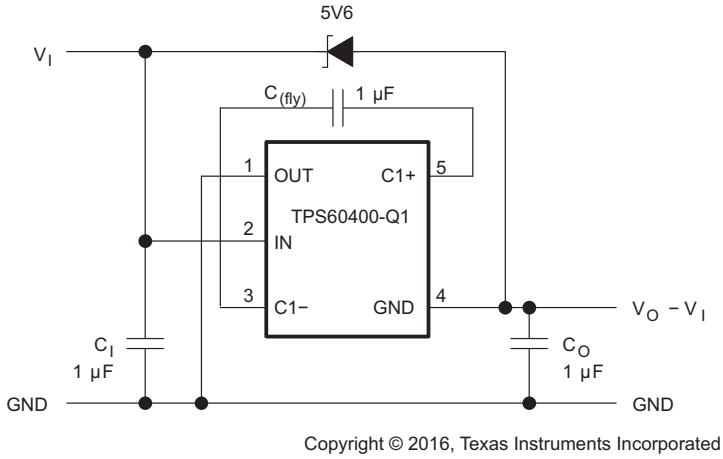


Figure 36. Step-Down Charge Pump Connection With Additional Zener Diode

10 Power Supply Recommendations

The TPS6040x-Q1 device family has no special requirements for its power supply. The power supply output needs to be rated according to the supply voltage, output voltage and output current of the TPS6040x-Q1.

11 Layout

11.1 Layout Guidelines

Figure 37 shows a PCB layout proposal for a single-layer board. Take care to connect all capacitors as close as possible to the device to achieve optimized output voltage ripple performance.

11.2 Layout Example

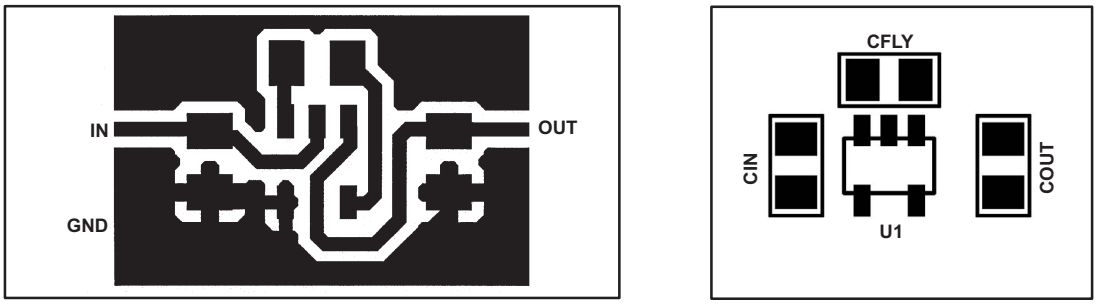


Figure 37. Recommended PCB Layout for TPS6040x-Q1 (Top Layer)

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS60400-Q1	Click here	Click here	Click here	Click here	Click here
TPS60401-Q1	Click here	Click here	Click here	Click here	Click here
TPS60402-Q1	Click here	Click here	Click here	Click here	Click here
TPS60403-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60400QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWP	Samples
TPS60401QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWQ	Samples
TPS60402QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWR	Samples
TPS60403QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AWS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS60400-Q1, TPS60401-Q1, TPS60402-Q1, TPS60403-Q1 :

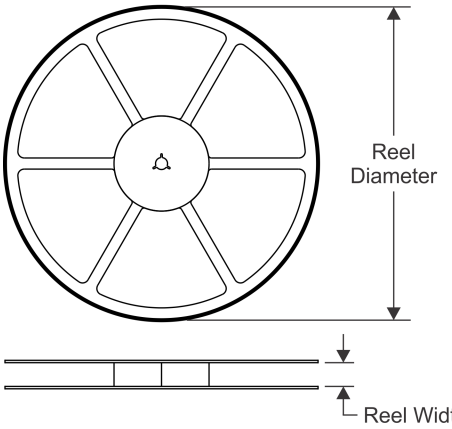
- Catalog : TPS60400, TPS60401, TPS60402, TPS60403

NOTE: Qualified Version Definitions:

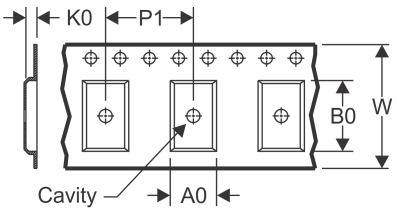
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

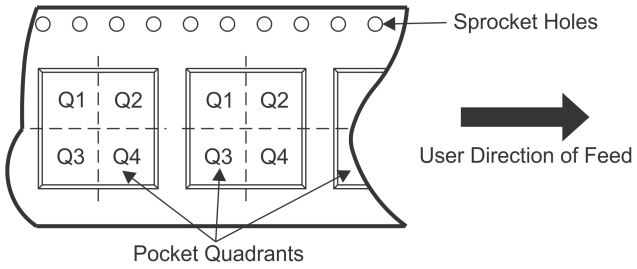


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

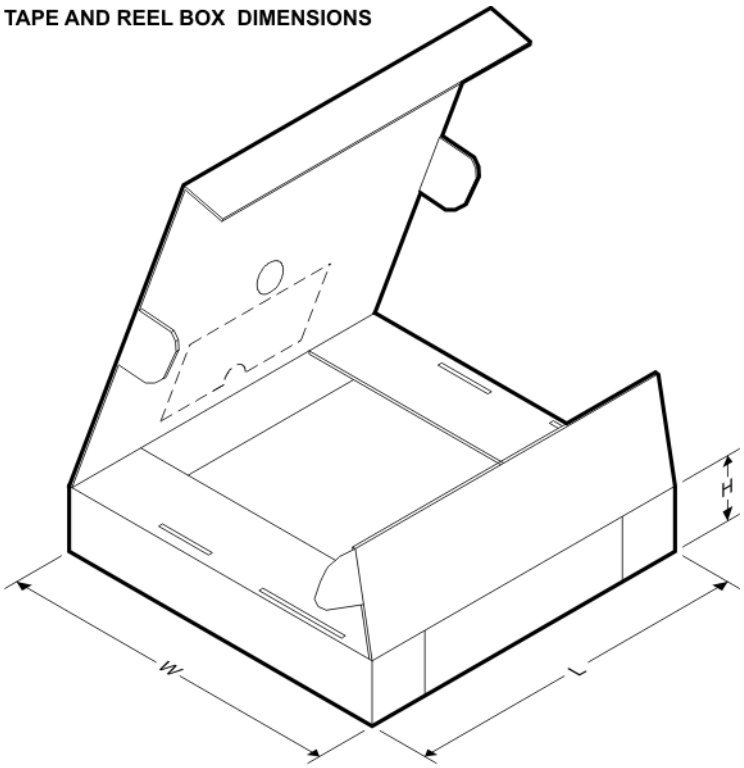
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60400QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS60401QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS60402QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS60403QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

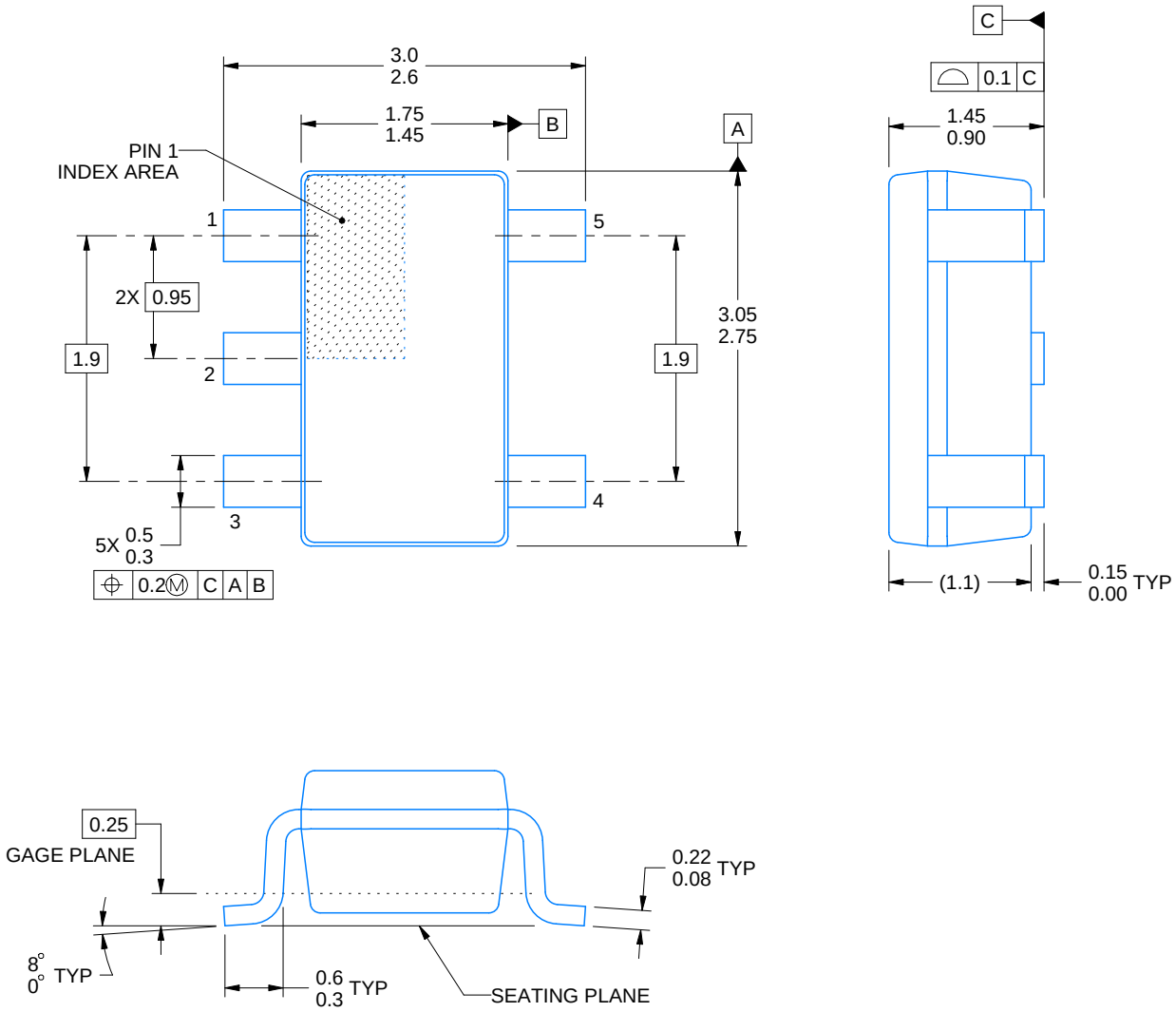
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60400QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS60401QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS60402QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS60403QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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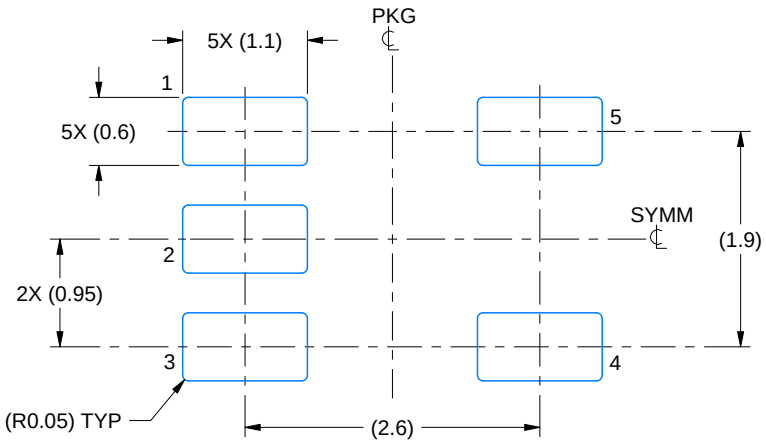
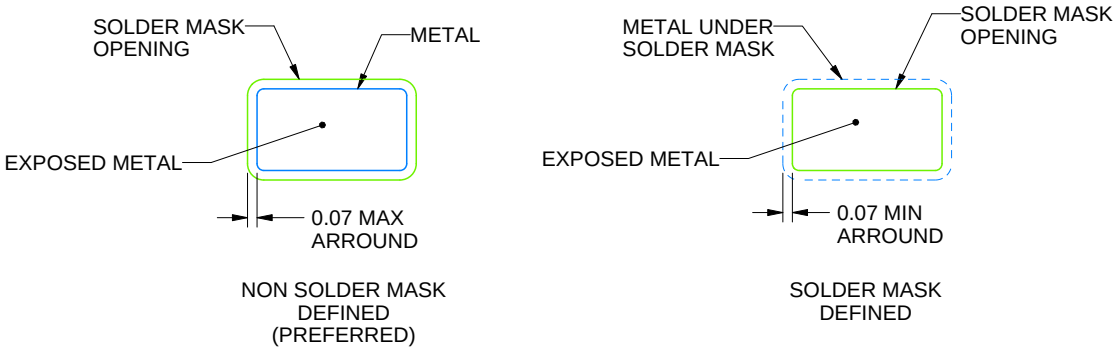
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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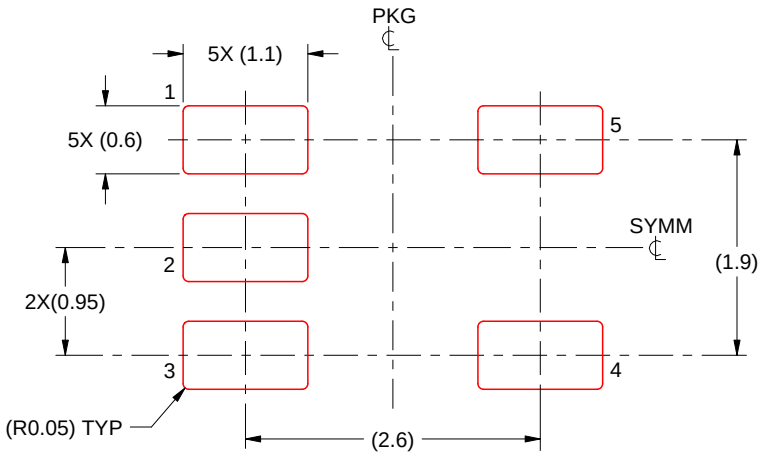
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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