TPS61196-Q1 6-String 400-mA WLED Driver with Independent PWM Dimming For Each String

1 Features

- 8-V to 30-V Input Voltage
- Up to 120-V Output Voltage
- 100-KHz to 800-kHz Programmable Switching Frequency
- Adaptive Boost Output for LED Voltages
- Six Current Sinks, 200-mA Continuous Output, 400-mA Pulse Output for Each String
- ±1.5% Current Matching Between Strings
- High Precision PWM Dimming Resolution up to 5000:1
- Programmable OVP Threshold
- Programmable Input UVLO Threshold
- Adjustable Soft-Start Time
- Built-in LED Open and Short Protection
- Built-in Schottky Diode Open and Short Protection
- Built-in ISET Short Protection
- Built-in IFB Short Protection
- Thermal Shutdown

2 Applications

- Automotive LCD Backlighting
- Automotive Cluster Displays
- Automotive Secondary Displays

3 Description

The TPS61196-Q1 provides a highly integrated solution for automotive LCD backlighting with an independent PWM dimming function for each string. This device is a current mode boost controller driving up to six WLED strings with multiple LEDs in series. Each string has an independent current regulator providing a LED current adjustable from 50 mA to 400 mA within ±1.5% matching accuracy. The minimal voltage at the current sink is programmable in the range of 0.3 V to 1 V to fit with different LED current settings. The input voltage range for the device is from 8 V to 30 V.

The TPS61196-Q1 adjusts the boost controller's output voltage automatically to provide only the voltage required by the LED string with the largest forward voltage drop plus the minimum required voltage at that string's IFB pin, thereby optimizing driver efficiency. Its switching frequency is programmed by an external resistor from 100 kHz to 800 kHz.

The TPS61196-Q1 supports direct PWM brightness dimming. Each string has an independent PWM control input. During the PWM dimming, the LED current is turned on or turned off at the frequency and duty cycle which are determined by the external PWM signal. The PWM frequency ranges from 90 Hz to 22 kHz.

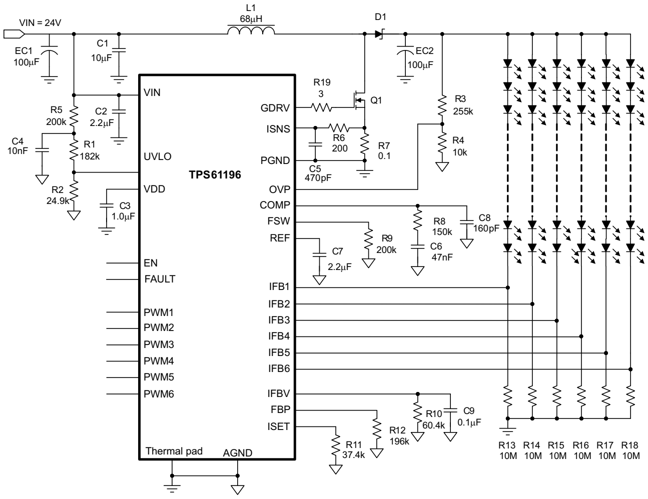
The TPS61196-Q1 integrates overcurrent protection, output short-circuit protection, ISET short-to-ground protection, diode open and short protection, LED open and short protection, and overtemperature shutdown circuit. In addition, the TPS61196-Q1 can detect the IFB pin short to ground to protect the LED string. The device also provides programmable input undervoltage lockout threshold and output overvoltage protection threshold.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61196-Q1	HTSSOP (28)	9.70 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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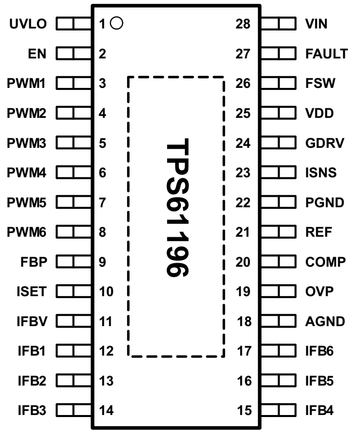
4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

5 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	UVLO	I	Low input voltage lock out. Use a resistor divider from V_{IN} to this pin to set the UVLO threshold.
2	EN	I	Enable and disable pin. EN high = enable, EN low = disable.
3,4,5,6,7,8	PWM1 to PWM6	I	PWM signal input pins. The frequency of PWM signal is in the range of 90 Hz to 22 kHz.
9	FBP	O	LED cross-short protection threshold program pin. Use a resistor to GND to set the threshold.
10	ISET	O	Connecting a resistor to the pin programs the IFB pin current level for full brightness (that is, 100% dimming).
11	IFBV	O	Minimum feedback voltage setting for LED strings.
12,13,14,15,16,17	IFB1 to IFB6	I	Regulated current sink input pins
18	AGND	G	Analog ground
19	OVP	I	Overvoltage protection detection input. Connect a resistor divider from output to this pin to program the OVP threshold.
20	COMP	O	Loop compensation for the boost converter. Connect a RC network to make loop stable.
21	REF	O	Internal reference voltage for the boost converter. Use a capacitor at this pin to adjust the soft start time. When two chips operate in parallel, connect the master's REF pin to the slave's COMP pin.
22	PGND	GND	External MOSFET current sense ground.
23	ISNS	I	External MOSFET current sense positive input.
24	GDRV	O	External switch MOSFET gate driver output.
25	VDD	O	Internal regulator output for device internal power supply. Connect a 1-µF ceramic capacitor to this pin.
26	FSW	O	Switching frequency setting pin. Use a resistor to set the frequency between 100 kHz to 800 kHz. An external input voltage above 3.5 V or below 0.5 V disables the internal clock and makes the device as slave device.
27	FAULT	O	Fault indicator. Open-drain output. Output high impedance when fault conditions happens.
28	VIN	I	Power supply input pin

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage(2)	VIN pin	–0.3	33	V
	FAULT pin	–0.3	V_{IN}	
	FB1 to IFB6 pins	–0.3	40	
	FBP, ISET, ISNS, IFBV pins	–0.3	3.3	
	EN, PWM1 to PWM6 pins	–0.3	20	
	GDRV pins	–0.3	7	
	GDRV 10-ns transient pins	–2	9	
	All other pins	–0.3	7	
Continuous power dissipation		See *Thermal Information*		
Operating junction temperature range		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	8		30	V
V_{OUT}	Output voltage	V_{IN}		120	V
L_1	Inductor	10		100	µH
C_{IN}	Input capacitor	10			µF
C_{OUT}	Output capacitor	22		220	µF
f_{SW}	Boost regulator switching frequency	100		800	kHz
f_{DIM}	PWM dimming frequency	0.09		22	kHz
T_A	Operating ambient temperature	–40		125	°C
T_J	Operating junction temperature	–40		125	°C

(1) Customers need to verify the component value in their application if the values are different from the recommended values.

6.4 Thermal Information

THERMAL METRIC[1]		PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	15.6	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	15.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN}= 24 V, C1 = 10 µF, C2 = 2.2 µF, C3 = 1 µF, EC1 = EC2 = 100 µF; Typical values are at T_A = 25°C, Minimum and Maximum limits are over the operating temperature range (T_A = –40°C to 125°C) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		8		30	V
V_{VIN_UVLO}	Undervoltage lockout threshold	V_{IN} falling		6.5	7	V
V_{VIN_HYS}	V_{IN} UVLO hysteresis			300		mV
I_{q_VIN}	Operating quiescent current into VIN	Device enabled, no switching, V_{IN} = 30 V			2	mA
I_{SD}	Shutdown current	V_{IN} = 12 V, V_{IN} = 30 V			25 50	µA
V_{DD}	Regulation voltage for internal circuit	0 mA < I_{DD} < 15 mA	5.7	6	6.3	V
EN and PWMx						
V_H	Logic high input on EN,PWMx	V_{IN} = 8 V to 30 V	1.8			V
V_L	Logic Low input on EN, PWMx	V_{IN} = 8 V to 30 V			0.8	V
R_{PD}	Pull-down resistance on EN, PWMx		0.8	1.6	3	MΩ
UVLO						
V_{UVLOTH}	Threshold voltage at UVLO pin		1.204	1.229	1.253	V
I_{UVLO}	UVLO input bias current	$V_{UVLO} = V_{UVLOTH}$ – 50 mV $V_{UVLO} = V_{UVLOTH}$ + 50 mV	–0.1 –4.3	 -3.9	0.1 –3.3	µA
SOFT START						
I_{SS}	Soft start charging current	PWM ON, V_{REF}< 2 V PWM ON, V_{REF}> 2 V		200 10		µA
CURRENT REGULATION						
V_{ISET}	ISET pin voltage		1.217	1.229	1.240	V
I_{ISET_P}	ISET short-to-ground protection threshold		120	150	180	µA
K_{ISET}	Current multiple I_{IFB}/I_{ISET}	I_{ISET} = 32.56 µA, V_{IFB} = 0.5 V	3932	3992	4052	
$I_{IFB(AVG)}$	Current accuracy	I_{ISET} = 32.56 µA, V_{IFB} = 0.5 V	127.4	130	132.6	mA
$K_{IFB(M)}$	Current matching; $(I_{FB(MAX)} – I_{FB(MIN)})/2I_{FB(AVG)}$	I_{ISET} = 32.56 µA, V_{IFB} = 0.5 V		0.5%	1.5%	
I_{IFB_LEAK}	IFB pin leakage current at dimming off	IFB voltage < 40 V			1	µA
I_{IFB_max}	Current sink max output current	V_{IFBV} = 350 mV	130			mA

Electrical Characteristics (continued)

V_{IN}= 24 V, C1 = 10 µF, C2 = 2.2 µF, C3 = 1 µF, EC1 = EC2 = 100 µF; Typical values are at T_A = 25°C, Minimum and Maximum limits are over the operating temperature range (T_A = –40°C to 125°C) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IFB REGULATION VOLTAGE						
V_{IFB}	Regulation voltage at IFB	Measured on V_{IFB}(min), other IFB voltages are 0.5 V above V_{IFB}(min). I_{IFB} = 130 mA, V_{IFBV} = 0.5 V		508		mV
I_{IFBV}	IFB Regulation voltage setting sourcing current at IFBV	V_{IFBV} = 0.5 V	0.247	0.25	0.253	I_{ISET}
V_{IFBV}	IFBV voltage setting range		0.3		1	V
BOOST REFERENCE VOLTAGE						
V_{REF}	Reference voltage range for Boost Controller		0		3.1	V
I_{REF_LEAK}	Leakage current at REF pin		–25		25	nA
OSCILLATOR						
f_{SW}	Switching frequency	R_{FSW} = 200 kΩ	187	200	213	kHz
V_{FSW}	FSW pin reference voltage			1.8		V
D_{max}	Maximum duty cycle	f_{SW} = 200 kHz	90%	94%	98%	
$t_{on(min)}$	Minimum pulse width			200		ns
V_{FSW_H}	Logic high input voltage		3.5			V
V_{FSW_L}	Logic low input voltage				0.5	V
ERROR AMPLIFIER						
I_{SINK}	Comp pin sink current	V_{OVP} = V_{REF} + 200 mV, V_{COMP} = 1 V		20		µA
I_{SOURCE}	Comp pin source current	V_{OVP} = V_{REF} – 200 mV, V_{COMP} = 1 V		20		µA
Gm_{EA}	Error amplifier transconductance		90	120	150	µs
R_{EA}	Error amplifier output resistance			20		MΩ
f_{EA}	Error amplifier crossover frequency			1000		kHz
GATE DRIVER						
$R_{GDRV(SRC)}$	Gate driver impedance when sourcing	V_{DD} = 6 V, I_{GDRV} = –20 mA		2	3	Ω
$R_{GDRV(SNK)}$	Gate driver impedance when sinking	V_{DD} = 6 V, I_{GDRV} = 20 mA		1	1.5	Ω
$I_{GDRV(SRC)}$	Gate driver source current	V_{GDRV} = 5 V	200			mA
$I_{GDRV(SNK)}$	Gate driver sink current	V_{GDRV} = 1 V	400			mA
$V_{ISNS(OC)}$	Overcurrent detection threshold	V_{IN} = 8 V to 30 V, T_J = 25°C to 125°C	376	400	424	mV
OVERVOLTAGE PROTECTION (OVP)						
V_{OVPTH}	Output voltage OVP threshold		2.95	3.02	3.09	V
I_{OVP}	Leakage current		–100	0	100	nA
V_{IFB_OVP}	IFBx over voltage threshold	PWM ON		38		V
LED SHORT DETECTION						
I_{FBP}	LED short detection sourcing current	V_{FBP} = 1 V	0.247	0.25	0.253	I_{ISET}
FAULT INDICATOR						
I_{FAULT_H}	Leakage current in high impedance	V_{FAULT} = 24 V		1		nA
I_{FAULT_L}	Sink current at low output	V_{FAULT} = 1 V	1	2		mA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			150		°C
T_{hys}	Thermal shutdown threshold hysteresis			15		°C

6.6 Typical Characteristics

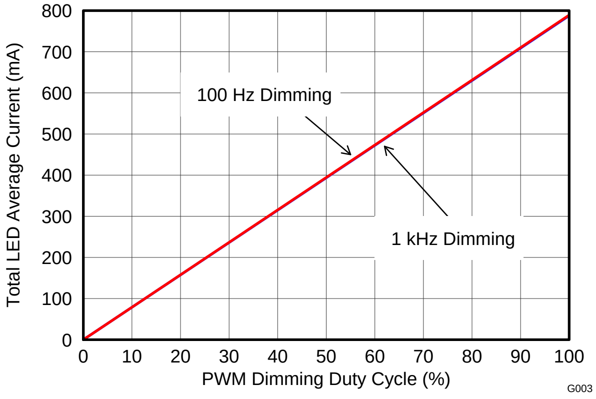


Figure 1. Dimming Linearity

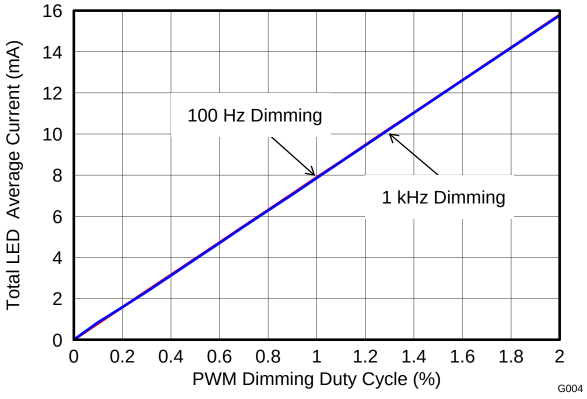


Figure 2. Dimming Linearity At Low Dimming Duty Cycle

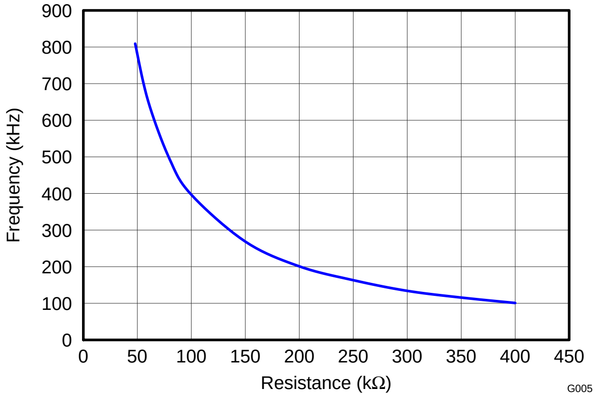


Figure 3. Switching Frequency Setting

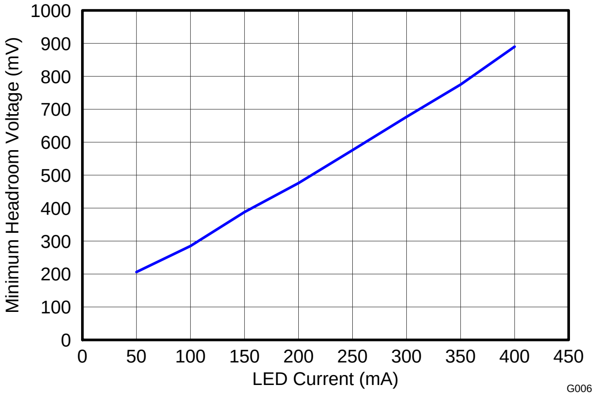


Figure 4. Recommended Minimum Headroom Voltage

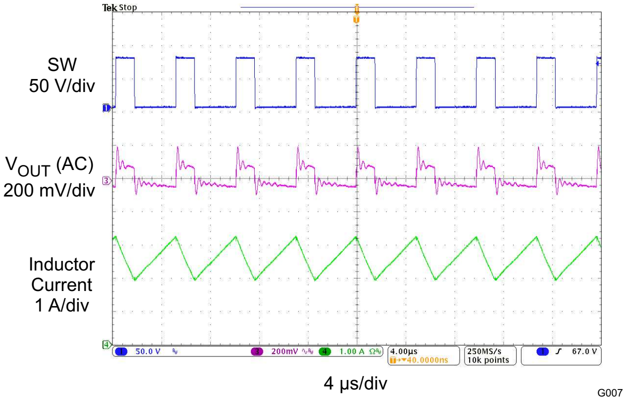


Figure 5. Boost Switching Waveform

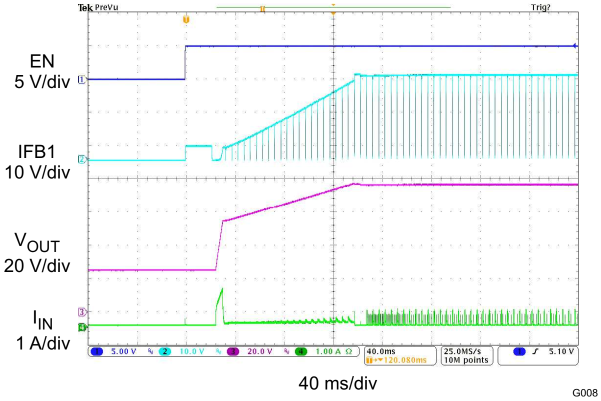


Figure 6. Start-up Waveform (1% Dimming)

Typical Characteristics (continued)

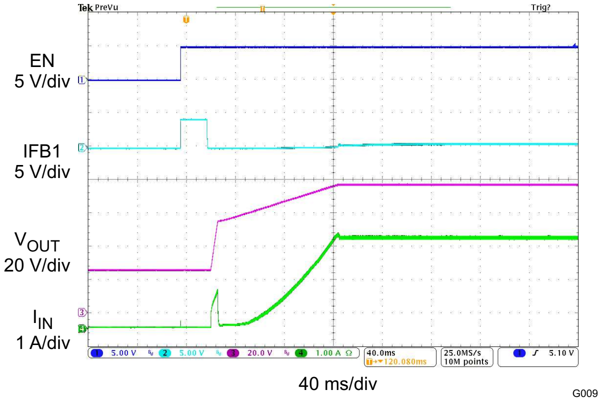


Figure 7. Start-up Waveform (100% Dimming)

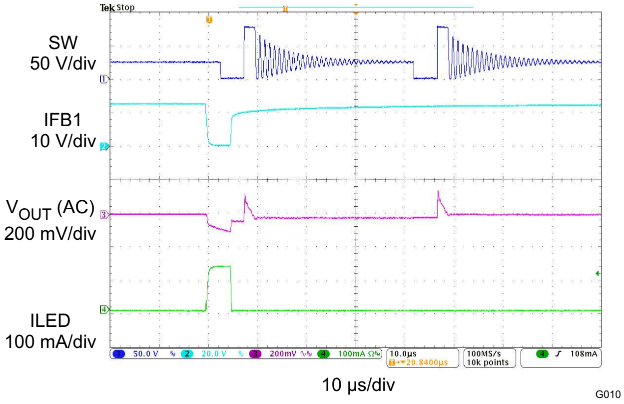


Figure 8. Dimming Waveform (0.1% Dimming)

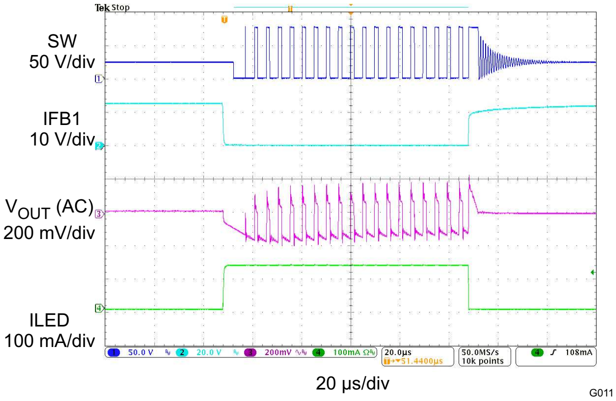


Figure 9. Dimming Waveform (2% Dimming)

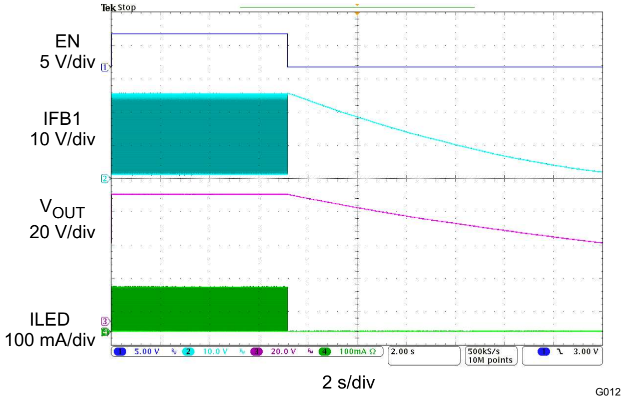


Figure 10. Shutdown Waveform (1% Dimming)

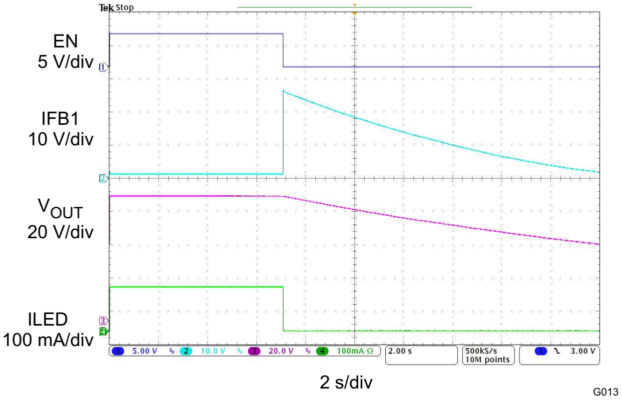


Figure 11. Shutdown Waveform (100% Dimming)

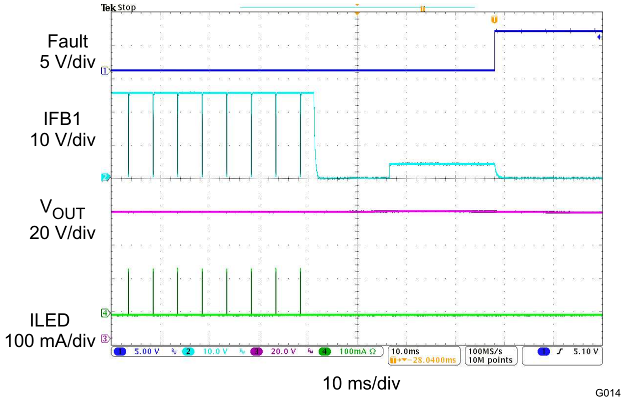


Figure 12. LED Open Protection (1% Dimming)

Typical Characteristics (continued)

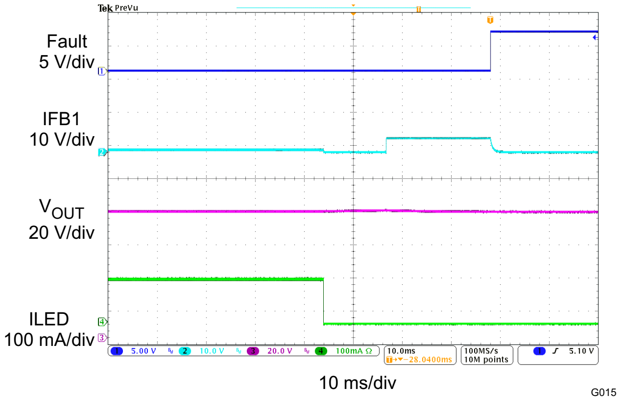


Figure 13. LED Open Protection (100% Dimming)

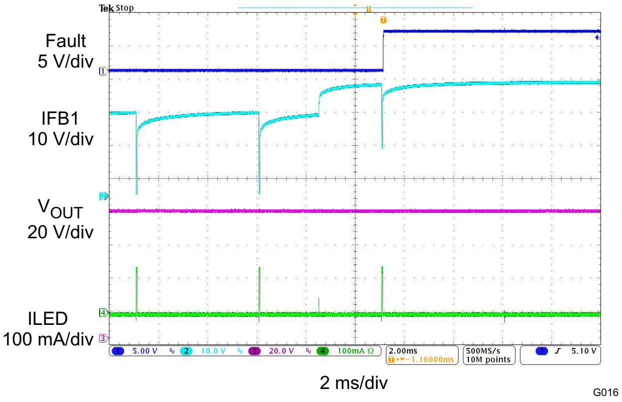


Figure 14. LED Short Protection (1% Dimming)

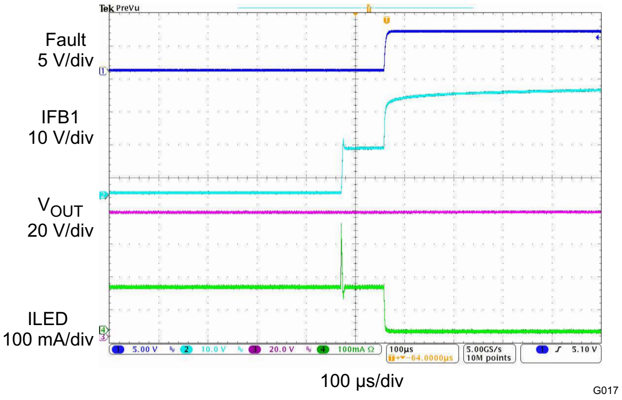


Figure 15. LED Short Protection (100% Dimming)

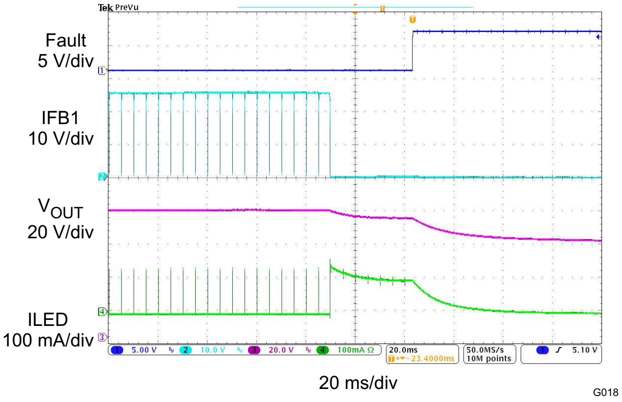


Figure 16. IFB Short To Ground Protection (1% Dimming)

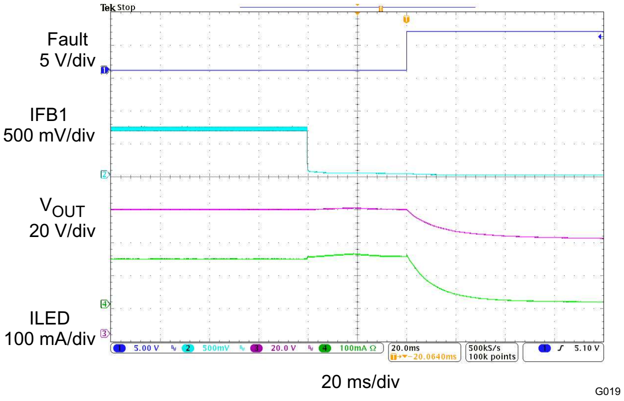


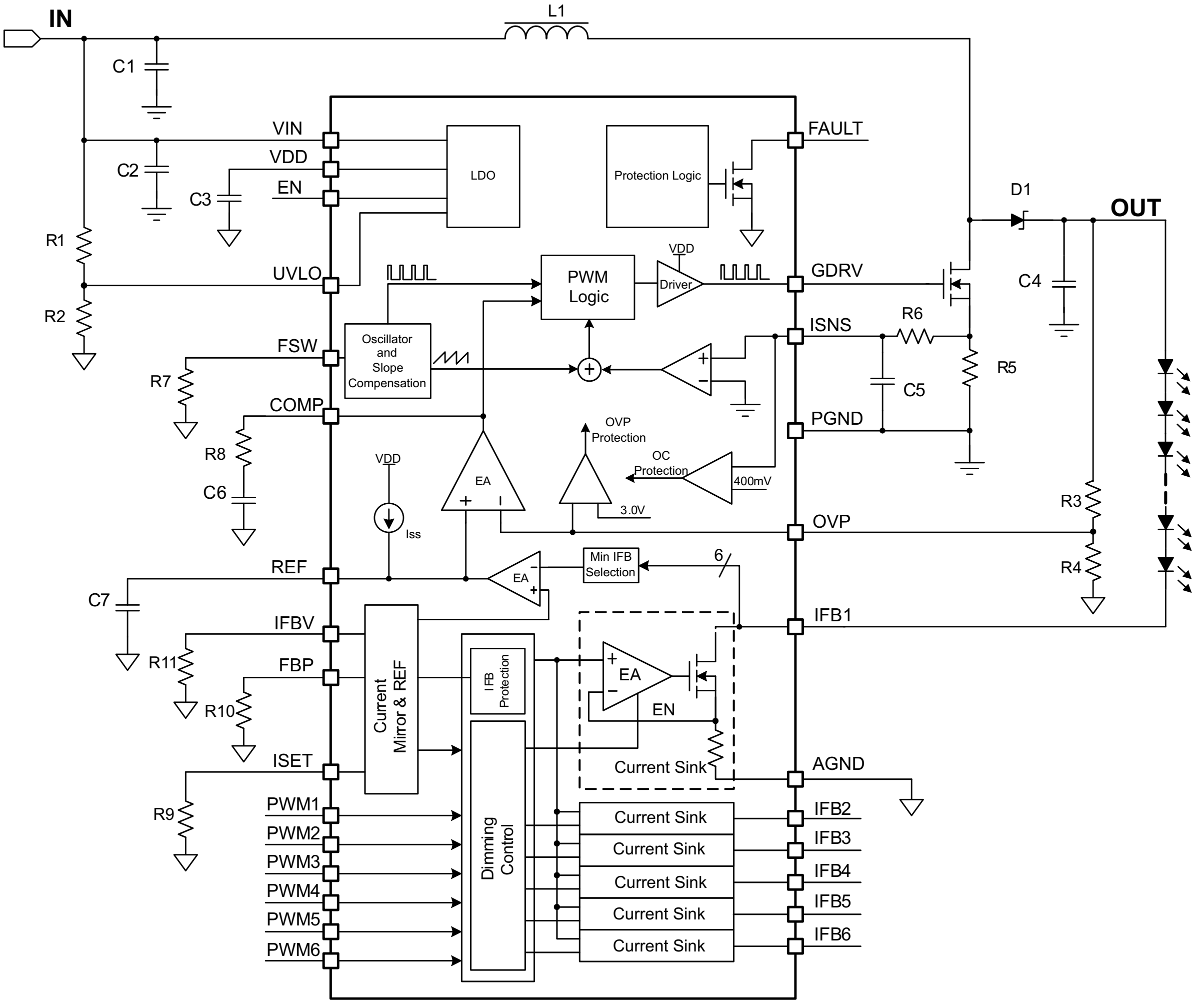
Figure 17. IFB Short-To-Ground Protection (100% Dimming)

7 Detailed Description

7.1 Overview

The TPS61196-Q1 provides a highly integrated solution for automotive LCD backlight with an independent PWM dimming function for each string. This device is a current mode boost controller driving up to six WLED strings with multiple LEDs in series. Each string has an independent current regulator providing a LED current adjustable from 50 mA to 400 mA within ±1.5% matching accuracy. The minimal voltage at the current sink is programmable in the range of 0.3 V to 1 V to fit with different LED current settings. The input voltage range for the device is from 8 V to 30 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Supply Voltage

The TPS61196-Q1 has a built-in linear regulator to supply the device analog and logic circuitry. The VDD pin, output of the regulator, must be connected to a 1-µF bypass capacitor. VDD only has a current sourcing capability of 15 mA. VDD voltage is ready after the EN pin is pulled high.

7.3.2 Boost Controller

The TPS61196-Q1 regulates the output voltage with current mode pulse width modulation (PWM) control. The control circuitry turns on an external switch FET at the beginning of each switching cycle. The input voltage is applied across the inductor and stores the energy as the inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current rises to the threshold set by the Error Amplifier (EA) output, the switch FET is turned off and the external Schottky diode is forward biased. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats each switching cycle. The switching frequency is programmed by an external resistor.

A ramp signal from the oscillator is added to the current ramp to provide slope compensation, shown in the *Functional Block Diagram*. The duty cycle of the converter is then determined by the PWM Logic block which compares the EA output and the slope compensated current ramp. The feedback loop regulates the OVP pin to a reference voltage generated by the minimum voltage across the IFB pins. The output of the EA is connected to the COMP pin. An external RC compensation network must be connected to the COMP pin to optimize the feedback loop for stability and transient response.

The TPS61196-Q1 consistently adjusts the boost output voltage to account for any changes in LED forward voltages. In the event that the boost controller is not able to regulate the output voltage due to the minimum pulse width ($t_{on(min)}$ in the *Electrical Characteristics*), the TPS61196-Q1 enters pulse skip mode. In this mode, the device keeps the power switch off for several switching cycles to prevent the output voltage from rising above the regulated voltage. This operation typically occurs in light load condition or when the input voltage is higher than the output voltage.

7.3.3 Switching Frequency

The switching frequency is programmed between 100 kHz to 800 kHz by an external resistor (R9 in the *Simplified Schematic*). To determine the resistance by a given frequency, use the curve in Figure 3 or calculate the resistance value by Equation 1. Table 1 shows the recommended resistance values for some switching frequencies.

$$f_{SW} = \frac{40000}{R9}(\text{kHz}) \quad (1)$$

Table 1. Recommended Resistance Values For Switching Frequencies

R9	f_{SW}
400 kΩ	100 kHz
200 kΩ	200 kHz
100 kΩ	400 kHz
80 kΩ	500 kHz
48 kΩ	800 kHz

7.3.4 Enable and Undervoltage Lockout

The TPS61196-Q1 is enabled with the soft start-up when the EN pin voltage is higher than 1.8 V. A voltage of less than 1 V disables the device.

An undervoltage lockout (UVLO) protection feature is provided. When the voltage at the VIN pin is less than 6.5 V, the device is powered off. The TPS61196-Q1 resumes the operation once the voltage at the VIN pin recovers above the hysteresis (V_{VIN_HYS}) more than the UVLO threshold of input falling voltage. If a higher UVLO voltage is required, use the UVLO pin as shown in Figure 18 to adjust the input UVLO threshold by using an external resistor divider. Once the voltage at the UVLO pin exceeds the 1.229-V threshold, the device is powered on, and a hysteresis current source of 3.9 µA is added. When the voltage at the UVLO pin drops lower than 1.229 V, the current source is removed. The resistors of R1, R2, and R5 can be calculated by Equation 2 from required V_{START} and V_{STOP}. To avoid noise coupling, the resistor divider R1 and R2 must be close to the UVLO pin. Placing a filter capacitor of more than 10 nF as shown in Figure 18 can eliminate the impact of the switching ripple and improve the noise immunity.

If the UVLO function is not used, pull up the UVLO pin to the VDD pin.

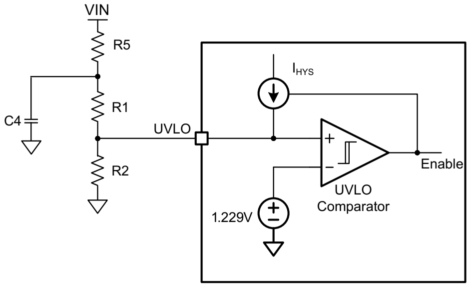


Figure 18. Undervoltage Lockout Circuit

$$R1 + R5 = \frac{V_{START} - V_{STOP}}{I_{HYS}}$$

$$R2 = (R1 + R5) \times \frac{1.229V}{V_{START} - 1.229V}$$

where

- I_{HYS} is 3.9 µA sourcing current from the UVLO pin. (2)

When the UVLO condition happens, the FAULT pin outputs high impedance. As long as the UVLO condition removes, the FAULT pin outputs low impedance.

7.3.5 Power-Up Sequencing and Soft Start-up

The input voltage, UVLO pin voltage, EN input signal and the input dimming PWM signal control the power up of the TPS61196-Q1. After the input voltage is above the required minimal input voltage of 7.5 V, the internal circuit is ready to be powered up. After the UVLO pin is above the threshold of 1.229 V and the EN signal is high, the internal LDO and logic circuit are activated. The device outputs a 20-ms pulse to detect the unused channels and remove them from the control loop. When any PWM dimming signal is high, the soft start-up begins. If the PWM dimming signals come before the EN signal is high, the soft start-up begins immediately after the detection of unused channels.

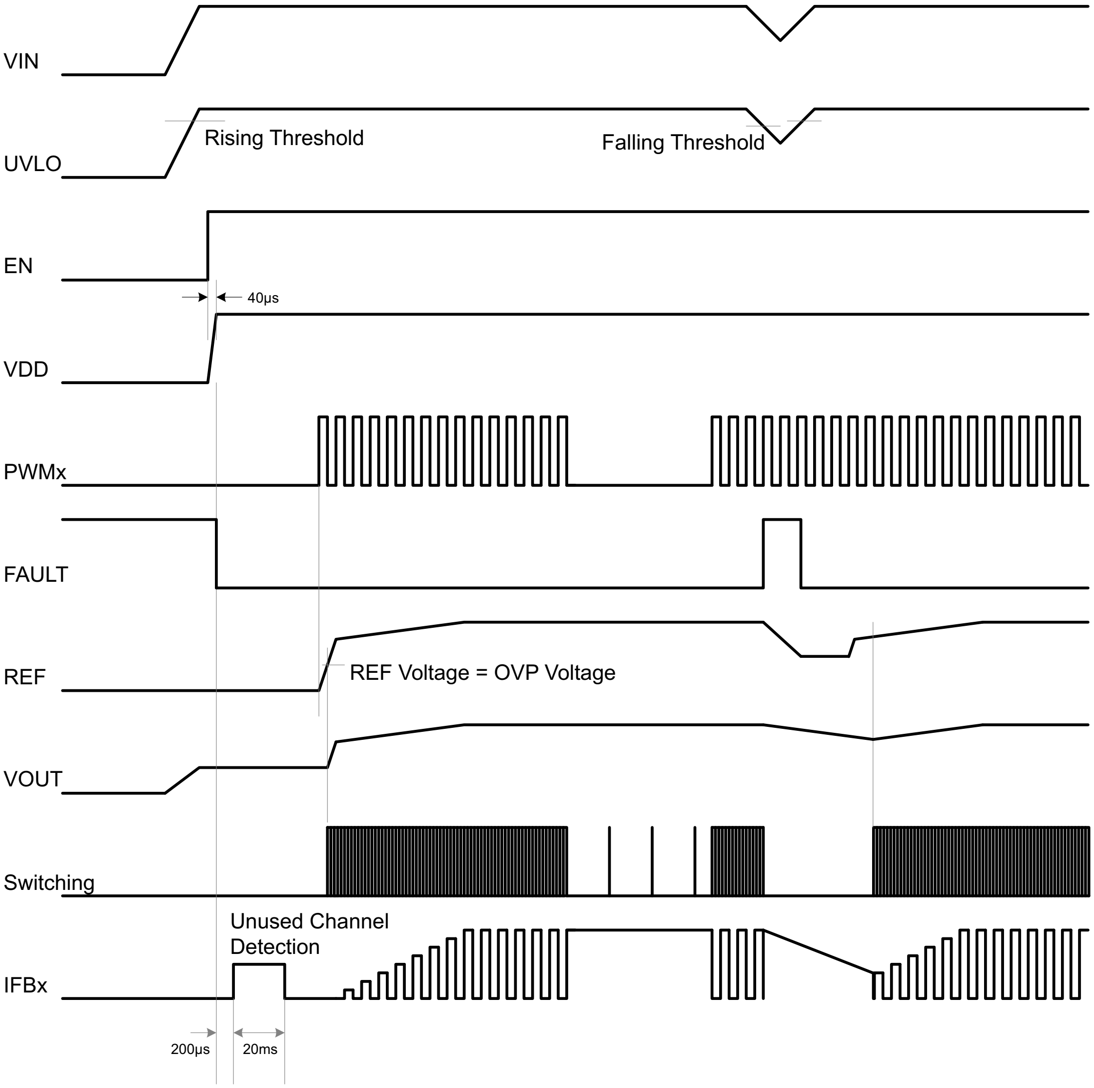


Figure 19. Power-Up Sequencing

The TPS61196-Q1 has integrated the soft-start circuitry working with an external capacitor at the REF pin to avoid inrush current during start-up. During the start-up period, the capacitor at the REF pin is charged with a soft-start current source. When the REF pin voltage is higher than the output feedback voltage at the OVP pin, the boost controller starts switching and the output voltage starts to ramp up. At the same time, the LED current sink starts to drive the LED strings. At the beginning of the soft start, the charge current is 200 µA. Once the voltage of the REF pin exceeds 2 V, the charge current changes to 10 µA and continues to charge the capacitor. When the current sinks are driving the LED strings, the IFB voltages are monitored. When the minimum IFB voltage is above 200 mV less than the setting voltage at the IFBV pin, the charge current is stopped, and the soft start-up is finished. The TPS61196-Q1 enters normal operation to regulate the minimum IFB voltage to the required voltage set by the resistor at the IFBV pin. The total soft start time is determined by the external capacitance. The capacitance must be within 1 µF to 4.7 µF for different start-up time and different output voltage.

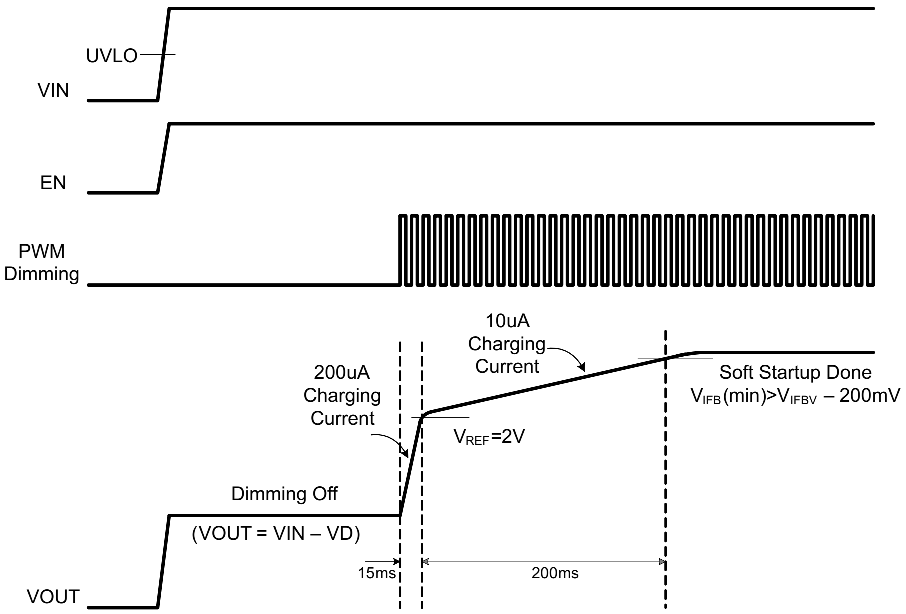


Figure 20. Soft-Start Waveforms

7.3.6 Unused Led String

If the application requires less than six LED strings, the TPS61196-Q1 simply requires connecting the unused IFB pin to ground through a resistor between 20 kΩ and 36 kΩ. Once the device is turned on, the TPS61196-Q1 uses a 60-µA current source to detect the IFB pin voltage. If the IFB voltage is between 1 V and 2.5 V, the device immediately disables this string during start-up.

7.3.7 Current Regulation

The six channel current sink regulators can be configured to provide up to 400 mA per string. The expected LED current is programmed by a resistor (R11 in the *Simplified Schematic*) at the ISET using Equation 3.

$$I_{LED} = \frac{V_{ISET}}{R11} \times K_{ISET}$$

where

- V_{ISET} is the ISET pin voltage of 1.229 V
- K_{ISET} is the current multiple of 3992. (3)

To sink the set LED current, the current sink regulator requires a minimum headroom voltage at the IFB pins for working properly. For example, when the LED current is set to 130 mA, the minimum voltage required at the IFB pin must be higher than 0.35 V. For other LED currents, refer to Figure 4 for recommended minimum headroom voltage required. The TPS61196-Q1 regulates the minimum voltage of the IFB pins to the IFBV voltage. The IFBV voltage is adjustable with an external resistor (R10 in the *Simplified Schematic*) at the IFBV pin. After choosing the minimum IFB voltage, the IFBV voltage must be set to this value and the setting resistance can be calculated by Equation 4.

$$V_{IFBV} = \frac{R10}{R11} \times 307.3(mV) \quad (4)$$

If a large LED current is set, the headroom voltage is required higher. This leads to more heat on the device. To maintain the total power dissipation in the range of the package limit, normally all strings can not sink large current in continuous mode but pulse mode.

7.3.8 PWM Dimming

LED brightness dimming is set by applying an external PWM signal of 90 Hz to 22 kHz to the PWM pins. Each LED string has an independent PWM input. Varying the PWM duty cycle from 0% to 100% adjusts the LED from minimum to maximum brightness respectively. The recommended minimum on time of the LED string is 10 µsec. Thus, the device has a minimum dimming duty cycle of 500:1 at 200 Hz.

When all PWM voltages are pulled low during dimming off, the TPS61196-Q1 turns off the LED strings and keeps the boost converter running at PFM mode. The output voltage is kept at the level which is a little bit lower than that when PWM is high. Thus, the device limits the output ripple due to the load transient that occurs during PWM dimming.

When all PWM voltages are pulled low for more than 20 ms, to avoid the REF pin voltage dropping due to the leakage current, the voltage of the REF pin is held by an internal reference voltage which equals to the REF pin voltage in normal dimming operation. Thus, the output voltage will be kept at the same level as the normal output voltage.

Since the output voltage in long time dimming off status is almost the same as the normal voltage for turning the LED on, the TPS61196-Q1 turns on the LED very fast without any flicker when recovering from long time dimming off to small duty cycle dimming on.

7.4 Device Functional Modes

7.4.1 Protections

The TPS61196-Q1 has a full set of protections making the system safe to any abnormal conditions. Some protections will latch the TPS61196-Q1 in off state until its power supply is recycled or it is disabled and then enabled again. In latch off state, the REF pin voltage is discharged to 0 V.

7.4.1.1 Switch Current Limit Protection Using the ISNS Pin

The TPS61196-Q1 monitors the inductor current through the voltage across a sense resistor (R7 in the *Simplified Schematic*) in order to provide current limit protection. During the switch FET on period, when the voltage at the ISNS pin rises above 400 mV (V_{ISNS} in the *Electrical Characteristics* table), the TPS61196-Q1 turns off the FET immediately and does not turn it back on until the next switch cycle. The switch current limit is equal to 400 mV / R7.

7.4.1.2 LED Open Protection

When one of the LED strings is open, the voltage at the IFB pin connecting to this LED string drops to zero during dimming-on time. The TPS61196-Q1 monitors the IFB voltage for 20 ms. If the IFB voltage is still below the threshold of 0.2 V, the current sink is disabled and an internal pull-up current is activated to detect the IFB voltage again. If the IFB voltage is pulled up to a high voltage, this LED string is recognized as LED open. As a result, the device deactivates the open IFB pin and removes it from the voltage feedback loop. Afterwards, the output voltage returns to the voltage required for the connected LED strings. The IFB pin currents of the connected strings remain in regulation during this process. If all the LED strings are open, the TPS61196-Q1 is latched off.

7.4.1.3 LED Short-Cross Protection Using the FBP Pin

If one or several LEDs short in one string, the corresponding IFB pin voltage rises but continues to sink the LED current, causing increased device power dissipation. To protect the device, the TPS61196-Q1 provides a programmable LED short-across protection feature by properly sizing the resistor on the FBP pin (R12 in the *Simplified Schematic*) using Equation 5.

$$V_{LED\_SHORT} = \frac{R12}{R11} \times 1.229V \tag{5}$$

If any IFB pin voltage exceeds the threshold (V_{LED_SHORT}), the device turns off the corresponding current sink and removes this IFB pin from the output voltage regulation loop. Current regulation of the remaining IFB pins is not affected.

Device Functional Modes (continued)

7.4.1.4 Schottky Diode Open Protection

When the device is powered on, it checks the topology connection first. After the TPS61196-Q1 delays 400 µs, it checks the voltage at the OVP pin to see if the Schottky diode is not connected or the boost output is hard-shorted to ground. If the voltage at the OVP pin is lower than 70 mV, the TPS61196-Q1 is locked in off state until the input power is recycled or it is enabled again.

7.4.1.5 Schottky Diode Short Protection

If the rectifier Schottky diode is shorted, the reverse current from output capacitor to ground is very large when the switcher MOSFET is turned on. Because the current mode control topology has a minimum edge blanking time to immunize against the spike current through the switcher, if the parasite inductance between the output capacitor through the switcher to ground is zero, the external MOSFET will be damaged in this short period due to the huge power dissipation in this case. But with a small parasite inductance, the power dissipation is limited. The boost converter works in minimum pulse width in this situation due to cycle by cycle over-current protection. The output voltage drops and the all-string-open protection is triggered because of the low voltage at all IFB pins. The TPS61196-Q1 is latched off.

7.4.1.6 IFB Overvoltage Protection During Start-up

When any of IFB pins reaches the threshold (V_{OVP_IFB}) of 38 V during start-up, the device stops switching and stays in latch-off immediately to protect from damage. In latch-off state, the REF pin voltage is discharged.

7.4.1.7 Output Overvoltage Protection Using the OVP Pin

Use a resistor divider to program the maximum output voltage of the boost converter. To ensure the LED string can be turned on with setting current, the maximum output voltage must be higher than the forward voltage drop of the LED string. The maximum required voltage can be calculated by multiplying the maximum LED forward voltage ($V_{FWD(max)}$) and number (n) of series LEDs , and adding extra 1 V to account for regulation and resistor tolerances and load transients.

The recommended bottom feedback resistor of the resistor divider (R4 in the *Simplified Schematic*) is 10 kΩ. Calculate the top resistor (R3 in the *Simplified Schematic*) using Equation 6, where V_{OVP} is the maximum output voltage of the boost converter.

$$R3 = \left(\frac{V_{OVP}}{3.02} - 1 \right) \times R4 \tag{6}$$

When the device detects that the voltage at the OVP pin exceeds overvoltage protection threshold of 3.02 V, indicating that the output voltage has exceeded the clamp threshold voltage, the TPS61196-Q1 clamps the output voltage to the set threshold. When the OVP pin voltage does not drop from the OVP threshold for more than 500 ms, the device is latched off until the input power or the EN pin voltage is re-cycled.

7.4.1.8 Output Short-to-Ground Protection

When the inductor peak current reaches twice the switch current limit in each switching cycle, the device immediately disables the boost controller until the fault is cleared. This protects the device and external components from damage if the output is shorted to ground.

7.4.1.9 IFB Short-to-Ground Protection

The IFB pin short to ground makes the LED current uncontrollable if there is no protection. If the device tries to increase the boost converter’s output voltage to lift the IFB voltage, it will make the situation worse and the LED string may be burned due to the high current. The TPS61196-Q1 implements a protection mechanism to protect the LED string in this failure mode.

If the IFB is short to ground before the TPS61196-Q1 is turned on, the device detects the IFB voltage by sourcing a 60 µA current during start-up. If the IFB voltage is less than 0.4 V during start-up, the start-up stops and the device outputs fault indication so as to protect the LED string during start-up.

Device Functional Modes (continued)

When a LED feedback pin is shorted to ground during normal operation, the device first turns off this LED string for a very short time and detects the IFB voltage again. If the IFB voltage is lower than 1.8 V, it sources a 60-µA current and detects the IFB voltage again in off state. If the IFB voltage is still less than 1.8 V, this means the IFB pin is shorted to ground. The boost converter is turned off and the REF voltage is discharged to ground to protect the LED string.

7.4.1.10 ISET Short-to-Ground Protection

The TPS61196-Q1 monitors the ISET pin voltage when the device is enabled. When the sourcing current from the ISET pin is larger than a threshold of 150 µA, the device disables the current sink because the ISET pin may be short to ground or the current setting resistor is too small. Once the current sourcing from the ISET pin recovers to the normal value, the current sink resumes working.

7.4.1.11 Thermal Protection

When the device junction temperature is over 150°C, the thermal protection circuit is triggered and shuts down the device immediately. The device automatically restarts when the junction temperature falls back to less than 135°C, with approximate 15°C hysteresis.

Table 2. Protection List

PROTECTION ITEM	RESULT	FAULT	LATCH OFF / RETRY
Diode open	Cannot start up	Y	Latch off
Diode short	Output voltage low	Y	Latch off
LED string open	LED string off	Y	LED string latch off
LED string short during start-up	IFB OVP	Y	Latch off
LEDshort	LED string off	Y	LED string latch off
IFB short to GND	Boost off	Y	Latch off
ISET short to GND	All LED strings off	Y	Retry
All LED strings open during start-up	VOUT OVP	Y	Latch off
Input voltage UVLO	Boost off	Y	Retry
Thermal shutdown	Shutdown	Y	Retry

7.4.2 Indication For Fault Conditions

The TPS61196-Q1 has an open-drain fault indicator pin to indicate abnormal conditions. When the device is operating normally, the voltage at the FAULT pin is low. When any fault condition happens, it is in high impedance, which can be pulled to high level through an external resistor. The FAULT pin can indicate following conditions:

- Overvoltage condition at the OVP or the IFB pin
- LED short and open
- IFB short to ground
- ISET short to ground
- Diode open and short
- Output short circuit
- Overtemperature

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When more LED strings are required in the application, the TPS61196-Q1 can work in master/slave mode. The TPS61196-Q1 can be set as slave device when the voltage at the FSW pin is below 0.5 V or above 3.5 V. The master TPS61196-Q1 has booster controller and outputs the power rail for all LED strings. The slave TPS61196-Q1 only works as a LED driver and feedbacks the required headroom voltage to the master by connecting the slave's COMP pin to the master's REF pin. The ISNS pin of the slave TPS61196-Q1 must be connected to ground. The slave's OVP pin voltage must be 3% higher than the voltage at the master's OVP pin. The slave device can combine all fault conditions happening on both master and slave devices by connecting the master's FAULT output to the FSW pin of the slave device. The slave's FAULT pin outputs the indication signal for all fault conditions.

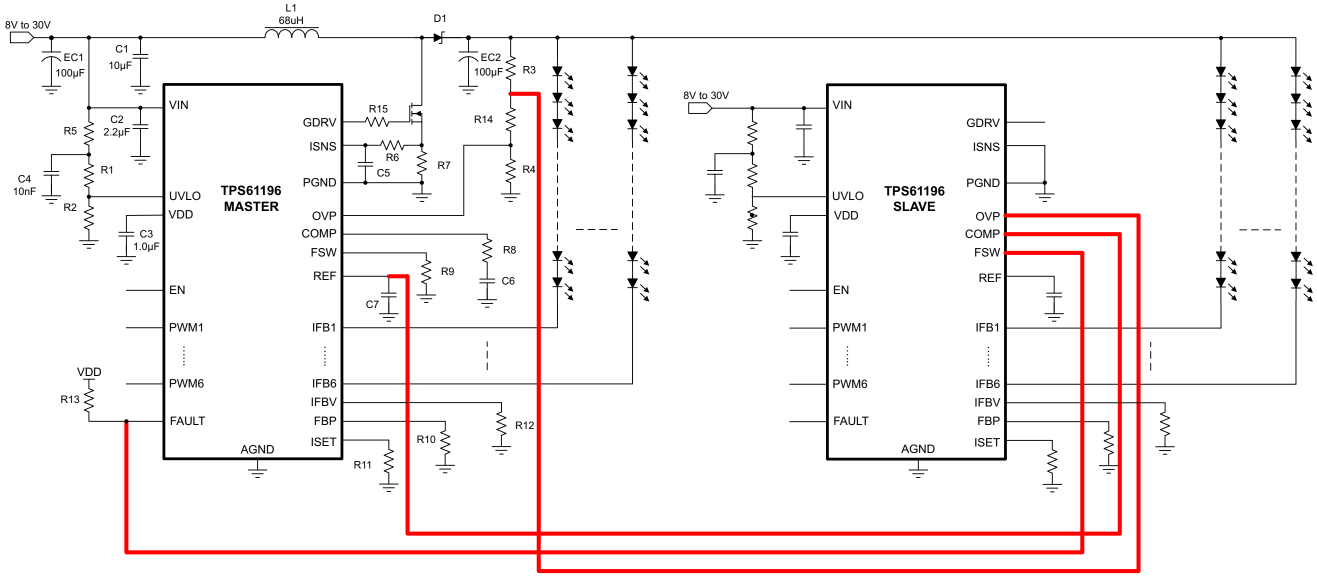


Figure 21. Multi-Chip Operation In Parallel

8.2 Typical Application

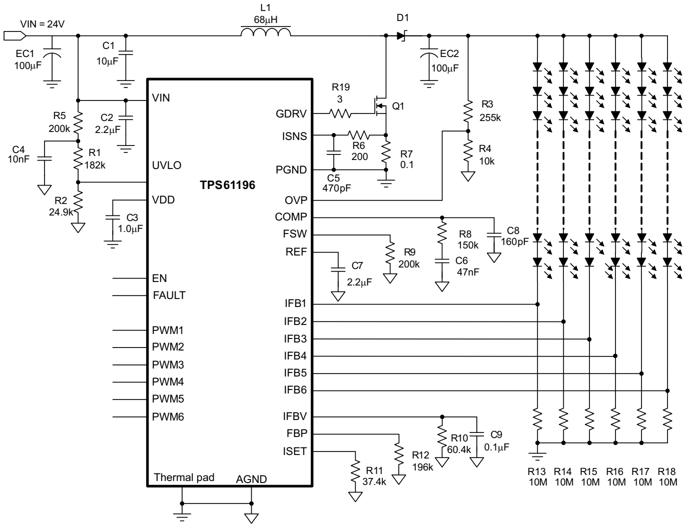


Figure 22. TPS61196-Q1 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 V to 16 V
Number of LED strings x number of LEDs per string	6 x 12
Forward voltage of LED string	36 V
LED string current	70 mA per channel
Switching frequency	200 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

The inductor is the most important component in switching power regulator design because it affects power supply steady state operation, transient behavior, and loop stability. The inductor value, DC resistance (DCR), and saturation current are important specifications to be considered for better performance. Although the boost power stage can be designed to operate in discontinuous mode at maximum load, where the inductor current ramps down to zero during each switching cycle, most applications will be more efficient if the power stage operates in continuous conduction mode, where a DC current flows through the inductor. Therefore, the Equation 8 and Equation 9 below are for CCM operation only. The TPS61196-Q1 is designed to work with inductor values between 10 µH and 100 µH, depending on the switching frequency. Running the controller at higher switching frequencies allows the use of smaller and/or lower profile inductors in the 10-µH range. Running the controller at slower switching frequencies requires the use of larger inductors, near 100 µH, to maintain the same inductor current ripple but may improve overall efficiency due to smaller switching losses. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation.

In a boost regulator, the inductor DC current can be calculated with Equation 7.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

where

- V_{OUT} = boost output voltage
- I_{OUT} = boost output current

- V_{IN} = boost input voltage
- η = power conversion efficiency, use 95% for TPS61196-Q1 applications (7)

The inductor current peak-to-peak ripple can be calculated with Equation 8.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times f_{SW} \times V_{OUT}}$$

where

- $\Delta I_{L(P\text{-}P)}$ = inductor ripple current
- L = inductor value
- f_{SW} = switching frequency
- V_{OUT} = boost output voltage
- V_{IN} = boost input voltage (8)

Therefore, the inductor peak current is calculated with Equation 9.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \tag{9}$$

Select an inductor, which saturation current is higher than calculated peak current. To calculate the worst-case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the switch FET and power diode. Besides the external switch FET, the overall efficiency is also affected by the inductor DCR. Usually the lower DC resistance shows higher efficiency. However, there is a trade-off between DCR and the inductor footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones.

8.2.2.2 Schottky Diode

The TPS61196-Q1 demands a high-speed rectification for optimum efficiency. Ensure that the diode's average and peak current rating exceed the output LED current and inductor peak current. In addition, the diode's reverse breakdown voltage must exceed the application output voltage.

8.2.2.3 Switch MOSFET And Gate Driver Resistor

The TPS61196-Q1 demands a power N-MOSFET (see Q1 in the *Figure 22*) as a switch. The voltage and current rating of the MOSFET must be higher than the application output voltage and the inductor peak current. The applications benefit from the addition of a resistor (See R19 in the *Figure 22*) connected between the GDRV pin and the gate of the switch MOSFET. With this resistor, the gate driving current is limited and the EMI performance is improved. A 3-Ω resistor value is recommended. The device exhibits lower efficiency when the resistor value is above 3 Ω due to the more switching loss of the external MOSFET.

8.2.2.4 Current Sense and Current Sense Filtering

R7 determines the correct overcurrent limit protection. To choose the right value of R7, start with the total system power needed P_{OUT}, and calculate the input current I_{IN} by Equation 7. Efficiency can be estimated between 90% to 95%. The second step is to calculate the inductor peak current based on the inductor value L using Equation 8 and Equation 9. The maximum R7 can now be calculated as R7(max) = V_{ISNS} / $I_{L(P)}$. It is recommended to add 20% or more margins to account for component variations. A small filter placed on the ISNS pin improves performance of the converter (See R6 and C5 in *Simplified Schematic*). The time constant of this filter should be approximately 100 ns. The range of R6 should be from about 100 Ω to 1 kΩ for best results. The C5 should be located as close as possible to the ISNS pin to provide noise immunity.

8.2.2.5 Output Capacitor

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability of the whole system. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$V_{RIPPLE(C)} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times C_{OUT}}$$

where

- V_{RIPPLE} is the peak-to-peak output voltage ripple
- D_{MAX} is the duty cycle of the boost converter. (10)

D_{MAX} is approximately equal to ($V_{OUT(MAX)}$ – $V_{IN(MIN)}$) / $V_{OUT(MAX)}$) in applications. Care must be taken when evaluating a capacitor's derating under DC bias. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance.

The ESR impact on the output ripple must be considered as well if tantalum or aluminum electrolytic capacitors are used. Assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the V_{RIPPLE} is: $V_{RIPPLE(ESR)} = I_{L(P)} \times ESR$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internally to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. Therefore, high ripple current type electrolytic capacitor with small ESR is used in typical application as shown in *Simplified Schematic*.

In the typical application, the output requires a capacitor in the range of 22 µF to 220 µF. The output capacitor affects the small signal control loop stability of the boost converter. If the output capacitor is below the range, the boost regulator may potentially become unstable.

8.2.2.6 Loop Consideration

The COMP pin on the TPS61196-Q1 is used for external compensation, allowing the loop response to be optimized for each application. The COMP pin is the output of the internal trans-conductance amplifier. The external resistor R8, along with ceramic capacitors C6 and C8 (see in *Simplified Schematic*), are connected to the COMP pin to provide poles and zero. The poles and zero, along with the inherent pole and zero in a peak current mode control boost converter, determine the closed loop frequency response. This is important to converter stability and transient response.

The first step is to calculate the pole and the right half plane zero of the peak current mode boost converter by Equation 11 and Equation 12.

$$f_P = \frac{2I_{OUT}}{2\pi V_{OUT} \times C_{OUT}} \tag{11}$$

$$f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi L \times I_{OUT}} \tag{12}$$

To make the loop stable, the loop must have sufficient phase margin at the crossover frequency where the loop gain is 1. To avoid the effect of the right half plane zero on the loop stability, choose the crossover frequency less than 1/5 of the f_{ZRHP}. Then calculate the compensation components by Equation 13 and Equation 14.

$$R8 = \frac{R7 \times 2\pi f_{co} \times C_{OUT}}{(1-D) \times Gm_{EA}} \times \frac{V_{OVP}}{V_{OVPTH}}$$

where

- V_{OVPTH} = 3.02 V which is the internal reference for the output overvoltage-protection setting voltage.
- Gm_{EA} is the trans-conductance of the error amplifier. Its typical value is 120 µS.
- f_{CO} is the crossover frequency, which normally is less than 1/5 of the f_{ZRHP} (13)

$$C6 = \frac{1}{2\pi f_P \times R8}$$

where

- f_P is the pole's frequency of the power stage calculated by Equation 11 (14)

If the output cap is the electrolytic capacitor, which may have large ESR, a capacitor is required to cancel the zero of the output capacitor. Equation 15 calculates the value of this capacitor.

$$C8 = \frac{C_{OUT} \times R_{ESR}}{R8} \tag{15}$$

8.2.3 Application Curves

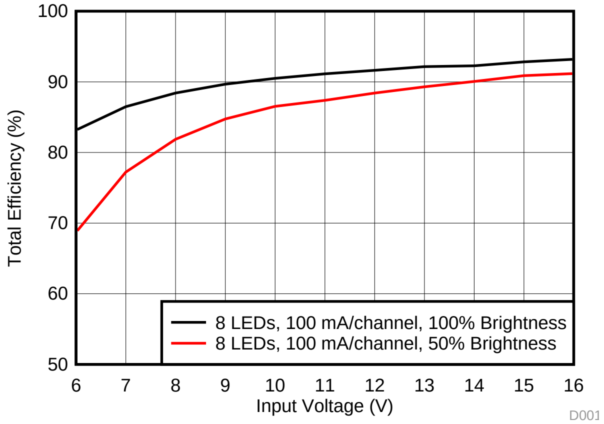


Figure 23. Efficiency vs Input Voltage (8 LEDs)

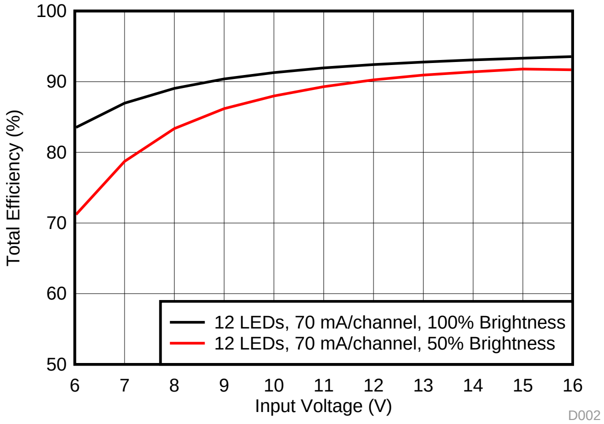


Figure 24. Efficiency vs Input Voltage (12 LEDs)

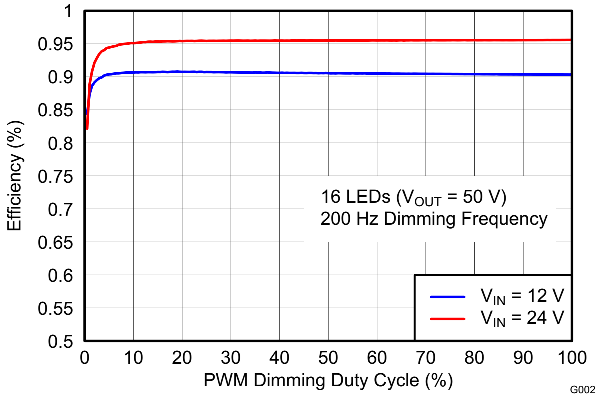


Figure 25. Efficiency (16 LEDs)

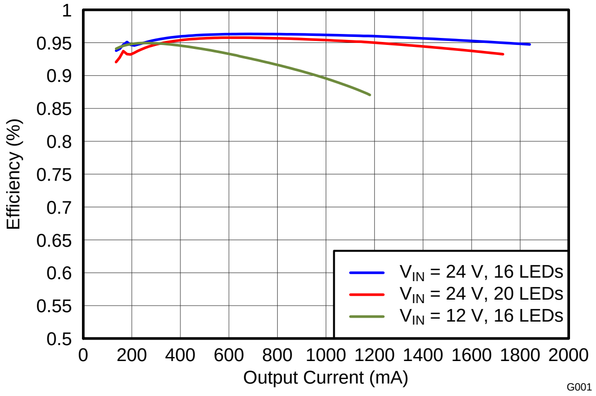


Figure 26. DC Load Efficiency

9 Power Supply Recommendations

The TPS61196-Q1 requires a single supply input voltage. This voltage can range between 8 V to 30 V and be able to supply enough current for a given application.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The VDD capacitor, C3 (see *Figure 22*) is the filter and noise decoupling capacitor for the internal linear regulator powering the internal digital circuits. It should be placed as close as possible between the VDD and PGND pins to prevent any noise insertion to digital circuits. The switch node at the drain of Q1 carries high current with fast rising and falling edges. Therefore, the connection between this node to the inductor and the Schottky diode should be kept as short and wide as possible. It is also beneficial to have the ground of the capacitor C3 close to the ground of the current sense resistor R7 since there is large driving current flowing between them. The ground of output capacitor EC2 should be kept close to input power ground or through a large ground plane because of the large ripple current returning to the input ground. When laying out signal grounds, it is recommended to use short traces separate from power ground traces and connect them together at a single point, for example on the thermal pad in the PWP package. Resistors R3, R4, R9, R10, R11, and R12 (see *Figure 22*) are setting resistors for switching frequency, LED current, protection threshold and feedback voltage programming. To avoid unexpected noise coupling into the pins and affecting the accuracy, these resistors need to be close to the pins with short and wide traces to GND. In the PWP package, the thermal pad needs to be soldered to the large ground plane on the PCB for better thermal performance. Additional thermal via can significantly improve power dissipation of the device.

10.2 Layout Example

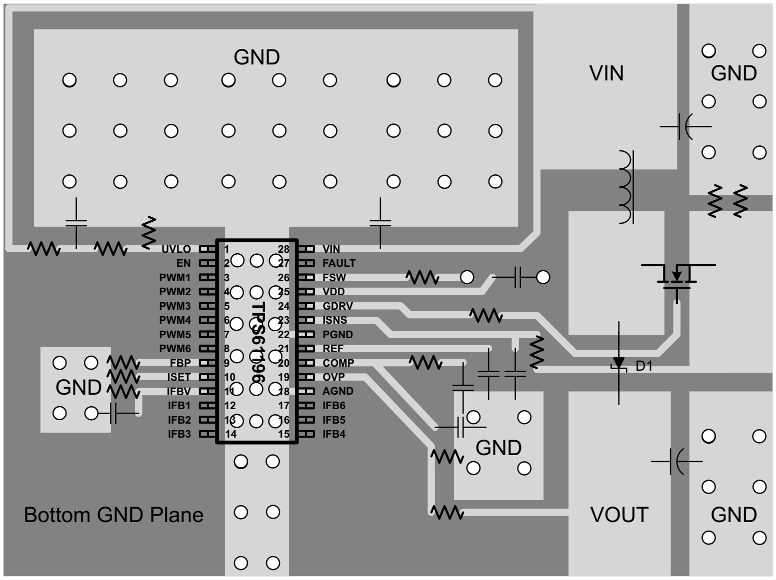


Figure 27. Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61196PWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS61196Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS61196-Q1 :

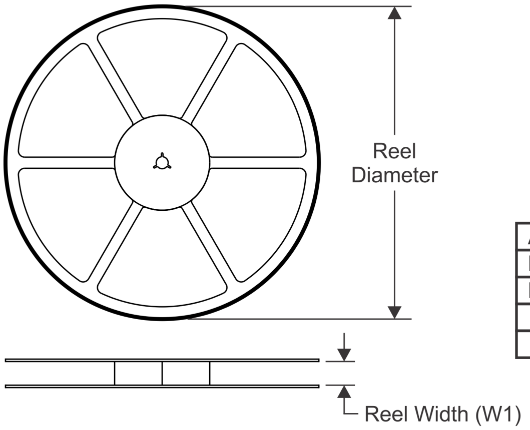
- Catalog: TPS61196

NOTE: Qualified Version Definitions:

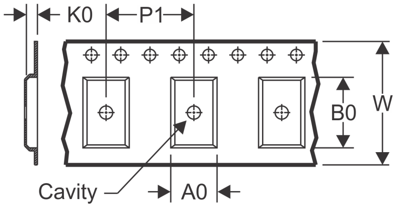
  - Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

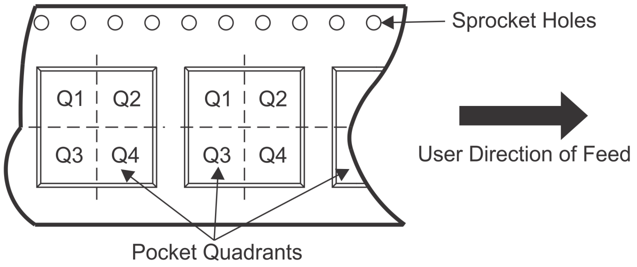


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

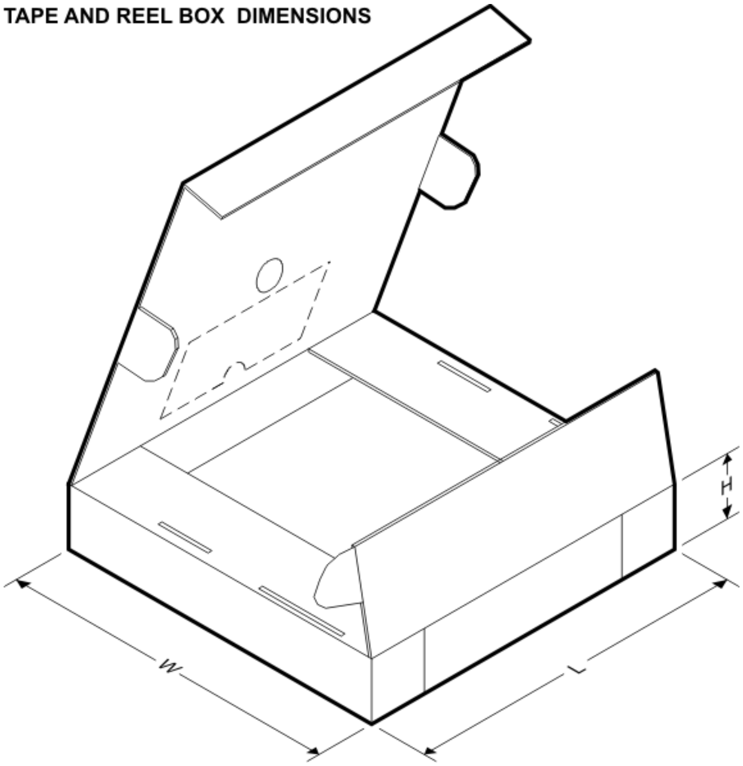
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61196PWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61196PWPRQ1	HTSSOP	PWP	28	2000	367.0	367.0	38.0

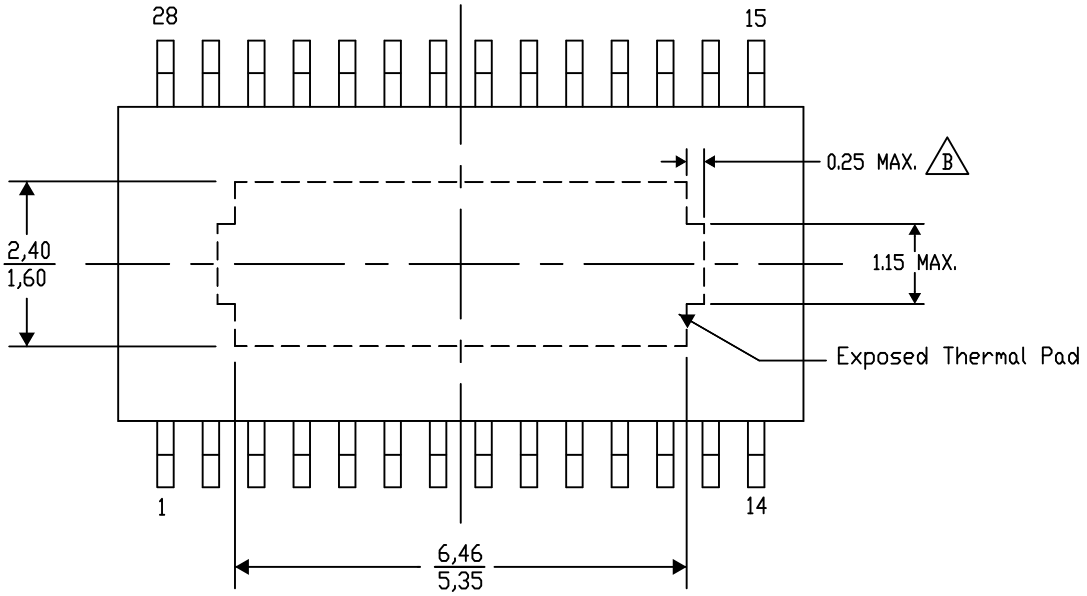
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

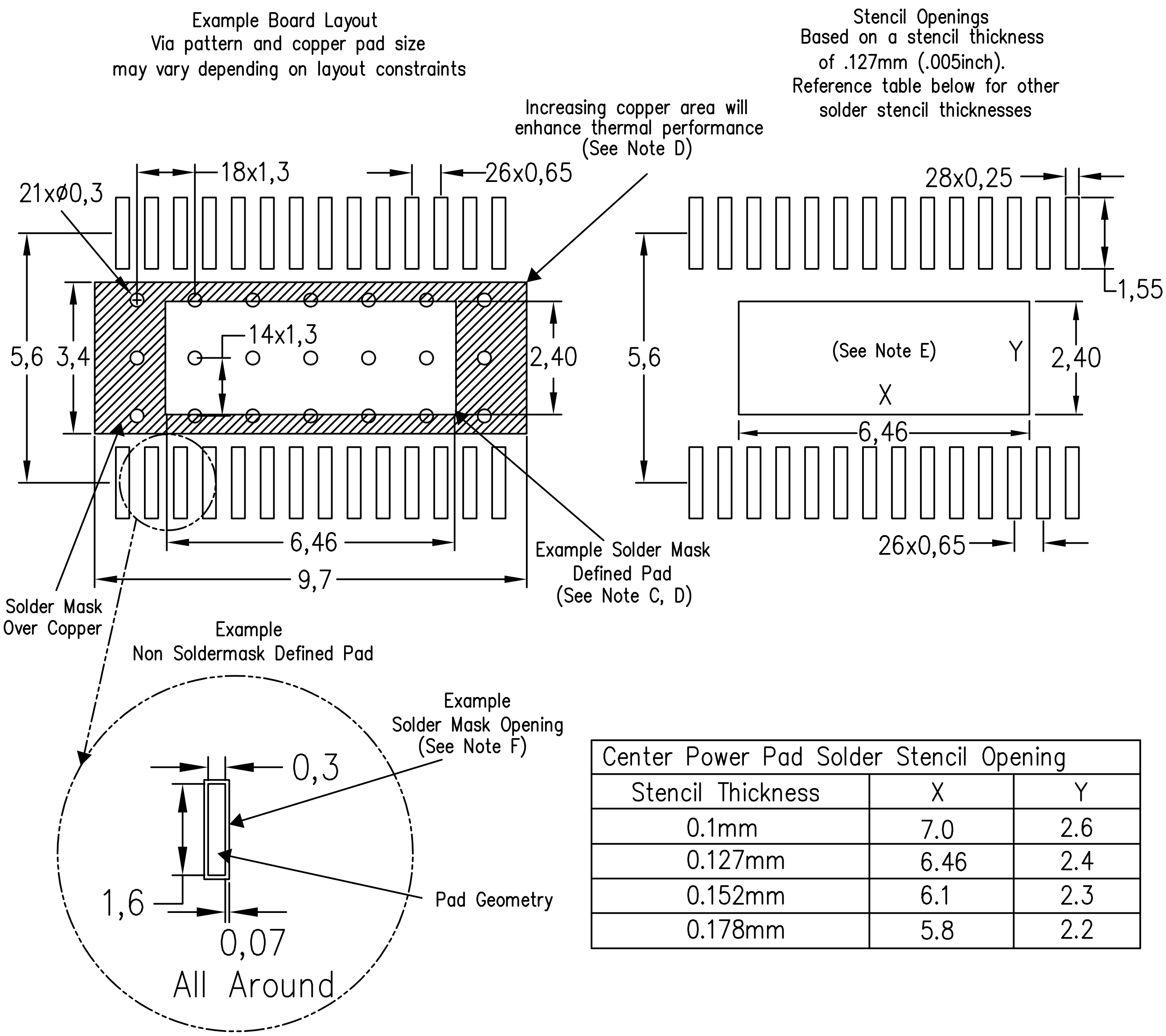
4206332-34/A0 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.0	2.6
0.127mm	6.46	2.4
0.152mm	6.1	2.3
0.178mm	5.8	2.2

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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