TEXAS INSTRUMENTS
TPS62860, TPS62861
ZHCSL99D – SEPTEMBER 2019 – REVISED MAY 2022

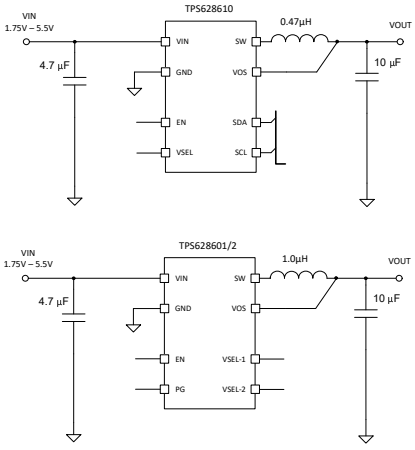
具有 I²C/VSEL 接口的 1.75V 至 5.5V 输入、0.6A/1A 同步降压转换器

1 特性

- 2.3 μA 工作静态电流
- 开关频率高达 4MHz
- 1% 的输出电压精度
- DVS 输出为 0.4V 至 1.9875V（阶跃为 12.5mV）
- 通过 I²C 用户接口进行调节
  - 输出电压预设
  - 斜坡速度
- 在运行期间通过 VSEL 引脚来切换 V_{OUT}
- 电源正常状态指示
- 支持小于 6mm² 的解决方案尺寸
- 支持小于 0.6mm 的解决方案高度
- 微型 8 引脚 0.35mm 间距 WCSP 封装
- 经过优化的引脚排列，可支持 0201 元件

2 应用

- 可穿戴电子产品
- 便携式电子产品
- 手机
- 医疗传感器贴片和患者监护仪



典型应用

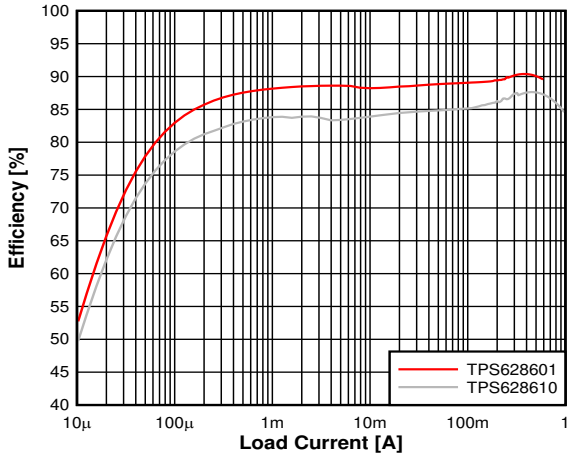
3 说明

TPS6286x 器件是具有 I2C 接口和 VSEL 接口的高频同步降压转换器。这些器件提供了高效、灵活和具有高功率密度的负载点直流/直流解决方案。该转换器在中高负载条件下以 PWM 模式运行，并在轻负载时自动进入省电运行模式，从而在整个负载电流范围内保持高效率。该器件还可强制进入 PWM 运行模式，以实现最小输出电压纹波。凭借其 DCS-Control 架构，该器件可实现出色的负载瞬态性能并符合严格的输出电压精度要求。通过 I²C 接口和专用 VSEL 引脚，可快速调整输出电压，使负载的功耗适应相关应用不断变化的性能需求。TPS6286x 系列提供两个 VSEL 引脚和四个出厂预设电压，支持在没有 I²C 接口的情况下使用。

器件信息

器件型号	电流	封装(1)	封装尺寸（标称值）
TPS628610	1A	DSBGA (8)	0.7 × 1.4 × 0.4 mm
TPS628601	0.6A	DSBGA (8)	0.7 × 1.4 × 0.4 mm
TPS628600	0.6A	DSBGA (8)	0.7 × 1.4 × 0.4 mm
TPS628602	0.6A	DSBGA (8)	0.7 × 1.4 × 0.4 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



效率与 I_{OUT}（$1.1V_{OUT}$、$3.8V_{IN}$）间的关系

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (March 2022) to Revision D (May 2022) — **Page**

- Corrected the internal fixed soft-start time test condition 6

Changes from Revision B (September 2020) to Revision C (March 2022) — **Page**

- 在数据表中添加了 TPS628602 1

5 Device Comparison Table

ORDERABLE PART NUMBER	OUTPUT CURRENT	DEFAULT V_O SETTING	f_{SW}	USER INTERFACE
TPS628600YCH	0.6 A	0.6 V, 1.1 V	1.5 MHz	EN, I2C, VSEL
TPS628601YCH	0.6 A	0.6 V, 0.7 V, 0.8 V, 1.0 V	1.5 MHz	2x VSEL, EN, PG
TPS628610YCH	1 A	0.6 V, 1.1 V	4 MHz	EN, I2C, VSEL
TPS628602YCH	0.6 A	1.05 V, 0.9 V, 0.875 V, 0.625 V	1.5 MHz	2x VSEL, EN, PG

6 Pin Configuration and Functions

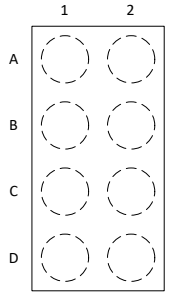


图 6-1. 8-Pin DSBGA YCH Package (Top View)

表 6-1. Pin Functions, TPS628610 and TPS628600

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	D2	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VOS	D1	IN	Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges V_{OUT} by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace.
VIN	C2	PWR	V_{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required.
SW	C1	PWR	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
VSEL	B2	IN	Voltage Selection Pin. Can be toggled during operation. LOW = 0.6 V, HIGH = 1.1 V
EN	B1	IN	A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up.
SDA	A2	IN	I^2C serial data pin. Do not leave floating.
SCL	A1	IN	I^2C serial clock pin. Do not leave floating.

表 6-2. Pin Functions, TPS628601, TPS628602

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	D2	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VOS	D1	IN	Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges VOUT by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace.
VIN	C2	PWR	VIN power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required.
SW	C1	PWR	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
PG	B2	OUT	Open-drain power-good output
EN	B1	IN	A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up.
VSEL-1	A2	IN	Voltage Selection Pin. Can be toggled during operation.

表 6-2. Pin Functions, TPS628601, TPS628602 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VSEL-2	A1	IN	Voltage Selection Pin. Can be toggled during operation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	6	V
Pin voltage	SW, DC	–0.3	V_{IN} + 0.3 V	V
Pin voltage	SW, transient < 10 ns, while switching	–2.5	9	V
Pin voltage	EN, VSEL, SDA, SCL, PG	–0.3	6	V
Pin voltage	VOS	–0.3	5	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		1.75		5.5	V
V_{OUT}	Output voltage range		0.4		1.9875	V
	Pin voltage	SW	0		5.5	V
	Pin voltage	EN, SDA, SCL, VSEL, PG	0		5.5	V
I_{OUT}	Output current range	TPS628610, V_{IN} > 2.3 V			1	A
I_{OUT}	Output current range	TPS628610, $V_{IN} \leqslant$ 2.3 V			0.7	A
I_{OUT}	Output current range	TPS628601			0.6	A
I_{PG}	Power-good input current capability				1	mA
T_J	Operating junction temperature		–40		125	°C
C_{IN}	Effective input capacitance		2	4.7		µF
L	Effective inductance	TPS628610	0.33	0.47	0.82	µH
COUT	Effective output capacitance	TPS628610	2		26	µF
L	Effective inductance	TPS628601	0.7	1.0	1.2	µH
COUT	Effective output capacitance	TPS628601	3		26	µF

7.4 Thermal Information

THERMAL METRIC		YCH (DSBGA) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.5	°C/W

7.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 3.6 V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	EN = VIN, I_{OUT} = 0 µA, V_{OUT} = 1.2 V device not switching, T_J = –40°C to +85°C		2.3	4	µA
		EN = VIN, I_{OUT} = 0 µA, V_{OUT} = 1.2 V, device switching		2.5		µA
$I_{SD(VIN)}$	VIN shutdown supply current	EN = GND, shutdown current into VIN VSEL, MODE = GND, T_J = –40°C to +85°C		120	250	nA
UVLO						
$V_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising		1.65	1.75	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling		1.56	1.7	V
$V_{UVLO(H)}$	VIN UVLO hysteresis			100		mV
LOGIC PINS						
V_{IH}	High-level input voltage threshold		0.8			V
V_{IL}	Low-level input voltage threshold				0.4	V
I_{LKG}	Input leakage current into SDA, SCL, VSEL	Pin connected to VIN, –40°C to 85°C		10	25	nA
	EN internal pulldown resistance	EN pin to GND		0.5		MΩ
I_{LKG}	Input leakage into EN	Pin connected to VIN, –40°C to 85°C		10	25	nA
VOUT VOLTAGE						
V_{OUT}	Output voltage accuracy	PWM mode, no load, T_J = 25°C to 85°C	–1%		+1%	
V_{OUT}	Output voltage accuracy	PWM mode, no load, T_J = –40°C to 125°C	–2%		+1.7%	
$I_{VOS(LKG)}$	VOS input leakage current	EN = VIN, V_{OUT} = 1.2 V (internal 12-MΩ resistor divider), T_J = –40°C to +85°C		100	400	nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, TPS62861x	V_{IN} = 3.6 V, V_{OUT} = 1.2 V, PWM operation		4		MHz
$f_{SW(FCCM)}$	Switching frequency, TPS62860x	V_{IN} = 3.6 V, V_{OUT} = 1.2 V, PWM operation		1.5		MHz
START-UP						
	Internal fixed soft-start time	from V_{OUT} = 0 V to 95% of VOUT nominal		0.125	0.2	ms
	EN HIGH to start of switching delay			500	1000	µs
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	I_{OUT} = 500 mA		120	170	mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	I_{OUT} = 500 mA		80	115	mΩ
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	TPS628610	1.3	1.45	1.55	A
$I_{LS(OC)}$	Low-side valley current limit	TPS628610	1.2	1.35	1.45	A
$I_{HS(OC)}$	High-side peak current limit	TPS628601	0.95	1.1	1.2	A
$I_{LS(OC)}$	Low-side valley current limit	TPS628601	0.85	1.0	1.1	A
$I_{LS(NOC)}$	Low-side negative current limit	Sinking current limit on LS FET				A
POWER GOOD						
V_{PGTH}	Power-good threshold	PGOOD low, VOS falling		93%		
V_{PGTH}	Power-good threshold	PGOOD high, VOS rising		96%		
$t_{PG:DLY}$	Power-good deglitch delay	PG rising edge		16		µs
$I_{PG;LKG}$	Input leakage current into the PG pin	V_{PG} = 5.0 V		10	100	nA
	PG pin output low-level voltage	I_{PG} = 1 mA			400	mV
OUTPUT DISCHARGE						
	Output discharge resistor on the VOS pin	EN = GND, IVOS = –10 mA into the VOS pin, T_J = –40°C to +85°C		7	11	Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold (1)	Temperature rising, PWM mode		160		°C

T_J = –40°C to +125°C, V_{IN} = 3.6 V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			20		°C

(1) Specified by design. Not production tested.

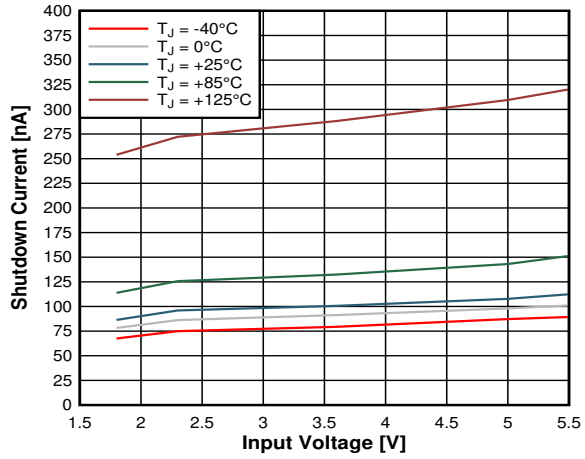
7.6 I²C Interface Timing Characteristics

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		Fast mode plus			1	MHz
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus	0.5			µs
t_{HD}, t_{STA}	Hold time (repeated) START condition	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus	0.5			µs
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
t_{SU}, t_{STA}	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
t_{SU}, t_{DAT}	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
		Fast mode plus	50			ns
t_{HD}, t_{DAT}	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	µs
		Fast mode plus	0			µs
t_{RCL}	Rise time of SCL signal	Standard mode			1000	ns
		Fast mode	20+0.1CB		300	ns
		Fast mode plus			120	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	Standard mode	20+0.1CB		1000	ns
		Fast mode	20+0.1CB		300	ns
		Fast mode plus			120	ns
t_{FCL}	Fall time of SCL signal	Standard mode	20+0.1CB		300	ns
		Fast mode			300	ns
		Fast mode plus			120	ns
t_{RDA}	Rise time of SDA signal	Standard mode			1000	ns
		Fast mode	20+0.1CB		300	ns
		Fast mode plus			120	ns

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{FDA}	Fall time of SDA signal	Standard mode			300	ns
		Fast mode	20+0.1CB		300	ns
		Fast mode plus			120	ns
t_{SU}, t_{STO}	Setup time of STOP condition	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
CB	Capacitive load for SDA and SCL	Standard mode			400	pF
		Fast mode			400	pF
		Fast mode plus			550	pF

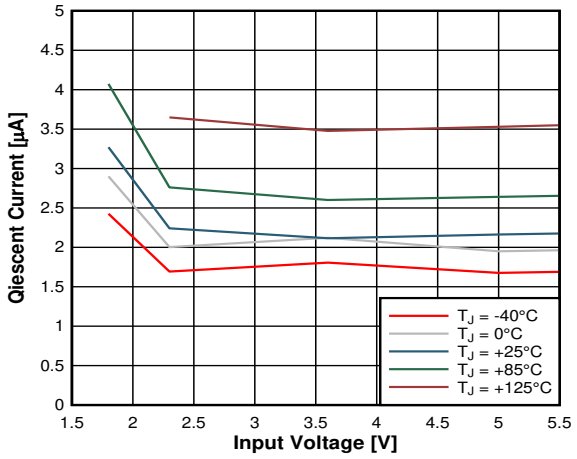
(1) All values referred to V_{IL} MAX and V_{IH} MIN levels in the *Electrical Characteristics* table.

7.7 Typical Characteristics



EN = GND

图 7-1. Shutdown Current I_{SD}



EN = VIN Device not switching

图 7-2. Quiescent Current I_Q

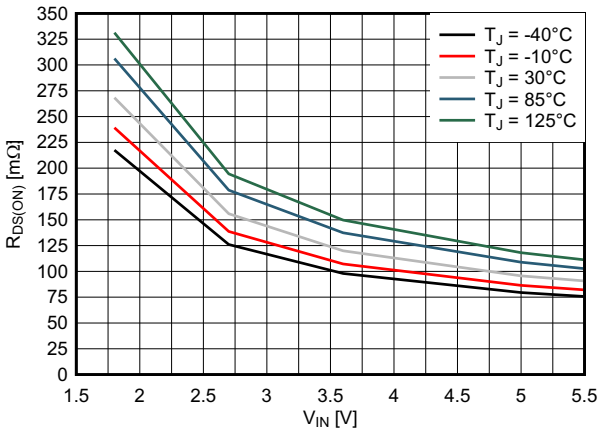


图 7-3. High-side Switch Drain Source Resistance $R_{DS(ON)}$

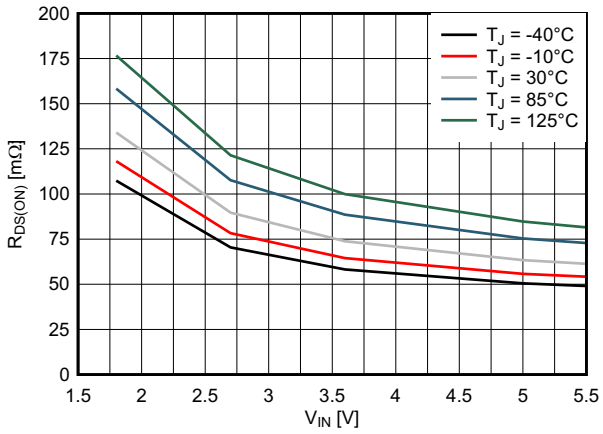


图 7-4. Low-side Switch Drain Source Resistance $R_{DS(ON)}$

8 Detailed Description

8.1 Overview

The TPS6286x is a high-frequency synchronous step-down converter with ultra-low quiescent current consumption and flexible output voltage by I²C or VSEL interface. Using TI's DCS-Control™ topology, the device extends the high efficiency operation area down to microamperes of load current during Power Save Mode Operation. TI's DCS-Control (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM mode operation. DCS-Control includes an AC loop which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

8.2 Functional Block Diagram

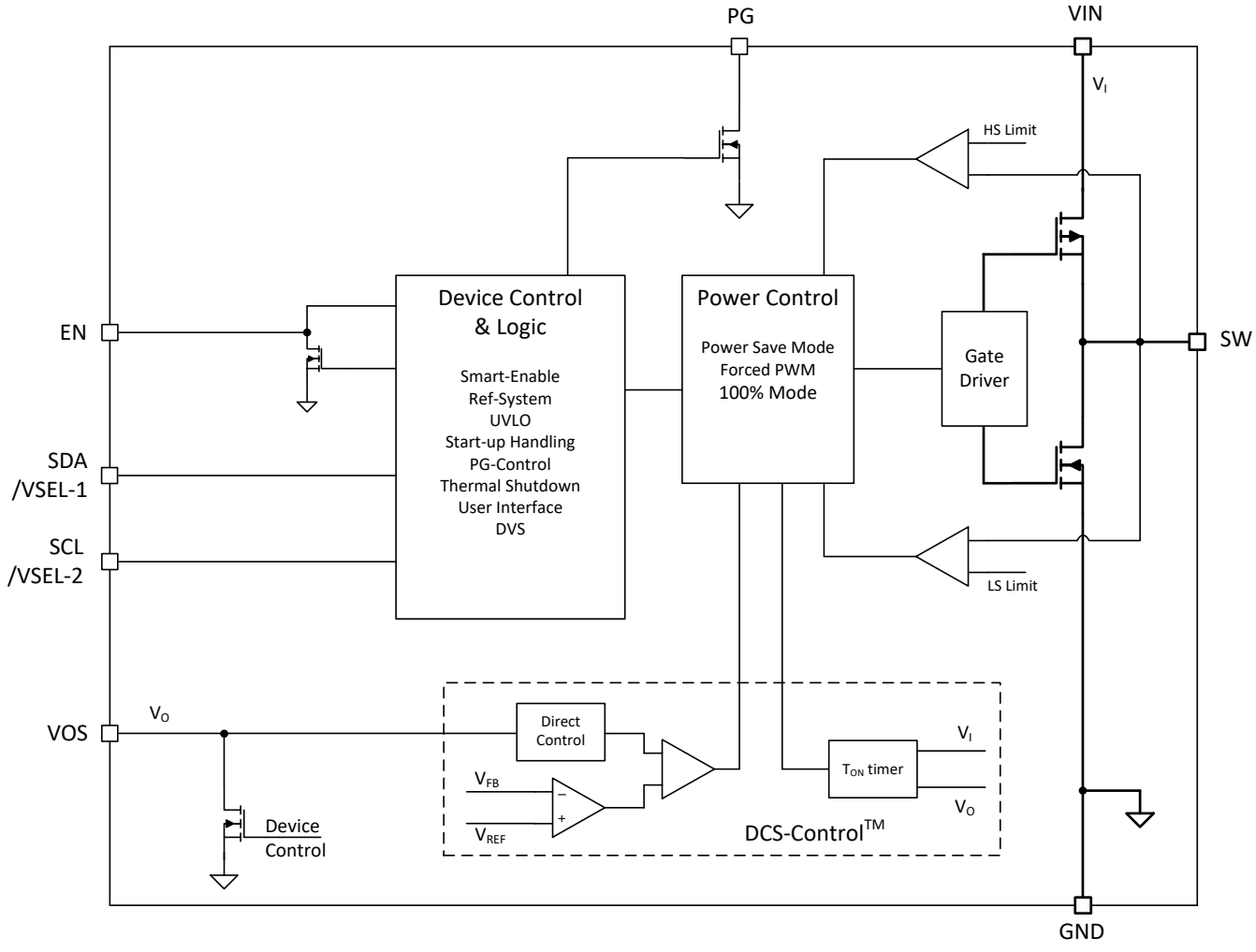


图 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Power Save Mode

As the load current decreases, the device enters Power Save Mode (PSM) operation. PSM occurs when the inductor current becomes discontinuous, which is when it reaches 0 A during a switching cycle. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

8.3.2 Forced PWM Operation

Through I^2C, set the device in forced PWM (FPWM) mode by the CONTROL register. The device switches continuously, even with a light load. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications. Efficiency at light load is lower in FPWM mode.

8.3.3 Smart Enable and Shutdown (EN)

An internal 500-kΩ resistor pulls the EN pin to GND and avoids the pin to be floating. This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin once the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

8.3.4 Soft Start

Once the device has been enabled with EN high, it initializes and powers up its internal circuits. This occurs during the regulator start-up delay time, t_{Delay}. Once t_{Delay} expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time, t_{Ramp}. See 图 8-2.

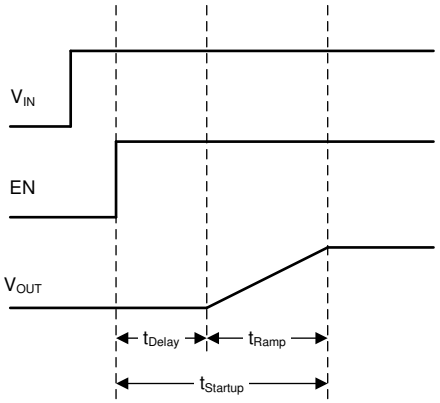


图 8-2. Start-up Sequence

8.3.5 Output Voltage Selection (VSEL) for TPS62860x

The optional VSEL Interface allows setting the output voltage by a 2-pin HIGH/LOW setting. Using and applying a digital pattern to the "VSEL-1" and "VSEL-2" pins sets the output voltage according to 表 8-1.

表 8-1. Target Output Voltage Setting by VSEL Interface

VSEL-2	VSEL-1	TPS628601	TPS628602	OPERATION MODE
0	0	0.6 V	1.05 V	PFM Mode
0	1	0.7 V	0.9 V	PFM Mode
1	0	0.8 V	0.875 V	PFM Mode
1	1	1.0 V	0.625 V	PFM Mode

8.3.6 Output Voltage Selection (VSEL and I^2C) for TPS628610

The TPS628610 has two options to select the output voltage.

It can be changed by the VSEL pin. Putting this pin "HIGH" selects the output voltage according to V_{OUT} register 2. Putting this pin "LOW" selects the voltage according to V_{OUT} Register 1. The pin can be toggled during operation.

It can also be selected by the value in the V_{OUT} register that is chosen by VSEL at the moment. The voltage changes right after the I^2C command is received.

8.3.7 Forced PWM Mode During Output Voltage Change

In normal operation, the device does not force PWM operation during VOUT change after VSEL toggle or I^2C command. For ramping down, this mode provides the remaining energy, stored in the output capacitor to the load of the DC/DC and save battery charge. See 图 9-14.

Through I^2C, the device can be set to forced PWM (FPWM) switching during output voltage change. This allows a controlled ramp of V_{OUT} up and especially down, regardless of the load condition. See 图 9-15.

This feature follows the internal I^2C ramp and is only recommended for the setting 1 mV/µs and 0.1 mV/µs. During the faster slopes (10 mV/µs and 5 mV/µs), the mode is likely to be left before the voltage reached the new target value.

8.3.8 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7 V (max) with falling VIN. The device starts at an input voltage of 1.8 V (max) rising VIN. Once the device re-enters operation out of an undervoltage lockout condition, it behaves like being enabled.

8.3.9 Power Good (PG)

The TPS6286x has a built-in Power-Good (PG) feature to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails or to indicate any overload behavior on the output. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN or thermal shutdown. VIN must remain present for the PG pin to stay LOW. When applying VIN the first time, PG stays HIGH until the first enabling of the device.

If the power-good output is not used, it is recommended to tie to GND or leave open.

表 8-2. Power Good Indicator Functional Table

LOGIC SIGNALS					PG STATUS
V_I	EN-PIN	THERMAL SHUTDOWN	V_O	DVS TRANSITION ACTIVE	
V_I > UVLO	HIGH	NO	V_O on target	NO	**High Impedance**
				YES	**LOW**
			V_O < target	x	**LOW**
		YES	x	x	**LOW**
	LOW	x	x	x	**LOW**
V_I < UVLO	x	x	x	x	**Undefined**

The PG indicator triggers immediately (after internal comparator delay) when Vo crosses the lower V_{PGTH} to indicate that the voltage has left the target setting. It features a delay after crossing the upper V_{PGTH} when going high to make sure Vo has reached the target again. 图 8-3 sketches the behavior.

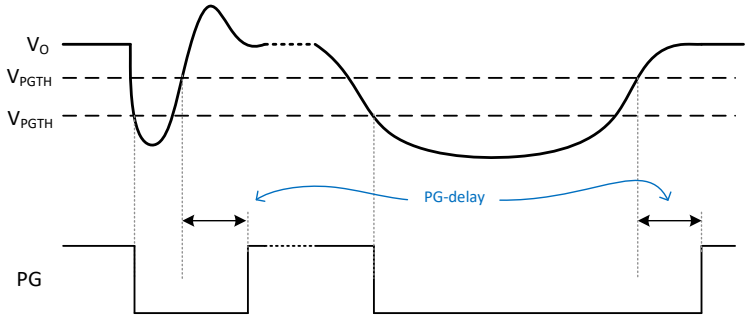


图 8-3. Power Good Transient and De-glitch Behavior

The PG Indicator is by default pulled low during DVS transition of the output voltage without any blanking or delay time. 图 8-3 shows an example of this behavior. After V_o has reached the new target, the PG is again active as shown in 图 8-3.

8.3.10 Switch Current Limit / Short Circuit Protection

The TPS6286x integrates a current limit on the high-side and low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, ILIMF, trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Once the inductor current through the low-side switch decreases below the low-side MOSFET current limit, ILIMF, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

8.3.11 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds the thermal shutdown temperature TSD of 160°C (typ), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When T_J decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set VOUT. The thermal shutdown is not active in Power Save Mode.

8.3.12 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge feature is only active once the device has been enabled at least once since the supply voltage was applied. The output discharge function is not active if the device is disabled and the supply voltage is applied the first time. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is $V_I > V_{TH\_UVLO-}$.

8.4 Programming

8.4.1 Serial Interface Description

I2C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see I²C-Bus Specification, Version .6, 2014). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open-drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives, transmits data, or both on the bus under control of the master device.

The device works as a *slave* and supports the following data transfer *modes*, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.8 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different and must not be used.

It is recommended that the I²C master initiates a STOP condition on the I²C bus after the initial power up of SDA and SCL pullup voltages to ensure reset of the I²C engine.

8.4.2 Standard- and Fast-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 图 8-4. All I²C-compatible devices recognize a start condition.

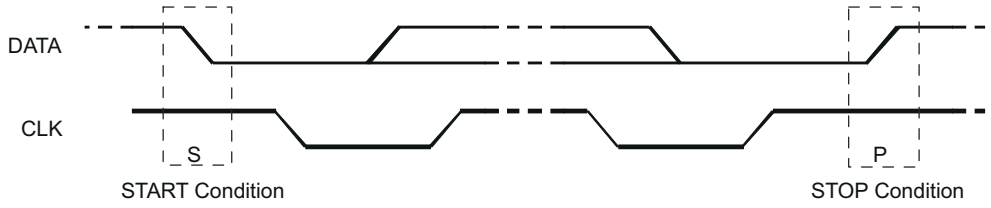


图 8-4. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 图 8-5). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see 图 8-6) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

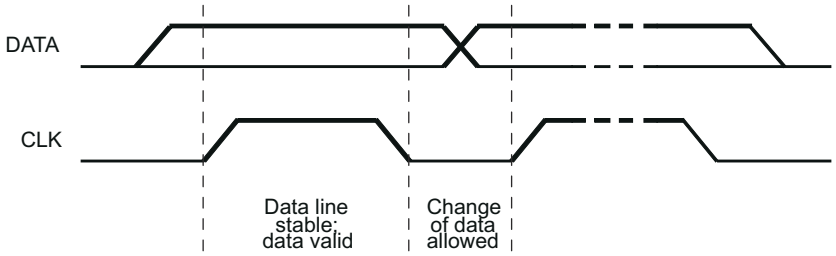


图 8-5. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An

acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 图 8-4). This releases the bus and stops the communication link with the addressed slave. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

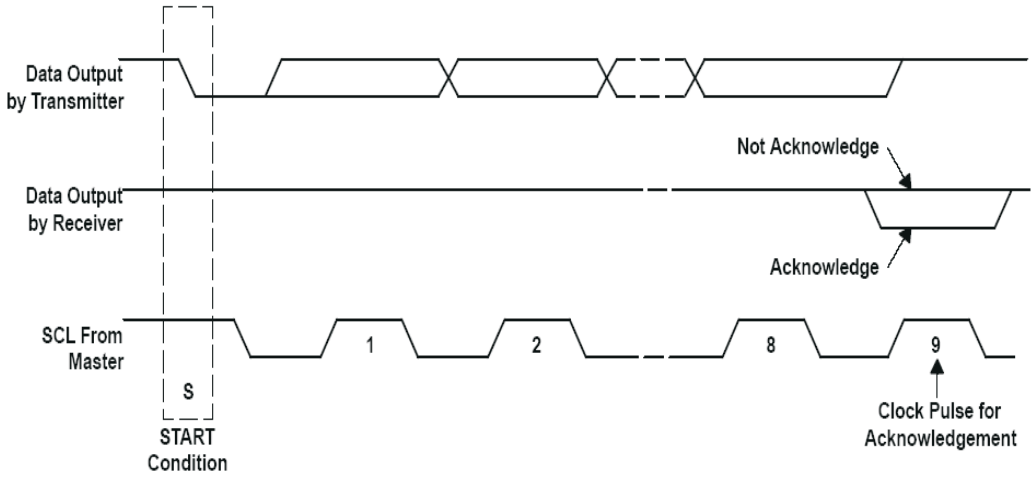


图 8-6. Acknowledge on the I^2C Bus

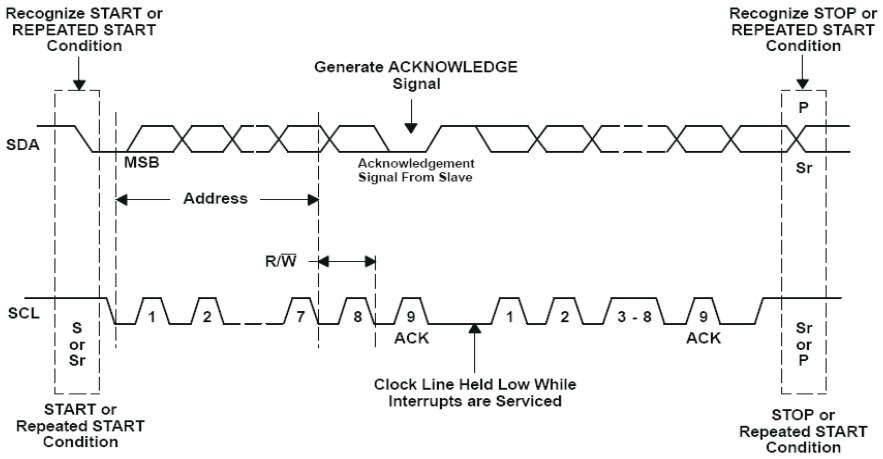


图 8-7. Bus Protocol

8.4.3 I^2C Update Sequence

The requires the following:

- A start condition
- A valid I^2C address
- A register address byte
- A data byte for a single update

After the receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^2C address selects the device. The device performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

图 8-8. "Write" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

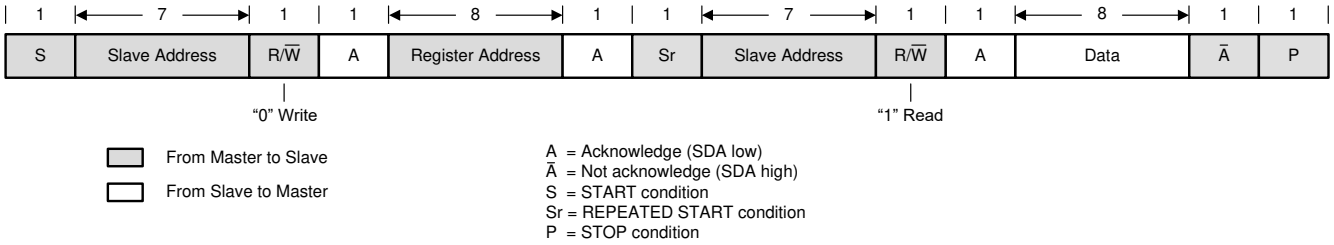


图 8-9. "Read" Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

8.4.4 I²C Register Reset

The I²C registers can be reset by the following:

- Pull the input voltage below 1.8 V (typ).
- A high to low transition on EN. The previous value of the "Enable Output Discharge" bit is latched until the next EN rising edge or pulling the input voltage below 1.0 V (typ).
- Set the Reset bit in the CONTROL register. When Reset is set to 1, all registers are reset to the default values and a new start-up begins immediately. After t_{Delay}, the I²C registers can be programmed again.

8.5 Register Map

表 8-3. Register Map

REGISTER ADDRESS (HEX)	REGISTER NAME	FACTORY DEFAULT (HEX)	DESCRIPTION
0x01	V_{OUT} Register 1	0x10	Sets the target output voltage
0x02	V_{OUT} Register 2	0x38	Sets the target output voltage
0x03	CONTROL Register		Sets miscellaneous configuration bits
0x05	STATUS Register	0x00	Returns status flags, cleared on read-out

8.5.1 Slave Address Byte

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	R/W

The slave address byte is the first byte received following the START condition from the master device. The 7-bit slave address is 0x40 and internally set.

8.5.2 Register Address Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	D2	D1	D0

Following the successful acknowledgment of the slave address, the bus master sends a byte to the device, which contains the address of the register to be accessed.

8.5.3 V_{OUT} Register 1

表 8-4. V_{OUT} Register 1 Description

REGISTER ADDRESS 0X01 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYP)节 8.5.3
6:0	VO1_SET	0x00	0.400 V
		0x01	0.4125 V
		...	
		0x10	**0.600 V** (default value)
		...	
		0x7E	1.975 V
		0x7F	1.9875 V

8.5.4 V_{OUT} Register 2

表 8-5. V_{OUT} Register 2 Description

REGISTER ADDRESS 0X02 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYP)节 8.5.4
7	Operation Mode	0x00	0 - Keep PFM/PWM selection as in CONTROL-Register 1 - sets the device in PWM operation for this Voltage selection
6:0	VO2_SET	0x00	0.400 V
		0x01	0.4125 V
		...	
		0x38	**1.10 V** (default value)
		...	
		0x7E	1.975 V
		0x7F	1.9875 V

8.5.5 CONTROL Register

表 8-6. CONTROL Register Description

REGISTER ADDRESS 0X03 READ/WRITE				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	Reset	W	0	1 - Reset all registers to default. This bit triggers a shutdown followed by a re-reading of the internal OTP settings and a new soft start.
6	Enable FPWM Mode during Output Voltage Change	R/W	1	0 - Keep the current mode status during output voltage change. 1 - Force the device in FPWM during output voltage change.
5	Software Enable Device	R/W	1	0 - Disable the device. All registers values are still kept. 1 - Re-enable the device with a new start-up without the t_{Delay} period.
4	Enable FPWM Mode	R/W	0	0 - Set the device in power save mode at light loads. 1 - Set the device in forced PWM mode at light loads.
3	Enable Output Discharge	R/W	1	0 - Disable output discharge. 1 - Enable output discharge. This setting is used for the next disable cycle (Software or Hardware).
2	Reserved			
0:1	Voltage Ramp Speed	R/W	11	00 - 10mV/µs 01 - 5 mV/µs 10 - 1 mV/µs 11 - 0.1 mV/µs

8.5.6 STATUS Register

表 8-7. STATUS Register Description

REGISTER ADDRESS 0X05 READ ONLY(1)				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	Reserved			
4	Thermal Shutdown Tripped	R	0	1: Thermal Shutdown has tripped since the last reading. 0: No Thermal Shutdown event occurred during the last reading.
3	Reserved			
2	Power Bad	R	0	1: Output voltage is or was below 0.95xVO 0: No Power Bad event occurred since last reading

表 8-7. STATUS Register Description (continued)

REGISTER ADDRESS 0X05 READ ONLY(1)				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
1:0	Reserved			

(1) All bit values are latched until the device is reset, or the STATUS register is read. Then, the STATUS register is reset to its default values.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application, TPS628610

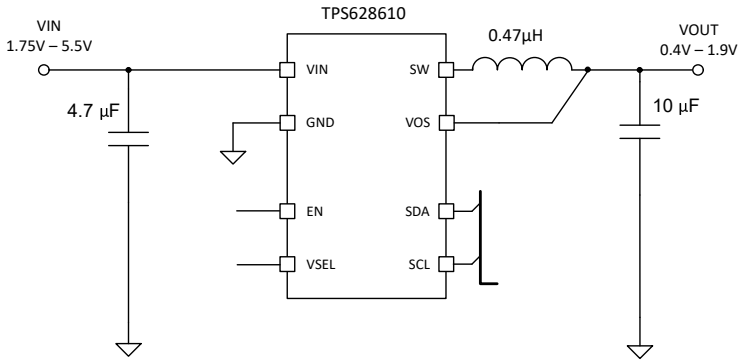


图 9-1. TPS628610, Typical Application

9.2.1 Design Requirements

表 9-1 shows the list of components for the application circuit and the characteristic application curves.

表 9-1. Components for Application Characteristic Curves

REFERENCE	DESCRIPTION	VALUE	SIZE [L x W X T]	MANUFACTURER(1)
TPS628610	Step down converter, 1 A		1.4 mm x 0.70 mm x 0.4 mm max.	Texas Instruments
C_{IN}	Ceramic capacitor, GRM155R60J475ME47D	4.7 µF	0402 (1 mm x 0.5 mm x 0.6 mm max.)	Murata
C_{OUT}	Ceramic capacitor, GRM155R60J106ME15D	10 µF	0402 (1 mm x 0.5 mm x 0.65 mm max.)	Murata
L	Inductor DFE18SANR47MG0L	0.47 µH	0603 (1.6 mm x 0.8 mm x 1.0 mm max.)	Murata

(1) See *Third-party Products Disclaimer*.

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple, and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to 方程式 1.

方程式 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current, as calculated with 方程式 2. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high side MOSFET switch current limit, I_{LIMF}.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- f = Switching frequency
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current

表 9-2 shows a list of possible inductors.

表 9-2. List of Possible Inductors

INDUCTANCE [µH]	INDUCTOR SERIES	SIZE IMPERIAL (METRIC)	DIMENSIONS L x W X T	SUPPLIER(1)
0.47	DFE18SAN_G0	0603 (1608)	1.6mm x 0.8mm x 1.0mm max	Murata
0.47	HTEB16080F	0603 (1608)	1.6mm x 0.8mm x 0.6mm max.	Cyntec
0.47	HTET1005FE	0402 (1005)	1.0mm x 0.5mm x 0.65mm max.	Cyntec
0.47	TFM160808ALC	0603 (1608)	1.6mm x 0.8mm x 0.8mm max.	TDK

(1) See *Third-party Products Disclaimer*

9.2.2.2 Output Capacitor Selection

The DCS-Control™ scheme of the TPS6286x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple.

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 9-3 outlines possible inductor and capacitor value combinations.

表 9-3. Recommended LC Output Filter Combinations

DEVICE	NOMINAL INDUCTOR VALUE [µH]	NOMINAL OUTPUT CAPACITOR VALUE [µF]			
		4.7 µF	10 µF	2 x 10 µF	22 µF
TPS628610	0.47(1)	√	√(3)	√	√
TPS62860x	1.0(2)	√	√(3)	√	√

(1) An effective inductance range of 0.33 µH to 0.82 µH is recommended. An effective capacitance range of 2 µF to 26 µF is recommended.
(2) An effective inductance range of 0.7 µH to 1.2 µH is recommended. An effective capacitance range of 3 µF to 26 µF is recommended.
(3) Typical application configuration. Other check marks indicate alternative filter combinations.

9.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR ceramic input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications, a 4.7-µF input capacitor is sufficient. When operating from a high impedance source, like a coin cell, a larger input buffer capacitor ⩾10 µF is recommended to avoid voltage drops during start-up and load transients. The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall current consumption.

表 9-4 shows a selection of input and output capacitors.

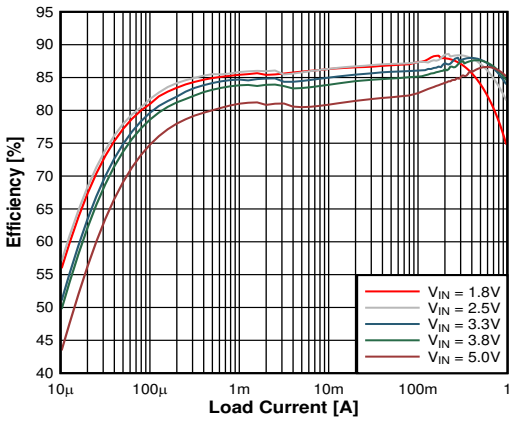
表 9-4. List of Possible Capacitors 节 9.2.2.3

CAPACITANCE [µ F]	CAPACITOR PART NUMBER	SIZE IMPERIAL (METRIC)	DIMENSIONS L x W X T	SUPPLIER(1)
4.7	GRM155R60J475ME47D	0402 (1005)	1.0mm x 0.5mm x 0.6mm max.	Murata
4.7	GRM035R60J475ME15	0201 (0603)	0.6mm x 0.3mm x 0.55mm max	Murata
10	GRM155R60J106ME15D	0402 (1005)	1.0mm x 0.5mm x 0.65mm max.	Murata

(1) See *Third-party Products Disclaimer*

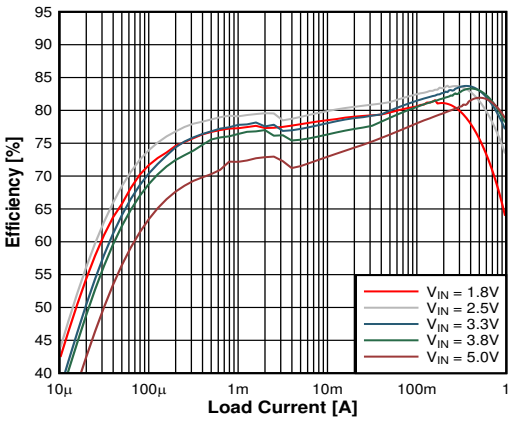
9.2.3 Application Curves

V_{IN} = 3.8 V, V_{OUT} = 1.1 V, TA = 25°C, BOM = 表 9-1, unless otherwise noted



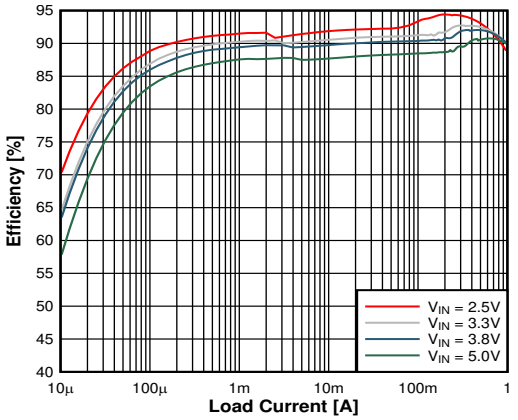
V_{OUT} = 1.1 V Auto Power Save Mode

图 9-2. Efficiency



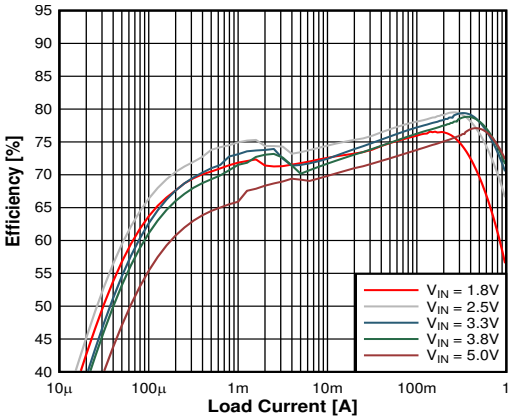
V_{OUT} = 0.6 V Auto Power Save Mode

图 9-3. Efficiency



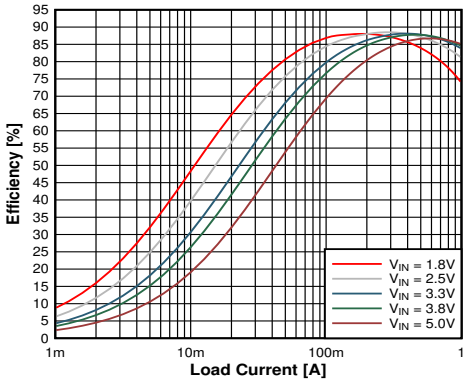
V_{OUT} = 1.9875 V Auto Power Save Mode

图 9-4. Efficiency



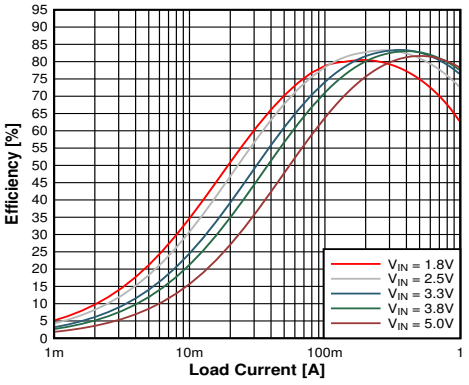
V_{OUT} = 0.4 V Auto Power Save Mode

图 9-5. Efficiency



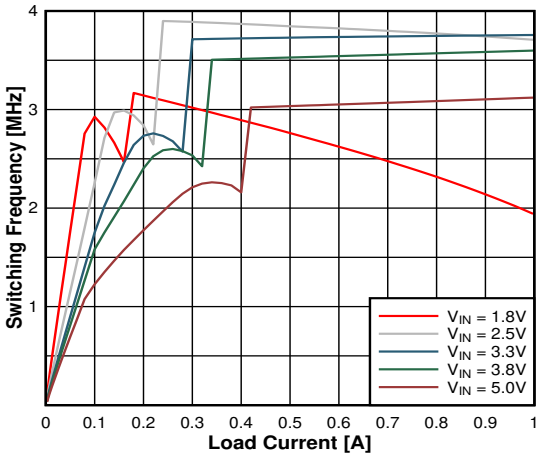
V_{OUT} = 1.1 V Forced PWM Operation

图 9-6. Efficiency, Inductor Comparison



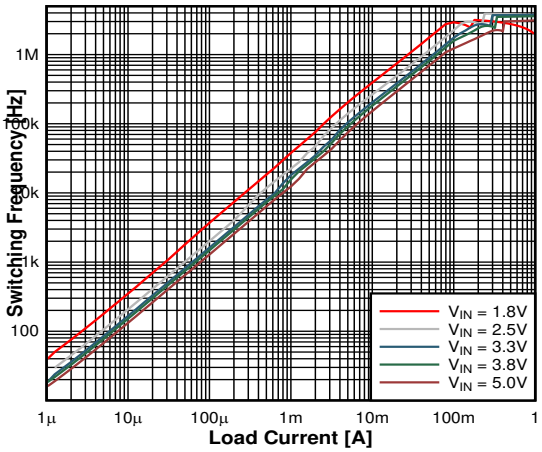
V_{OUT} = 0.6 V Forced PWM operation

图 9-7. Efficiency



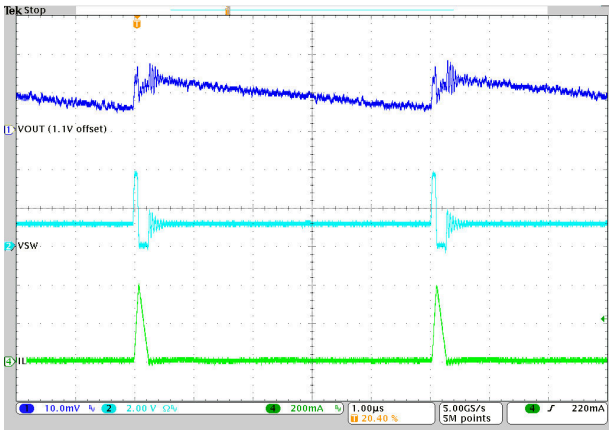
V_{OUT} = 1.1 V Auto Power Save Mode

图 9-8. Switching Frequency



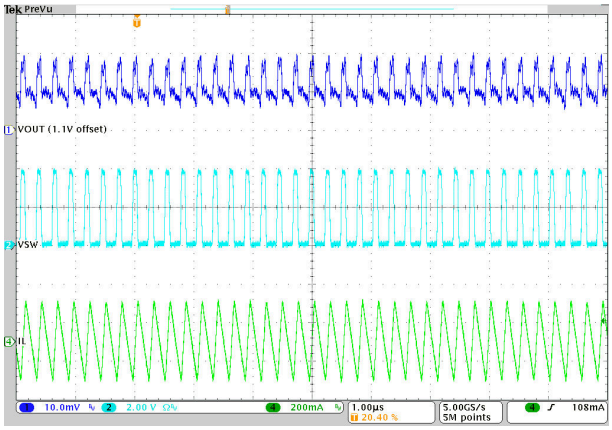
V_{OUT} = 1.1 V

图 9-9. Switching Frequency



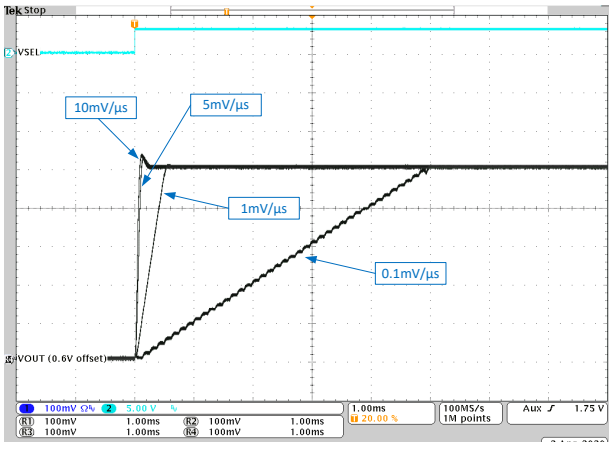
VSEL = HIGH

图 9-10. PFM Mode Operation



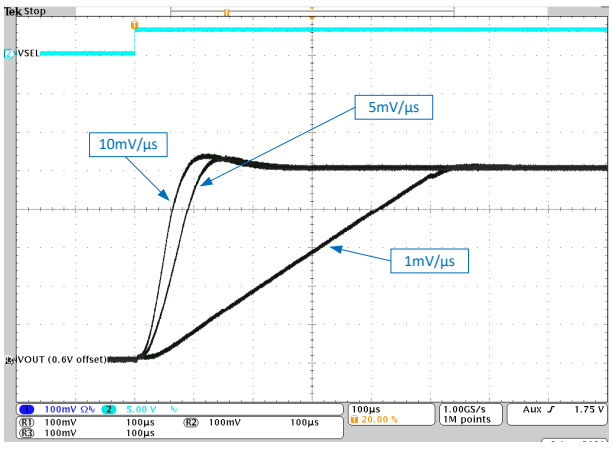
I_{OUT} = 500 mA VSEL = HIGH

图 9-11. PWM-Mode Operation



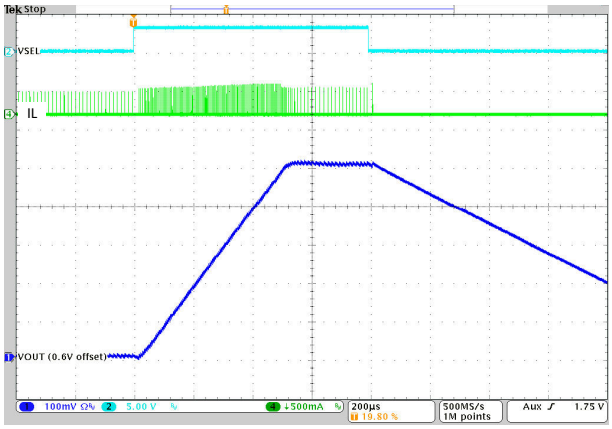
Default voltage setting

图 9-12. DVS by VSEL, Different Ramp Speed Settings



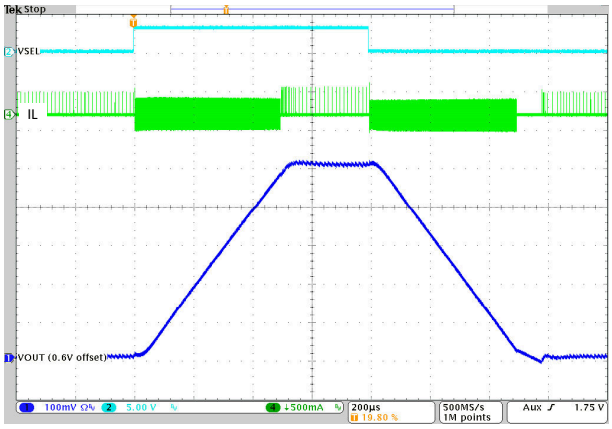
Default voltage setting

图 9-13. DVS by VSEL, Different Ramp Speed Settings



Power Save Mode is active

图 9-14. Standard Operation: V_{OUT} Change



Power Save Mode is active

图 9-15. FPWM-Mode During V_{OUT} Change Enabled

9.2.4 Typical Application, TPS628600, TPS62860x

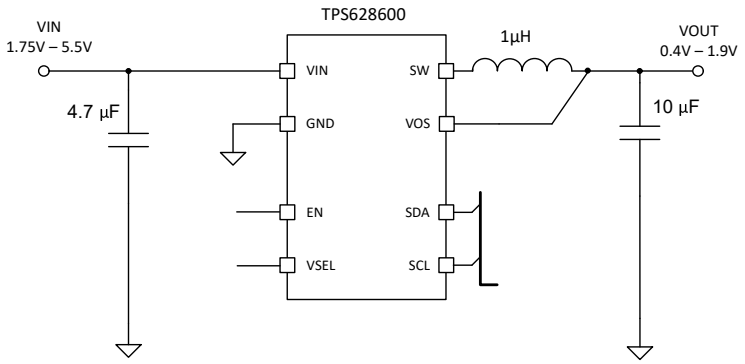


图 9-16. TPS628600, Typical Application

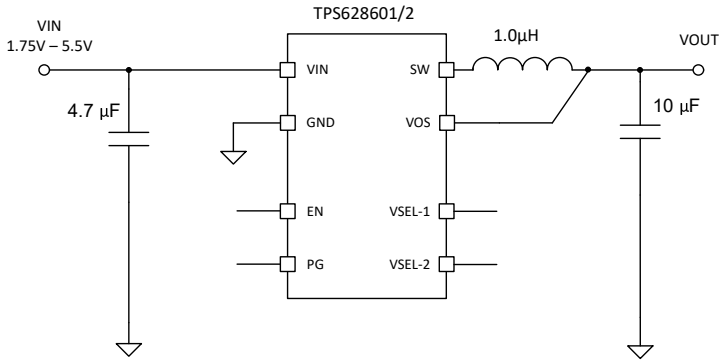


图 9-17. TPS62860x, Typical Application

9.2.4.1 Design Requirements

表 9-5 shows the list of components for the application circuit and the characteristic application curves.

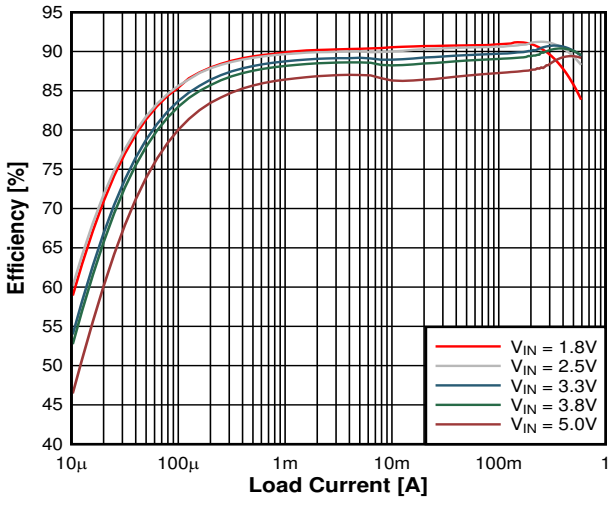
表 9-5. Components for Application Characteristic Curves

REFERENCE	DESCRIPTION	VALUE	SIZE [L x W X T]	MANUFACTURER(1)
TPS628610	Step down converter, 1 A		1.4 mm x 0.70 mm x 0.4 mm max.	Texas Instruments
C_{IN}	Ceramic capacitor, GRM155R60J475ME47D	4.7 µF	0402 (1 mm x 0.5 mm x 0.6 mm max.)	Murata
C_{OUT}	Ceramic capacitor, GRM155R60J106ME15D	10 µF	0402 (1 mm x 0.5 mm x 0.65 mm max.)	Murata
L	Inductor DFE201610E	1 µH	0805 (2.0 mm x 1.6 mm x 1.0 mm max.)	Murata

9.2.4.2 Detailed Design Procedure

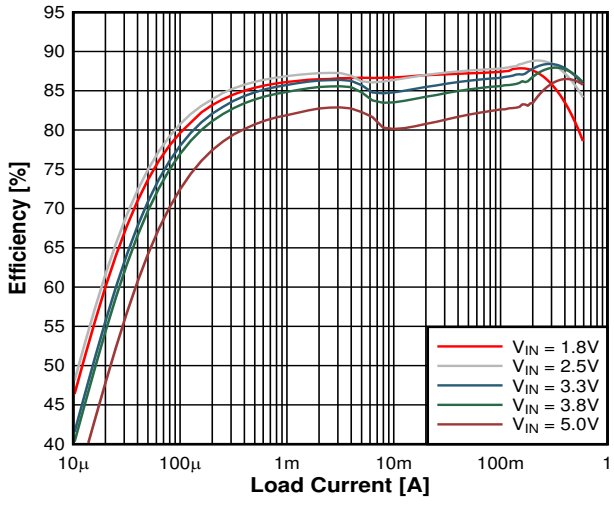
See 节 9.2.2.

9.2.4.3 Application Curves



V_{OUT} = 1.1 V Auto Power Save Mode

图 9-18. Efficiency



V_{OUT} = 0.7 V Auto Power Save Mode

图 9-19. Efficiency

10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS6286x.

11 Layout

11.1 Layout Guidelines

The pinout of TPS6286x has been optimized to enable a single top layer PCB routing of the IC and its critical passive components such as CIN, COUT, and L. Furthermore, this pin out allows you to connect tiny components such as 0201 (0603) size capacitors and 0402 (1005) size inductor. A solution size smaller than 5 mm^2 can be achieved with a fixed output voltage.

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor must be placed as close as possible to the VIN and GND pins of the IC. This is the most critical component placement.
- The VOS line is a sensitive, high impedance line and must be connected to the output capacitor and routed away from noisy components and traces (for example, SW line) or other noise sources.

11.2 Layout Example

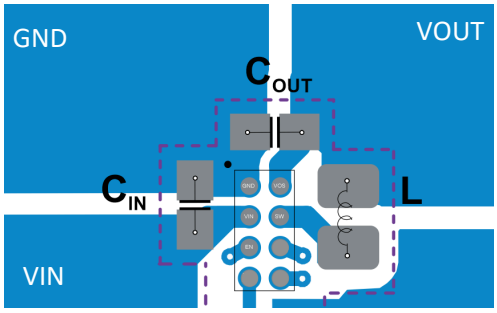


图 11-1. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 第三方产品免责声明

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12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

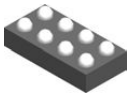
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

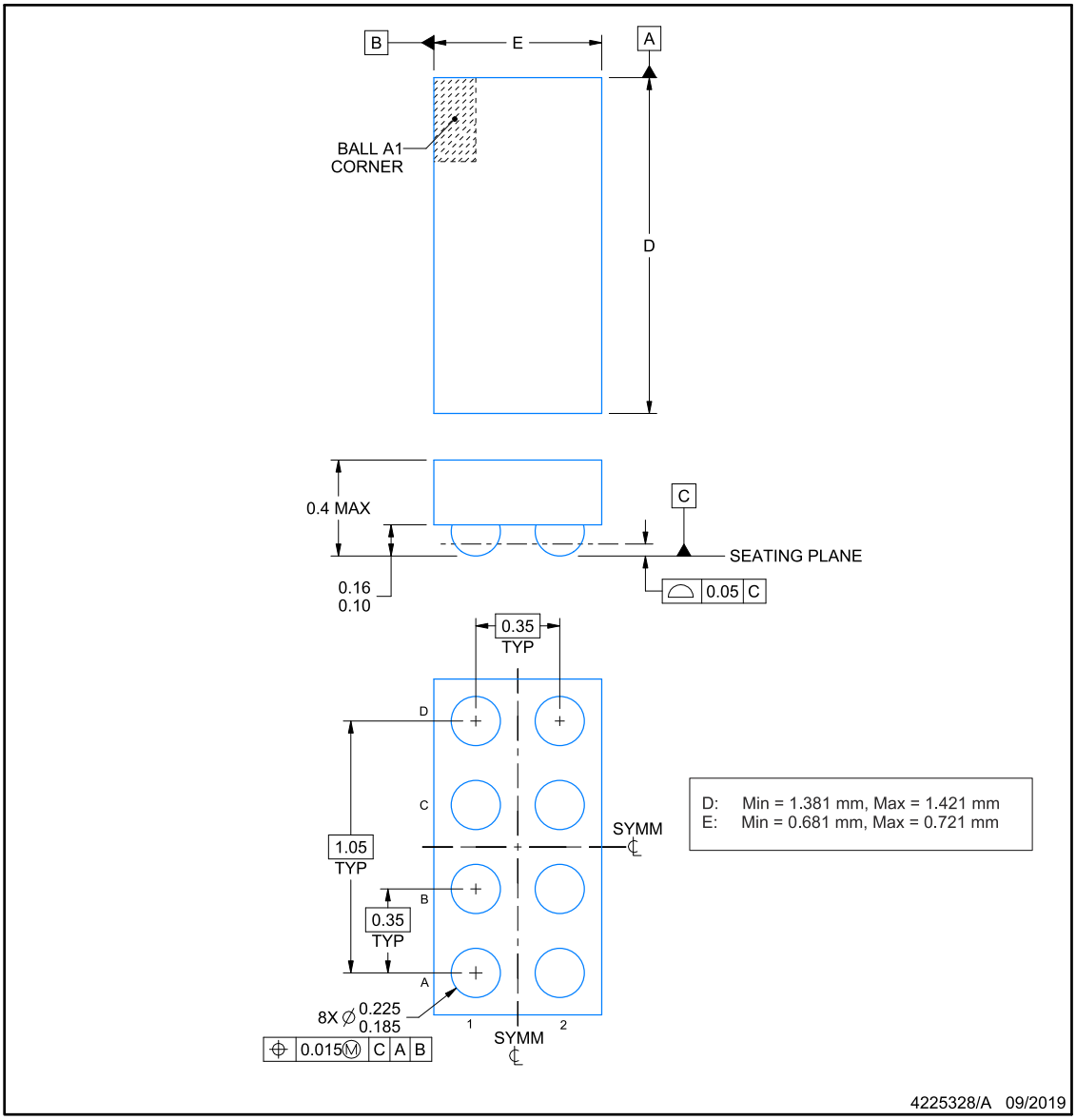


PACKAGE OUTLINE

YCH0008

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

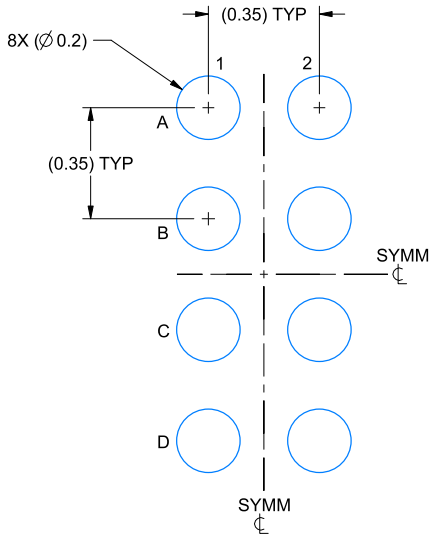
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

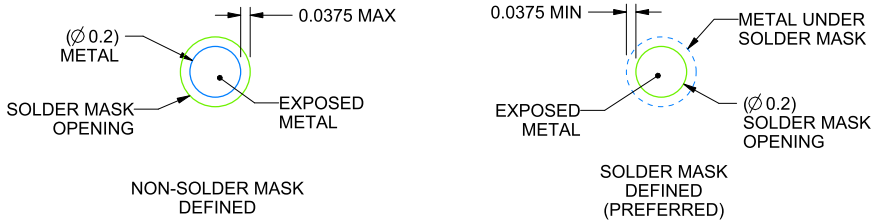
YCH0008

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4225328/A 09/2019

NOTES: (continued)

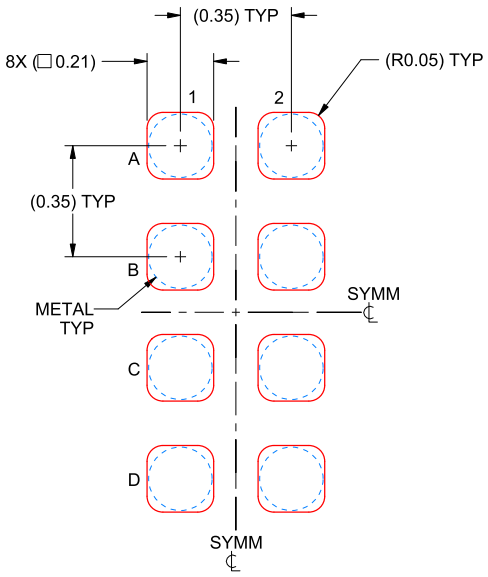
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCH0008

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS628600YCHR	ACTIVE	DSBGA	YCH	8	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
TPS628601YCHR	ACTIVE	DSBGA	YCH	8	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
TPS628610YCHR	ACTIVE	DSBGA	YCH	8	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

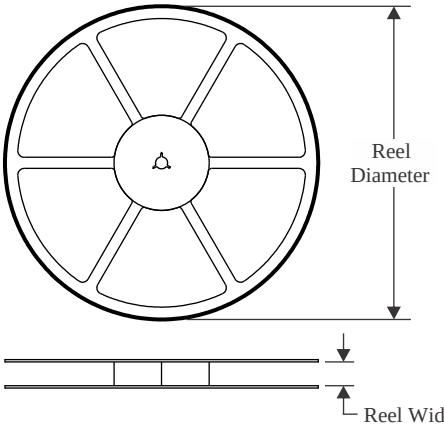
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

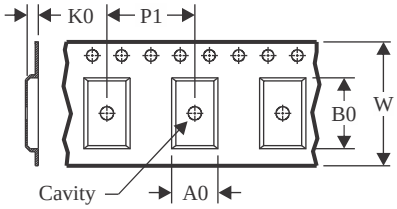
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

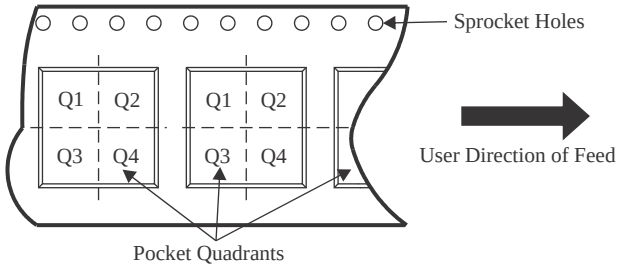


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

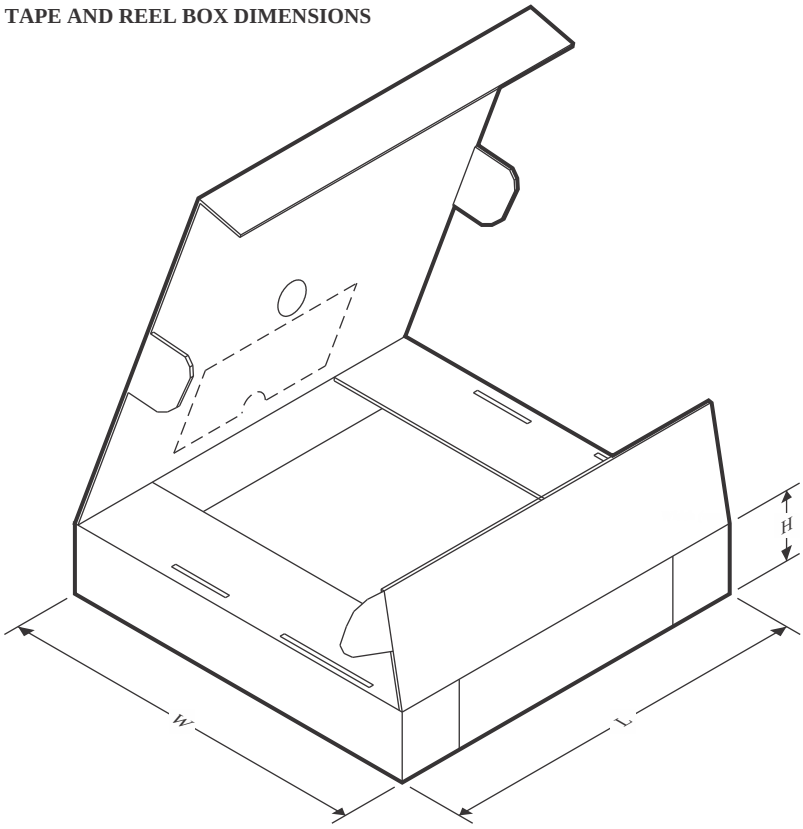
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628600YCHR	DSBGA	YCH	8	12000	180.0	8.4	0.8	1.5	0.47	2.0	8.0	Q1
TPS628601YCHR	DSBGA	YCH	8	12000	180.0	8.4	0.8	1.5	0.47	2.0	8.0	Q1
TPS628610YCHR	DSBGA	YCH	8	12000	180.0	8.4	0.8	1.5	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS628600YCHR	DSBGA	YCH	8	12000	182.0	182.0	20.0
TPS628601YCHR	DSBGA	YCH	8	12000	182.0	182.0	20.0
TPS628610YCHR	DSBGA	YCH	8	12000	182.0	182.0	20.0

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