13-Channel Level Shifter With Op-Amp for LCD TVs and Monitors

Check for Samples: TPS65198

FEATURES

- **Six CLK Outputs**
- **VST and RESET Outputs**
- **ODD and EVEN Outputs**
- **VGH_F and VGH_R Outputs**
- **Panel DISCHARGE Output**
- **Supports Forward and Reverse Operation**
- **Abnormal Operation Detection**
- **Supports all Display Resolutions**
- **High-Speed Operational Amplifier**
- **28-Pin 4×4 mm QFN Package**

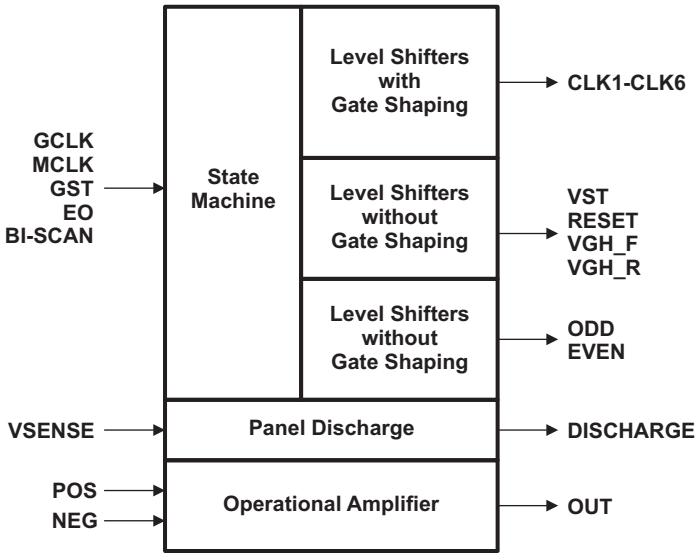
APPLICATIONS

- **LCD TVs and Monitors Using GIP Technology**

DESCRIPTION

The TPS65198 provides an integrated level shifter solution, primarily intended for TV and monitor applications using GIP technology. The device features a built-in state machine that generates twelve output signals from the five input signals provided by the timing controller (T-CON). In addition, the TPS65198 generates a signal to discharge the display panel during power-down and a high-speed operational amplifier for buffering the system's V_{COM} voltage.

Level shifter outputs are forced to a safe state (V_{GL}) during abnormal panel operation, which is indicated by the T-CON using the EO and GST signals.



ORDERING INFORMATION(1)

TA	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65198RUYR	28-Pin 4×4 QFN	TPS65198

(1) The device is supplied taped and reeled, with 3000 devices per reel.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	GCLK, MCLK, GST, EO, BI-SCAN, VSENSE		7	V
	VGH1, VGH2, RE		40	
	VGL		–25	
	VGH1 with respect to VGL, VGH2 with respect to VGL		60	
	POS, NEG, OUT, AVDD		20	
	CLK1, CLK2, CLK3, CLK4, CLK5, CLK6, VST, RESET, VGH-F, VGH_R, EVEN, ODD, DISCHARGE	–25	40	
ESD Rating	Human Body Model		2	kV
	Machine Model		200	V
	Charged Device Model		700	V
	Ambient temperature, T_A	–40	85	°C
	Junction temperature, T_J	–40	150	°C
	Storage temperature, T_{STG}	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to the GND pin.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS65198	UNITS
		QFN (28) PIN	
θ_{JA}	Junction-to-ambient thermal resistance	33.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	23.6	
θ_{JB}	Junction-to-board thermal resistance	6.7	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	6.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{GH1}	Level shifter positive supply voltage range	15		38	V
V_{GH2}		15		38	V
V_{GL}	Level shifter negative supply voltage range	–3		–23	V
V_{GH1}-V_{GL}		18		56	V
V_{GH2}-V_{GL}	Level shifter differential supply voltage range	18		56	V
AV_{DD}	Op-amp positive supply voltage range	8		20	V
T_A	Operating ambient temperature	–40	25	85	°C
T_J	Operating junction temperature	–40	85	125	°C

ELECTRICAL CHARACTERISTICS

V_{GH1}= 28V, V_{GH2}= 28V, V_{GL}= –10V, AV_{DD} = 15V, T_A = –40°C to 85°C; Typical values are at 25°C (unless otherwise noted)

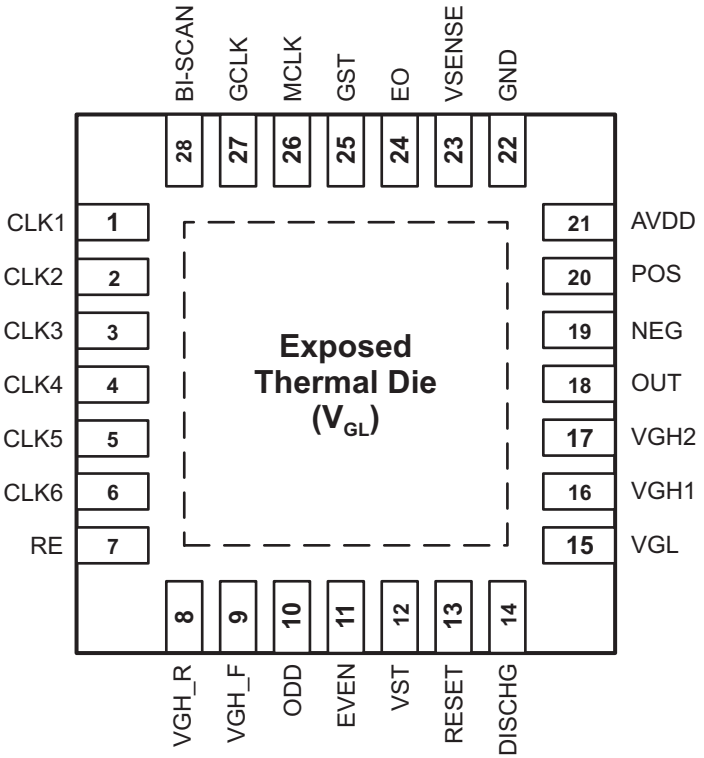
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LEVEL SHIFTER						
POWER SUPPLY						
I_{GH1}	Positive supply current	GST, GCLK, MCLK, EO, BI-SCAN = 0 V		0.4		mA
I_{GH2}	Positive supply current	GST, GCLK, MCLK, EO, BI-SCAN = 0 V		0.06		mA
I_{GL}	Negative supply current	GST, GCLK, MCLK, EO, BI-SCAN = 0V		0.13		mA
UVLO	UVLO threshold	V_{GH1} rising		9.2		V
		V_{GH1} falling		3.4		
INPUT SIGNALS (GCLK, MCLK, GST, EO, BI-SCAN)						
V_{IH}	High input voltage threshold	Input rising			1.4	V
V_{IL}	Low input voltage threshold	Input falling	0.8			V
I_{IN}	Input current	GST, GCLK, MCLK, EO = 0 V			±100	nA
		GST, GCLK, MCLK, EO = 3.3 V			±100	nA
		BI-SCAN = 3.3 V	24	33	44	µA
$R_{PULL-DOWN}$	BI-SCAN pin internal pull-down resistor			100		kΩ
LEVEL SHIFTERS (CLK1 to CLK8)						
$r_{DS(ON)}$	High side ON resistance	I_{OUT} = 10 mA, sourcing (high side)		12		Ω
	Low side ON resistance	I_{OUT} = 10 mA, sinking (low side)		7		
t_{PLH}	GCLK rising edge propagation delay	GCLK rising edge to CLK rising edge, C_{OUT} = 150 pF		50	100	ns
t_{PHL}	MCLK falling edge propagation delay	MCLK falling edge to CLK falling edge, C_{OUT} = 150 pF		50	100	ns
LEVEL SHIFTERS (VST, RESET, ODD, EVEN, VGH_F, VGH_R)						
$r_{DS(ON)}$	High side ON resistance	I_{OUT} = 10 mA, sourcing (high side)		35		Ω
	Low side ON resistance	I_{OUT} = 10 mA, sinking (low side)		16		
t_{PLH}	GCLK rising edge propagation delay	GST rising edge to VST rising edge, C_{OUT} = 150 pF		50	100	ns
		GST rising edge to RESET rising edge, C_{OUT} = 150 pF		50	100	
t_{PHL}	GCLK falling edge propagation delay	GST falling edge to VST falling edge, C_{OUT} = 150 pF		50	100	ns
		GST falling edge to RESET falling edge, C_{OUT} = 150 pF		50	100	
t_{PLH}	EO rising edge propagation delay	EO rising edge to ODD falling edge, C_{OUT} = 150 pF		50	100	ns
		EO rising edge to EVEN falling edge, C_{OUT} = 150 pF		50	100	
t_{PHL}	EO falling edge propagation delay	EO falling edge to ODD rising edge, C_{OUT} = 150 pF		50	100	ns
		EO falling edge to EVEN rising edge, C_{OUT} = 150 pF		50	100	
t_{SU}	EO set-up time during abnormal operation	EO to GST rising edge		50	100	ns
t_{PLH}	BI-SCAN rising edge propagation delay	BI-SCAN rising edge to VGH_R rising edge, C_{OUT} = 150 pF		50	100	ns
		BI-SCAN rising edge of VGH_F falling edge, C_{OUT} = 150 pF		50	100	
t_{PHL}	BI-SCAN falling edge propagation delay	BI-SCAN falling edge to VGH_F rising edge, C_{OUT} = 150 pF		50	100	ns
		BI-SCAN falling edge of VGH_F falling edge, C_{OUT} = 150 pF		50	100	
t_{12}	Bi-SCAN dead time	VGH_F falling edge to VGH_R rising edge, C_{OUT} = 150 pF	20	500	1000	ns
t_{13}		VGH_R falling edge to VGH_F rising edge, C_{OUT} = 150 pF	20	500	1000	
GATE SHAPING (RE)						
$r_{DS(ON)}$	Gate shaping resistance	Measured between active CLK channel and RE at 10 mA		70		Ω
t_{PHL}	MCLK rising edge propagation delay	MCLK rising edge to CLK falling edge, C_{OUT} = 150 pF		65	100	ns

ELECTRICAL CHARACTERISTICS (continued)

V_{GH1}= 28V, V_{GH2}= 28V, V_{GL}= –10V, AV_{DD} = 15V, T_A = –40°C to 85°C; Typical values are at 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PANEL DISCHARGE (DISCHG)						
V_{SENSEL}	Discharge threshold voltage	V_{SENSE} falling	1.275	1.5	1.725	V
V_{HYS}	Discharge threshold voltage hysteresis	V_{SENSE} rising		100		mV
I_{SENSE}	VSENSE input current	V_{SENSE} = 2 V			±1	µA
$r_{DS(ON)}$	High side ON resistance	I_{OUT} = 10 mA, sourcing (high side)		35		Ω
	Low side ON resistance	I_{OUT} = 10 mA, sinking (low side)		16		
OPERATIONAL AMPLIFIER						
I_{AVDD}	Supply current	V_{CM} = 7.5 V, unity gain, no load		4	6	mA
V_{IO}	Input offset voltage	V_{CM} = 7.5 V	–25		25	mV
I_{IB}	Input bias current	V_{CM} = 7.5 V	–100		100	nA
BW	Unity gain 3 dB bandwidth	V_{CM} = 7.5 V, V_{IN} = 63 mV_{PP}, no load		70		MHz
AV_{OL}	Open loop gain	V_{CM} = 7.5 V, no load		80		dB
CMRR	Common-mode rejection ratio	CMRR = ΔV_{CM} / ΔV_{OS}, V_{CM} = 5.5 V to 9.5 V		90		dB
PSRR	Power supply rejection ratio	PSRR = ΔAV_{DD} / ΔV_{OS}, AV_{DD} = 8V to 20 V		80		dB
$r_{DS(ON)}$	High-side output resistance	V_{POS} = 9.5 V, V_{NEG} = 7.5 V, I_{OUT} = 10 mA		15		Ω
	Low-side output resistance	V_{POS} = 7.5 V, V_{NEG} = 9.5 V, I_{OUT} = 10 mA		35		
I_{PK}	Peak output current	Unity gain, V_{POS} = 7.25V, V_{OUT} = 7.5V	200	414		mA
		Unity gain, V_{POS} = 7.75V, V_{OUT} = 7.5V	200	344		

PIN ASSIGNMENT
TOP VIEW



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
CLK1	1	O	CLK1 output
CLK2	2	O	CLK2 output
CLK3	3	O	CLK3 output
CLK4	4	O	CLK4 output
CLK5	5	O	CLK5 output
CLK6	6	O	CLK6 output
RE	7	O	Gate shaping resistor connection
VGH_R	8	O	VGH_R output
VGH_F	9	O	VGH_F output
ODD	10	O	ODD output
EVEN	11	O	EVEN output
VST	12	O	VST output
RESET	13	O	RESET output
DISCHG	14	O	DISCHG output
VGL	15	P	Negative supply voltage
VGH1	16	P	Positive supply voltage for all outputs except ODD and EVEN
VGH2	17	P	Positive supply voltage for ODD and EVEN outputs
OUT	18	O	Operational amplifier output
NEG	19	I	Operational amplifier inverting input
POS	20	I	Operational amplifier non-inverting input
AVDD	21	P	Operational amplifier positive supply

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	22	P	Ground
VSENSE	23	I	Voltage sense input for discharge function
EO	24	I	EO input
GST	25	I	GST input
MCLK	26	I	MCLK input
GCLK	27	I	GCLK input
BI-SCAN	28	I	BI-SCAN input
Exposed Thermal Die	N/A	P	Connect to V_{GL}

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

TITLE		TEST CONDITIONS	FIGURE
Peak Output Current vs	CLKx	10nF load	Figure 1
	VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 2
	DISCHARGE		Figure 3
Rise Time vs	CLKx	47Ω + 10nF load	Figure 4
	VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 5
	DISCHARGE		Figure 6
	CLKx	150 pF load	Figure 7
	VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 8
	DISCHARGE		Figure 8
Fall Time vs	CLKx	47Ω + 10nF load	Figure 10
	VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 11
	DISCHARGE		Figure 12
	CLKx	150 pF load	Figure 13
	VST, RESET, ODD, EVEN, VGH_F, VGH_R		Figure 14
	DISCHARGE		Figure 15
V_{SENSE} Threshold vs	VSENSE, DISCH		Figure 16
Power-Up Sequence vs	CLKs, VGH, VGL		Figure 17
Power-Down Sequence vs	CLKs, VGH, VGL, DISCH		Figure 18
Small-Signal 3dB Bandwidth	AVDD = 15 V, VCM = 7.5 V, V_{IN} = 63 mV_{PP}, Unity gain, $R_{FEEDBACK}$ = 0 Ω	No load	Figure 19
Peak Output Current	AVDD = 15 V, VCM = 7.5 V, V_{IN} = 2 V_{PP}, Open-loop	10 nF load	Figure 20
Slew Rate	V_{OUT} falling	C_{OUT} = 150pF, No Load	Figure 21

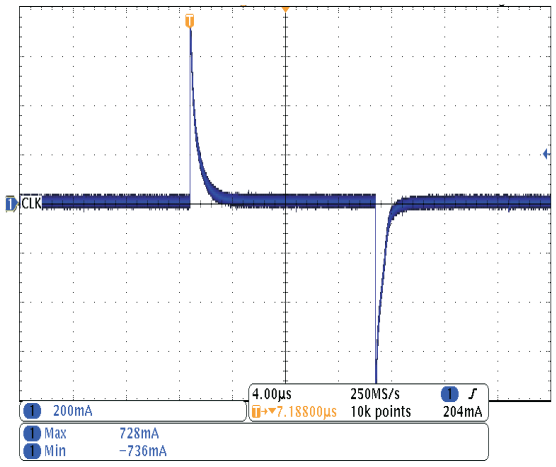


Figure 1. Peak Output Current - CLKs

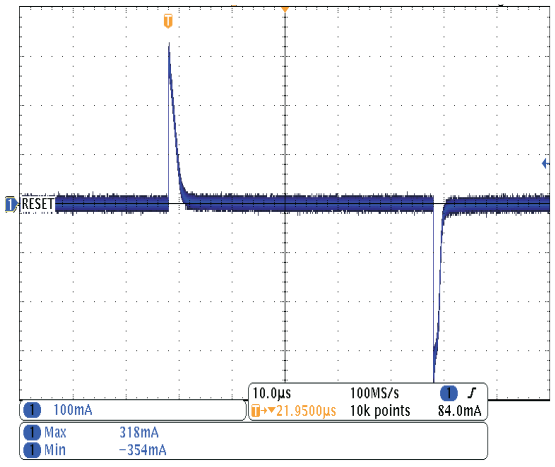


Figure 2. Peak Output Current - VST, RESET, etc.

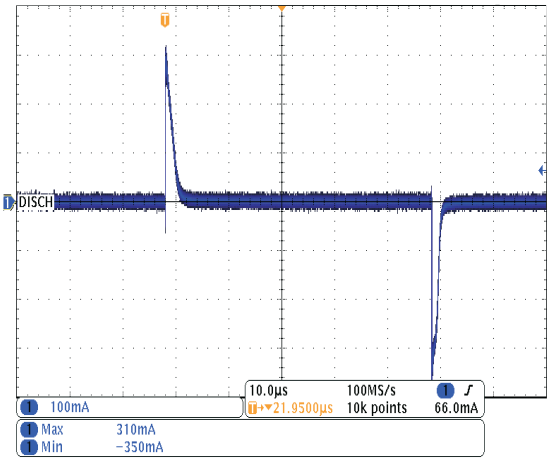


Figure 3. Peak Output Current - DISCHARGE

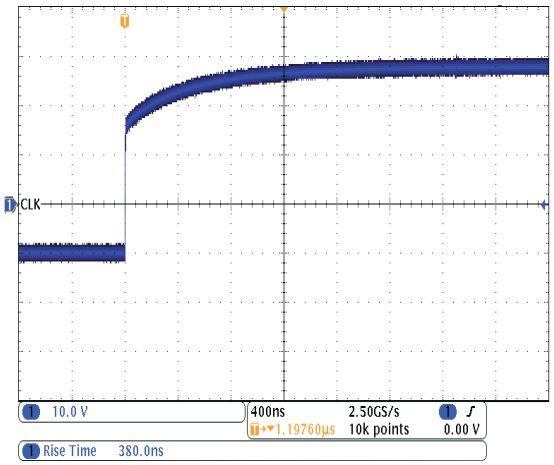


Figure 4. Rise Time - CLKs

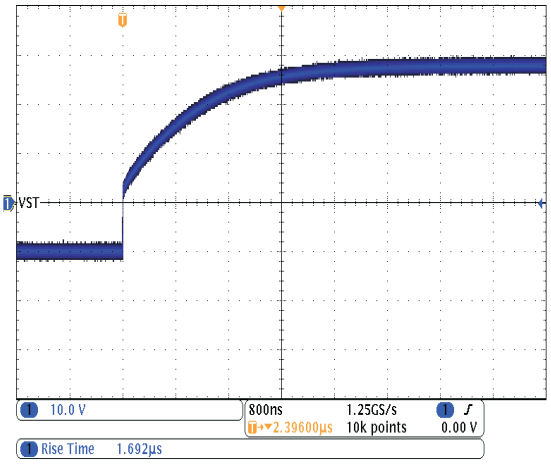


Figure 5. Rise Time – VST, RESET, etc.

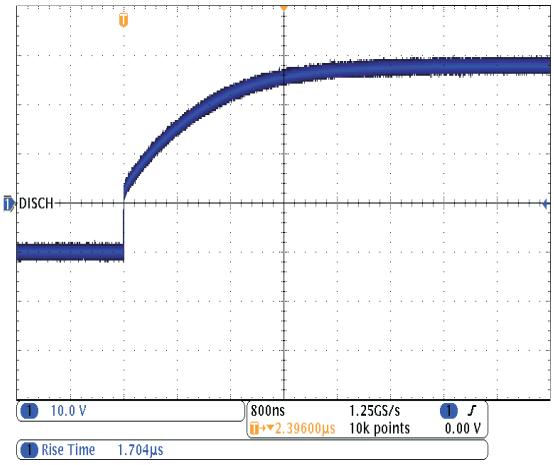


Figure 6. Rise Time – DISCHARGE

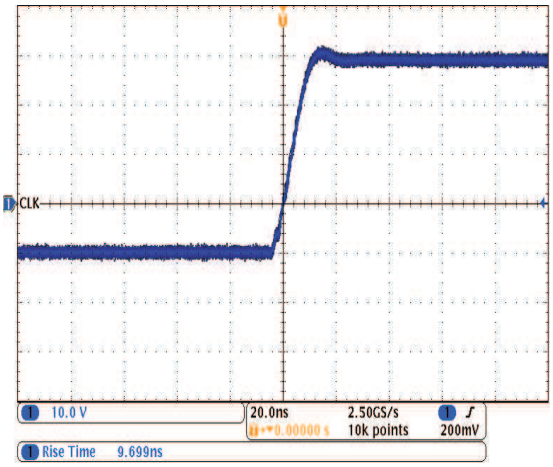


Figure 7. Rise Time - CLKs

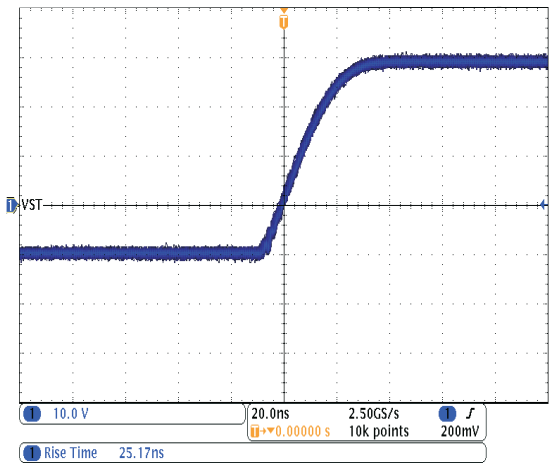


Figure 8. Rise Time - VST, RESET, etc.

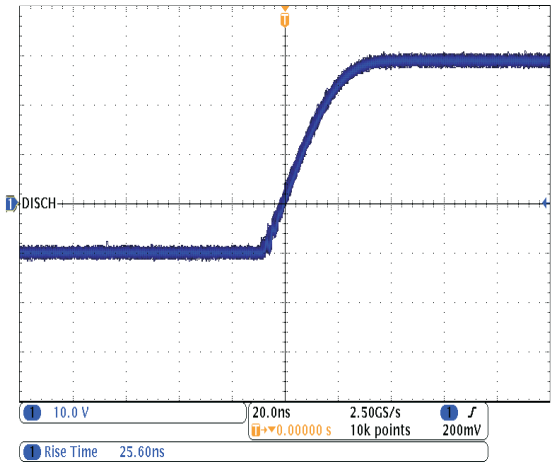


Figure 9. Rise Time - DISCHARGE

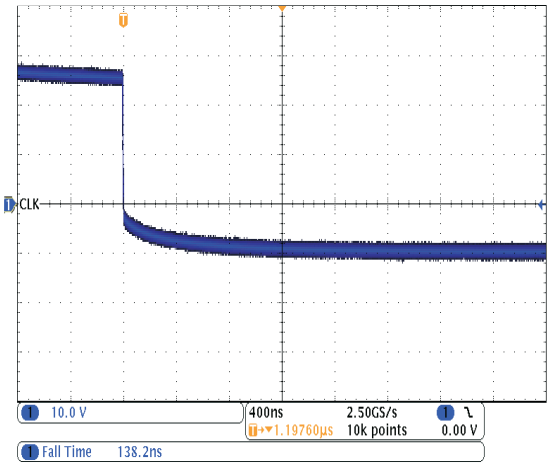


Figure 10. Fall Time – CLKs

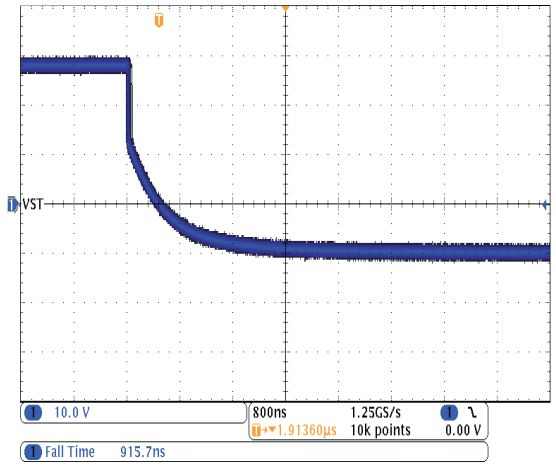


Figure 11. Fall Time – VST, RESET, etc.

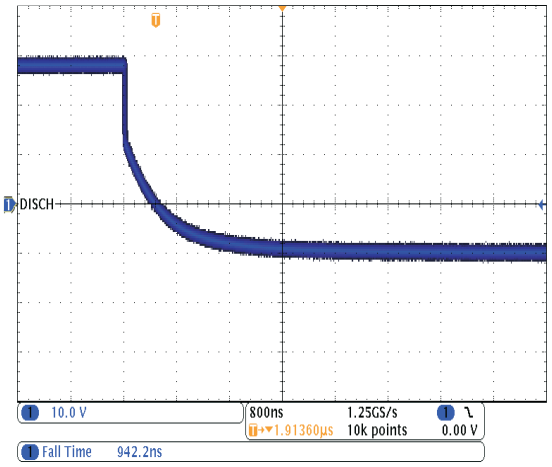


Figure 12. Fall Time – DISCHARGE

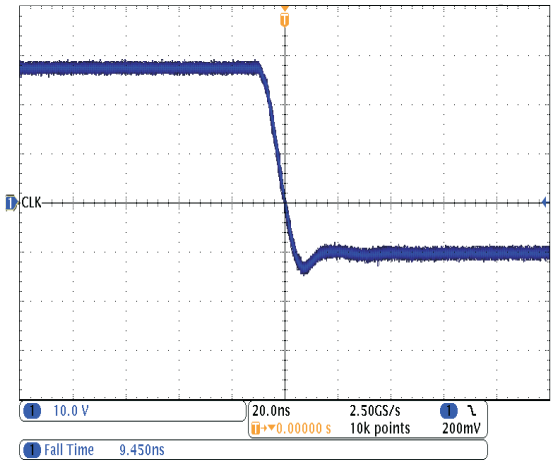


Figure 13. Fall Time – CLKs

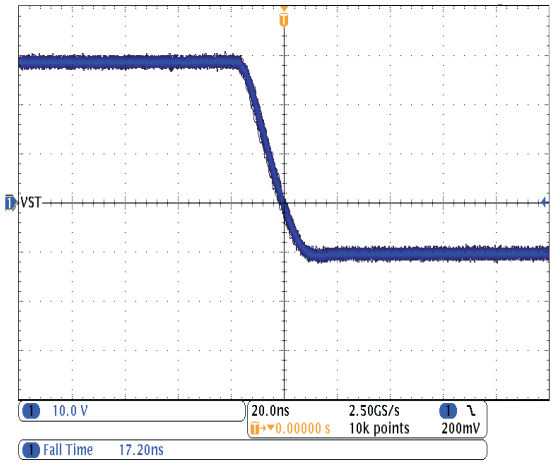


Figure 14. Fall Time – VST, RESET, etc.

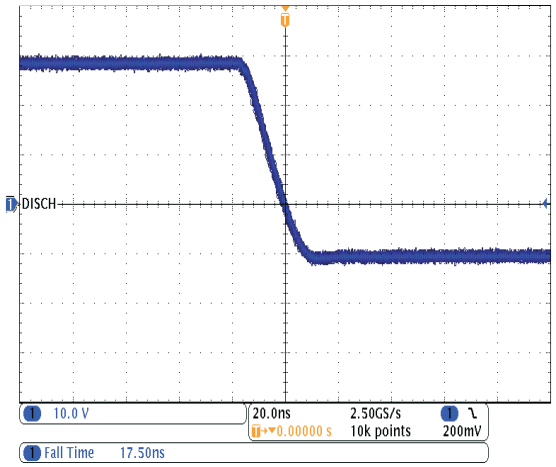


Figure 15. Fall Time – DISCHARGE

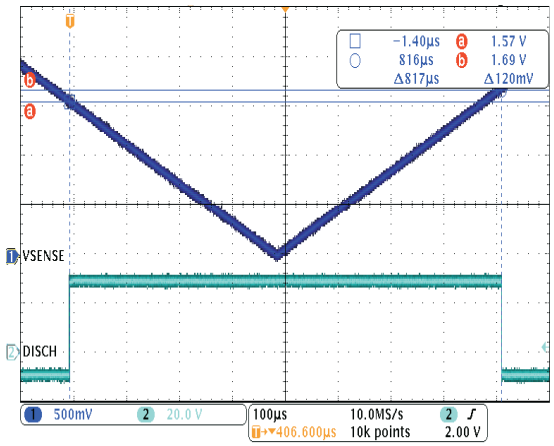


Figure 16. V_{SENSE} Threshold – VSENSE, DISCHARGE

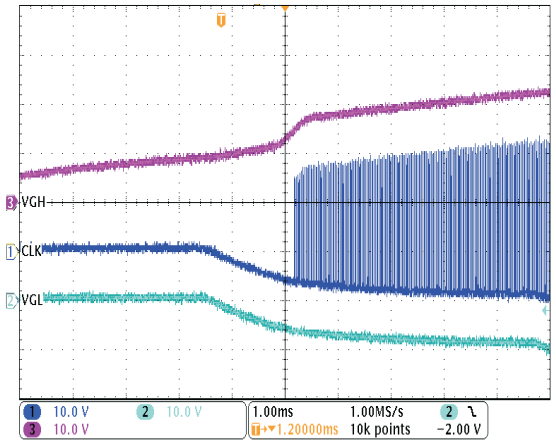


Figure 17. Power Up Sequence

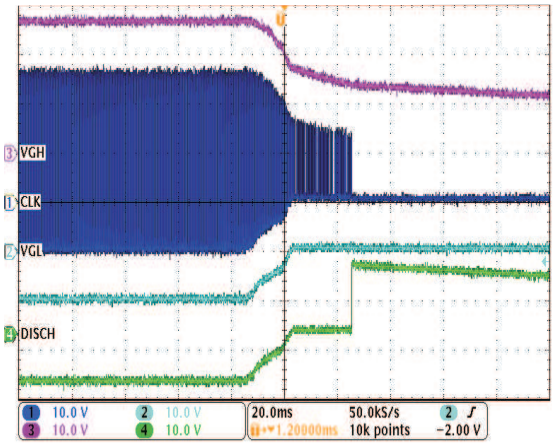


Figure 18. Power Down Sequence

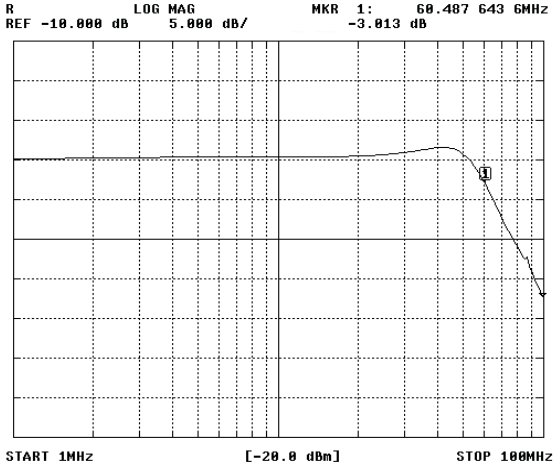


Figure 19. Small-Signal 3dB Bandwidth

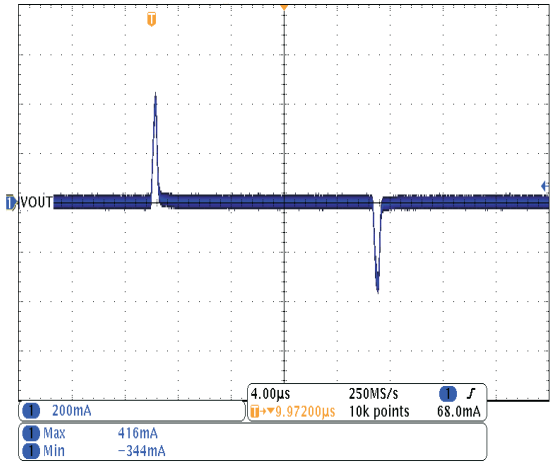


Figure 20. Peak Output Current

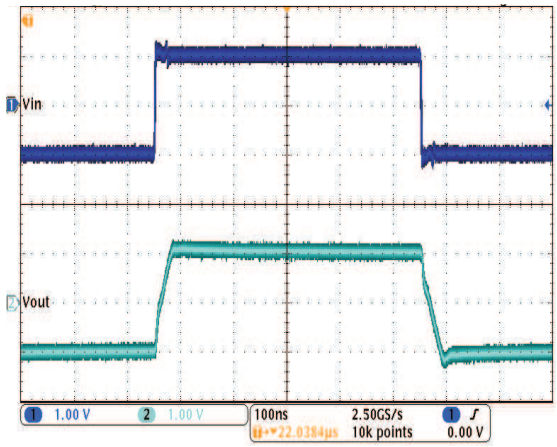


Figure 21. Slew Rate

DETAILED DESCRIPTION

Level Shifter

An internal block diagram of the level shifter block is shown in Figure 22.

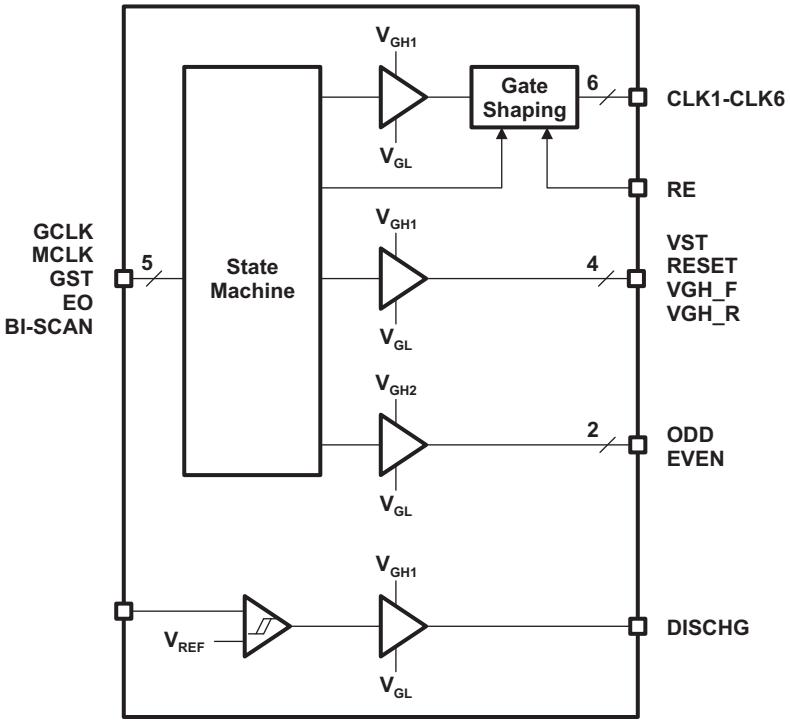


Figure 22. Internal Block Diagram

State Machine

The state machine generates 12 output signals (all outputs except DISCHG) from the five input signals, as described below.

GCLK

The rising edge of GCLK defines the rising edge of the active CLK channel. The phase difference between adjacent CLK signals is 60°, which means that the frequency of the output clocks is exactly one sixth the frequency of the GCLK signal (see Figure 23 to Figure 26).

The falling edge of GCLK has no effect.

MCLK

The rising edge of MCLK defines the start of gate-shaping for the active CLK channel. The phase difference between adjacent CLK signals is 60°, which means that the frequency of the output clocks is exactly one sixth the frequency of the MCLK signal (see Figure 23 to Figure 26).

The falling edge of MCLK defines the falling edge of the active CLK channel (and, by definition, the end of gate-shaping).

GST

The function of the GST signal depends on the state of GCLK when the GST pulse occurs. When GCLK is low (see Figure 23 and Figure 29, and section describing VST behavior):

- the rising edge of GST defines the rising edge of VST
- the falling edge of GST defines the falling edge of VST
- the GST signal indicates the start of a new frame, and resets all internal counters in the state machine

When GCLK is high (see Figure 24 and Figure 26 and section describing RESET behavior):

- the rising edge of GST defines the rising edge of RESET
- the falling edge of GST defines the falling edge of RESET

EO

During normal operation a pulse applied to EO toggles the ODD and EVEN outputs (see section below describing the ODD and EVEN outputs).

See also section describing Abnormal Operation.

BI-SCAN

The BI-SCAN signal is used to select forward or reverse operation.

During forward operation (BI-SCAN=low), VGH_F=high, VGH_R=low and the clock signals are output in the following order:

(start of frame) 4 – 5 – 6 – 1 – 2 – 3 – 4 – 5 – 6 – 1 – 2 – 3 . . . . . 4 – 5 – 6 – 1 – 2 – 3 (end of frame)

During reverse operation (BI-SCAN=high), VGH_F=low, VGH_R=high and the clock signals are output in the following order:

(start of frame) 3 – 2 – 1 – 6 – 5 – 4 – 3 – 2 – 1 – 6 – 5 – 4 . . . . . 3 – 2 – 1 – 6 – 5 – 4 (end of frame)

The BI-SCAN pin is internally pulled down by a 100kΩ (typical) resistor.

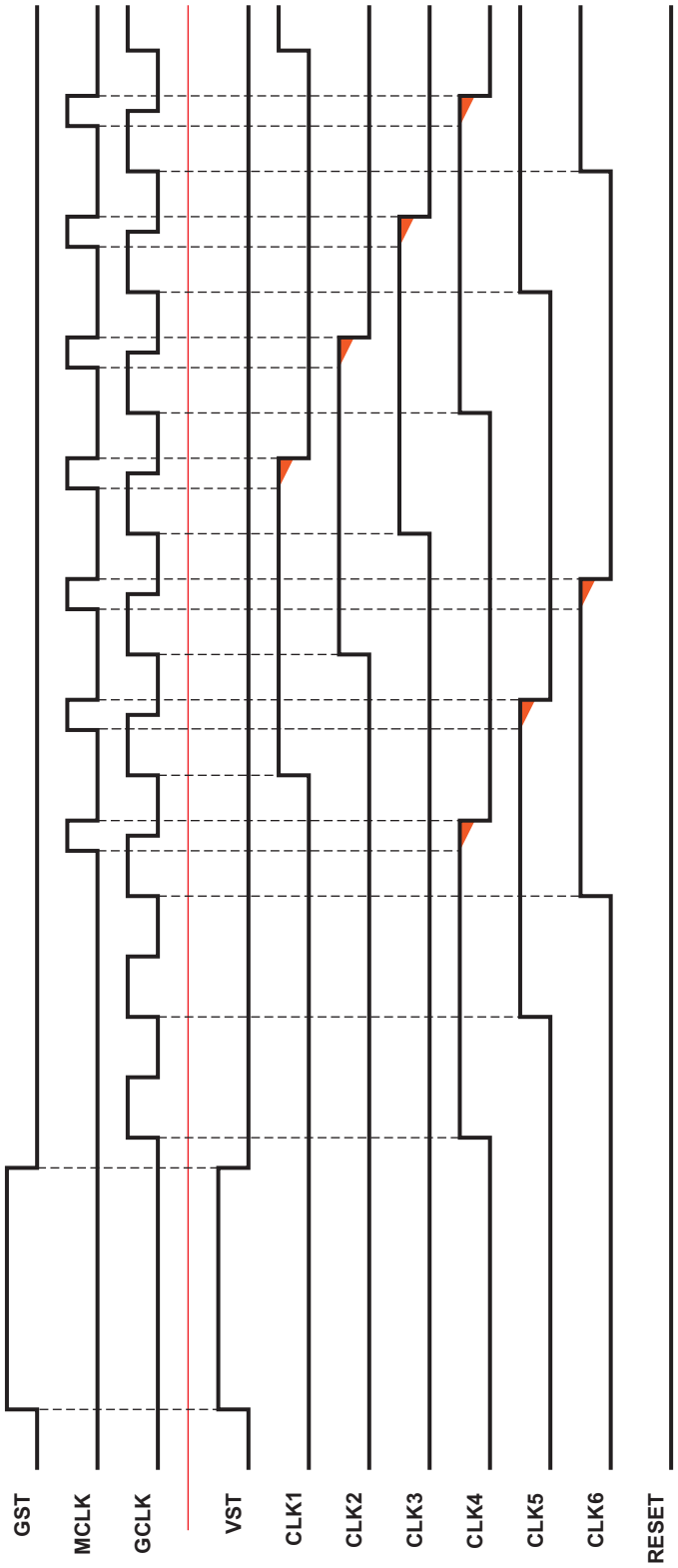


Figure 23. Timing Diagram: Normal Operation, Start of Frame

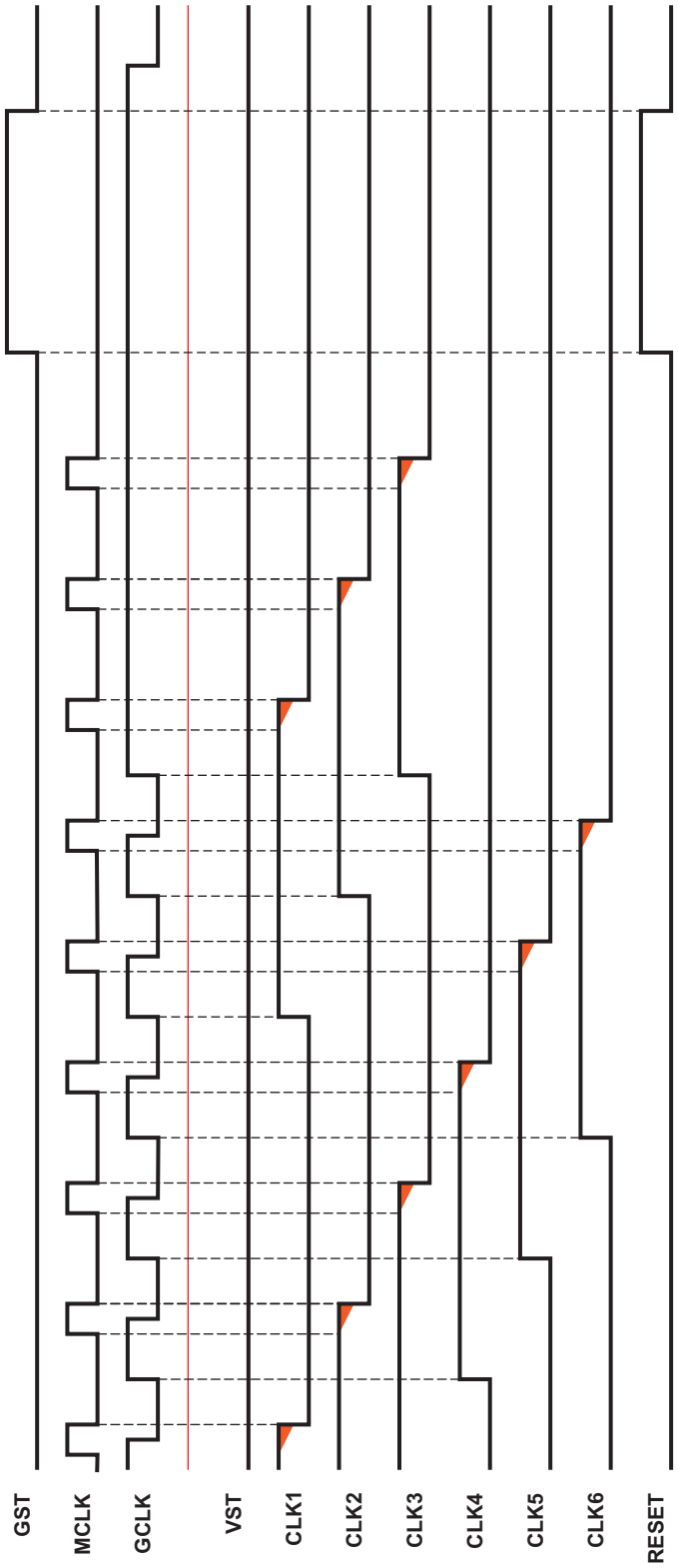


Figure 24. Timing Diagram: Normal Operation, End of Frame

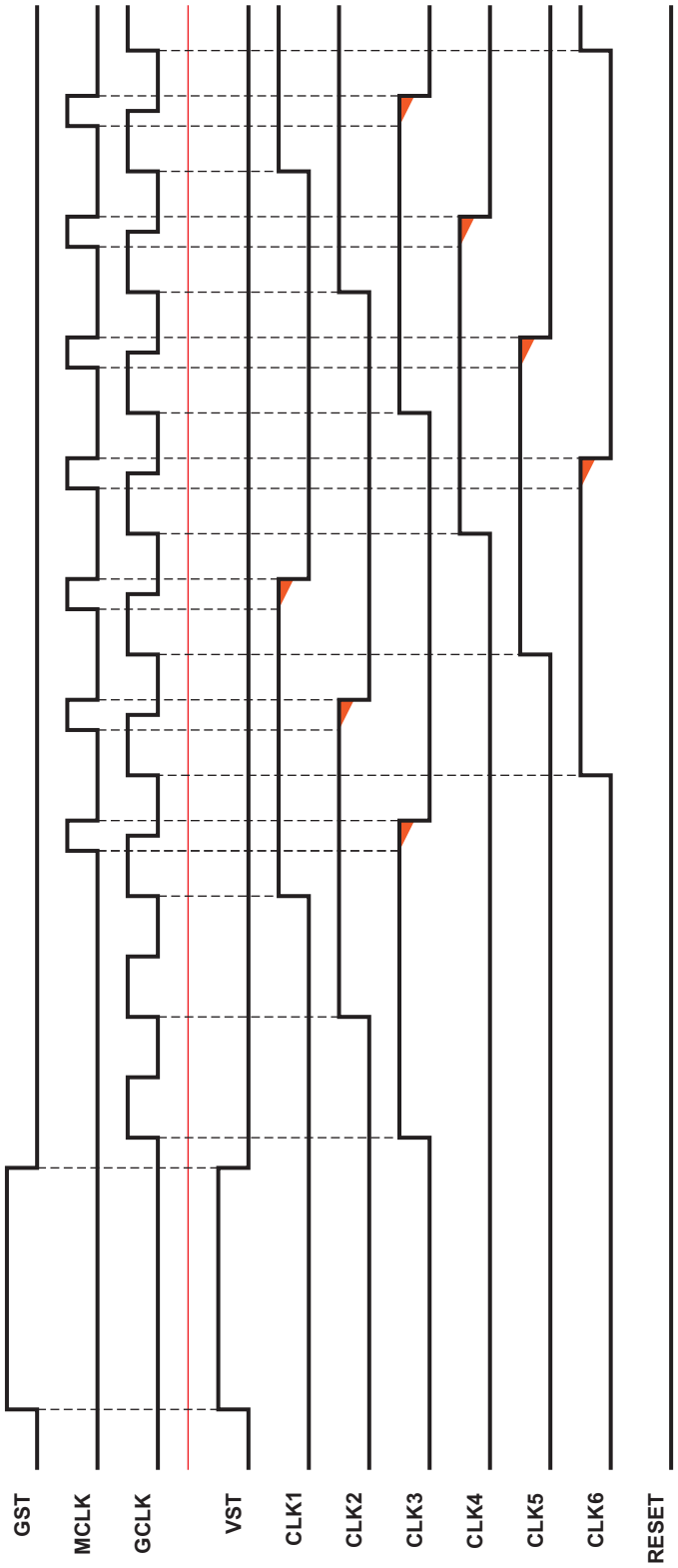


Figure 25. Timing Diagram: Reverse Operation, Start of Frame

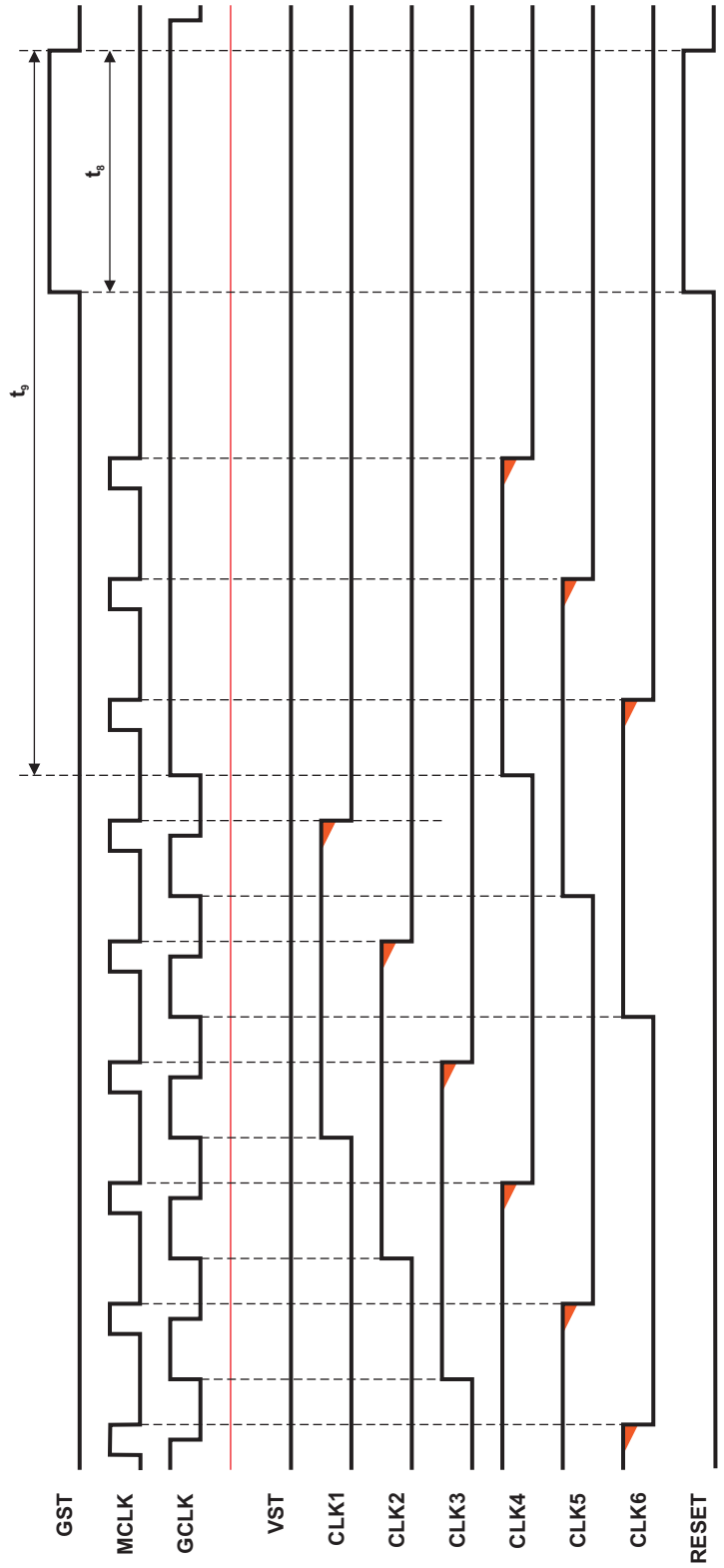


Figure 26. Timing Diagram: Reverse Operation, End of Frame

VGH_F and VGH_R

The VGH_F and VGH_R signals follow the BI-SCAN and GST inputs in accordance with Table 1.

Table 1. Truth Table

	INPUTS			OUTPUTS		NORMAL OCCURRENCE
	BI-SCAN	GST	Q	VGH_F	VGH_R	
Normal	1	X	X	0	1	Reverse, power-up Forward to reverse
	0	X	0	1	0	Forward, power-up
	0	↑	1	1	0	Reverse to forward
	0	0	0	1	0	Forward, power-down
	0	0	1	0	1	Reverse, power-down
Abnormal	Same as Normal mode					

The VGH_F and VGH_R outputs feature a dead time (t_{12} and t_{13}) such that when BI-SCAN changes state VGH_F and VGH_R are temporarily both low before the active channel goes high (see Figure 27).

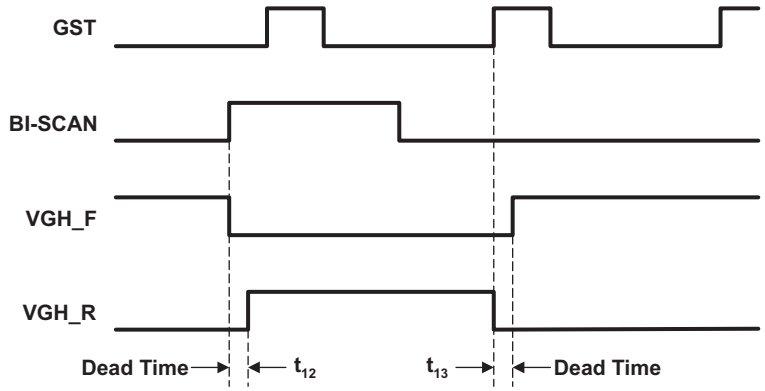


Figure 27. VGH_F and VGH_R Operation, Showing Dead Time

To ensure the VGH_F and VGH_R outputs remain valid during power-down (when the BI-SCAN signal may not be valid), the BI-SCAN signal is latched on every rising edge of GST (see Figure 28).

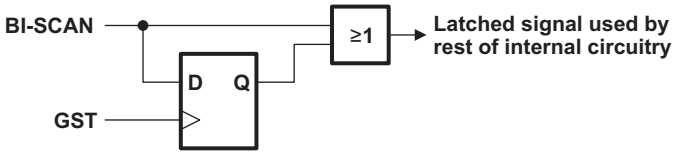


Figure 28. BI-SCAN Latching Scheme

The VGH_F and VGH_R channels follow a well defined characteristic during power-up and power-down (see Power Supply Sequencing).

VST

The VST signal follows the GST and GCLK input signals in accordance with the truth table below (see also Figure 23 to Figure 26).

	INPUTS		OUTPUT
OPERATION	GST	GCLK	VST
Normal	1	0	1
	1	1	0
	0	X	0

	INPUTS		OUTPUT
OPERATION	GST	GCLK	VST
Abnormal	X	X	0

RESET

The RESET output is derived from the GST and GCLK signals in accordance with the truth table below (see also Figure 23 to Figure 26).

	INPUTS		OUTPUT
OPERATION	GST	GCLK	VST
Normal	0	X	0
	1	0	0
	1	1	1
Abnormal	X	X	0

ODD and EVEN

The ODD and EVEN outputs toggle on the rising edge of the EO input signal in accordance with the truth table below. The pulse width of the EO signal defines a dead time during which both ODD and EVEN outputs are temporarily low (see Figure 29).

	INPUT	OUTPUTS	
OPERATION	EO	EVEN	ODD
Power-Up	X	1	0
Normal	↑	toggle(1)	toggle(1)
Abnormal	X	1	0

(1) With dead time

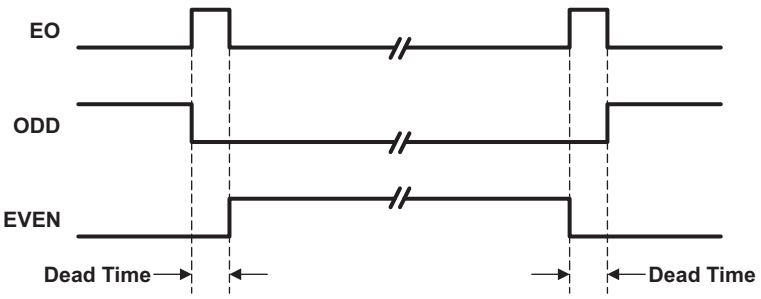


Figure 29. ODD and EVEN Generation, Showing Dead Time

Abnormal Operation

The TPS65198 supports abnormal operation. Abnormal operation is detected when EO is high during the rising edge of GST (see Figure 30), after which the level shifter outputs are forced to the following state:

1. CLK1-CLK6 low
2. VST, RESET low
3. ODD and EVEN in power-up state (EVEN high, ODD low) (2)
4. VGH_F and VGH_R not changed (outputs follow BI-SCAN input as in normal operation)

Normal operation is resumed the next time EO is low during the rising edge of GST. Upon exiting abnormal operation the state machine adopts its normal start-of-frame initial state.

(2) Note that because of the dead time introduced by the EO signal during normal operation, a short low pulse may appear on the EVEN output when abnormal operation is detected (see Figure 30).

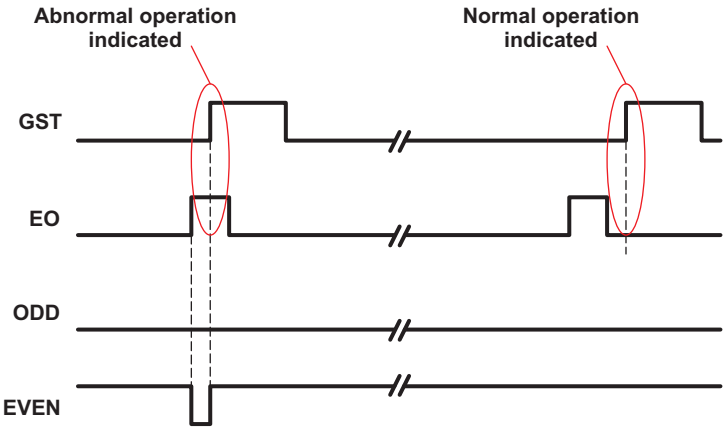


Figure 30. EO During Abnormal Operation, EVEN Initially High

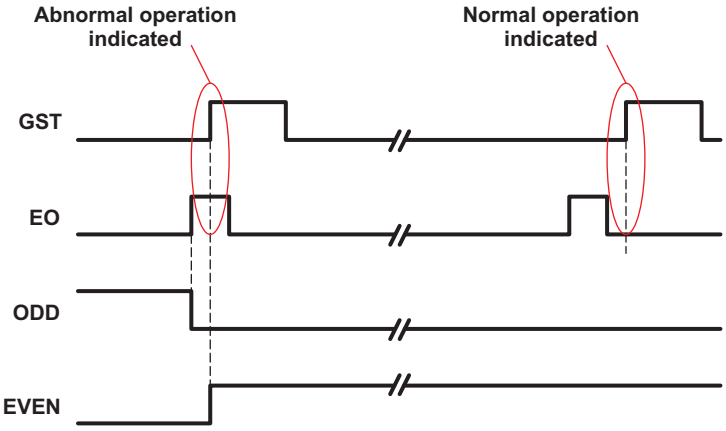


Figure 31. EO During Abnormal Operation, EVEN Initially Low

CLK1 to CLK6

The CLK outputs go high on the rising edge of GCLK and go low on the falling edge of MCLK. The CLK outputs' frequency is exactly one sixth of the GCLK and MCLK frequencies and adjacent CLK channels are separated by 60° phase difference.

The CLK outputs are generated in a specific order that depends on whether the device is operating in forward or reverse mode (see Figure 23 to Figure 26 and the section describing BI-SCAN operation).

Gate Voltage Shaping

The clock outputs CLK1 to CLK6 support gate voltage shaping, which can help reduce image flickering in certain applications. A simplified block diagram of one of the clock channels is shown in Figure 32.

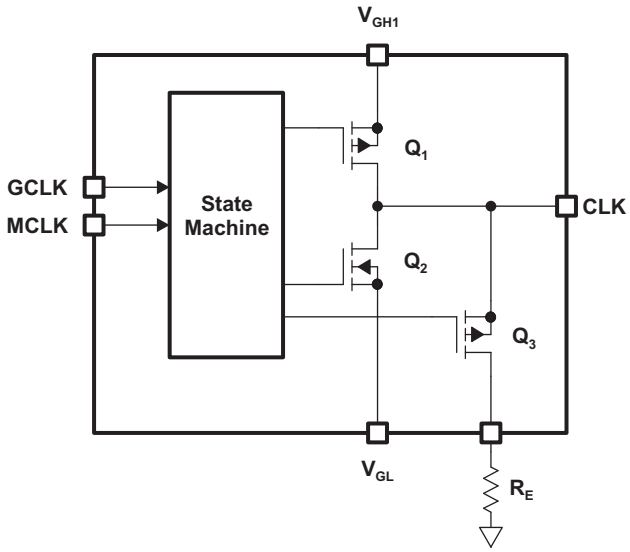


Figure 32. CLK Output Stage

- On the rising edge of the GCLK, the active channel's Q_1 is enabled and its Q_2 disabled; the output goes to V_{GH1}.
- Gate voltage shaping starts on the rising edge of MCLK, which disables Q_1 and enables Q_3. The LCD panel's pixel and storage capacitor now discharge through Q_3 at a rate determined by the external resistor R_E (see Figure 33).
- On the falling edge of MCLK, Q_3 is disabled and Q_2 enabled; the output goes to V_{GL}.

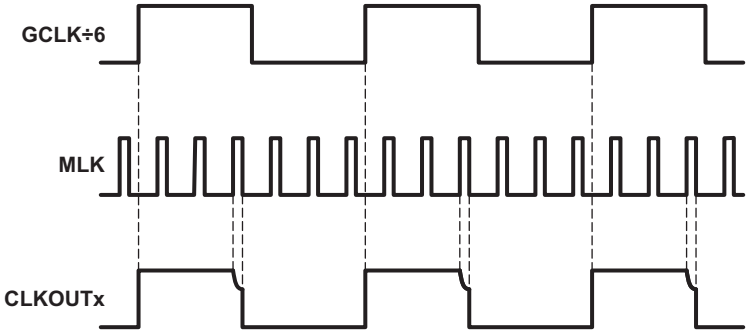


Figure 33. Gate Shaping Timing Diagram

Panel Discharge

In addition to the 12 level shifter channels described above, the TPS65198 contains one output specifically intended for discharging the LCD panel during power-down (see Figure 34). The discharge channel uses the input signal connected to the VSENSE pin, which features a Schmitt trigger input stage. Figure 34 and Figure 35 show the discharge behavior during power-up and power-down.

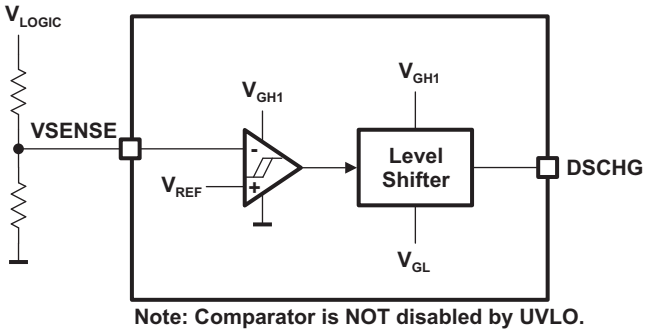


Figure 34. Discharge Internal Block Diagram

When the discharge function is active, the level shifter outputs enter Abnormal Mode, as defined below.

Power Supply Sequencing (CLK1-CLK6, VST, RESET)

These outputs track V_{GL} when $V_{GH1}<V_{UVLO}$ or $V_{SENSE}<V_{REF}$ and operate normally when $V_{GH1}>V_{UVLO}$ and $V_{SENSE}>V_{REF}$ (see Figure 35 and Figure 36).

Power Supply Sequencing (ODD, EVEN)

EVEN tracks V_{GL} when $V_{GH1}<V_{UVLO}$ and operates normally when $V_{GH1}>V_{UVLO}$ and $V_{SENSE}>V_{REF}$ (see Figure 35 and Figure 36). EVEN tracks V_{GH} when $V_{SENSE}<V_{REF}$.

ODD tracks V_{GL} when $V_{GH1}<V_{UVLO}$ and operates normally when $V_{GH1}>V_{UVLO}$ and $V_{SENSE}>V_{REF}$ (see Figure 35 and Figure 36). ODD tracks V_{GL} when $V_{SENSE}<V_{REF}$.

Power Supply Sequencing (VGH_F, VGH_R)

VGH_F and VGH_R track V_{GL} when $V_{GH1}<V_{UVLO}$ and operate normally when $V_{GH1}>$VUVLO (see Figure 35 and Figure 36).

During power-down these outputs remain in the state they were when the last rising edge of GST occurred.

Power Supply Sequencing (Panel Discharge)

- During power-up, when $V_{SENSE}<V_{REF}$, DSCHG tracks V_{GL}.
- During normal operation, when $V_{SENSE}>V_{REF}$, DSCHG tracks V_{GL}.
- During power-down, when $V_{SENSE}<V_{REF}$, DSCHG tracks V_{GH}.

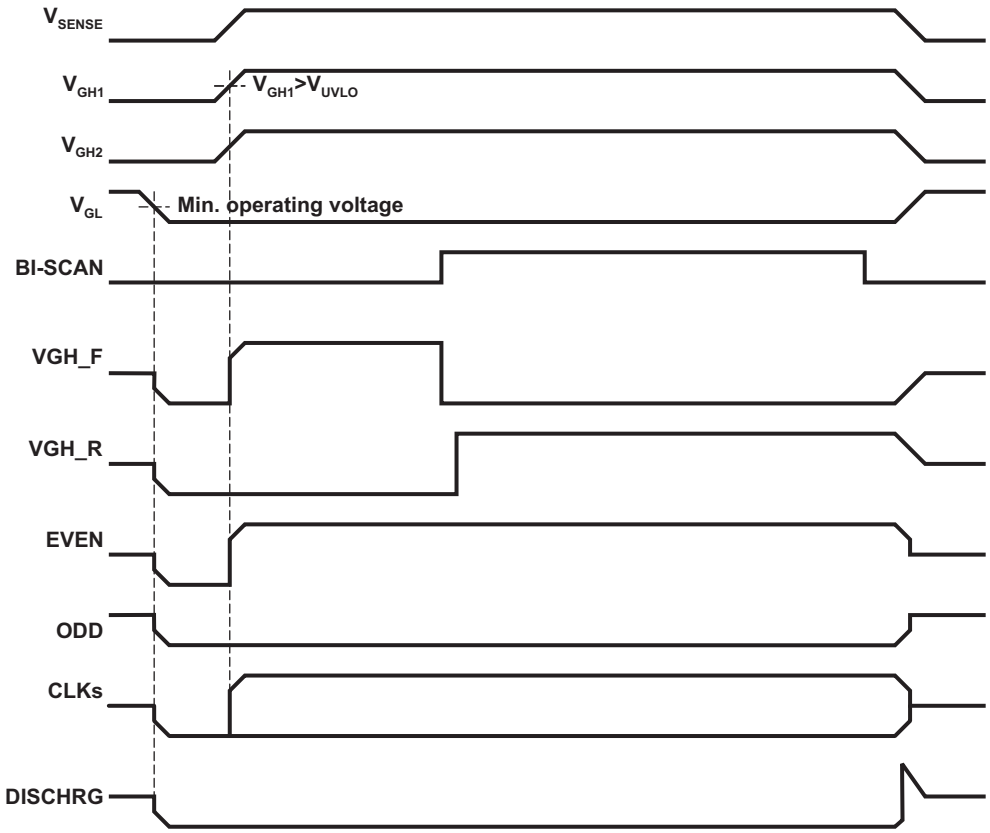


Figure 35. Power Supply Sequencing During Forward Operation

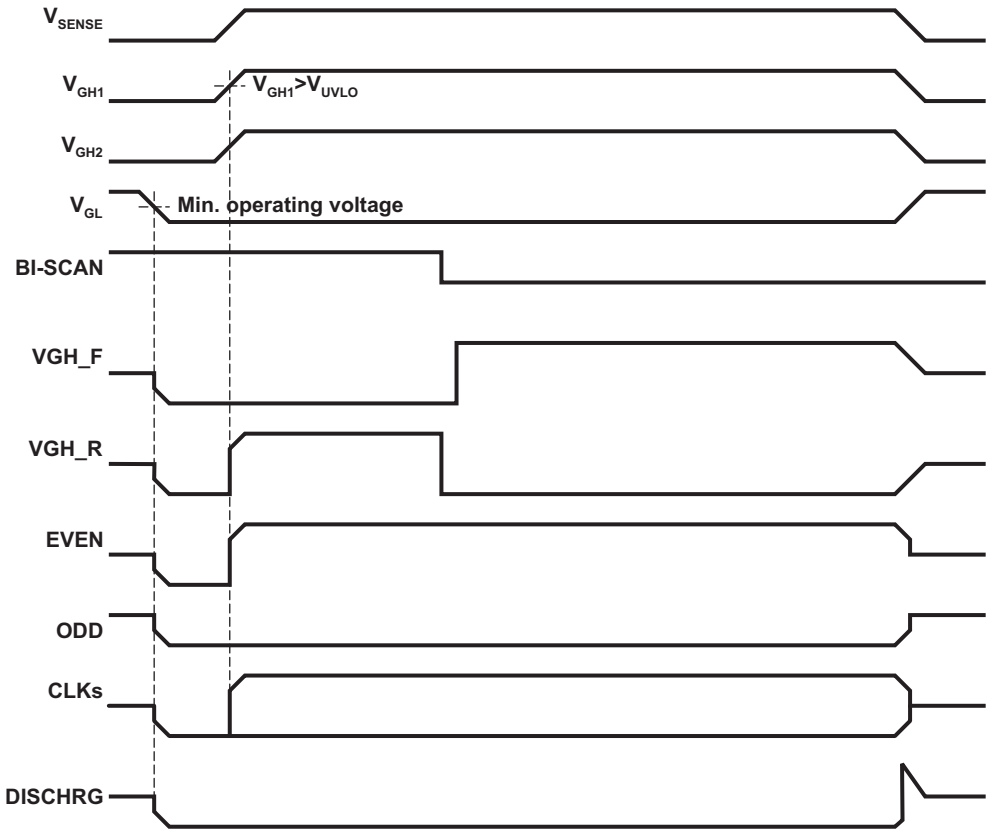


Figure 36. Power Supply Sequencing During Reverse Operation

Operational Amplifier

The operational amplifier included in the TPS65198 has been optimized for buffering the V_{COM} voltage used in LCD panels. Its high slew rate, high output current and wide bandwidth enable it to drive the dynamic loads present on V_{COM}. Like most operational amplifiers, this amplifier may become unstable if a highly capacitive load is connected to its output. It is therefore recommended **not** to connect additional capacitance between V_{COM} and GND in an attempt to decouple it. Not only could this create stability problems, the high performance of the operational amplifier mean that such measures are unnecessary in typical applications.

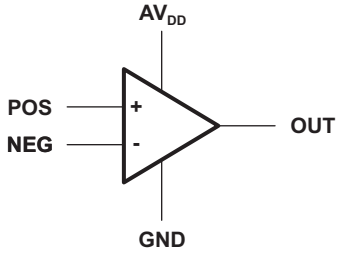


Figure 37. Operational Amplifier Block Diagram

APPLICATION INFORMATION

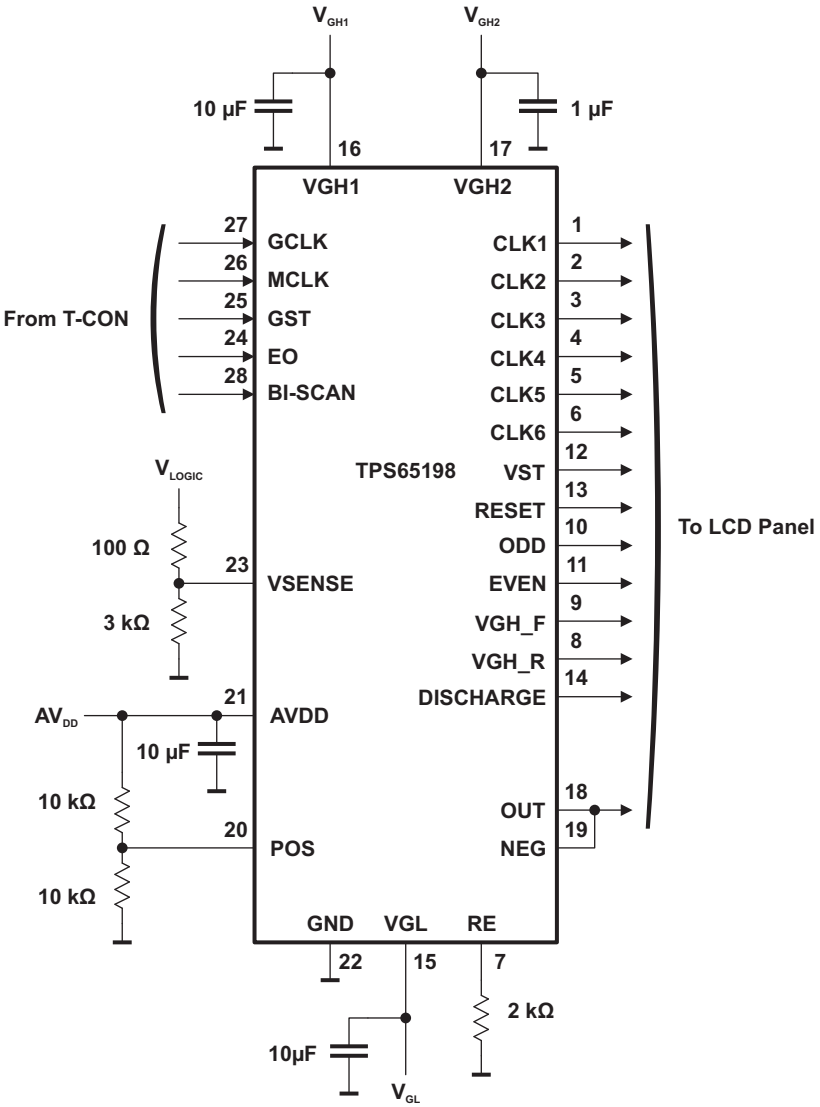


Figure 38. Typical Application Circuit

REVISION HISTORY

Changes from Original (June 2011) to Revision A **Page**

- Changed Condition statement of the Electrical Characaterisics table from T_J to T_A 3
- Changed Condition statement of the Electrical Characaterisics table from T_J to T_A 4
- Added I_{PK} spec to Elec Characteristics table. 4

Changes from Revision A (November 2011) to Revision B **Page**

- Changed V_{IH} spec from 2.0 MAX to 1.4 MAX in Typical Characteristics 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65198RUYR	ACTIVE	WQFN	RUY	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65198	Samples
TPS65198RUYT	ACTIVE	WQFN	RUY	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65198	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

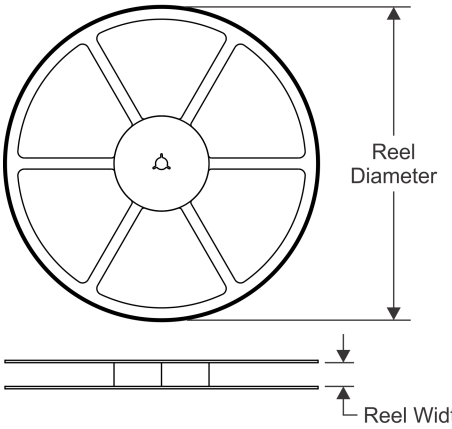
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

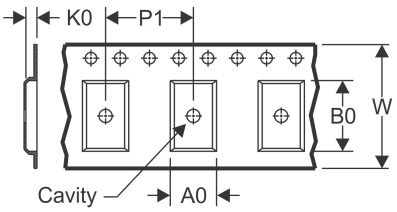
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

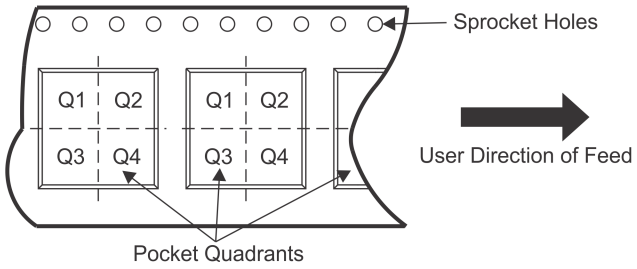


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

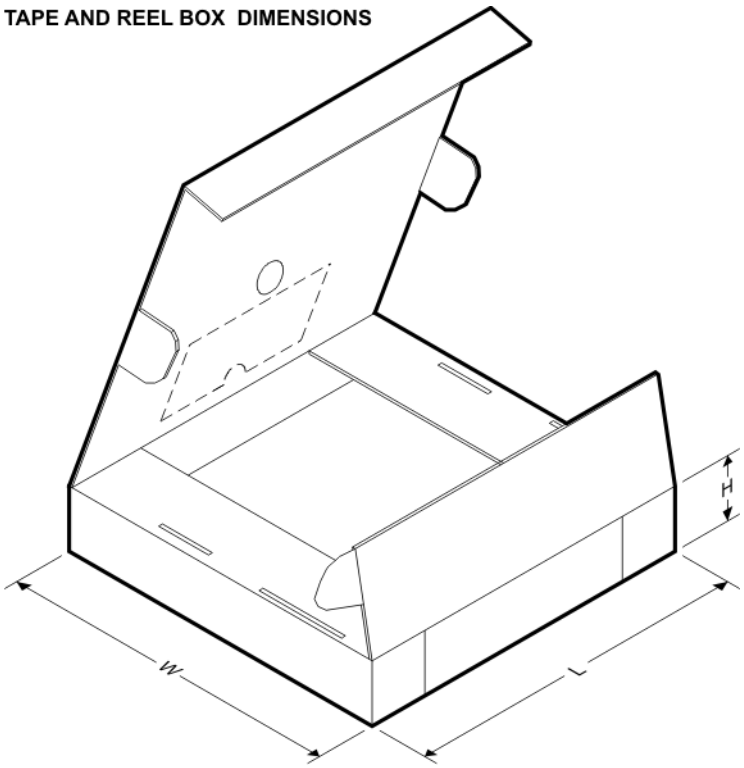
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65198RUYR	WQFN	RUY	28	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65198RUYT	WQFN	RUY	28	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65198RUYT	WQFN	RUY	28	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

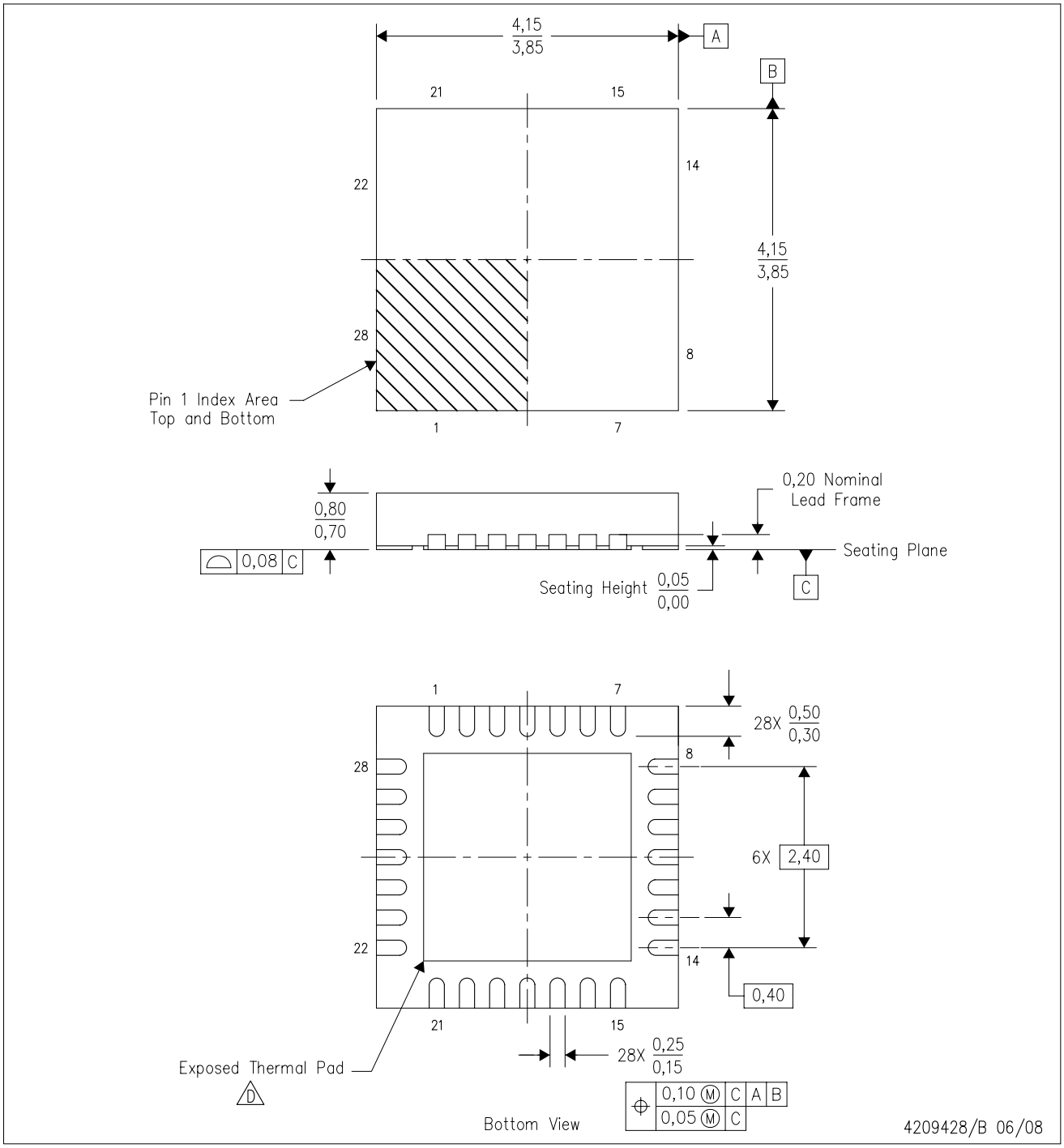
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65198RUYR	WQFN	RUY	28	3000	367.0	367.0	35.0
TPS65198RUYT	WQFN	RUY	28	250	210.0	185.0	35.0
TPS65198RUYT	WQFN	RUY	28	250	210.0	185.0	35.0

RUY (S–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

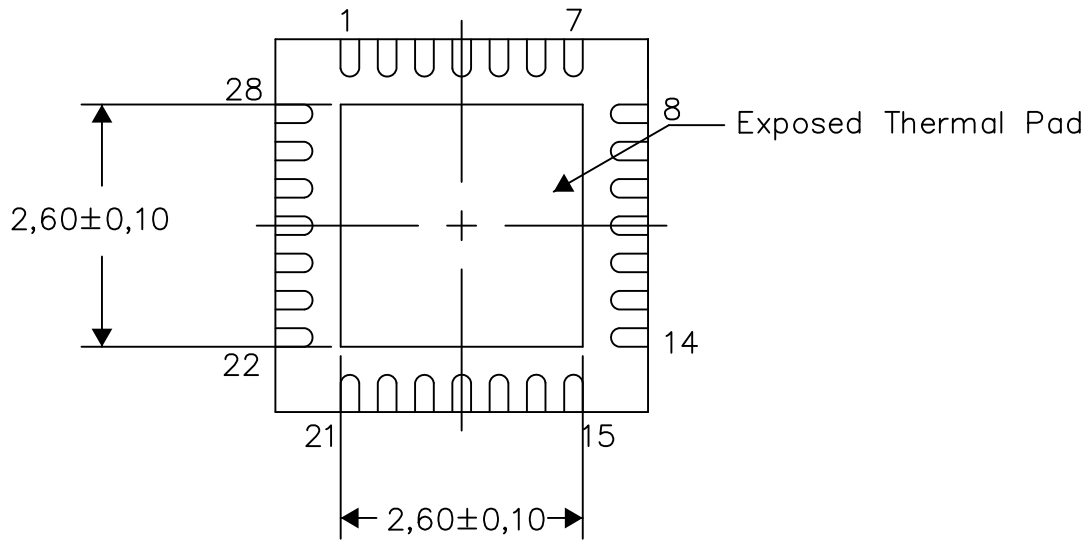
RUY (S–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



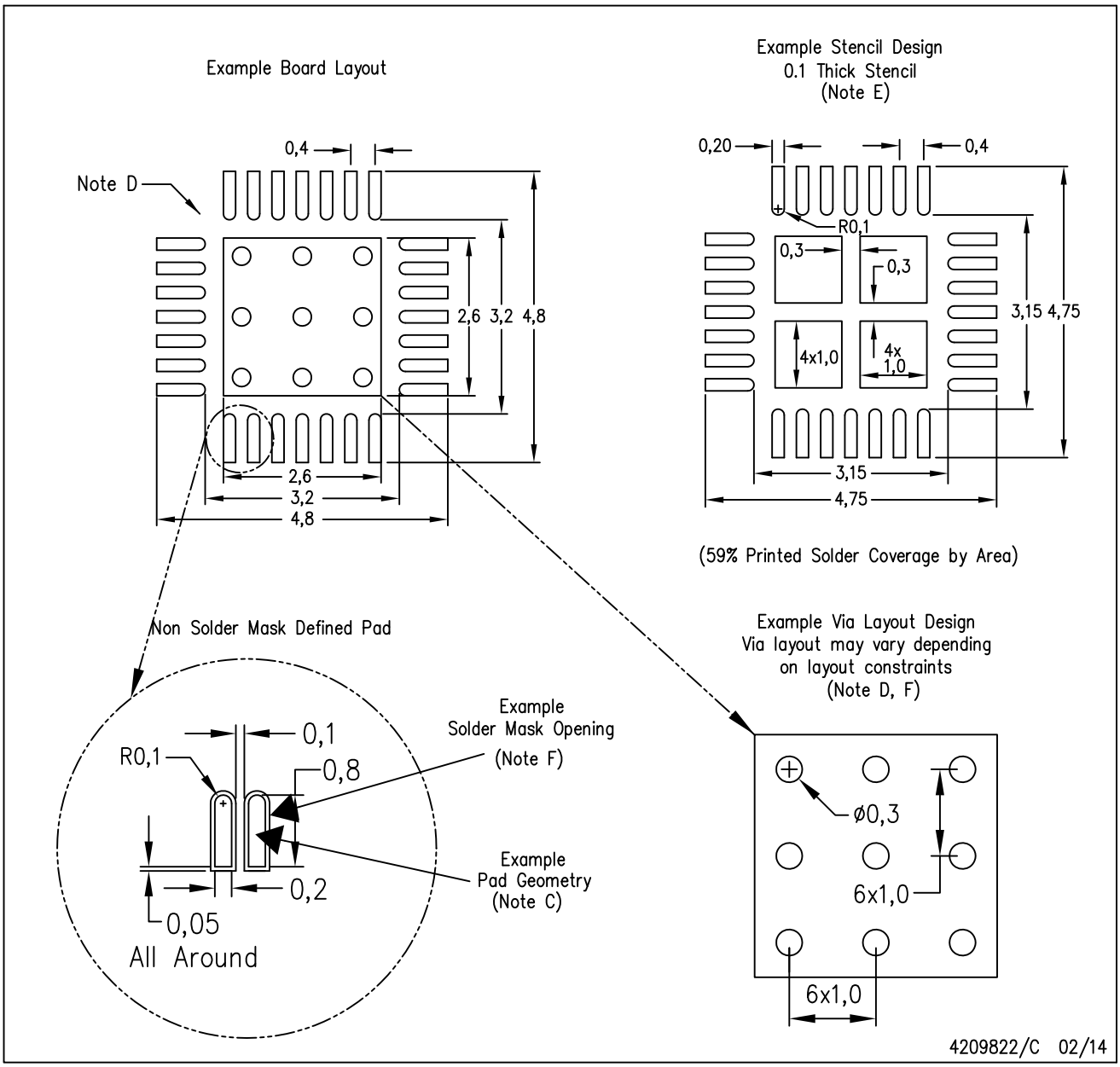
Bottom View

Exposed Thermal Pad Dimensions

4209490/D 02/14

NOTE: All linear dimensions are in millimeters

RUY (S–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65198RUYR	ACTIVE	WQFN	RUY	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65198	Samples
TPS65198RUYT	ACTIVE	WQFN	RUY	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65198	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

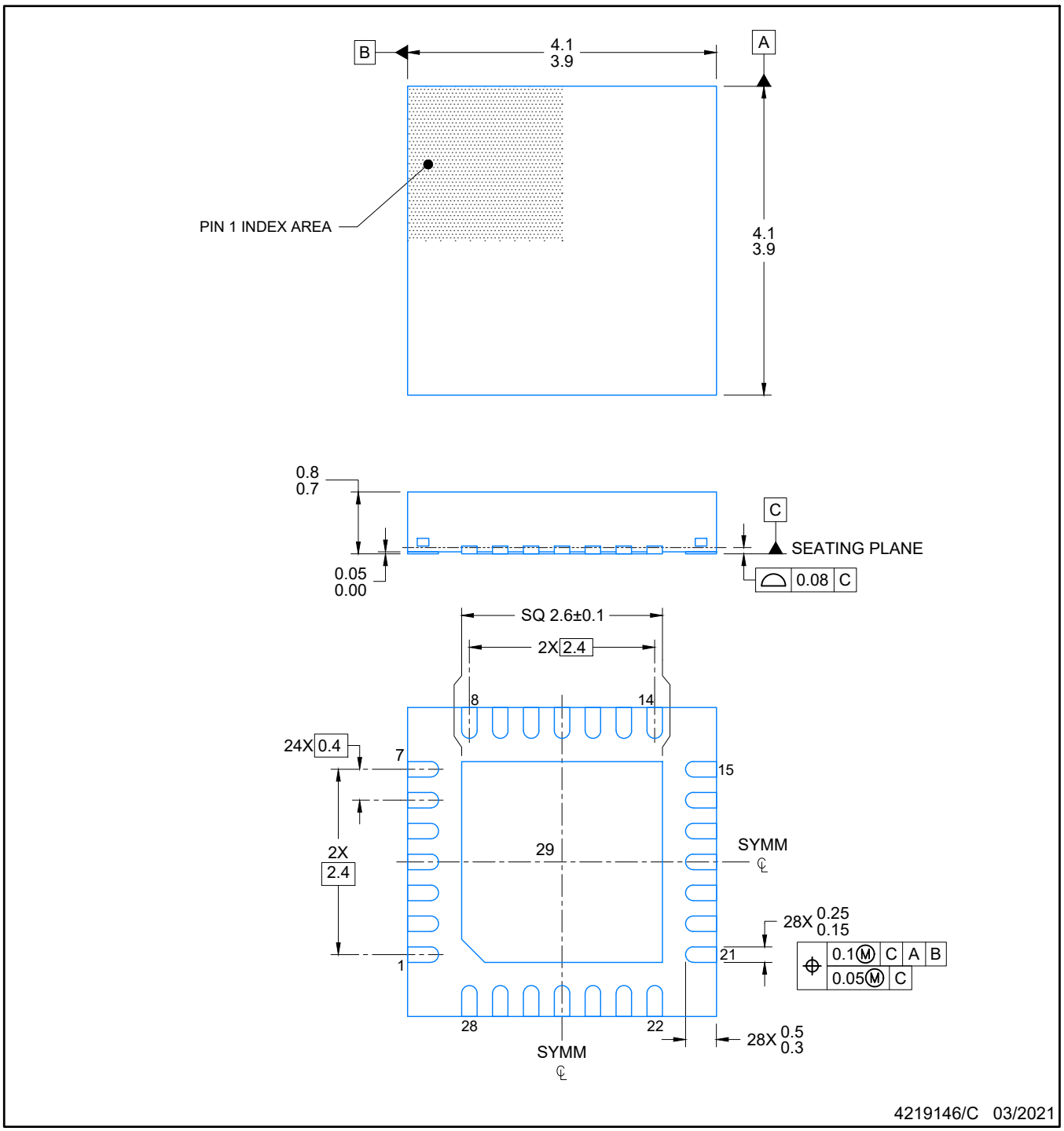
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RUY0028A

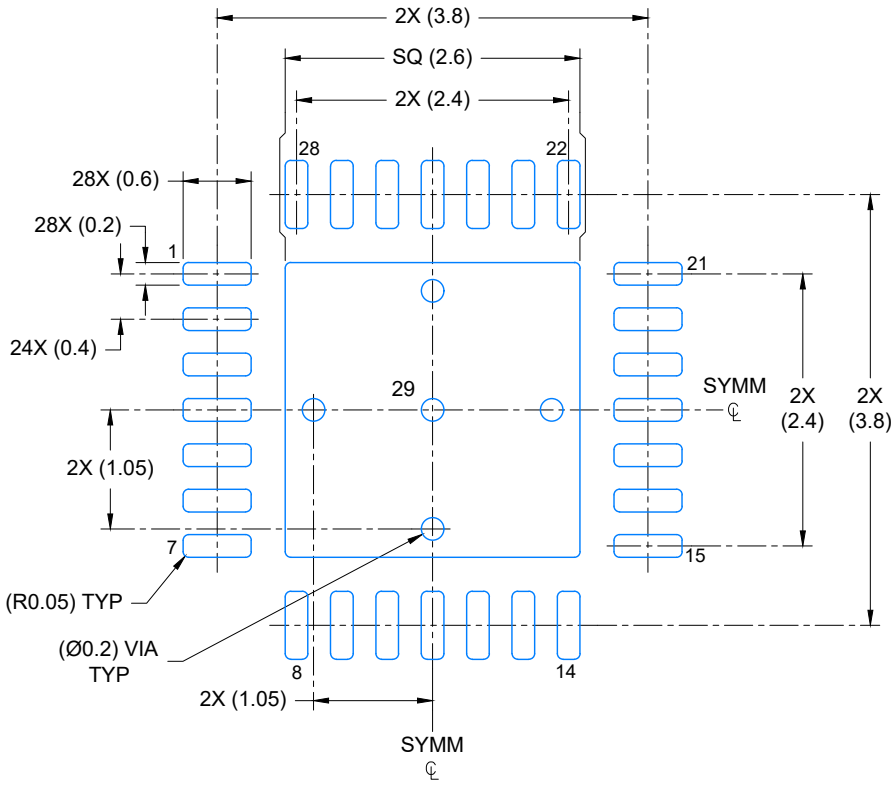
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

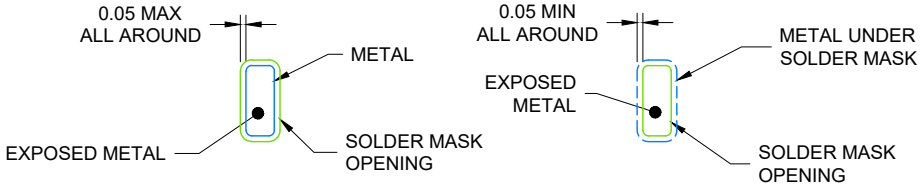


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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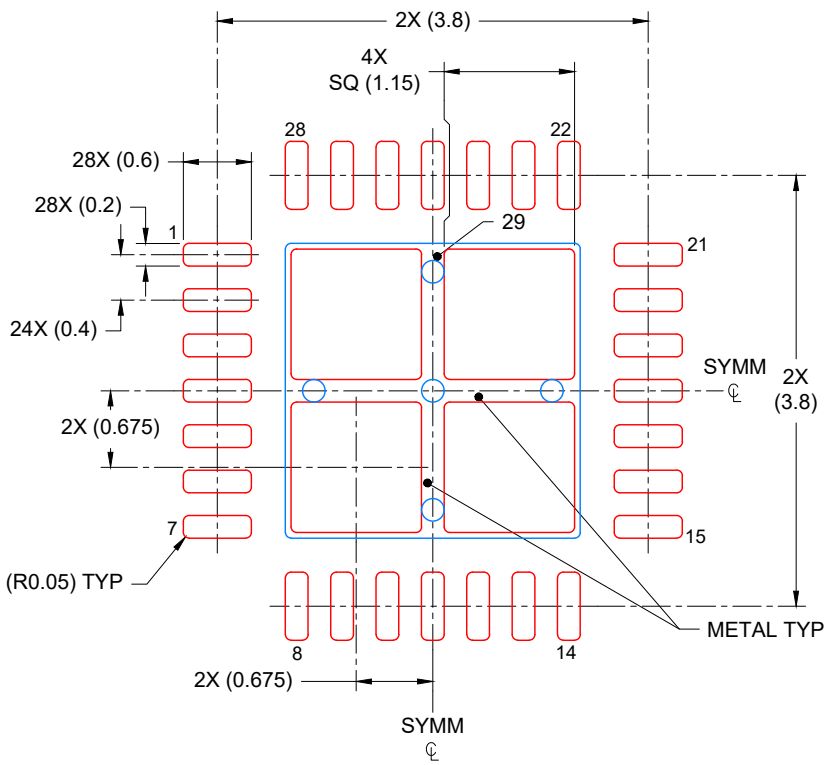
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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