

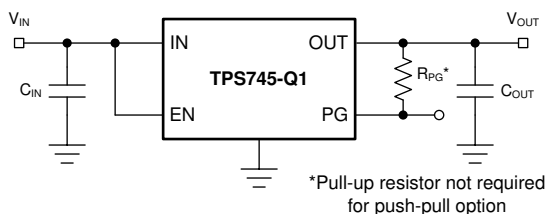
# TPS745-Q1 采用小型可湿性侧面 WSON 封装且具有电源正常状态指示功能的汽车类 500mA LDO

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：-40°C 至 +125°C， $T_A$
- 器件结温：-40°C 至 150°C
- 封装：
  - 2mm × 2mm 可湿性侧面 WSON 封装
  - 3mm × 3mm 可湿性侧面 VSON 封装
- 输入电压范围：1.5V 至 6.0V
- 输出电压范围：
  - 固定电压：0.65V 至 5.0V
  - 可调节电压：0.55V 至 5.5V
- 高 PSRR：100kHz 时为 45dB
- 输出精度： $\pm 0.85\%$  (25°C)， $\pm 1.5\%$  (最大值)
- 电源正常输出选项：
  - 开漏和推挽
- 超低压降：
  - 500mA 时为 160mV (最大值) ( $3.3V_{OUT}$ )
- 与 1 $\mu$ F 或更大的电容器搭配使用时可保持稳定
- 低  $I_Q$ ：25  $\mu$ A (典型值)、1.5  $\mu$ A (关断)
- 有源输出放电
- 提供功能安全
  - 可提供用于功能安全系统设计的文档
- 低热阻：
  - DRV (6 引脚 WSON)， $R_{\theta JA} = 80.3^\circ\text{C/W}$
  - DRB (8 引脚 VSON)， $R_{\theta JA} = 55.5^\circ\text{C/W}$

## 2 应用

- 汽车音响主机
- 前置摄像头和后置摄像头
- 汽车仪表组显示屏
- 远程信息处理控制单元
- 中距离、短距离雷达



典型应用：固定电压版本

## 3 说明

TPS745-Q1 是一款具有电源正常指示功能的 500mA 超低压降稳压器 (LDO)。此器件采用具有可湿性侧面的小型 6 引脚 2mm × 2mm WSON 封装和小型 8 引脚、3mm × 3mm VSON 封装，便于进行光学检测。TPS745-Q1 具有低静态电流消耗，并且可提供快速线路和负载瞬态性能。

TPS745-Q1 支持 1.5V 至 6.0V 的输入电压范围和 0.55V 至 5.5V 的外部可调输出电压范围，因而是一款灵活的后置稳压器件。该器件还提供固定输出电压，为常用电压轨供电。

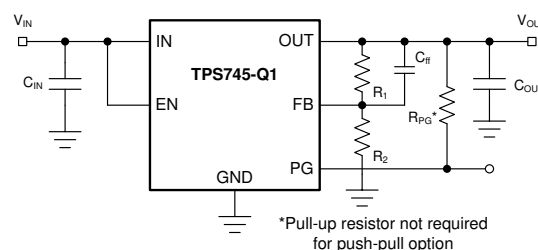
TPS745-Q1 具有可监控反馈引脚电压的电源正常 (PG) 输出，用于指示输出电压状态。EN 输入和 PG 输出可用于对系统中多个电源进行定序。

TPS745-Q1 在与支持小尺寸总体解决方案的小型陶瓷输出电容器搭配使用时，可保持稳定。精密带隙和误差放大器具有高精度特性，在 25°C 时可提供  $\pm 0.85\%$  (最大值) 的精度，在整个工作温度范围内可提供  $\pm 1.5\%$  (最大值) 的精度。该器件包括集成的热关断、电流限制和欠压锁定 (UVLO) 功能。TPS745-Q1 具有内部折返电流限制，有助于在短路事件中减少热耗散。

### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS745-Q1	可湿性侧面 WSON (6)	2.00mm × 2.00mm
	可湿性侧面 VSON (8)	3.00mm × 3.00mm

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用：可调电压版本



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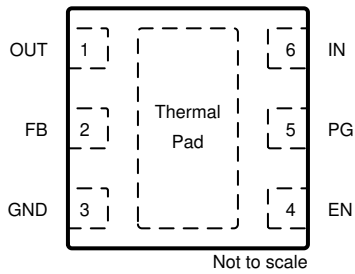
## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

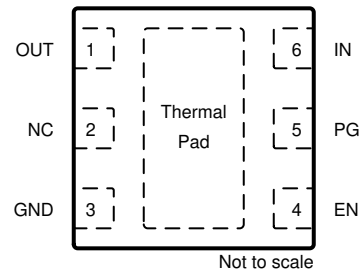
Changes from Revision B (January 2021) to Revision C (May 2022)	Page
• 将 DRB $R_{\theta JA}$ 从 $62.0^{\circ}C/W$ 更改为 $55.5^{\circ}C/W$ 并添加了功能安全要点.....	1
• 通篇将 DRB 封装的 WSON 更改为 VSON.....	1
• Updated thermal table to reflect correct values and package name.....	5

Changes from Revision A (October 2019) to Revision B (January 2021)	Page
• 将 DRB 封装从预发布更改为量产数据.....	1
• Added limits to $I_{SC}$ and $t_{STR}$ .....	5
• Changed $V_{DO}$ and $V_{OL(PG)}$ conditions to correct values.....	5

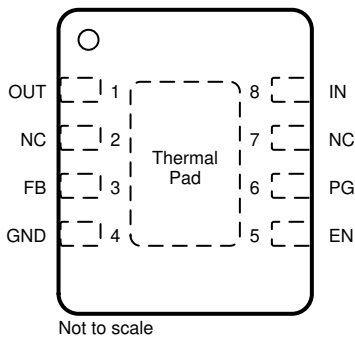
## 5 Pin Configuration and Functions



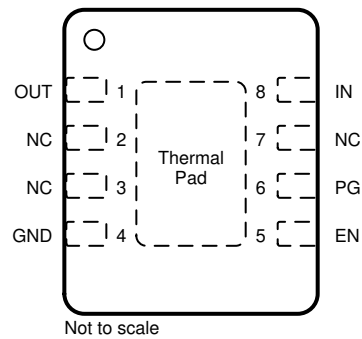
**图 5-1. DRV Package, 6-Pin Adjustable WSON (Top View)**



**图 5-2. DRV Package, 6-Pin Fixed WSON (Top View)**



**图 5-3. DRB Package, 8-Pin Adjustable VSON (Top View)**



**图 5-4. DRB Package, 8-Pin Fixed VSON (Top View)**

**表 5-1. Pin Functions**

NAME	PIN				I/O	DESCRIPTION
	DRV (Fixed)	DRV (Adjust)	DRB (Fixed)	DRB (Adjust)		
EN	4	4	5	5	Input	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.
FB	—	2	—	3	—	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
GND	3	3	4	4	—	Ground pin.
IN	6	6	8	8	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the <a href="#">Recommended Operating Conditions</a> table and the <a href="#">Input and Output Capacitor Selection</a> section. Place the input capacitor as close to the output of the device as possible.
NC	2	—	2, 3, 7	2, 7	—	No internal connection. Ground this pin for better thermal performance.
OUT	1	1	1	1	Output	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the <a href="#">Recommended Operating Conditions</a> table and the <a href="#">Input and Output Capacitor Selection</a> section. Place the output capacitor as close to output of the device as possible.
PG	5	5	6	6	Output	Power-good output. Available in open-drain and push-pull topologies. A pullup resistor is only required for the open-drain type. For the open-drain version, if the power-good functionality is not being used, ground this pin or leave floating. For the push-pull version, if the power-good functionality is not being used, leave this pin floating.
Thermal Pad					—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply, $V_{IN}$	- 0.3	6.5	V
	Enable, $V_{EN}$	- 0.3	6.5	
	Feedback, $V_{FB}$	- 0.3	2.0	
	Power-good, $V_{PG}$	- 0.3	6.5	
	Output, $V_{OUT}$	- 0.3	$V_{IN} + 0.3$ <sup>(2)</sup>	
Current	Output, $I_{OUT}$	Internally limited		
	Power-good, $I_{PG}$		±10	mA
Temperature	Operating junction, $T_J$	- 40	150	°C
	Storage, $T_{stg}$	- 65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The absolute maximum rating is  $V_{IN} + 0.3$  V or 6.0 V, whichever is smaller.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011, corner pins	±750
		Charged-device model (CDM), per AEC Q100-011, other pins	±500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	1.5		6.0	V
$V_{OUT}$	Output voltage	Adjustable only		5.5	V
		Fixed only	0.65	5.0	
$I_{OUT}$	Output current	0		500	mA
$C_{IN}$	Input capacitor	1			μF
$C_{OUT}$	Output capacitor <sup>(1)</sup>	1		220	μF
$C_{FF}$	Feed-forward capacitor		10		nF
$V_{EN}$	Enable voltage	0		6.0	V
$f_{EN}$	Enable toggle frequency			10	kHz
$V_{PG}$	PG voltage	0		6.0	V
$T_J$	Junction operating temperature	- 40		150	°C

- (1) Minimum derated capacitance of 0.47 μF is required for stability.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS745-Q1		UNIT
		DRV (WSON)	DRB (VSON)	
		6 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	80.3	55.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	98.7	70.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	44.8	28.0	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	6.1	4.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	45.0	28.0	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	20.8	10.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$ , unless otherwise noted; all typical values are at  $T_J = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>FB</sub>	Feedback voltage	Adjustable only		0.55		V
	Output accuracy <sup>(1)</sup>	T <sub>J</sub> = 25°C	- 0.85%		0.85%	
		-40°C ≤ T <sub>J</sub> ≤ 85°C	- 1.00%		1.00%	
		-40°C ≤ T <sub>J</sub> ≤ 150°C	- 1.50%		1.50%	
	Line regulation	V <sub>OUT(NOM)</sub> + 0.5 V <sup>(2)</sup> ≤ V <sub>IN</sub> ≤ 6.0 V		2	7.5	mV
	Load regulation	0.1 mA ≤ I <sub>OUT</sub> ≤ 500 mA, V <sub>IN</sub> ≥ 2.0 V		0.030		V/A
I <sub>GND</sub>	Ground current	I <sub>OUT</sub> = 0 mA	T <sub>J</sub> = 25°C	25	32	μA
			-40°C ≤ T <sub>J</sub> ≤ 150°C	25	36	
I <sub>SHDN</sub>	Shutdown current	V <sub>EN</sub> ≤ 0.3 V, 1.5 V ≤ V <sub>IN</sub> ≤ 6.0 V	-40°C ≤ T <sub>J</sub> ≤ 125°C	0.1	1	μA
			-40°C ≤ T <sub>J</sub> ≤ 150°C	0.1	1.55	
I <sub>FB</sub>	Feedback pin current	Adjustable only		0.01	0.1	μA
I <sub>CL</sub>	Output current limit	V <sub>OUT(NOM)</sub> < 1.0 V, V <sub>OUT</sub> = V <sub>OUT(NOM)</sub> - 0.2 V, V <sub>IN</sub> = 2.0 V	515	720	865	mA
		V <sub>OUT(NOM)</sub> ≥ 1.0 V, V <sub>OUT</sub> = V <sub>OUT(NOM)</sub> × 0.85, V <sub>IN</sub> = V <sub>OUT(NOM)</sub> + 1.0 V				
I <sub>SC</sub>	Short-circuit current limit	V <sub>OUT</sub> = 0 V	V <sub>OUT(NOM)</sub> < 1.0 V, V <sub>IN</sub> = 2.0 V	200	350	mA
			V <sub>OUT(NOM)</sub> ≥ 1.0 V, V <sub>IN</sub> = V <sub>OUT(NOM)</sub> + 1.0 V			
V <sub>DO</sub>	Dropout voltage	I <sub>OUT</sub> = 500 mA, V <sub>OUT</sub> = 0.95 × V <sub>OUT(NOM)</sub>	0.65 V ≤ V <sub>OUT</sub> < 0.8 V <sup>(3)</sup>	720	910	mV
			0.8 V ≤ V <sub>OUT</sub> < 1.0 V	585	780	
			1.0 V ≤ V <sub>OUT</sub> < 1.2 V	420	600	
			1.2 V ≤ V <sub>OUT</sub> < 1.5 V	285	430	
			1.5 V ≤ V <sub>OUT</sub> < 1.8 V	180	265	
			1.8 V ≤ V <sub>OUT</sub> < 2.5 V	140	215	
			2.5 V ≤ V <sub>OUT</sub> < 3.3 V	105	170	
	3.3 V ≤ V <sub>OUT</sub> ≤ 5.5 V	95	160			
PSRR	Power-supply rejection ratio	V <sub>OUT</sub> = 1.8 V, V <sub>IN</sub> = 2.8 V, I <sub>OUT</sub> = 500 mA, C <sub>OUT</sub> = 2.2 μF	f = 1 kHz	57		dB
			f = 100 kHz	42		
			f = 1 MHz	35		
V <sub>N</sub>	Output noise voltage	BW = 10 Hz to 100 kHz, V <sub>OUT</sub> = 0.9 V, V <sub>IN</sub> = 1.9 V		53		μV <sub>RMS</sub>
V <sub>UVLO</sub>	Undervoltage lockout	V <sub>IN</sub> falling	1.17	1.30	1.42	V
		V <sub>IN</sub> rising	1.21	1.34	1.47	

## 6.5 Electrical Characteristics (continued)

at operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$ , unless otherwise noted; all typical values are at  $T_J = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO,HYST}$	Undervoltage lockout hysteresis	$V_{IN}$ hysteresis		40		mV
$t_{STR}$	Startup time	From EN low-to-high transition to $V_{OUT} = V_{OUT(NOM)} \times 0.95$	200	500	650	$\mu\text{s}$
$V_{EN(HI)}$	EN pin high voltage (enabled)		1.0			V
$V_{EN(LO)}$	EN pin low voltage (disabled)				0.3	V
$I_{EN}$	Enable pin current	$V_{IN} = V_{EN} = 6.0\text{ V}$		10		nA
$R_{PULLDOWN}$	Pulldown resistance	$V_{IN} = 6.0\text{ V}$		95		$\Omega$
$PG_{HHTH}$	PG high threshold	$V_{OUT}$ increasing	89	92	96	$\%V_{OUT}$
$PG_{LTH}$	PG low threshold	$V_{OUT}$ decreasing	86	90	93	$\%V_{OUT}$
$PG_{HYST}$	PG hysteresis			2		$\%V_{out}$
$V_{OL(PG)}$	PG pin low-level output voltage	$V_{IN} \geq 1.5\text{V}$ , $I_{SINK} = 1.0\text{ mA}$			300	mV
		$V_{IN} \geq 2.75\text{V}$ , $I_{SINK} = 2.0\text{ mA}$				
$V_{OH(PG)}$	PG pin high-level output voltage <sup>(4)</sup>	$V_{OUT} \geq 1.0\text{V}$ , $I_{SOURCE} = 0.04\text{ mA}$	0.8 x $V_{OUT}$			V
		$V_{OUT} \geq 1.4\text{V}$ , $I_{SOURCE} = 0.2\text{ mA}$				
		$V_{OUT} \geq 2.5\text{V}$ , $I_{SOURCE} = 0.5\text{ mA}$				
		$V_{OUT} \geq 4.5\text{V}$ , $I_{SOURCE} = 1.0\text{ mA}$				
$I_{kg(PG)}$	PG pin leakage current <sup>(5)</sup>	$V_{OUT} > PG_{HHTH}$ , $V_{PG} = 6.0\text{ V}$		7	50	nA
$T_{SD}$	Thermal shutdown	Shutdown, temperature increasing		170		$^\circ\text{C}$
		Reset, temperature decreasing		155		

- When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
- $V_{IN} = 1.5\text{ V}$  for  $V_{OUT} < 1.0\text{ V}$ .
- Dropout is not tested for nominal output voltages below  $0.65\text{ V}$  since the input voltage may be below UVLO.
- Push-pull version only. The push-pull option is supported only for  $V_{OUT} \geq 1.0\text{ V}$ .
- Open-drain version only.

## 6.6 Timing Requirements

Parameter		MIN	TYP	MAX	UNIT
$t_{PGDH}$	PG delay time rising, time from 92% $V_{OUT}$ to 20% of PG <sup>(1)</sup>	135	165	178	$\mu\text{s}$
	'B' version <sup>(2)</sup>	4.5	5	5.5	ms
$t_{PGDL}$	PG delay time falling, time from 90% $V_{OUT}$ to 80% of PG <sup>(1)</sup>	1.5	7	10	$\mu\text{s}$

- Output overdrive = 10%.
- See the Device Nomenclature table for more information on available PG timings.

### 6.7 Typical Characteristics

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  (unless otherwise noted)

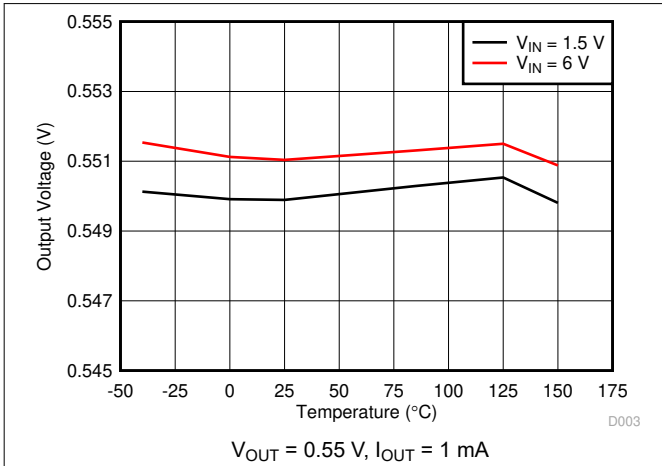


图 6-1. Output Voltage vs Ambient Temperature

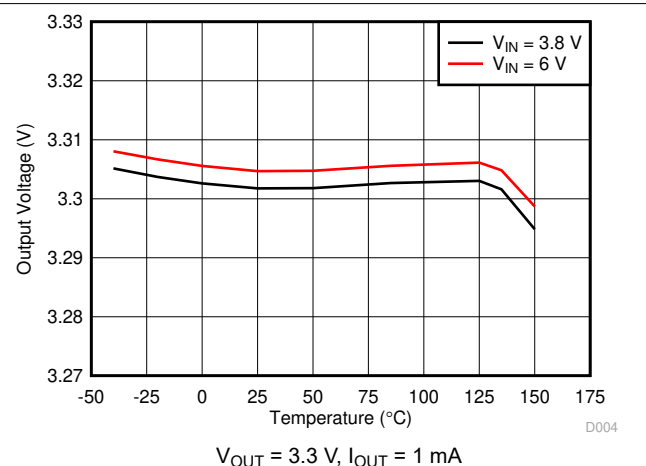


图 6-2. Output Voltage vs Ambient Temperature

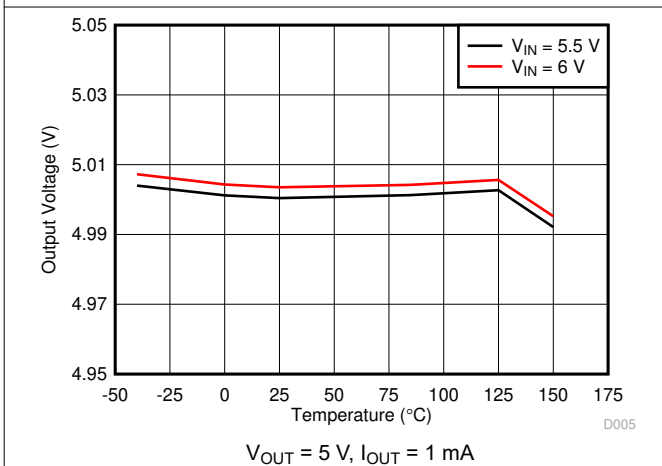


图 6-3. Output Voltage vs Ambient Temperature

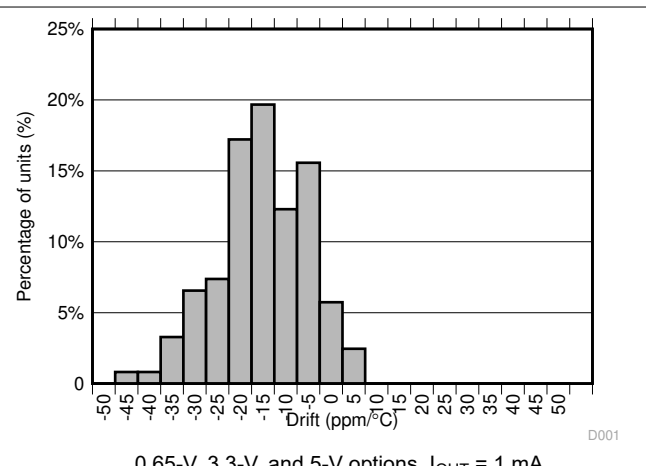


图 6-4. Temperature Drift Histogram (-40°C to +25°C)

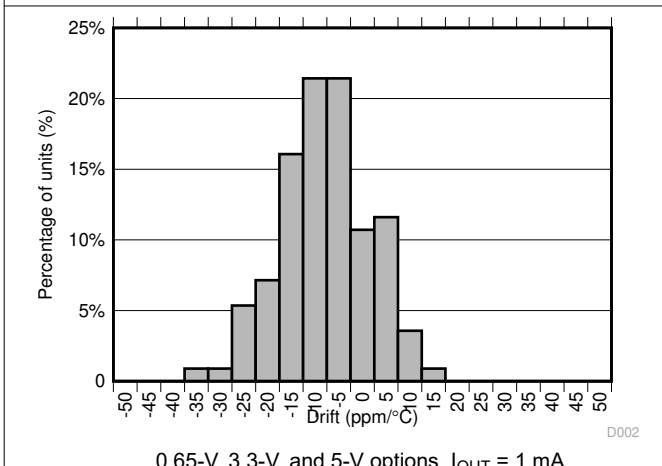


图 6-5. Temperature Drift Histogram (25°C to 150°C)

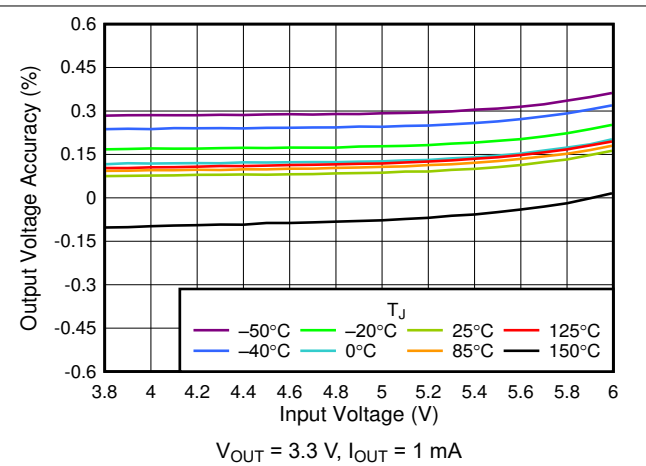
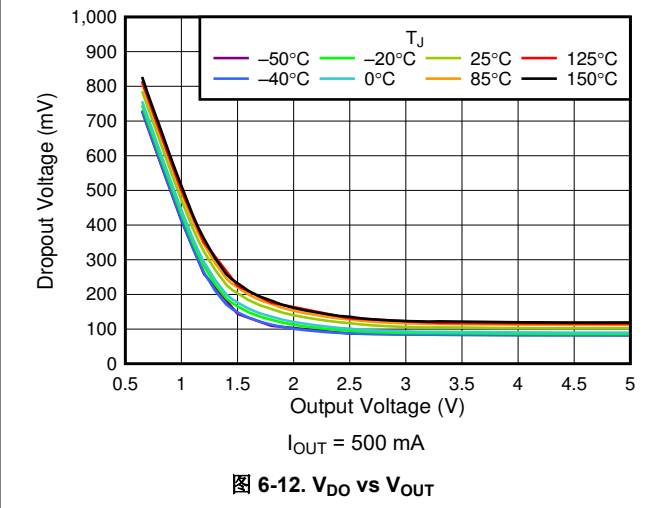
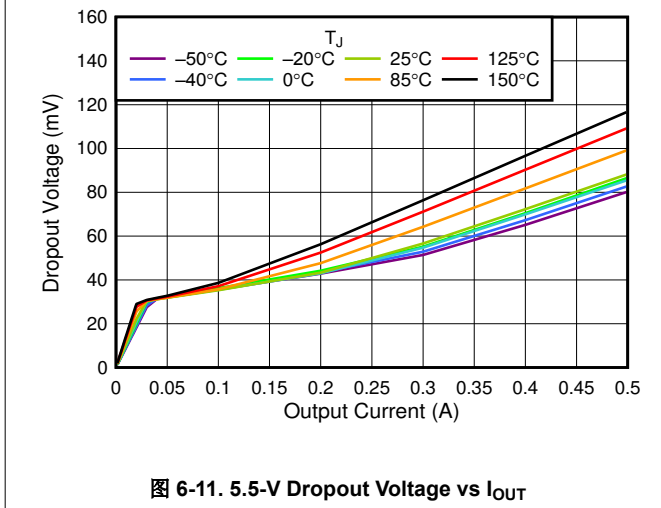
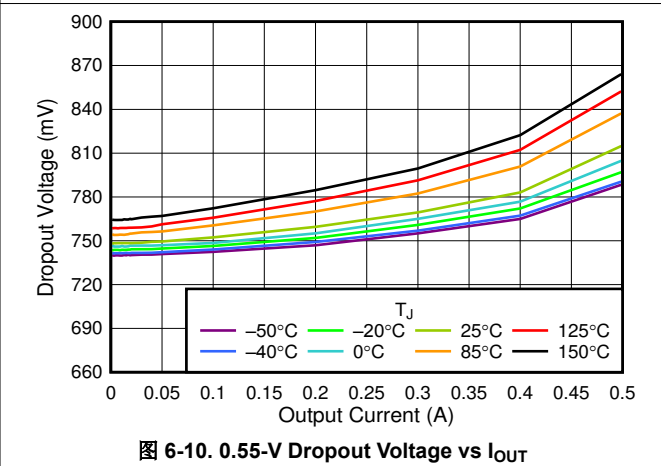
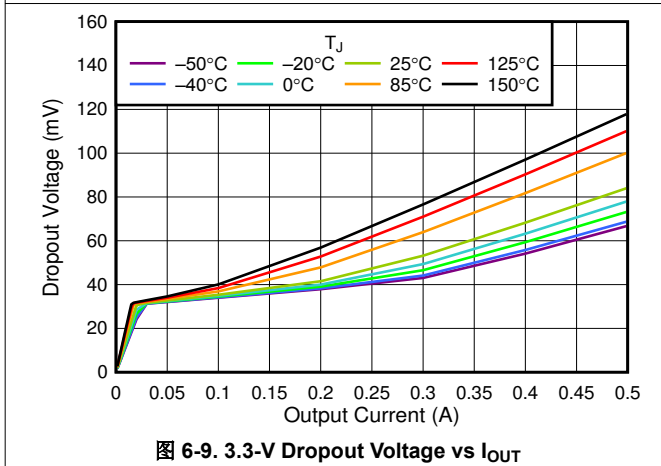
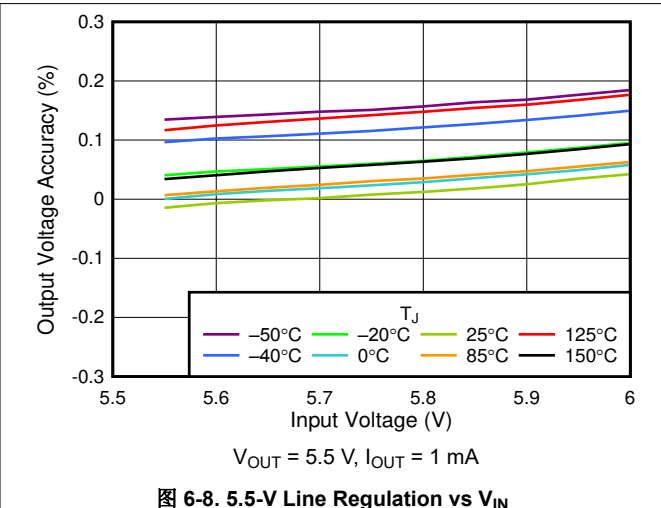
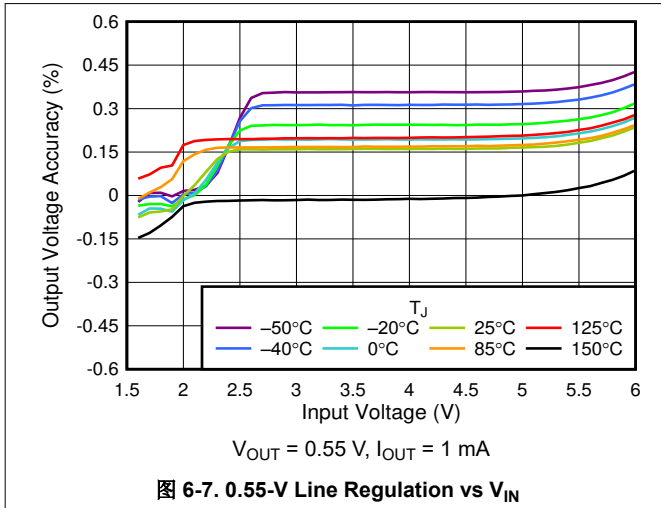


图 6-6. 3.3-V Line Regulation vs  $V_{IN}$

### 6.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)





### 6.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)

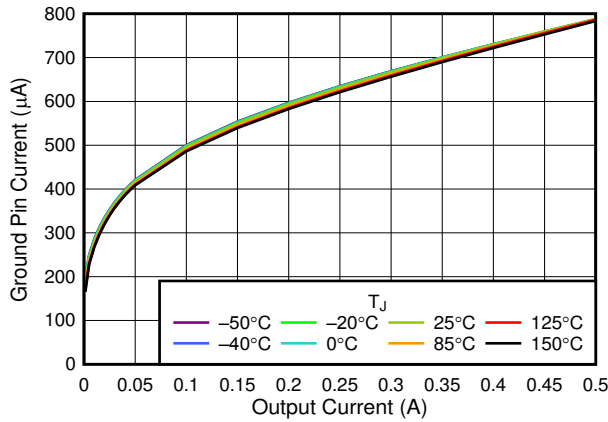


图 6-13.  $I_{GND}$  vs  $I_{OUT}$

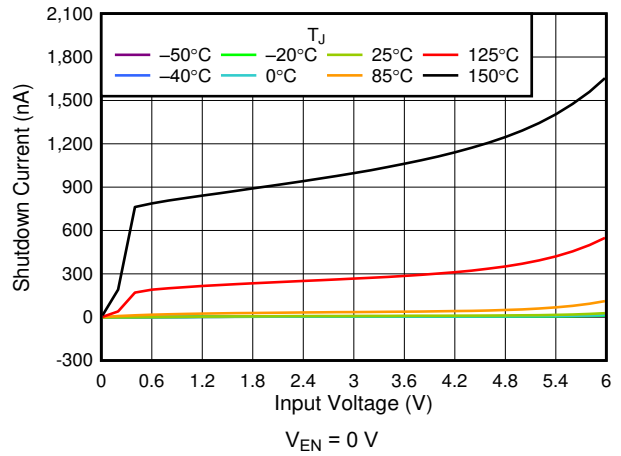
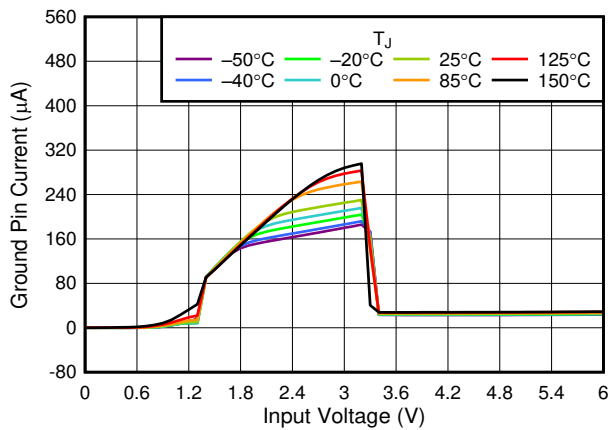


图 6-14.  $I_{SHDN}$  vs  $V_{IN}$



$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 0\text{ mA}$

图 6-15.  $I_Q$  vs  $V_{IN}$

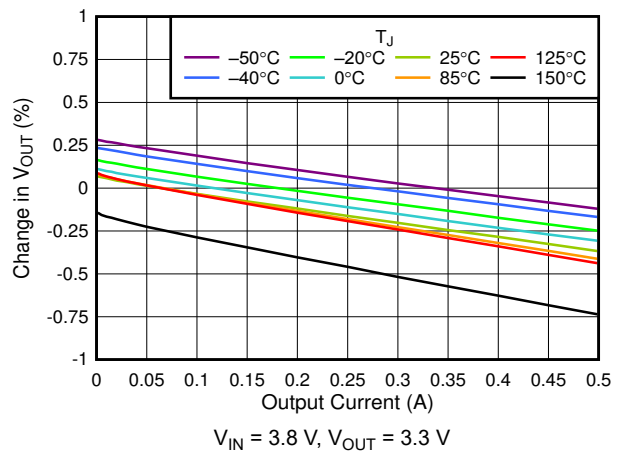
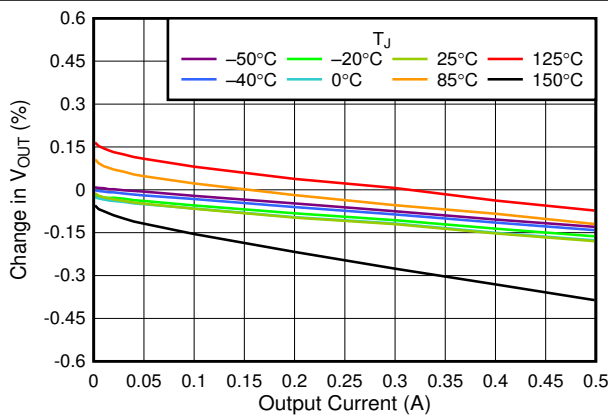
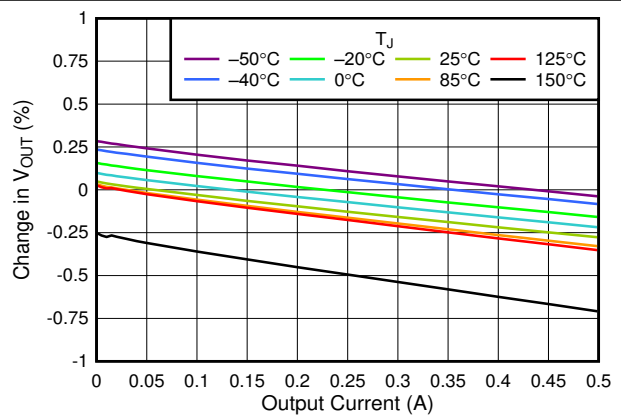


图 6-16. 3.3-V Load Regulation vs  $I_{OUT}$



$V_{IN} = 2\text{ V}$ ,  $V_{OUT} = 0.55\text{ V}$

图 6-17. 0.55-V Load Regulation vs  $I_{OUT}$



$V_{IN} = 6\text{ V}$ ,  $V_{OUT} = 5.5\text{ V}$

图 6-18. 5.5-V Load Regulation vs  $I_{OUT}$

### 6.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)

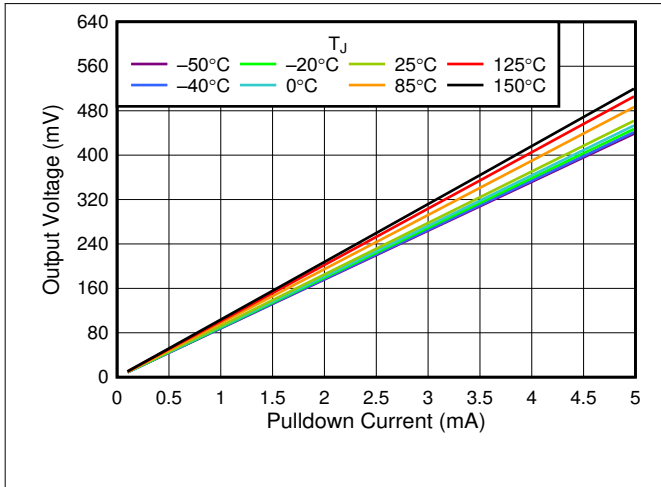


图 6-19.  $V_{OUT}$  vs  $I_{OUT}$  Pulldown Resistor

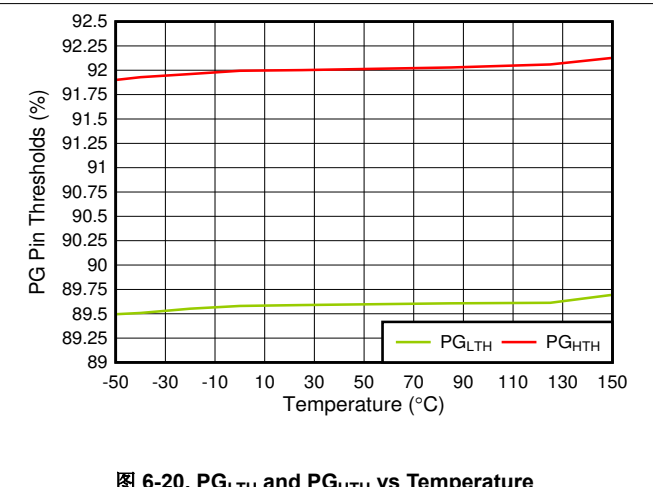


图 6-20.  $P_{GLTH}$  and  $P_{GHTH}$  vs Temperature

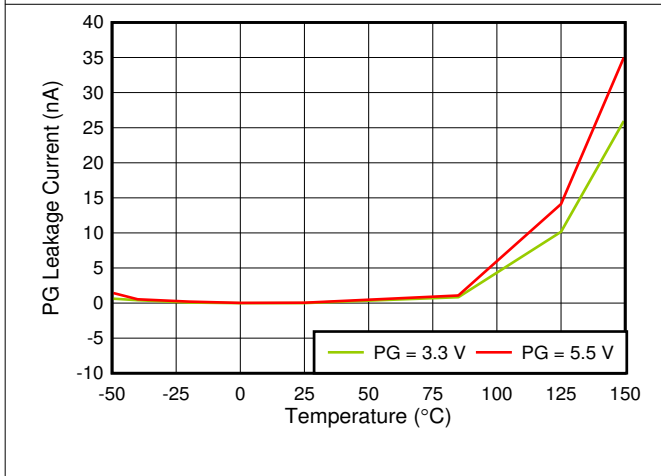


图 6-21.  $I_{kg(PG)}$  vs Temperature and PG Pin Voltage

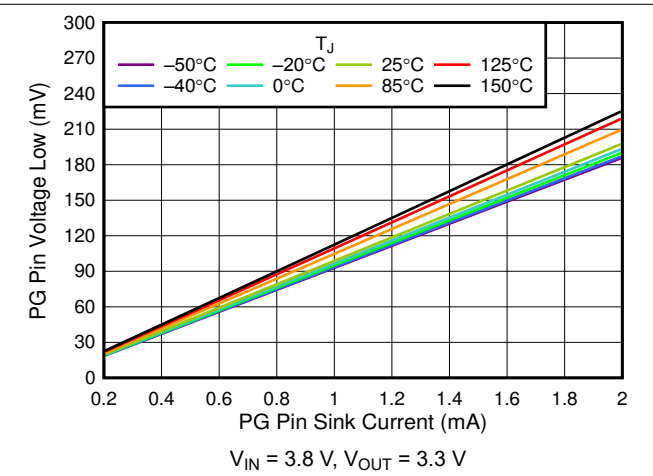


图 6-22.  $V_{OL(PG)}$  vs PG Pin Sink Current

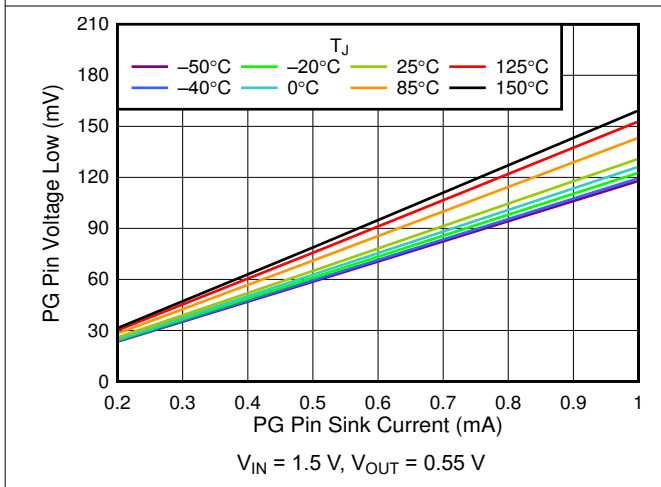


图 6-23.  $V_{OL(PG)}$  vs PG Pin Sink Current

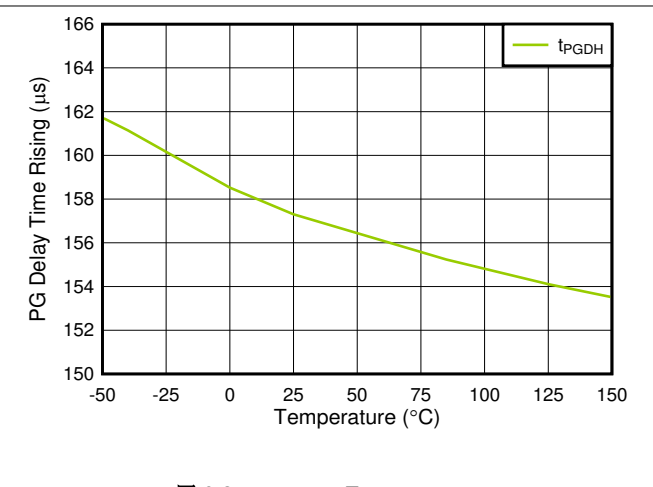


图 6-24.  $t_{PGDH}$  vs Temperature

### 6.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)

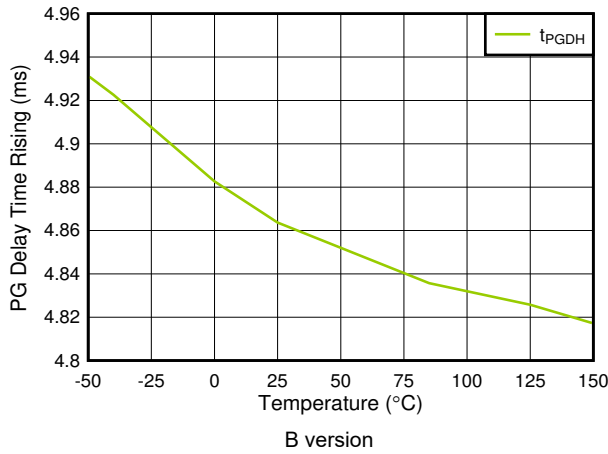


图 6-25.  $t_{PGDH}$  vs Temperature (For TPS746B Only)

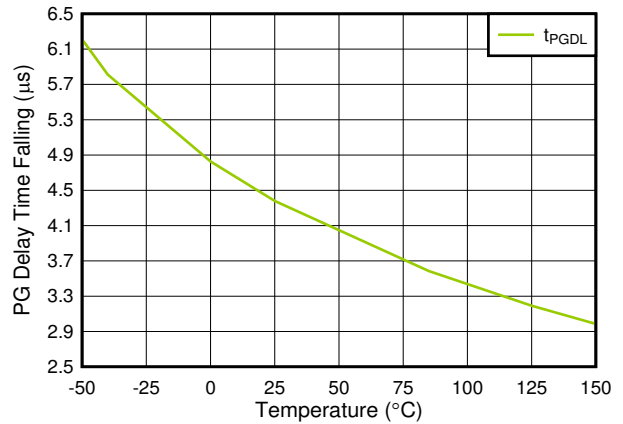


图 6-26.  $t_{PGDL}$  vs Temperature

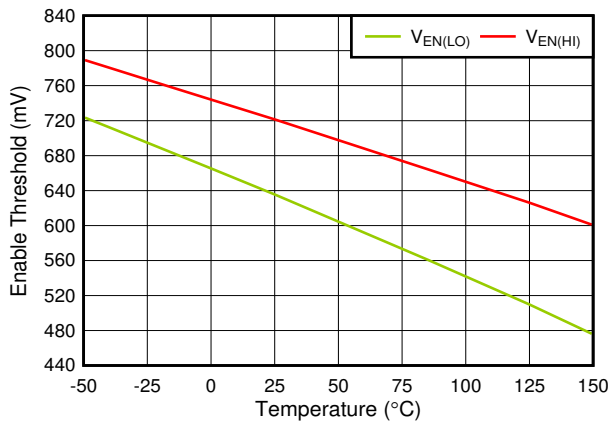


图 6-27.  $V_{EN(HI)}$  and  $V_{EN(LO)}$  vs Temperature

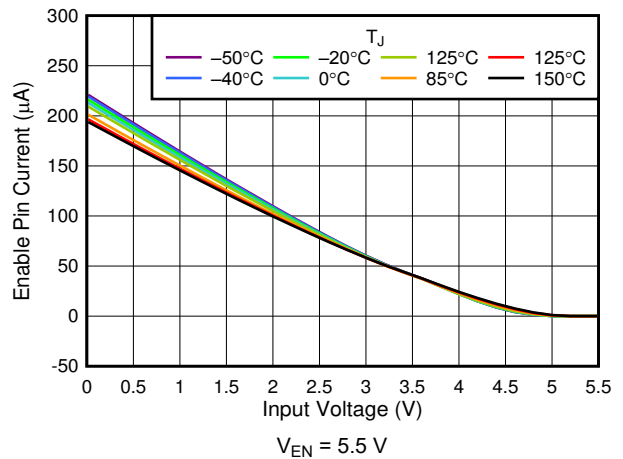


图 6-28.  $I_{EN}$  vs  $V_{IN}$

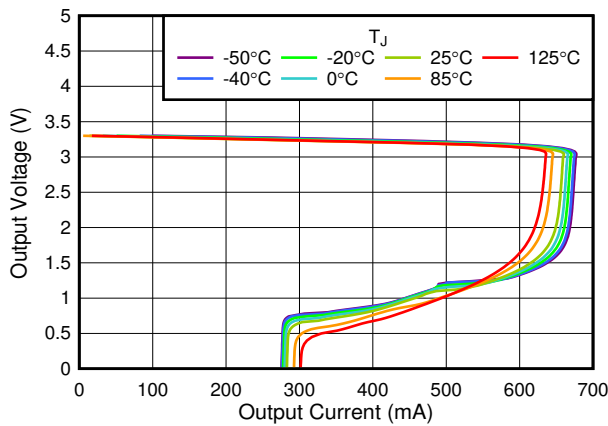


图 6-29. 3.3-V  $V_{OUT}$  vs  $I_{OUT}$

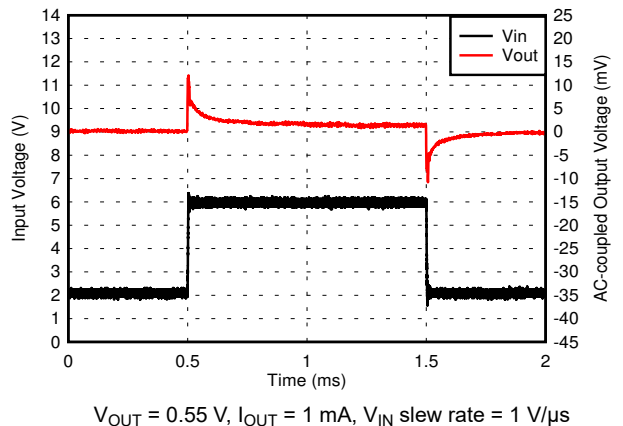
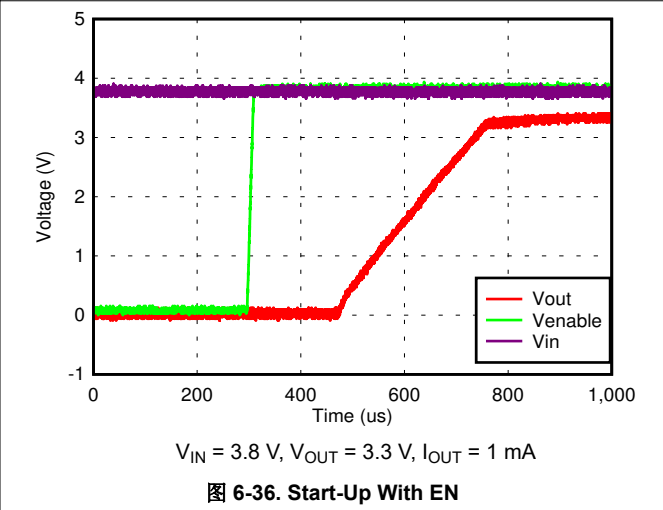
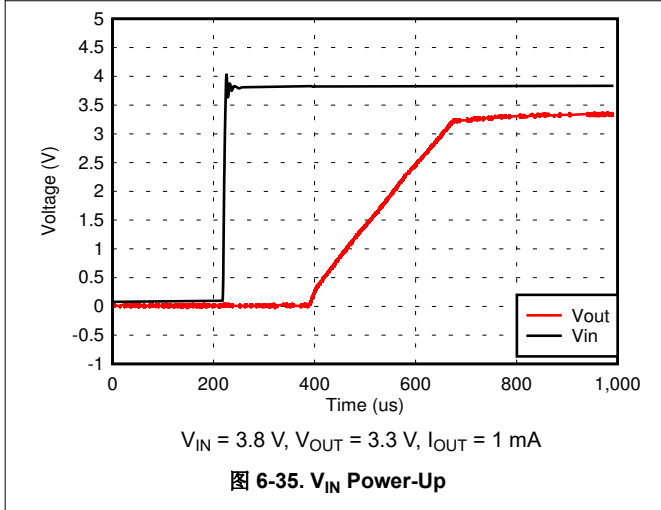
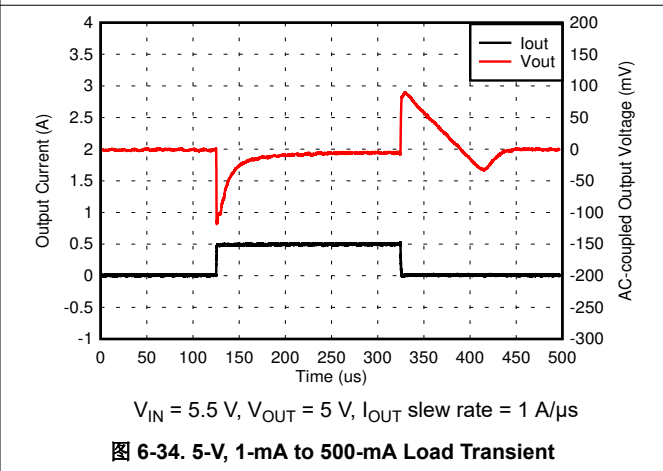
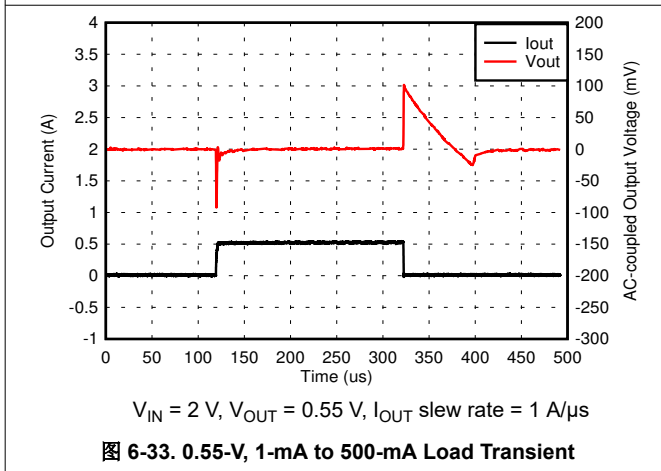
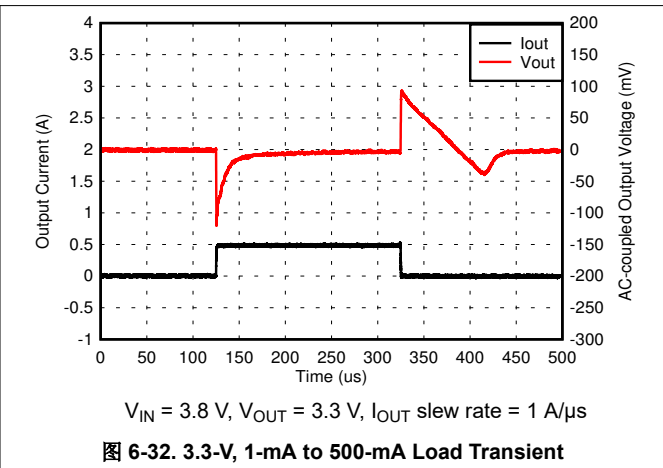
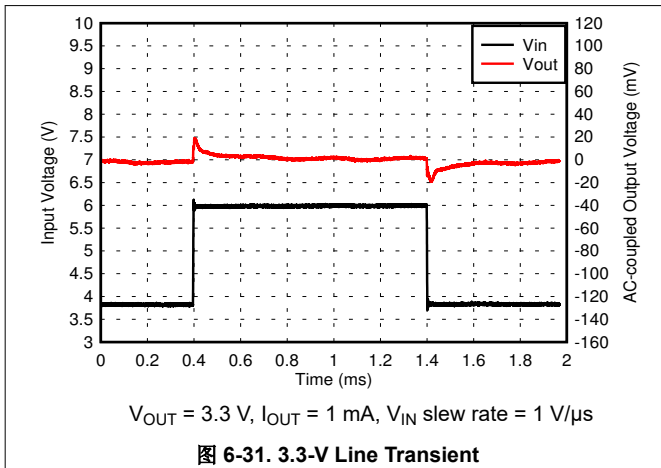


图 6-30. 0.55-V Line Transient

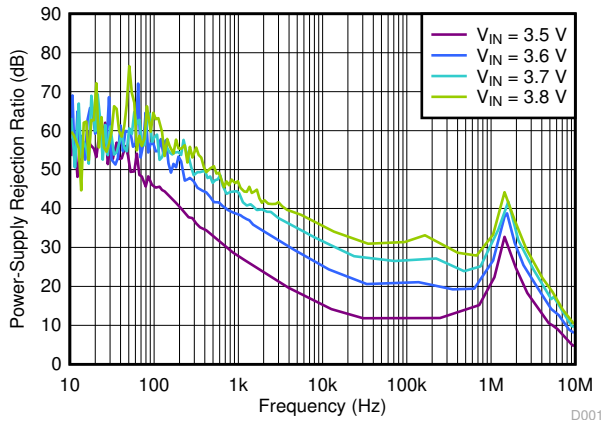
### 6.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$  (unless otherwise noted)



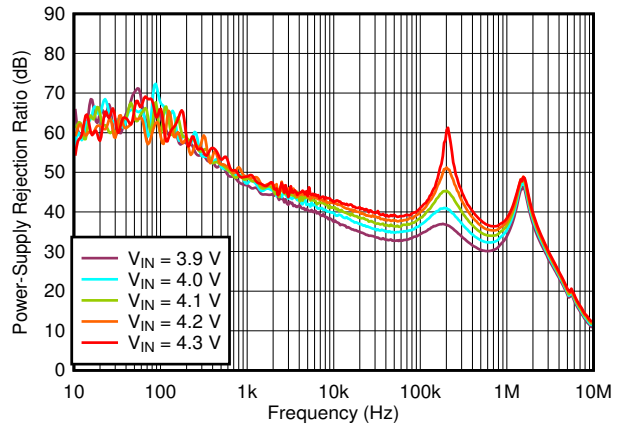
### 6.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  (unless otherwise noted)



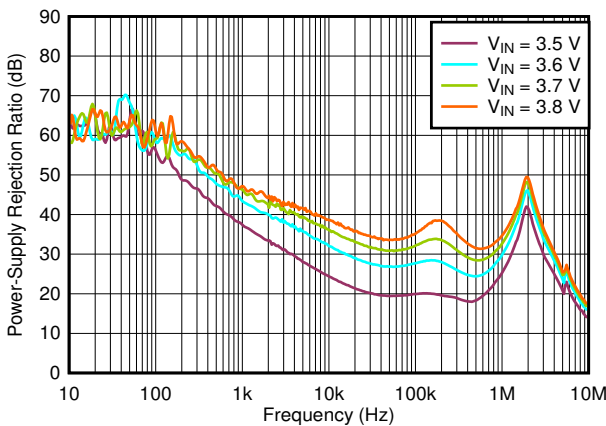
$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$

图 6-37. PSRR vs Frequency and  $V_{IN}$



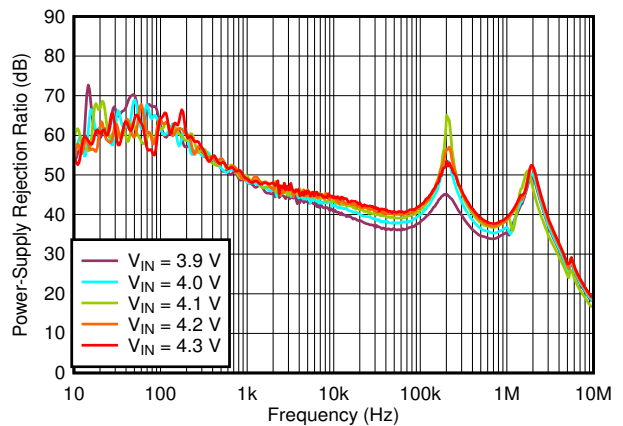
$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$

图 6-38. PSRR vs Frequency and  $V_{IN}$



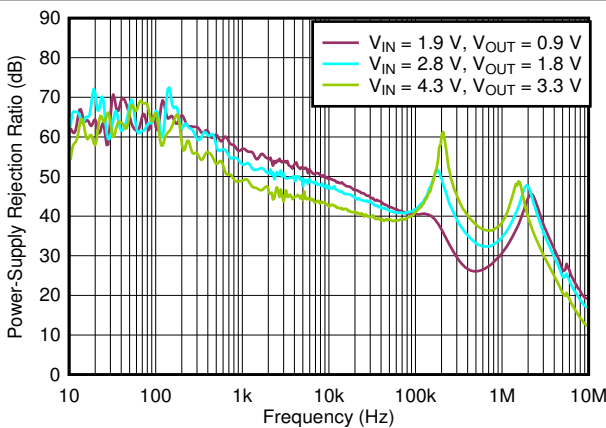
$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 250\text{ mA}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$

图 6-39. PSRR vs Frequency and  $V_{IN}$



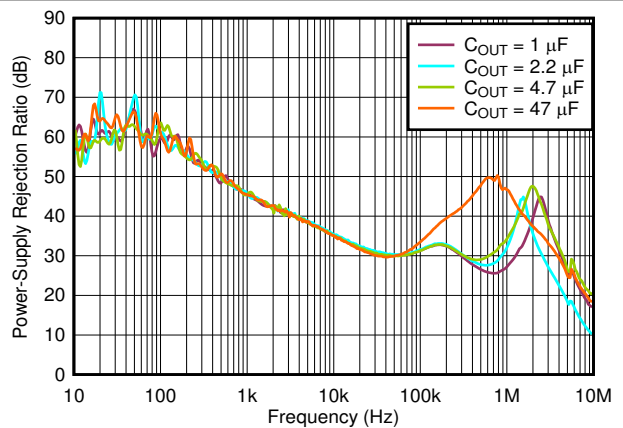
$V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 250\text{ mA}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$

图 6-40. PSRR vs Frequency and  $V_{IN}$



$I_{OUT} = 500\text{ mA}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$

图 6-41. PSRR vs Frequency

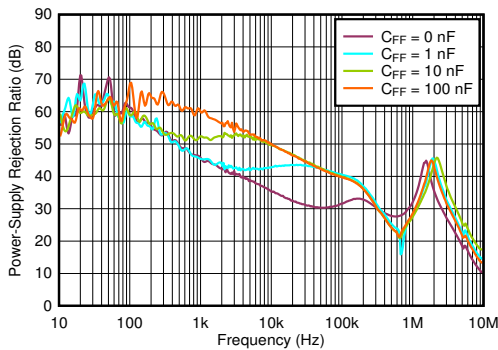


$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$

图 6-42. PSRR vs Frequency and  $C_{OUT}$

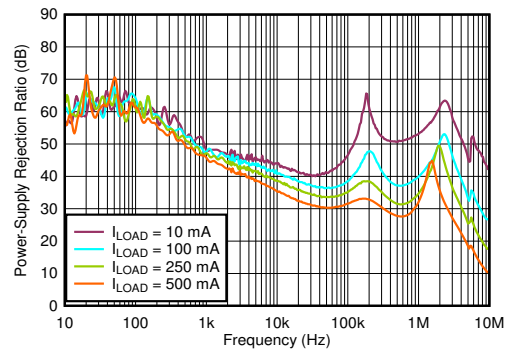
### 6.7 Typical Characteristics (continued)

at operating temperature range  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $1.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$  (unless otherwise noted)



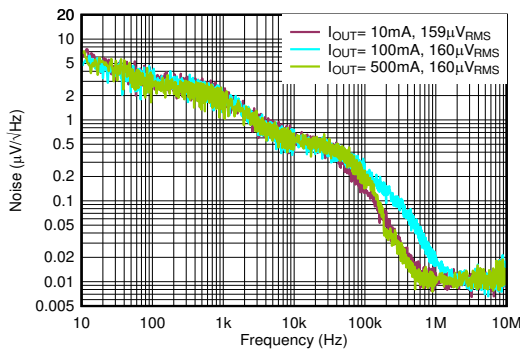
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$

图 6-43. PSRR vs Frequency and  $C_{FF}$



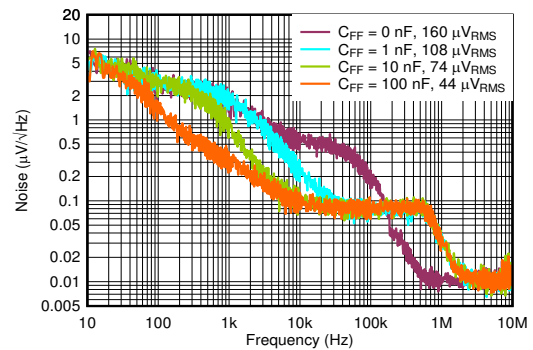
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$

图 6-44. PSRR vs Frequency and  $I_{LOAD}$



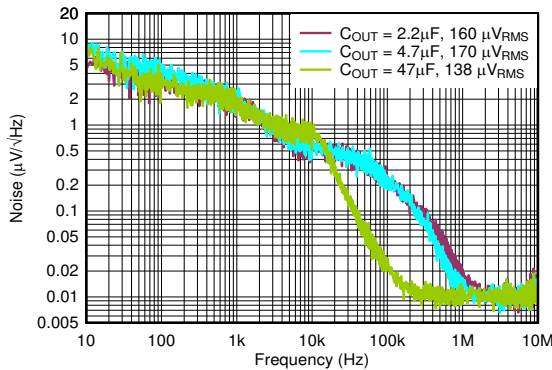
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ ,  $V_{RMS}\text{ BW} = 10\text{ Hz to }100\text{ kHz}$

图 6-45. Output Spectral Noise Density vs Frequency and  $I_{OUT}$



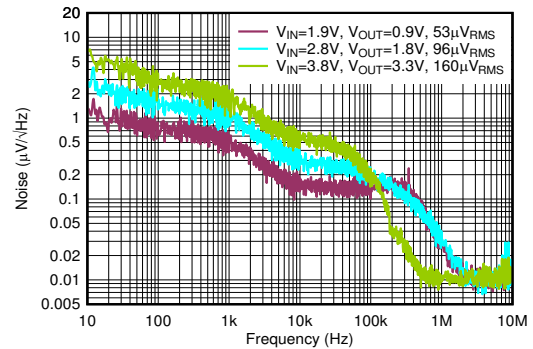
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ ,  $V_{RMS}\text{ BW} = 10\text{ Hz to }100\text{ kHz}$

图 6-46. Output Spectral Noise Density vs Frequency and  $C_{FF}$



$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} = 100\text{ mA}$ ,  $C_{FF} = 0\ \mu\text{F}$ ,  $V_{RMS}\text{ BW} = 10\text{ Hz to }100\text{ kHz}$

图 6-47. Output Spectral Noise Density vs Frequency and  $C_{OUT}$



$I_{OUT} = 500\text{ mA}$ ,  $C_{OUT} = 2.2\ \mu\text{F}$ ,  $V_{RMS}\text{ BW} = 10\text{ Hz to }100\text{ kHz}$

图 6-48. Output Spectral Noise Density vs Frequency

## 7 Detailed Description

### 7.1 Overview

The TPS745-Q1 is a low-dropout regulator (LDO) that consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, good PSRR with low dropout voltage, make this device ideal for automotive applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ .

### 7.2 Functional Block Diagrams

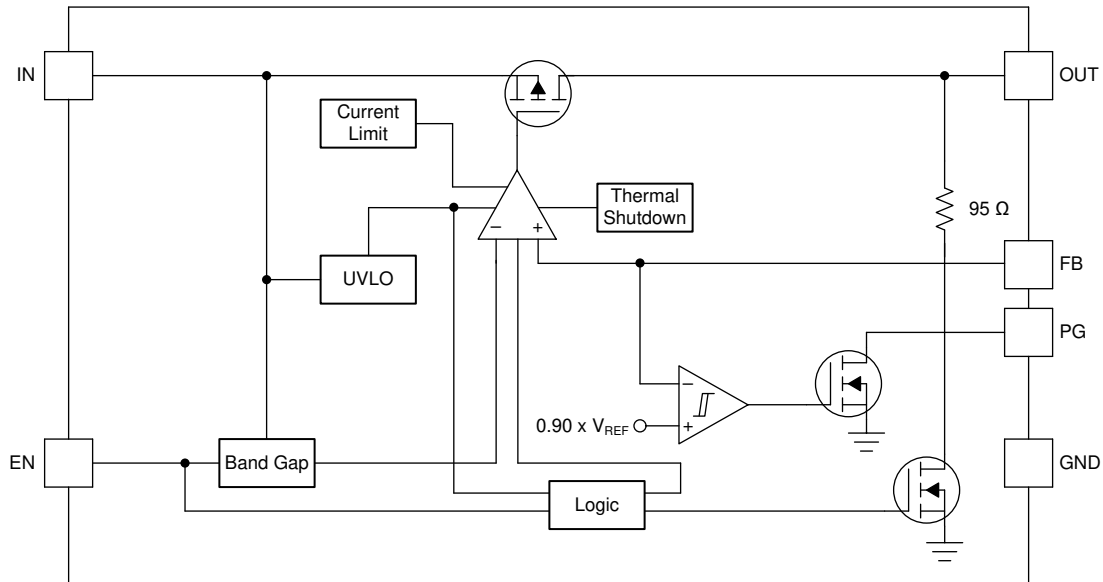


图 7-1. Adjustable Version With Open-Drain Power-Good

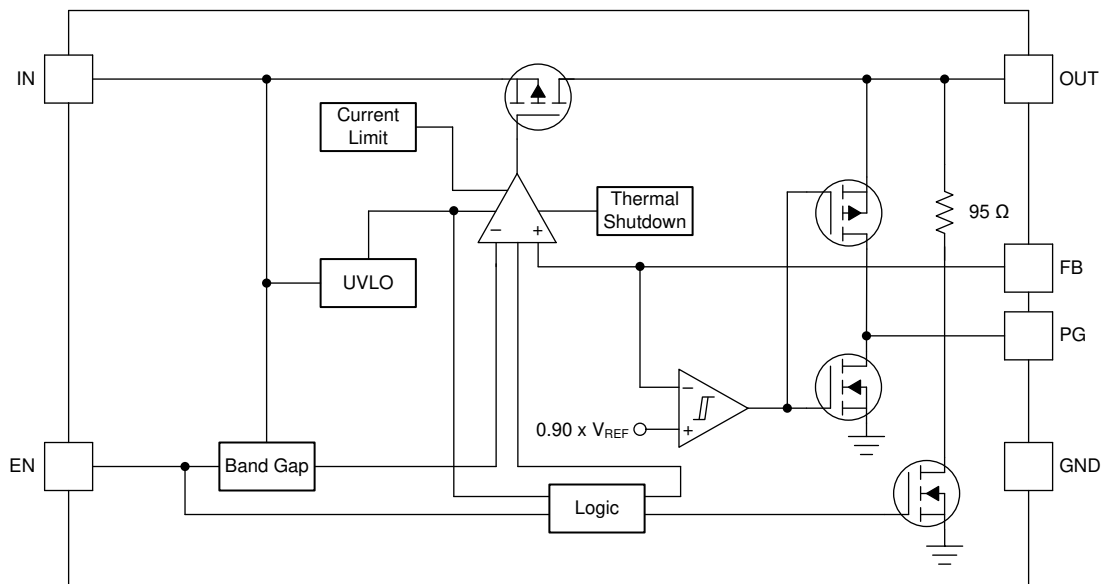


图 7-2. Adjustable Version With Push-Pull Power-Good

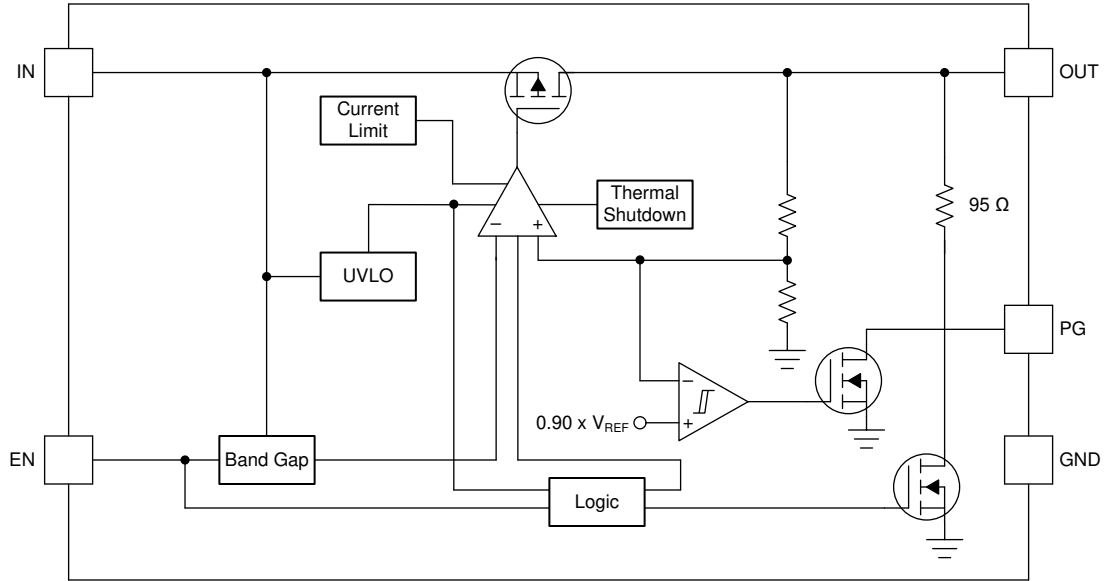


图 7-3. Fixed Voltage Version With Open-Drain Power-Good

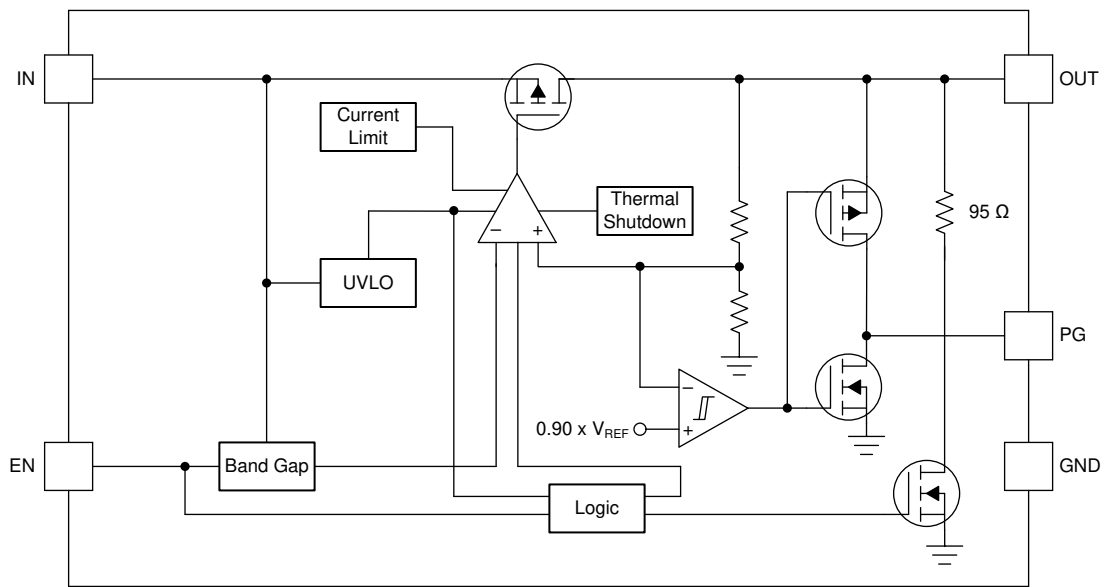


图 7-4. Fixed Voltage Version With Push-Pull Power-Good



## 7.3 Feature Description

### 7.3.1 TPS745-Q1 Comparison

表 7-1 lists the three different power-good (PG) options for the TPS745-Q1.

表 7-1. TPS745-Q1 Comparison Table

DEVICE	POWER-GOOD DELAY	POWER-GOOD TYPE
TPS745xxPQWDRVRQ1, TPS745xxPQWDRBRQ1	150 $\mu$ s	Open-drain
TPS745xxPBQWDRVRQ1	5 ms	Open-drain
TPS745xxPCQWDRVRQ1	150 $\mu$ s	Push-pull

### 7.3.2 Undervoltage Lockout (UVLO)

The TPS745-Q1 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage ( $V_{UVLO}$ ). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When  $V_{IN}$  is less than  $V_{UVLO}$ , the output is connected to ground with a pulldown resistor ( $R_{PULLDOWN}$ ). When the device enters UVLO, the PG output is pulled low.

### 7.3.3 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed  $V_{EN(HI)}$ . Turn off the device by forcing the EN pin to drop below  $V_{EN(LO)}$ . If shutdown capability is not required, connect EN to IN. When the device is disabled, the PG output pin is pulled low.

The TPS745-Q1 has an internal pulldown MOSFET that connects an  $R_{PULLDOWN}$  resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance ( $C_{OUT}$ ) and the load resistance ( $R_L$ ) in parallel with the pulldown resistor ( $R_{PULLDOWN}$ ). 方程式 1 calculates the time constant:

$$\tau = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \times C_{OUT} \quad (1)$$

### 7.3.4 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ( $V_{FOLDBACK}$ ). In a high-load current fault with the output voltage above  $V_{FOLDBACK}$ , the brick-wall scheme limits the output current to the current limit ( $I_{CL}$ ). When the voltage drops below  $V_{FOLDBACK}$ , a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ( $I_{SC}$ ).  $I_{CL}$  and  $I_{SC}$  are listed in the *Electrical Characteristics* table.

For this device,  $V_{FOLDBACK} = 0.4 \times V_{OUT(NOM)}$ .

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power  $[(V_{IN} - V_{OUT}) \times I_{CL}]$ . When the device output is shorted and the output is below  $V_{FOLDBACK}$ , the pass transistor dissipates power  $[(V_{IN} - V_{OUT}) \times I_{SC}]$ . If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application report](#).

图 7-5 shows a diagram of the foldback current limit.

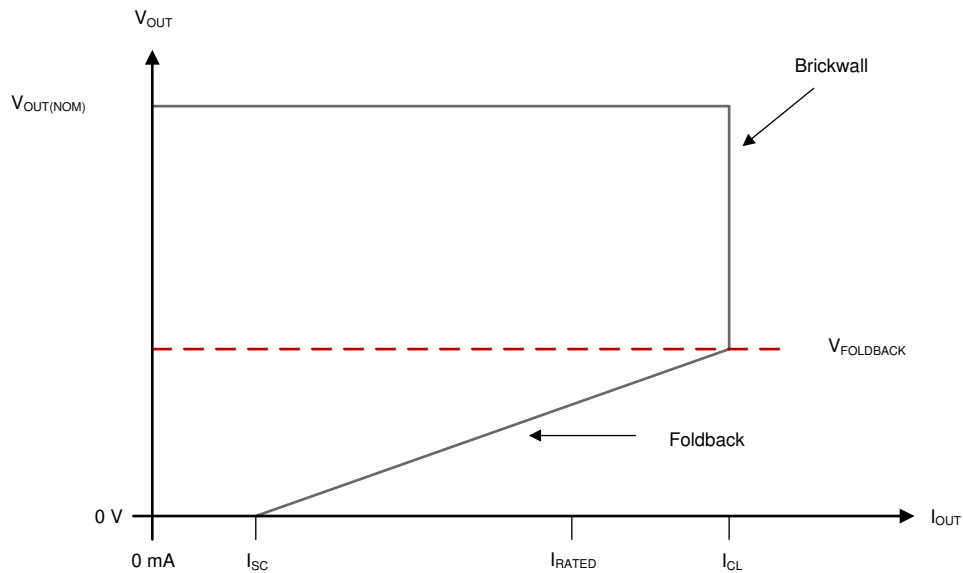


图 7-5. Foldback Current Limit

### 7.3.5 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately  $170^{\circ}\text{C}$ . Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately  $155^{\circ}\text{C}$ , the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the regulator from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the  $(V_{IN} - V_{OUT})$  voltage and the load current. For reliable operation, limit junction temperature to  $150^{\circ}\text{C}$  maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS745-Q1 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TPS745-Q1 into thermal shutdown degrades device reliability.

## 7.4 Device Functional Modes

### 7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**表 7-2. Device Functional Mode Comparison**

OPERATING MODE	PARAMETER			
	$V_{IN}$	$V_{EN}$	$I_{OUT}$	$T_J$
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

### 7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ( $V_{OUT(nom)} + V_{DO}$ )
- The output current is less than the current limit ( $I_{OUT} < I_{CL}$ )
- The device junction temperature is less than the thermal shutdown temperature ( $T_J < T_{SD}$ )
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout,  $V_{IN} < V_{OUT(NOM)} + V_{DO}$ , directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ( $V_{OUT(NOM)} + V_{DO}$ ), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

#### 8.1.1 Adjustable Device Feedback Resistors

图 8-1 显示了 TPS745P-Q1 的输出电压可以通过使用电阻分压网络从 0.55 V 调整到 5.5 V。

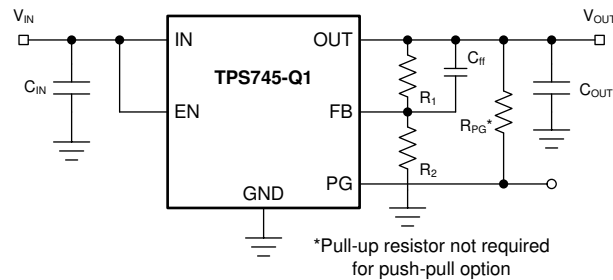


图 8-1. Adjustable Operation

The adjustable-version device requires external feedback divider resistors to set the output voltage.  $V_{OUT}$  is set using the feedback divider resistors,  $R_1$  and  $R_2$ , according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the  $V_{OUT}$  equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

#### 8.1.2 Input and Output Capacitor Selection

The TPS745-Q1 requires an output capacitance of 0.47  $\mu\text{F}$  or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220  $\mu\text{F}$ .

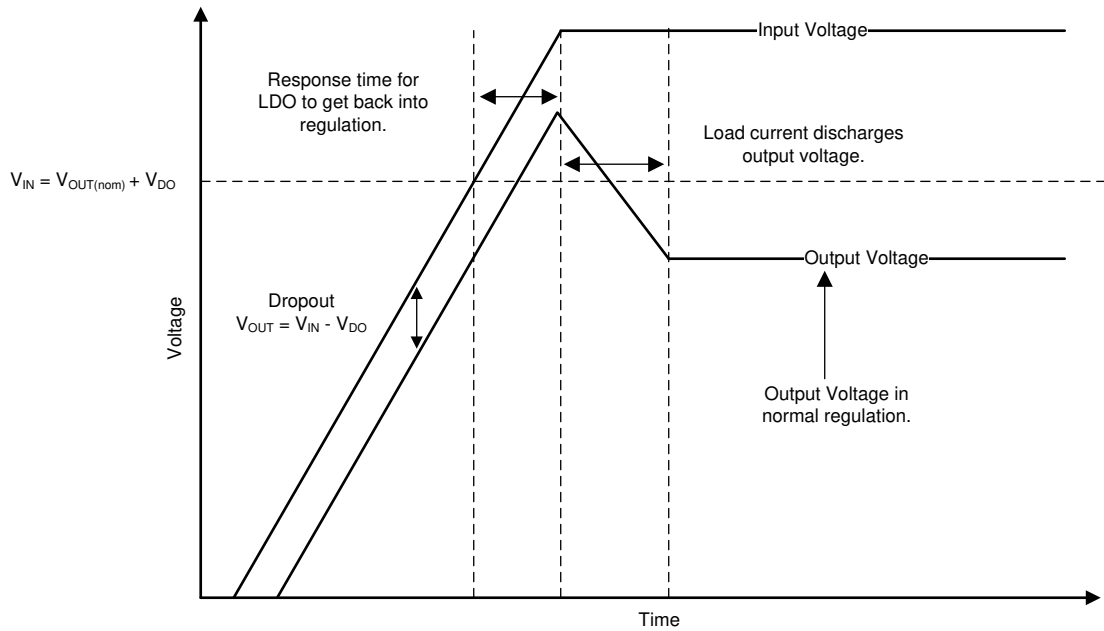
Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

### 8.1.3 Dropout Voltage

The TPS745-Q1 uses a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as  $(V_{IN} - V_{OUT})$  approaches dropout operation.

### 8.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on  $V_{IN}$  during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in [图 8-2](#), when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.



**图 8-2. Start-Up Into Dropout**

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. [图 8-3](#) illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage ( $V_{GS}$ ) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

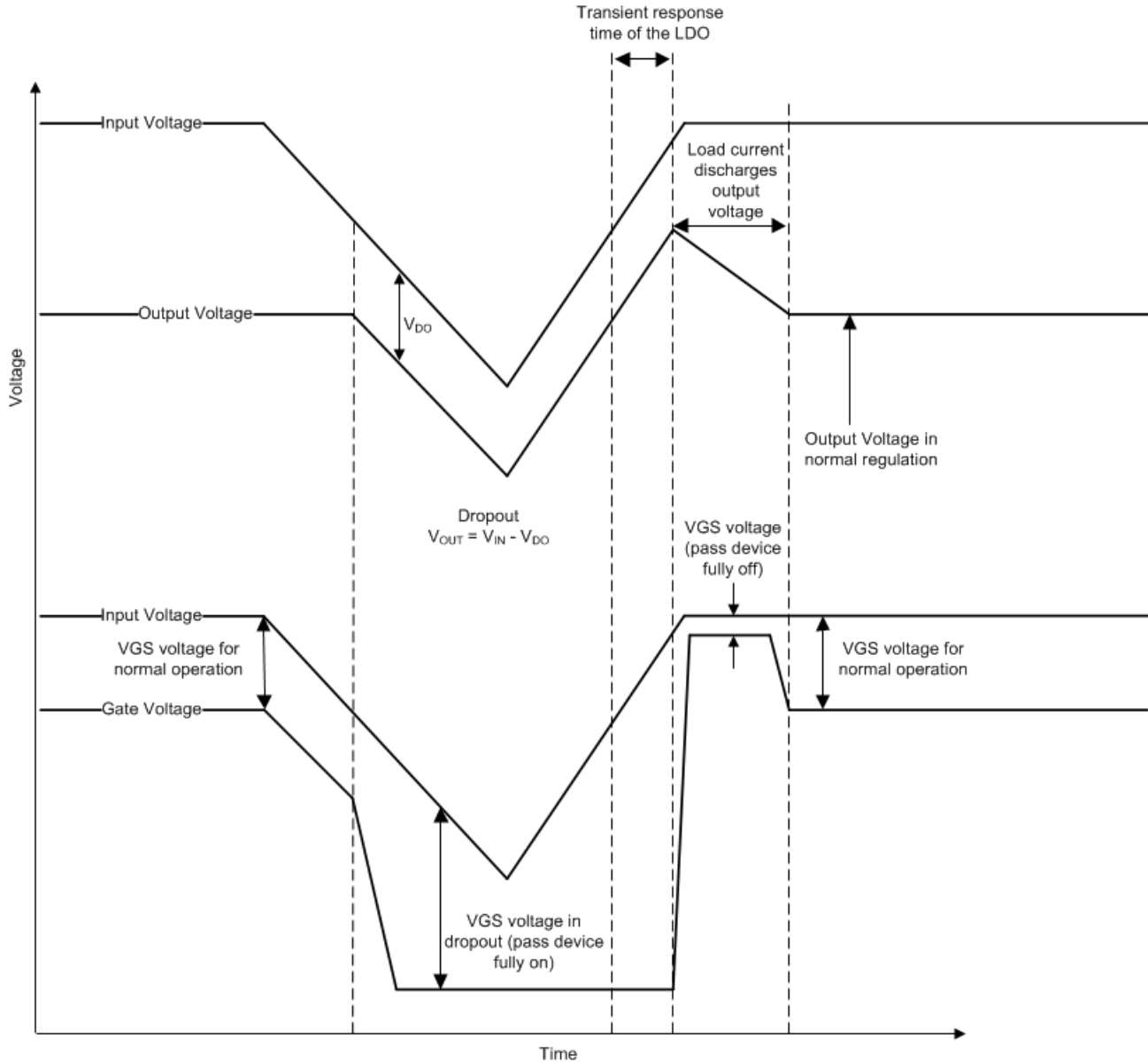


图 8-3. Line Transients From Dropout

### 8.1.5 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

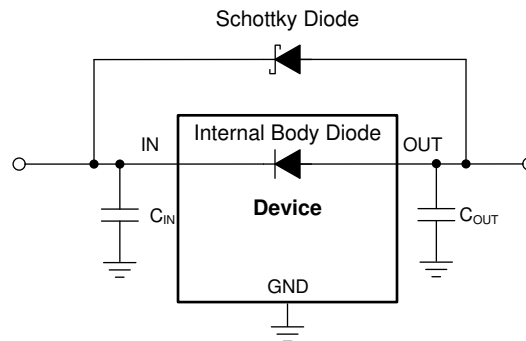
- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of  $V_{OUT} > V_{IN} + 0.3\text{ V}$ :

- If the device has a large  $C_{OUT}$  and the input supply collapses with little or no load current
- The output is biased when the input supply is not established

- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. 图 8-4 shows one approach of protecting the device.



**图 8-4. Example Circuit for Reverse Current Protection Using a Schottky Diode**

### 8.1.6 Power Dissipation ( $P_D$ )

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation ( $P_D$ ).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

#### 备注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ( $T_A$ ) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) of the combined PCB and device package and the temperature of the ambient air ( $T_A$ ).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ( $R_{\theta JA}$ ) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

图 8-5 和 图 8-6 illustrate the functions of  $R_{\theta JA}$  and  $\psi_{JB}$  versus copper (Cu) area and thickness. These plots are generated with a 101.6-mm x 101.6-mm x 1.6-mm printed circuit board (PCB) of two and four layers. For the four-layer board, the inner planes use a 1-oz copper thickness. Outer layers are simulated with both 1-oz and 2-oz copper thickness. A 2 x 1 array of thermal vias of 300- $\mu$ m drill diameter and 25- $\mu$ m Cu plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane.

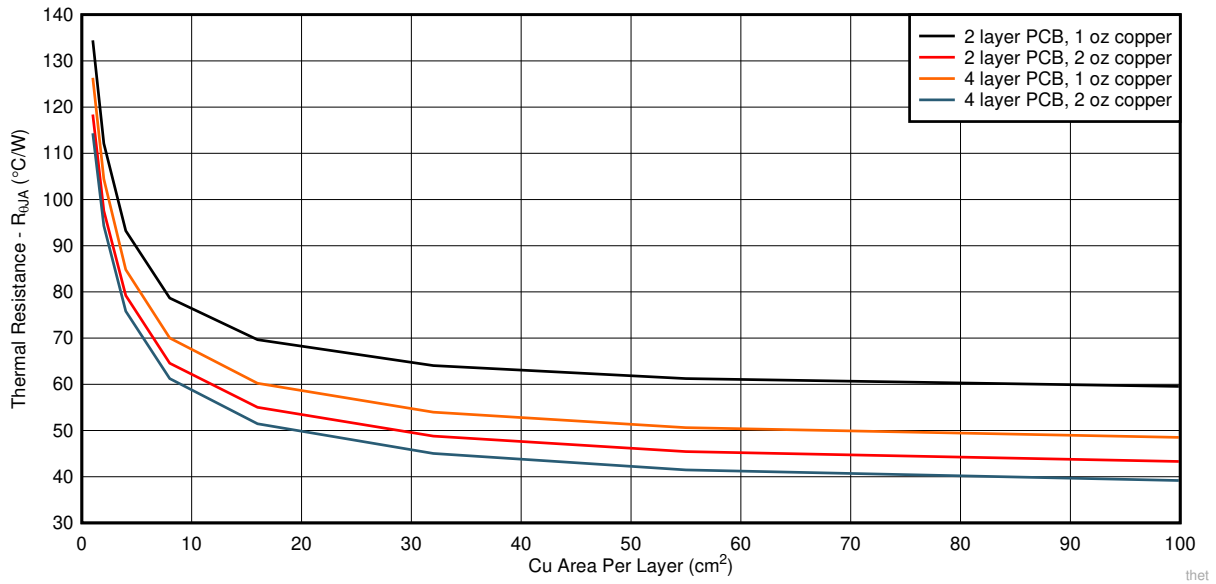


图 8-5.  $R_{\theta JA}$  versus Cu Area for the WSON (DRV) Package

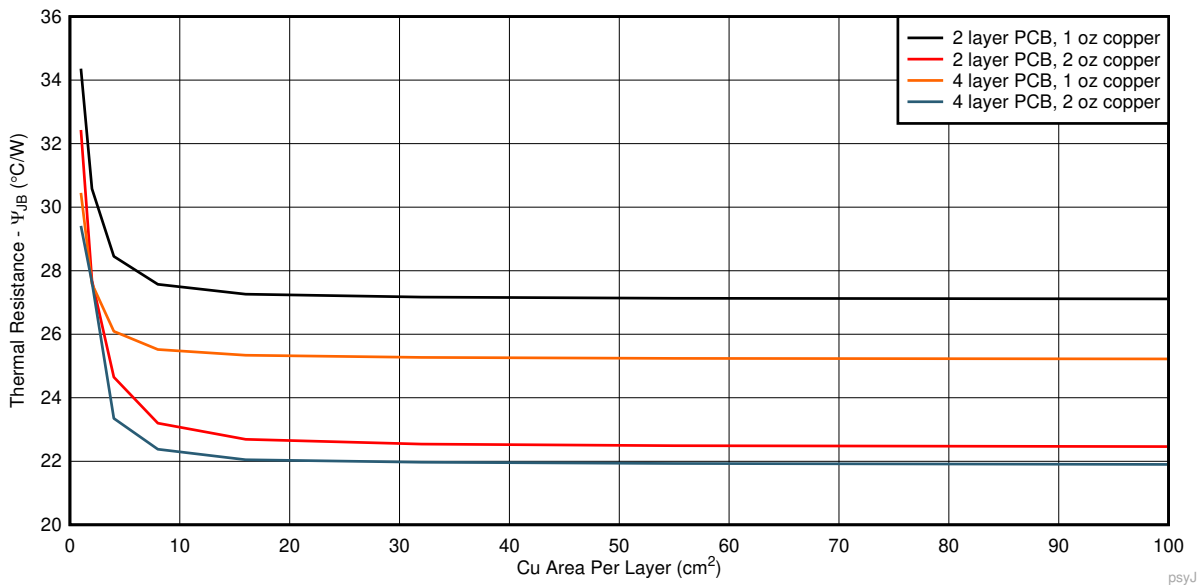
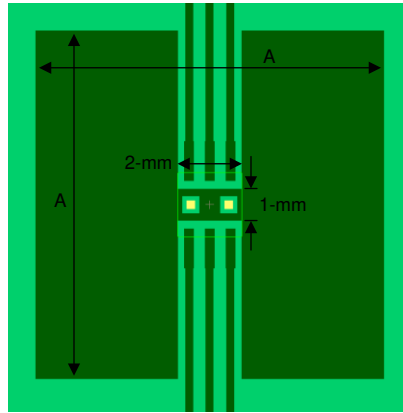


图 8-6.  $\Psi_{JB}$  versus Cu Area for the WSON (DRV) Package



As shown in 图 8-7, each layer has a copper plane of equal area.



Buried plane and bottom layer Cu ground planes are modeled with Area = AxA

图 8-7. Board parameters used for simulation

For a more comprehensive study of how thermal resistance varies with copper area and thickness, see the [An empirical analysis of the impact of board layout on LDO thermal performance application report](#). As shown in 图 8-8, modifying board layout to be more thermally enhanced can lower the  $R_{\theta JA}$  value from 80.3°C/W to 46.8°C/W or better.

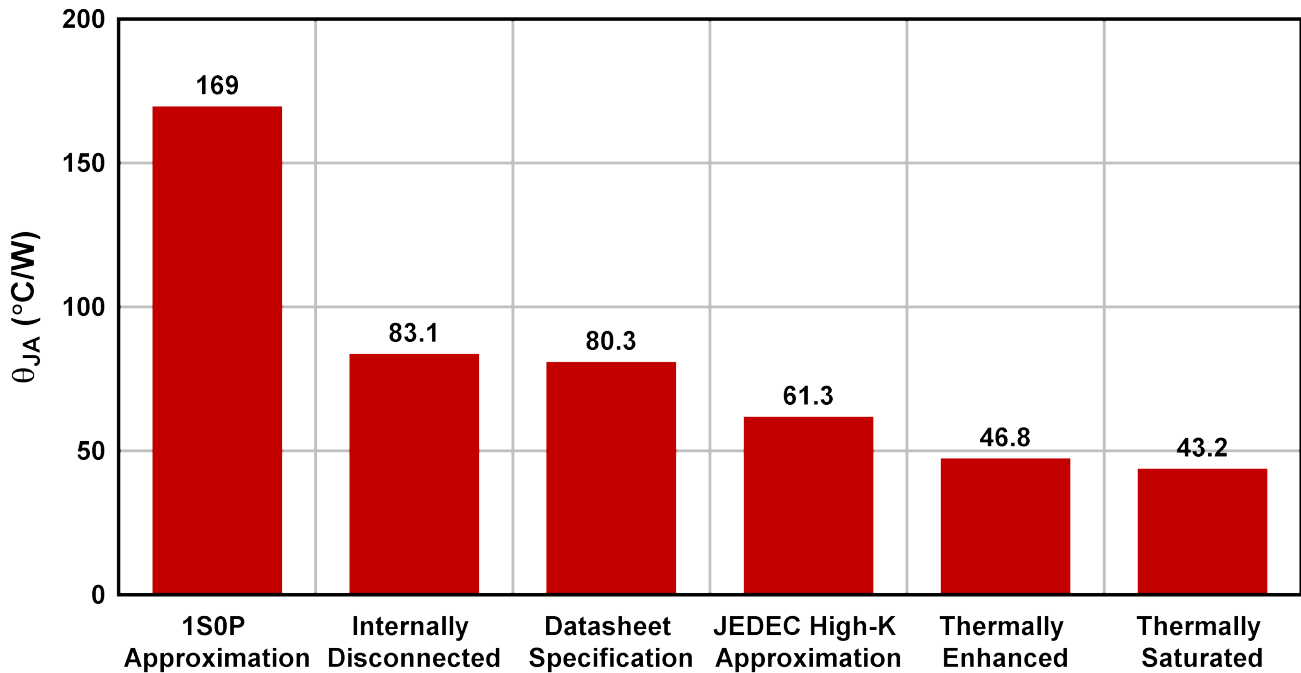


图 8-8. TPS745-Q1 (WSO)  $R_{\theta JA}$  versus Board Layout

### 8.1.7 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage ( $PG_{LTH}$ ), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds  $PG_{HTH}$ , the PG pin becomes high impedance. The open-drain output requires a pullup resistor. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Additionally, the open-drain output can be tied to other open-drain outputs to implement AND logic. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device. Using a pullup resistor from 10 k $\Omega$  to 100 k $\Omega$  is recommended. The push-pull power-good option does not require the pullup resistor and instead has a high logic signal that correlates with the output voltage of the device. The push-pull option is supported only for  $V_{OUT} \geq 1.0$  V. The push-pull option is supported only for  $V_{OUT} \geq 1.0$  V. Do not tie the push-pull output to other logic outputs.

When using a feed-forward capacitor ( $C_{FF}$ ), the time constant for the LDO start-up is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO start-up and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application report](#).

The state of PG is only valid when the TPS745-Q1 operates above the minimum input voltage of the device and power-good is asserted, regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. When the input voltage falls below approximately 0.8 V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output pulled high. Connecting the power-good pullup resistor to the output voltage can help minimize this effect.

### 8.1.8 Feed-Forward Capacitor ( $C_{FF}$ )

For the adjustable-voltage version device, a feed-forward capacitor ( $C_{FF}$ ) can be connected from the OUT pin to the FB pin.  $C_{FF}$  improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended  $C_{FF}$  values are listed in the *Recommended Operating Conditions* table. A higher capacitance  $C_{FF}$  can be used; however, the startup time increases. For a detailed description of  $C_{FF}$  tradeoffs, see the [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application report](#).

### 8.1.9 Start-Up Sequencing

If  $V_{EN}$  is greater than  $V_{UVLO}$  rising (min), the input pin (IN) must sink 1 mA of current to avoid the device being turned on with a floating input pin.

## 8.2 Typical Application

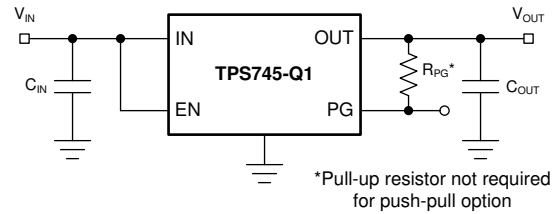


图 8-9. TPS745-Q1 Typical Application

### 8.2.1 Design Requirements

表 8-1 summarizes the design requirements for 图 8-9.

表 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.3 V
Output voltage	1.8 V, ±1%
Input current	300 mA, maximum
Output load	300-mA DC
Maximum ambient temperature	105°C

### 8.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2 µF are selected to give the maximum output capacitance in a small, low-cost package; see the [Input and Output Capacitor Selection](#) section for details.

#### 8.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During start-up, the input current is higher as a result of the inrush current charging the output capacitor. Use [方程式 6](#) to calculate the current through the input.

$$I_{OUT(t)} = \left[ \frac{C_{OUT} \times dV_{OUT}(t)}{dt} \right] + \left[ \frac{V_{OUT}(t)}{R_{LOAD}} \right] \quad (6)$$

where:

- $V_{OUT}(t)$  is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$  is the slope of the  $V_{OUT}$  ramp
- $R_{LOAD}$  is the resistive load impedance

### 8.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) and the total power dissipation ( $P_D$ ). Use 方程式 7 to calculate the power dissipation. Multiply  $P_D$  by  $R_{\theta JA}$  as 方程式 8 shows and add the ambient temperature ( $T_A$ ) to calculate the junction temperature ( $T_J$ ).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (7)$$

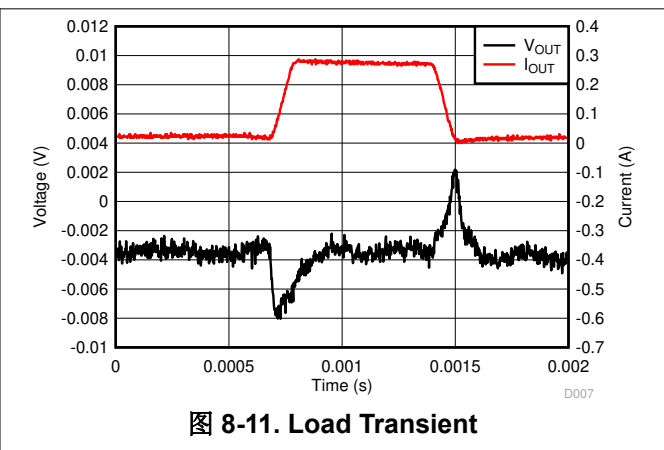
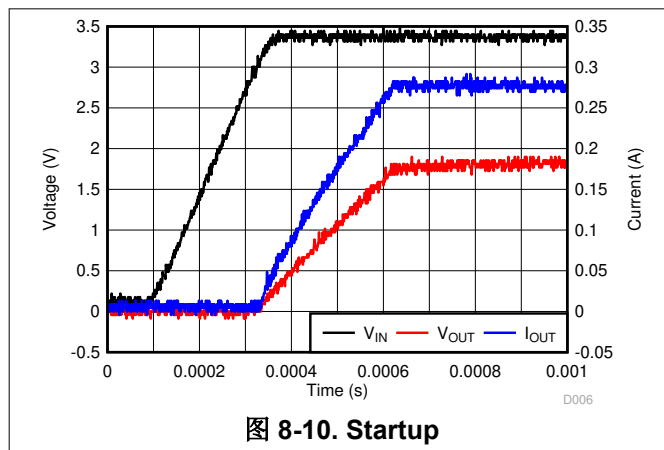
$$T_J = R_{\theta JA} \times P_D + T_A \quad (8)$$

Calculate the maximum ambient temperature according to 方程式 9 and 方程式 10. The maximum ambient temperature is 113.86°C for the example conditions.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (9)$$

$$T_{A(MAX)} = 150^\circ\text{C} - 80.3^\circ\text{C/W} \times (3.3\text{ V} - 1.8\text{ V}) \times (0.3\text{ A}) = 113.86^\circ\text{C} \quad (10)$$

### 8.2.3 Application Curves



## 9 Power Supply Recommendations

The TPS745-Q1 is designed to operate from an input voltage supply range from 1.5 V to 6.0 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance. Connect a low output impedance power supply directly to the IN pin of the TPS745-Q1.

## 10 Layout

### 10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Only place tented thermal vias directly beneath the thermal pad of the DRV or DRB package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

### 10.2 Layout Examples

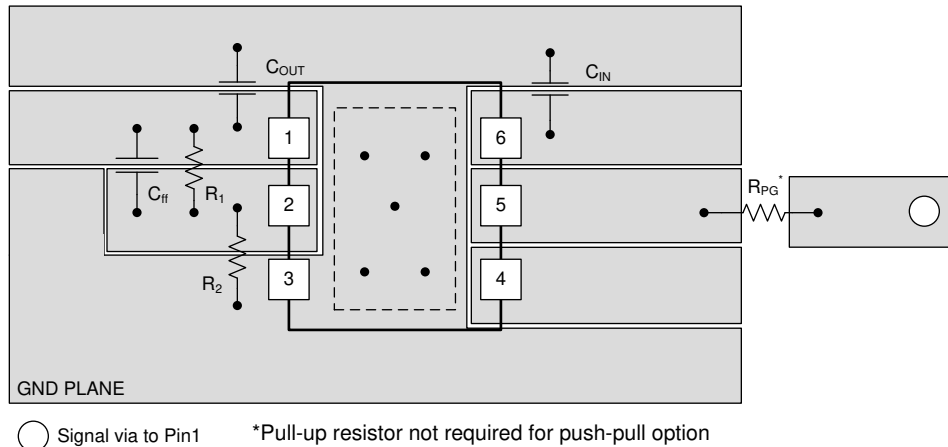


图 10-1. Layout Example for the DRV Package

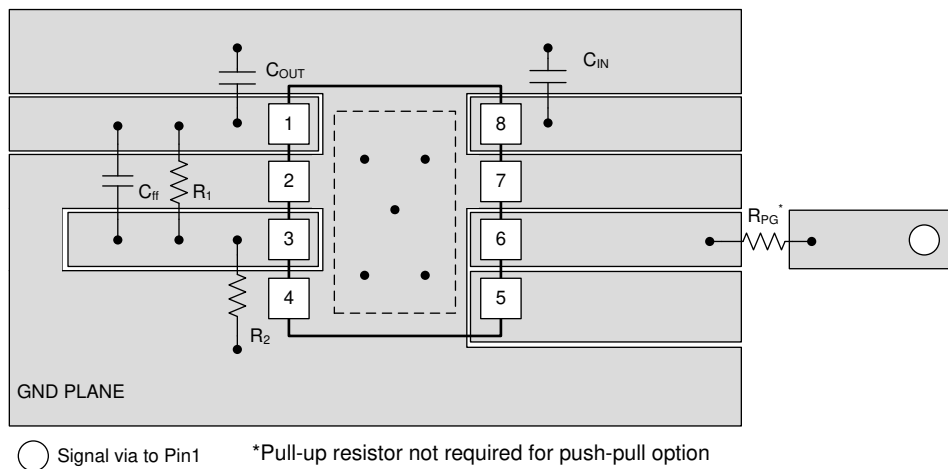


图 10-2. Layout Example for the DRB Package

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Device Nomenclature

表 11-1. Device Nomenclature<sup>(1) (2)</sup>

PRODUCT	V <sub>OUT</sub>
TPS745xx(x)PvQWyyyzQ1	<p><b>xx(x)</b> is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V; 01 = adjustable).</p> <p><b>P</b> indicates an active output discharge feature. All members of the TPS745-Q1 family actively discharge the output when the device is disabled.</p> <p><b>v</b> indicates the topology of the power-good output and the timing associated with the power-good delay.</p> <ul style="list-style-type: none"> <li>If unused, indicates an open-drain power-good output with a 150-<math>\mu</math>s delay.</li> <li>If <b>B</b>, indicates a open-drain power-good output with a 5-ms delay.</li> <li>If <b>C</b>, indicates a push-pull power-good output with a 150-<math>\mu</math>s delay.</li> </ul> <p><b>Q</b> indicates that this device is a Grade-1 device in accordance with the AEC-Q100 standard.</p> <p><b>W</b> indicates the package has wettable flanks.</p> <p><b>yyy</b> is the package designator.</p> <p><b>z</b> is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).</p> <p><b>Q1</b> indicates that this device is an automotive grade (AEC-Q100) device.</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on [www.ti.com](http://www.ti.com).
- (2) Output voltages from 0.65 V to 5.0 V in 50-mV increments are available. Contact the factory for details and availability.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [An empirical analysis of the impact of board layout on LDO thermal performance application report](#)
- Texas Instruments, [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application report](#)

#### 11.3 接收文档更新通知

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#### 11.4 支持资源

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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#### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

### **Mechanical, Packaging, and Orderable Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74501PBQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	1S36	<a href="#">Samples</a>
TPS74501PCQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	1ZF6	<a href="#">Samples</a>
TPS74501PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74501P	<a href="#">Samples</a>
TPS74501PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1S26	<a href="#">Samples</a>
TPS74507PQWDRBRQ1	PREVIEW	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 125		
TPS745105PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	1S66	<a href="#">Samples</a>
TPS74510PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74510P	<a href="#">Samples</a>
TPS74510PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1S56	<a href="#">Samples</a>
TPS745115PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	745115	<a href="#">Samples</a>
TPS74511PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74511P	<a href="#">Samples</a>
TPS74511PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1S76	<a href="#">Samples</a>
TPS745125PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	745125	<a href="#">Samples</a>
TPS74512PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74512P	<a href="#">Samples</a>
TPS74512PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1S86	<a href="#">Samples</a>
TPS745135PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	745135	<a href="#">Samples</a>
TPS74513PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74513P	<a href="#">Samples</a>
TPS74515PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74515P	<a href="#">Samples</a>
TPS74515PQWDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1S96	<a href="#">Samples</a>
TPS74517PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74517P	<a href="#">Samples</a>
TPS74518PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74518P	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74518PQWDRVRQ1	ACTIVE	WSO	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1SA6	<a href="#">Samples</a>
TPS74522PQWDRVRQ1	ACTIVE	WSO	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1SB6	<a href="#">Samples</a>
TPS74525PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74525P	<a href="#">Samples</a>
TPS74525PQWDRVRQ1	ACTIVE	WSO	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1SC6	<a href="#">Samples</a>
TPS74528PQWDRBRQ1	PREVIEW	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74528PQWDRVRQ1	ACTIVE	WSO	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1SD6	<a href="#">Samples</a>
TPS74529PQWDRBRQ1	PREVIEW	SON	DRB	8	3000	TBD	Call TI	Call TI	-40 to 125		
TPS74529PQWDRVRQ1	ACTIVE	WSO	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1SE6	<a href="#">Samples</a>
TPS74530PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74530P	<a href="#">Samples</a>
TPS74533PCQWDRVRQ1	ACTIVE	WSO	DRV	6	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	1ZE6	<a href="#">Samples</a>
TPS74533PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74533P	<a href="#">Samples</a>
TPS74533PQWDRVRQ1	ACTIVE	WSO	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1SF6	<a href="#">Samples</a>
TPS74534PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74534P	<a href="#">Samples</a>
TPS74550PQWDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	74550P	<a href="#">Samples</a>
TPS74550PQWDRVRQ1	ACTIVE	WSO	DRV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1T36	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS745-Q1 :**

- Catalog : [TPS745](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74501PBQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74501PCQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74501PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74501PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS745105PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74510PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74510PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS745115PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74511PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74511PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS745125PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74512PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74512PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS745135PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74513PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74515PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74515PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74517PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74518PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74518PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74522PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74525PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74525PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74528PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74529PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74530PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74533PCQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74533PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74533PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS74534PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74550PQWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74550PQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74501PBQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74501PCQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74501PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74501PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS745105PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74510PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74510PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS745115PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74511PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74511PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS745125PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74512PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74512PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS745135PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74513PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74515PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74515PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74517PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74518PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74518PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74522PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74525PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74525PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74528PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74529PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74530PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74533PCQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74533PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74533PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS74534PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74550PQWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS74550PQWDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0

**DRB 8**

**GENERIC PACKAGE VIEW**

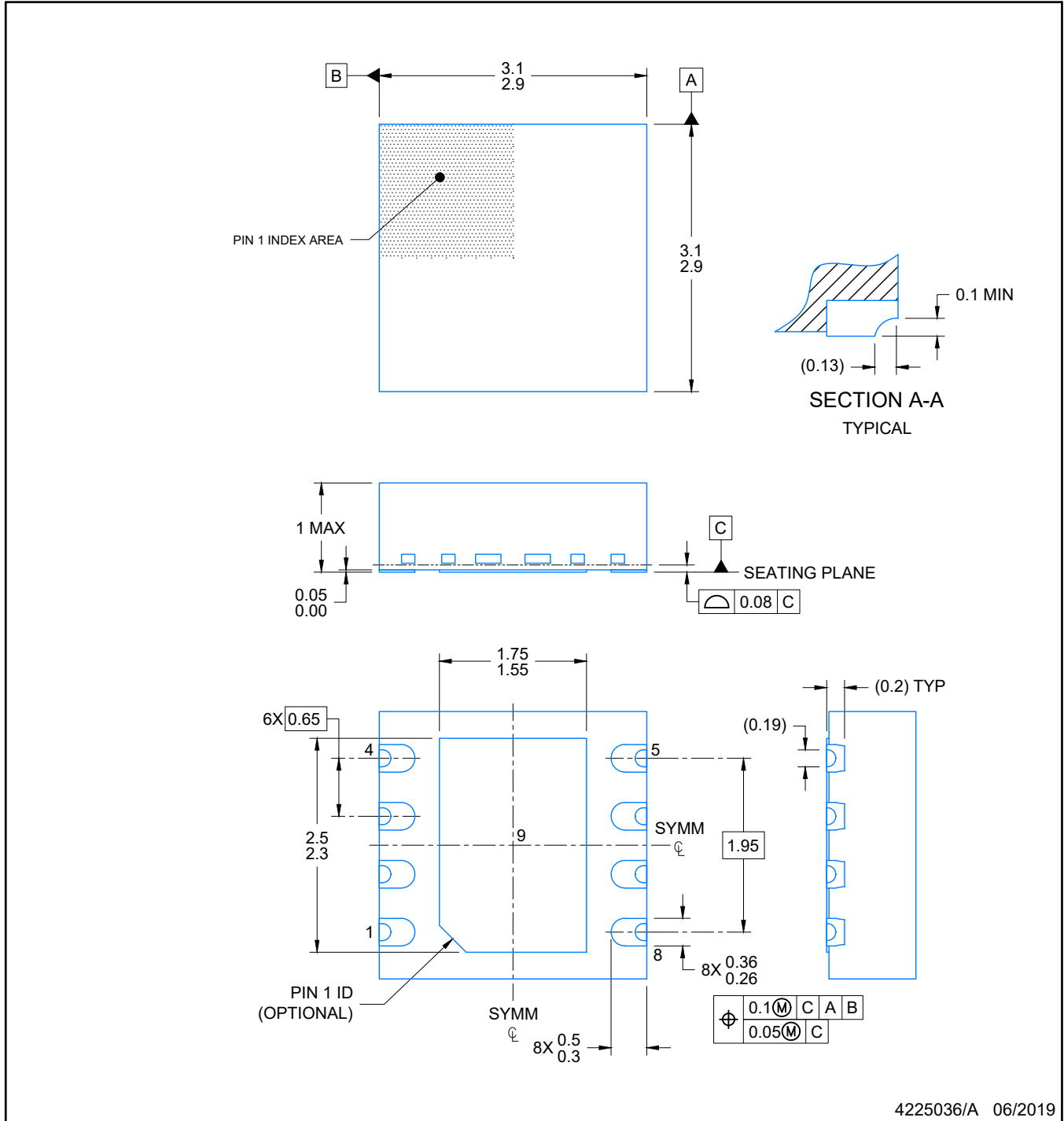
**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203482/L



4225036/A 06/2019

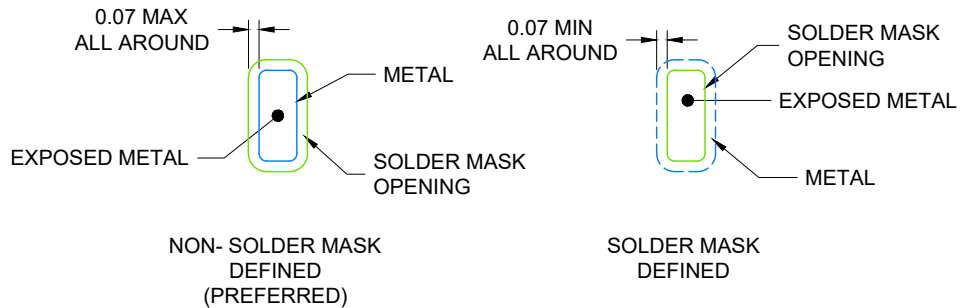
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.





LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

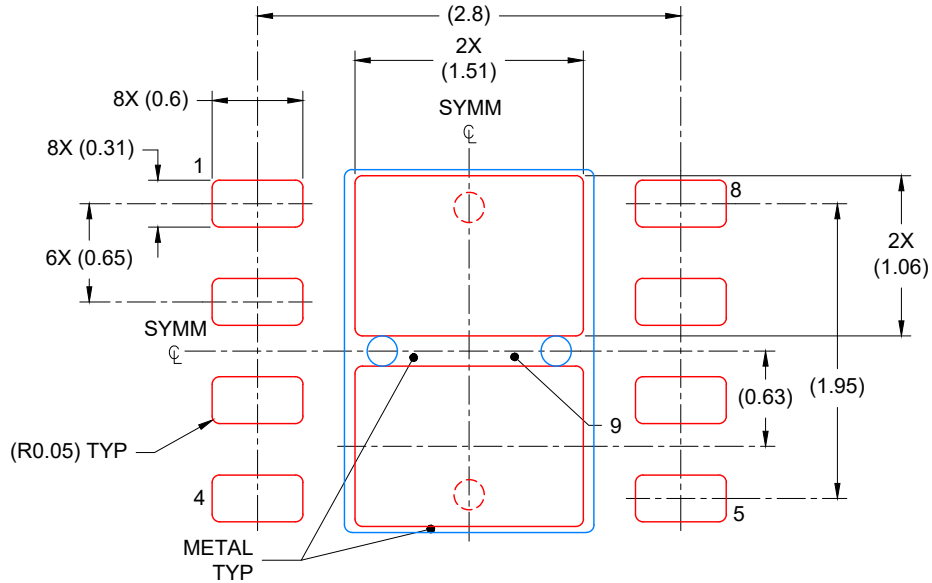


SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 81% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

DRV 6

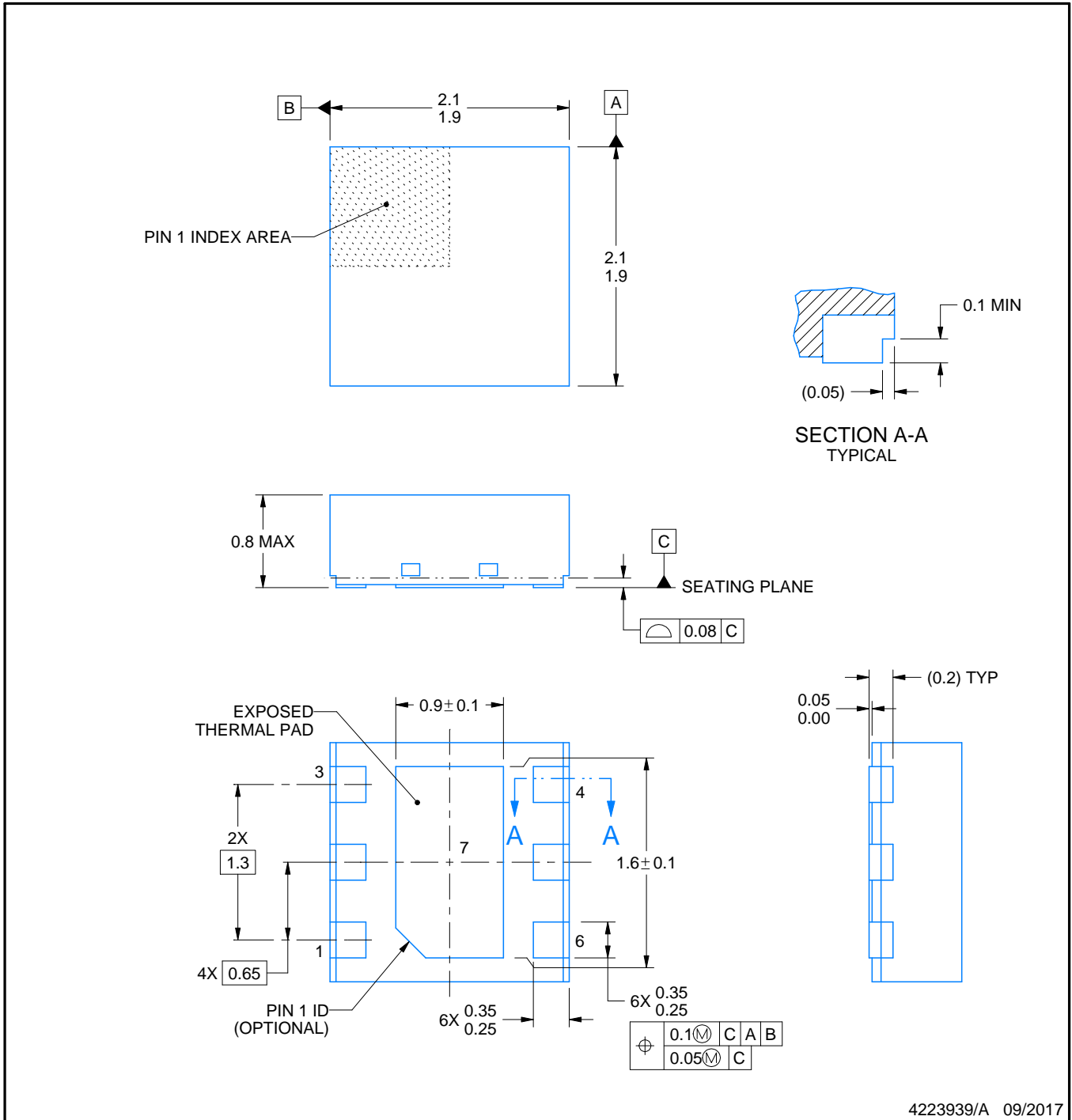
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4206925/F



NOTES:

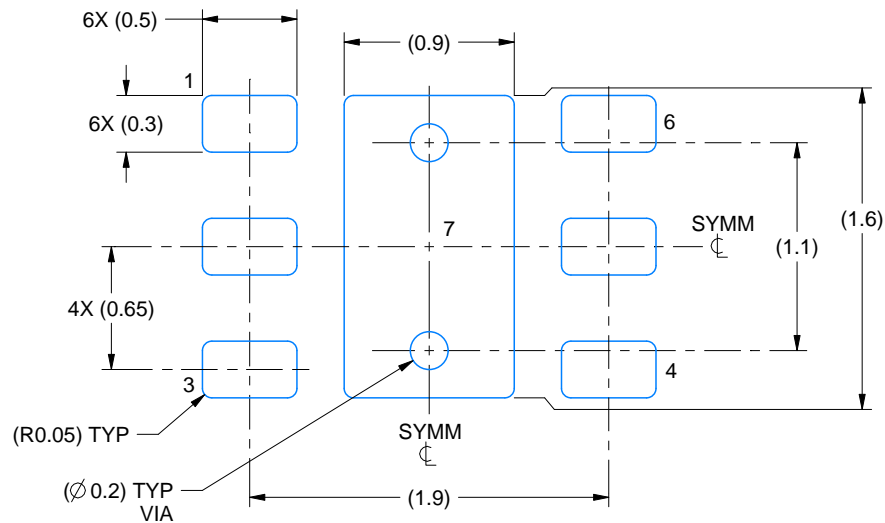
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

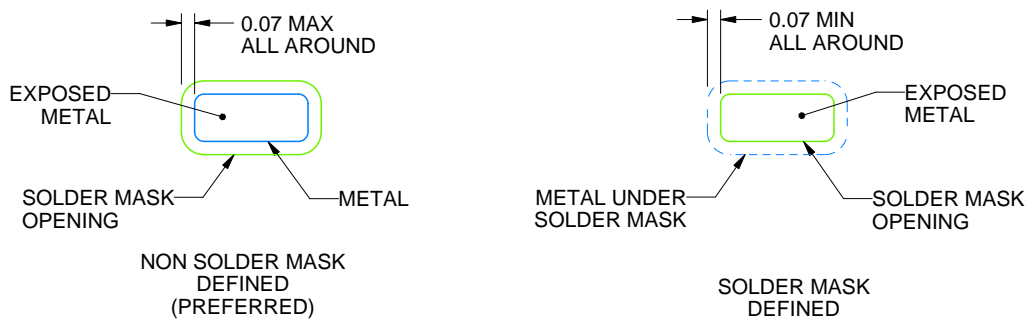
DRV0006C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:25X



SOLDER MASK DETAILS

4223939/A 09/2017

NOTES: (continued)

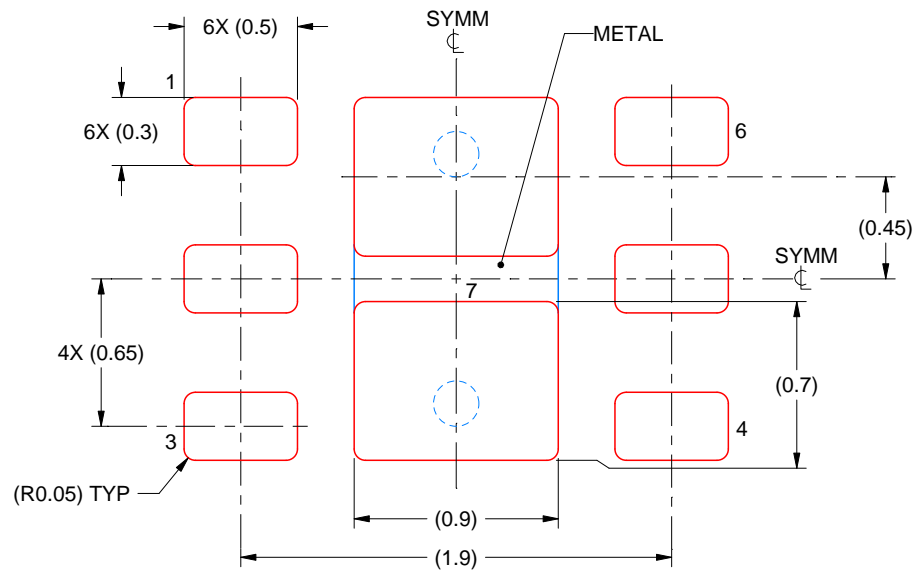
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DRV0006C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7:  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

4223939/A 09/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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