Off-Line Primary Side Sensing Controller with PFC

Check for Samples: TPS92314, TPS92314A

FEATURES

- **Regulates LED Current Without Secondary Side Sensing**
- **Adaptive ON-time Control with Inherent PFC**
- **Critical-Conduction-Mode (CRM) with Zero-Current Detection (ZCD) for Valley Switching**
- **Programmable Switch Turn ON Delay**
- **Programmable Constant ON-Time (COT)**
- **Over Current Limit Options:**
  - **TPS92314: 1.15V**
  - **TPS92314A: 2.0V**
- **Advanced Over Current and Over Voltage Protection**
- **Internal Over-temperature Protection**
- **8-Pin SOIC Package**

APPLICATIONS

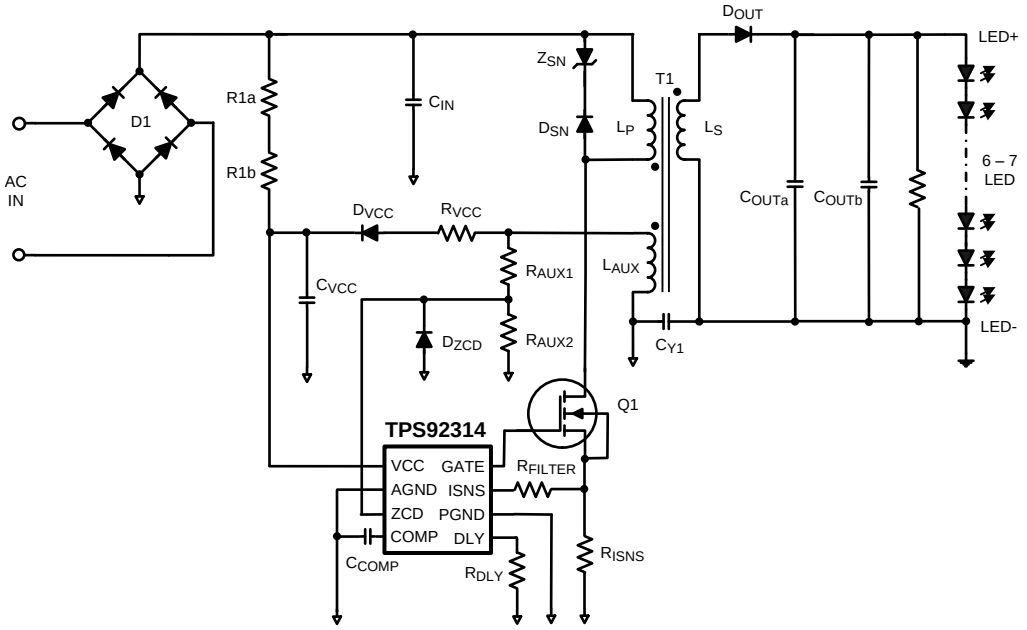
- **Residential LED Lamps: A19 (E26/27, E14), PAR30/38, GU10**
- **Solid State Lighting**

DESCRIPTION

The TPS92314/14A is an off-line controller specifically designed to drive high power LEDs for lighting applications. Features include adaptive constant on-time control and quasi-resonant switching. Resonant switching allows for a reduced EMI signature and increased system efficiency. Thus, the device introduces a low external parts count and high level of integration. The control algorithm of TPS92314/14A adjusts the on time with reference to the primary side inductor peak current and secondary side inductor discharge time dynamically, the response time of which is set by an external capacitor.

The over current protection is implemented by a cycle by cycle current limit of the primary inductor current. TPS92314A has a higher OCP threshold which is more suitable for universal line application and TPS92314 can optimize the system cost. Other supervisory features of the TPS92314/14A include VCC over voltage protection and under-voltage lockout, output LEDs over-voltage protection and controller thermal shutdown. The TPS92314/14A is available in 8-pin SOIC package.

TYPICAL APPLICATION



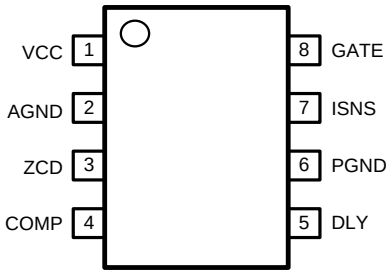


Figure 1. 8-Pin SOIC (Top View)
See D Package

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	VCC	Power supply Input	This pin provides power to the internal control , connect a 10μF~20μF capacitor to ground for filtering.
2	AGND	Small signal Ground	Control signal ground return.
3	ZCD	Zero crossing detection input	The pin senses the voltage of the auxiliary winding for zero current detection.
4	COMP	Compensation network	Output of the error amplifier. Connect a capacitor from this pin to ground to determine the frequency response of average current control loop.
5	DLY	Delay control input	Connect a resistor from this pin to ground to set the delay between switching ON and OFF periods.
6	PGND	Power Ground	Gate driver ground return.
7	ISNS	Current sense voltage feedback	Switching MOSFET current sense pin.
8	GATE	Gate driver output	The output provides the gate driver of the power switching MOSFET.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

	VALUE / UNITS
VCC to GND	–0.3V to 40V
DLY,COMP,ZCD to GND	–0.3V to 7V
ISNS to GND	–0.3V to 7V
GATE to GND	(5ns,-6V) -0.3V to 12V
ESD Susceptibility: HBM (2)	±2 kV
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_{J-MAX})	+150°C
Maximum Lead Temperature (Solder and Reflow)	260°C

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For specifications and test conditions, see the Electrical Characteristics. All voltages are with respect to the potential at the GND pin, unless otherwise specified.
(2) Human Body Model, applicable std. JESD22-A114-C.

RECOMMENDED OPERATING CONDITIONS

	VALUE / UNITS
Supply Voltage range VCC	13V to 35V
Junction Temperature (T_J)	-40°C to +125°C
Thermal Resistance (θ_{JA}) (1)	162°C/W

(1) This $R_{\theta JA}$ typical value determined using JEDEC specifications JESD51-1 to JESD51-11. However junction-to-ambient thermal resistance is highly board layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

ELECTRICAL CHARACTERISTICS

V_{CC} = 18V unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the full Operating Temperature Range. Data sheet minimum and maximum specification limits are specified by design, test or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
SUPPLY VOLTAGE INPUT (VCC)						
$V_{CC-UVLO}$	VCC Turn on threshold		22.5 / **21.7**	25.4	28.3 / **29.5**	V
	VCCTurn off threshold		10.4 / **10.1**	12.9	15.3 **/ 16.0**	V
	Hysteresis			12.5		
$I_{STARTUP}$	Startup Current	V_{CC}=$V_{CC-UVLO}$–3.0V		22.2	**25.8**	µA
V_{CC-OVP}	Over voltage protection threshold		**32.7**	35.5	**38.0**	V
I_{VCC}	Operating supply current	Not switching	**0.8**	1.2	**1.8**	mA
		65kHz switching		2.3	3.0	mA
ZERO CROSS DETECT (ZCD)						
I_{ZCD}	ZCD bais current	V_{ZCD}= 5V		0.01	1	uA
$V_{ZCD-OVP}$	ZCD over-voltage threshold		**3.9**	4.3	**4.7**	V
T_{OVP}	Over voltage de-bounce time			3		cycle
$V_{ZCD-ARM}$	ZCD Arming threshold	V_{ZCD} = Increasing	**1.04**	1.23	**1.42**	V
$V_{ZCD-TRIG}$	ZCD Trigger threshold	V_{ZCD} = Decreasing	**0.48**	0.6	**0.77**	V
$V_{ZCD-HYS}$	ZCD Hysteresis	$V_{ZCD-ARM}$-$V_{ZCD-TRIG}$		0.61		V
COMPENSATION (COMP)						
$I_{COMP-SOURCE}$	Internal reference current for primary side current regulation	V_{COMP} = 2.0V, V_{ISNS} = 0V, Measure at COMP pin		27		µA

(1) Typical numbers are at 25°C and represent the most likely norm.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 18V unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the full Operating Temperature Range. Data sheet minimum and maximum specification limits are specified by design, test or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
gm_{ISNS}	ISNS error amp trans-conductance	Δ V_{ISNS} to Δ I_{COMP} at V_{COMP} = 2.5V		96		µmho
DELAY CONTROL (DLY)						
V_{DLY}	DLY pin internal reference voltage		**1.21**	1.24	**1.3**	V
$I_{DLY-MAX}$	DLY source current	V_{DLY}= 0V	**250**	450		µA
CURRENT SENSE (ISNS)						
$V_{ISNS-OCP}$	Over Current Limit Detection Threshold	TPS92314	1.07	1.15	1.22	V
$V_{ISNS-OCP}$	Over Current Limit Detection Threshold	TPS92314A	1.90	2.0	2.10	V
I_{ISNS}	Current Sense Bias Current	V_{ISNS}= 5V	-1		1	µA
T_{OCP}	Over current Limit Detection Propagation Delay	Measure ISNS pin pulse width with V_{ISNS} = 5V		256		ns
GATE DRIVER (GATE)						
V_{GATE-H}	GATE low voltage	IGATE = 50mA source	**7.6**	9.4		V
V_{GATE-L}	GATE high drive voltage	IGATE = 50mA sink		85	**125**	mV
$t_{GATE-RISE}$	Rise Time	CLOAD = 1nF		94		ns
$t_{GATE-FALL}$	Fall Time	CLOAD = 1nF		16		ns
T_{ON-MIN}	Minimum ON time	With ZCD signal.	**311**	500	**900**	ns
T_{ON-MAX}	Maximum ON time		**27**	43.9	**61**	µs
$T_{OFF-MIN}$	Minimum OFF time		**1.00**	1.50	**1.93**	µs
$T_{OFF-MAX}$	Maximum OFF time	ZCD = GND	**67**	117	**151**	µs
$T_{OFF-START}$	Maximum OFF time when start up.	Maximum OFF time at first 511 switching after UVLO	**44**	78	**102**	µs
$T_{OFF-OCP}$	Maximum OFF time when OCP	OFF time when V_{ISNS} =4V.		233		µs
THERMAL SHUTDOWN						
TSD	Thermal shutdown temperature	See (2)		165		°C
	Thermal Shutdown hysteresis			20		°C

(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typ.) and disengages at T_J = 145°C (typ).

TYPICAL PERFORMANCE CHARACTERISTICS

All curves taken at V_{CC}=18V with configuration in typical application for driving seven power LEDs with I_{LED}=350mA shown in this datasheet. T_A=25°C, unless otherwise specified.

$V_{CC-UVLO}$ vs Temperature

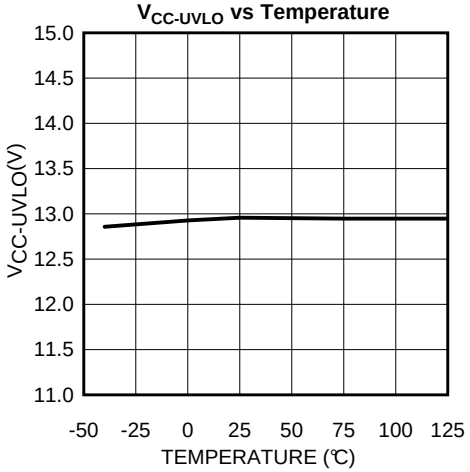


Figure 2.

V_{CC} Startup Voltage vs Temperature

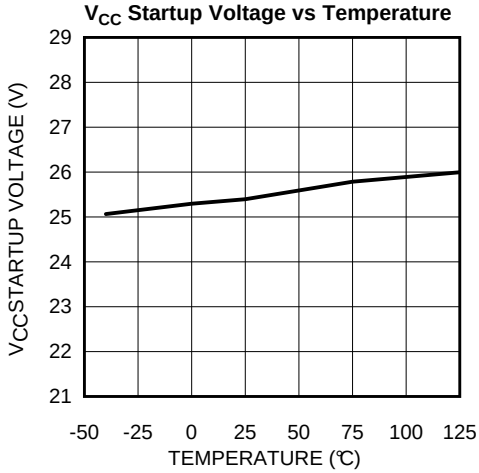


Figure 3.

$T_{OFF-MAX}$ vs Temperature

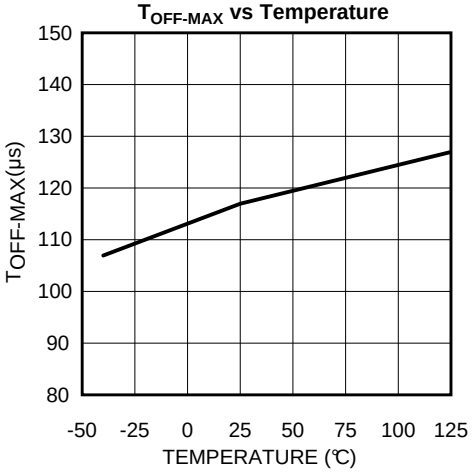


Figure 4.

T_{ON-MIN} vs Temperature

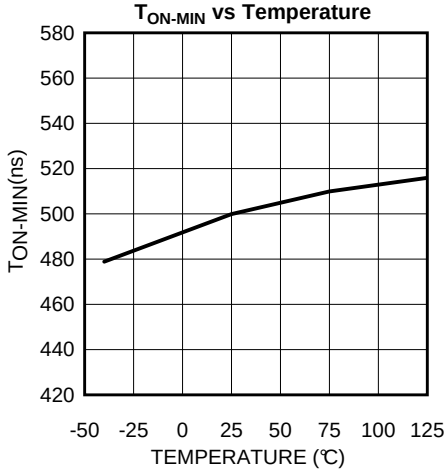


Figure 5.

I_{VCC-SD} vs Temperature

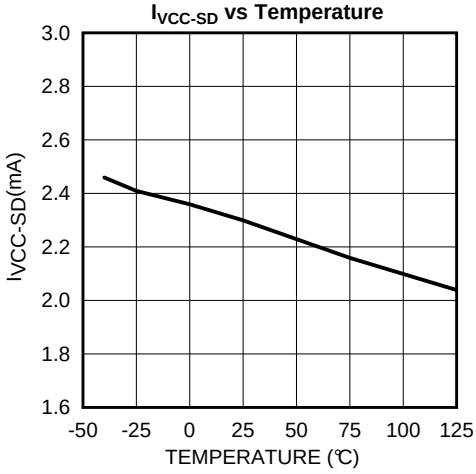


Figure .

$V_{ZCD-OVP}$ vs Temperature

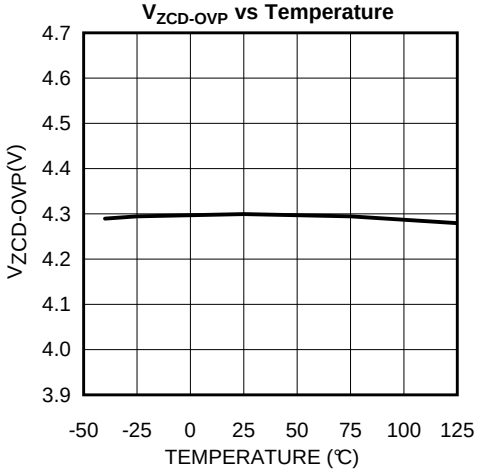


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

All curves taken at V_{CC}=18V with configuration in typical application for driving seven power LEDs with I_{LED}=350mA shown in this datasheet. T_A=25°C, unless otherwise specified.

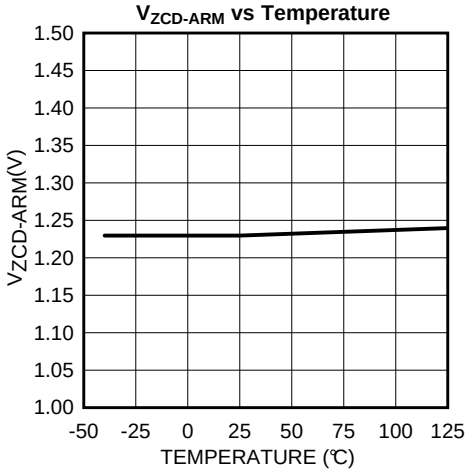


Figure 7.

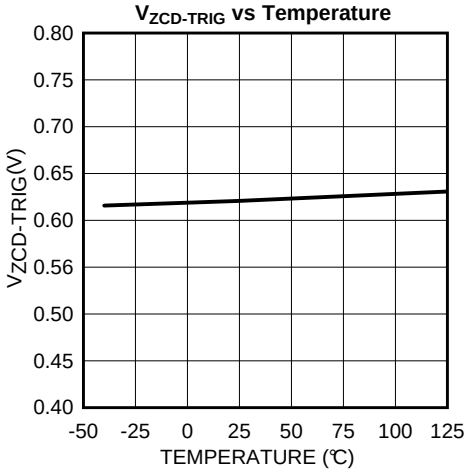


Figure 8.

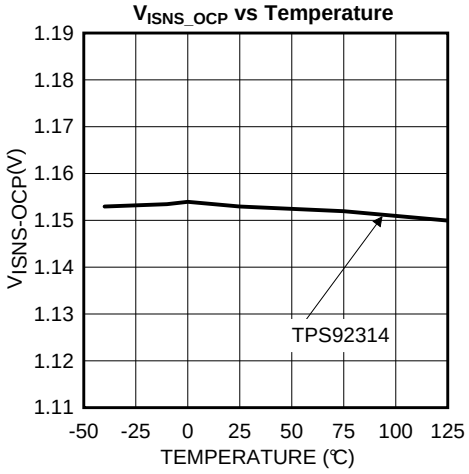


Figure 9.

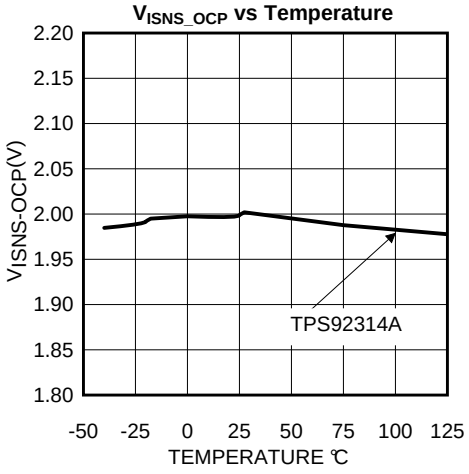


Figure 10.

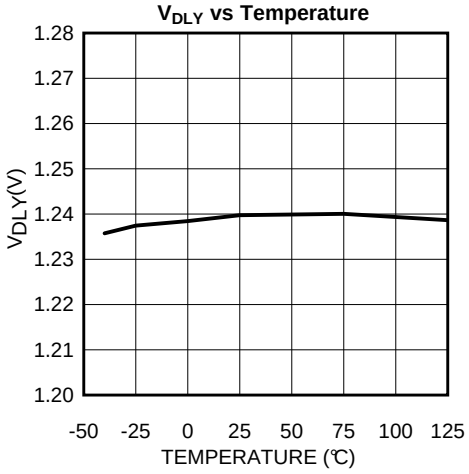


Figure 11.

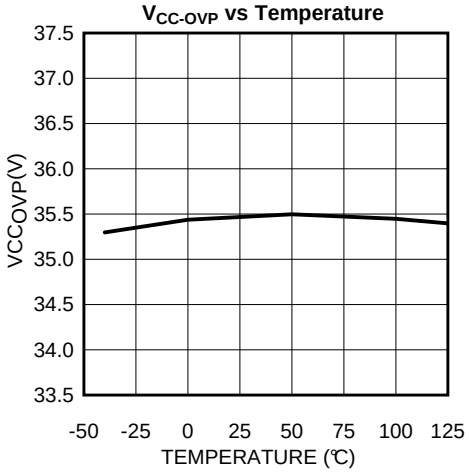


Figure 12.

SIMPLIFIED INTERNAL BLOCK DIAGRAM

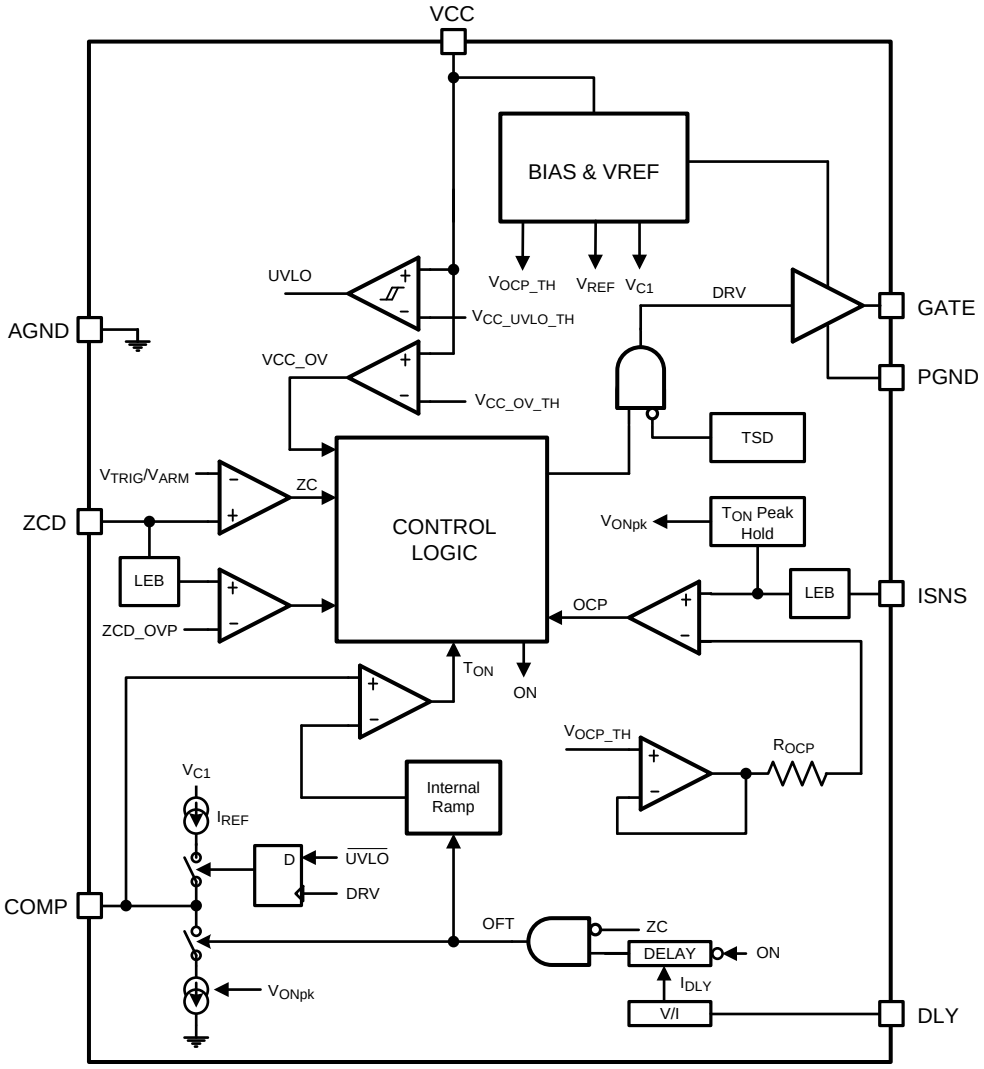


Figure 13. Simplified Block Diagram

APPLICATION INFORMATION

The TPS92314/14A is an off-line controller specifically designed to drive LEDs. This device operates in Critical Conduction Mode (CRM) with adaptive Constant ON-Time control, so that high power factor can be achieved naturally. The TPS92314/14A can be configured as an isolated or non-isolated off-line converter. Refer to TPS92314/14A typical schematic, on the front page, in the following discussion. The TPS92314/14A flyback converter consists of a transformer which includes three windings L_P, L_S and L_{AUX}. An external MOSFET Q_1 and inductor current sensing resistor R_{ISNS}. Secondary side components are secondary side transformer winding L_S, output diode D_{OUT}, and output capacitor C_{OUT}. An auxiliary winding is required, and serves two functions. Auxiliary power is developed from the winding to power the TPS92314/14A after start-up, and detect the zero crossing point due to the end of a complete switching cycle. During the on-period, Q_1 is turned on, and current flows through L_P, Q_1 and R_{ISNS} to ground, input energy is stored in the primary inductor L_P. Simultaneously, the I_{SNS} pin of the device monitors the voltage of the current sensing resistor R_{ISNS} to perform the cycle-by-cycle inductor current limit function. During the time MOSFET Q_1 is off, current flow in L_P ceases and the energy stored during the on cycle is released to output and auxiliary circuits. During Q_1 off-time current in the secondary winding L_S charges the output capacitor C_{OUT} through D_{OUT} and supplies the LED load. During Q_1 on-time, C_{OUT} is responsible to supply load current to LED load during subsequent on-period. Also during Q_1 off-time current is delivered to the auxiliary winding through D_{VCC} and powers the TPS92314/14A. The voltage across L_{AUX}, V_{LAUX} is fed back to the ZCD pin through a resistor divider network formed by R_{AUX1} and R_{AUX2} to perform zero crossing detection of V_{LAUX}, which determines the end of the off-period of a switching cycle. The next on period of a new cycle will be initiated after an inserted delay of 2 x t_{DLY}. The t_{DLY} is programmable by a single resistor connecting the DLY pin and ground. The setting of the delay time, t_{DLY} will be described in a separate paragraph. The driver signal t_{ON} time width is generated by comparing an internal generated saw-tooth waveform with the voltage on the COMP pin (V_{COMP}). Since V_{COMP} is slow varying, t_{ON} is nearly constant within an AC line cycle. The duration of the off-period (t_{OFF}) is determined by the rate of discharging of the secondary current through the transformer. Also,

$$I_{LS\text{-}PEAK} = n \times I_{LP\text{-}PEAK} \quad (1)$$

where

- n is the turn ratio of L_P and L_S.

Figure 14 shows the typical waveforms in normal operation.

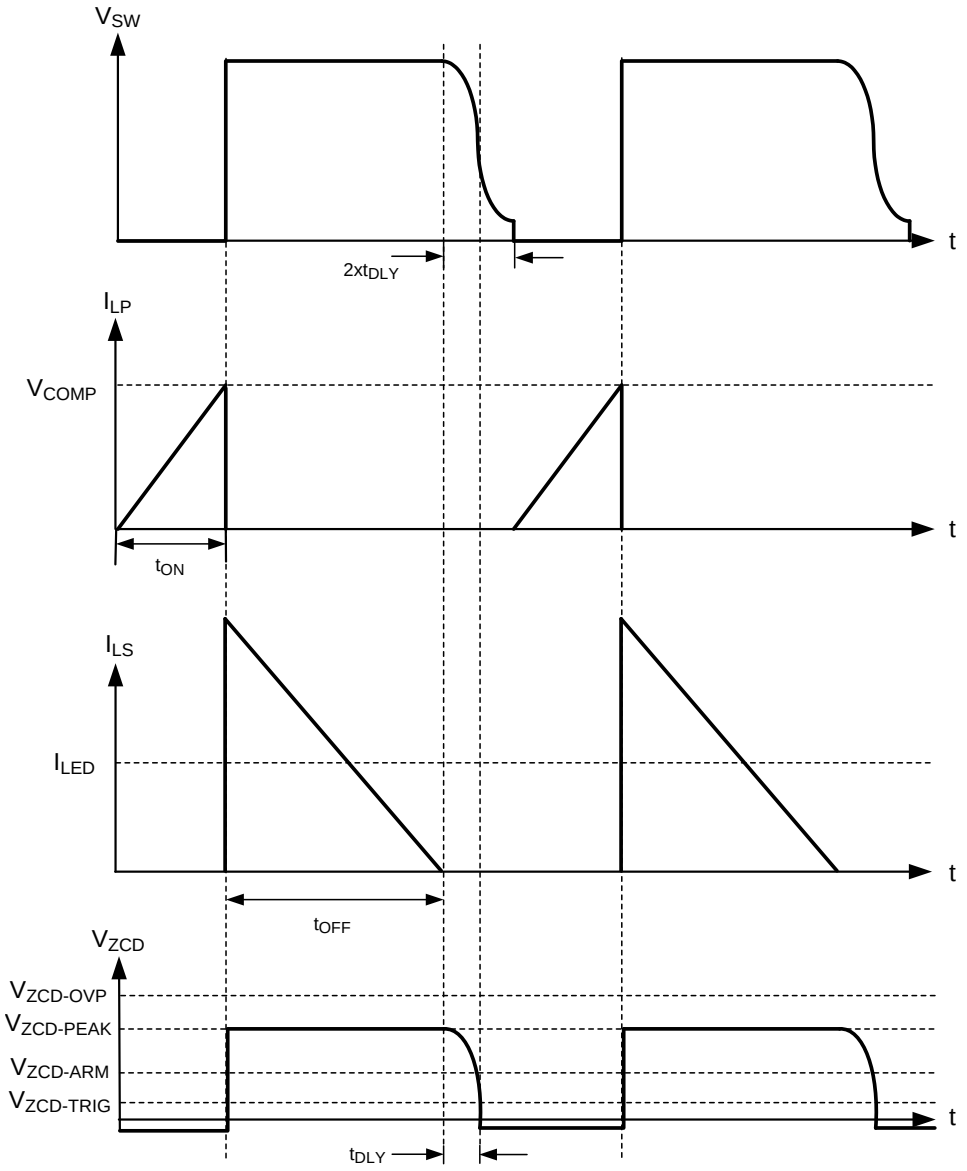


Figure 14. Primary and Secondary Side Current Waveforms

Startup Bias and UVLO

During startup, the TPS92314/14A is powered from the AC line through R_1 and bridge diode D_1 (Typical Application on front page). In the startup state, most of the internal circuits of the TPS92314/14A are shut down in order to minimize internal quiescent current. When V_{CC} reaches the rising threshold of the $V_{CC-UVLO}$ (typically 26V), the TPS92314/14A is operating in a low switching frequency mode, where t_{ON} and t_{OFF} are fixed to 1.5µs and 72µs. When $V_{ZCD–PEAK}$ is higher than $V_{ZCD-ARM}$, the TPS92314/14A enters normal operation.

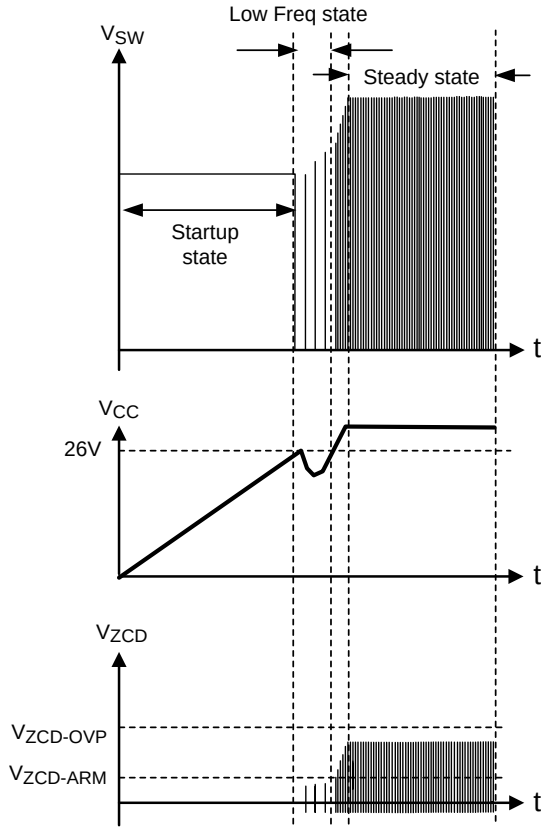


Figure 15. Start up Bias Waveforms

Zero Crossing Detection

To minimized the switching loss of the power MOSFET, a zero crossing detection circuit is embedded in the TPS92314/14A. V_{LAUX} is AC voltage coupled from V_{SW} by means of the transformer, with the lower part of the waveform clipped by D_{ZCD}. V_{LAUX} is fed back to the ZCD pin to detect a zero crossing point through a resistor divider network which consists of R_{AUX1} and R_{AUX2}. The next turn on time of Q_1 is selected V_{SW} is the minimum, an instant corresponding to a small delay after the zero crossing occurs. (Figure 15) The actual delay time depends on the drain capacitance of the Q_1 and the primary inductance of the transformer (L_P). Such delay time is set by a single external resistor as described in Delay Setting section.

During the off-period at steady state, V_{ZCD} reaches its maximum $V_{ZCD-PEAK}$ (Figure 14), which is scalable by the turn ratio of the transformer and the resistor divider network R_{AUX1} and R_{AUX2}. It is recommended that $V_{ZCD-PEAK}$ is set to 3V during normal operation.

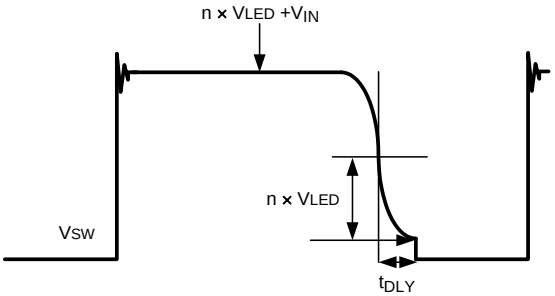


Figure 16. Switching Node Waveforms

Delay Time Setting

In order to reduce EMI and switching loss, the TPS92314/14A inserts a delay between the off-period and the on-period. The delay time is set by a single resistor which connects across the DLY pin and ground, and their relationship is shown in Figure 17. The optimal delay time depends on the resonance frequency between L_P and the drain to source capacitance of Q_1 (C_{DS}). Circuit designers should optimize the delay time according to the following equation.

$$f_{SW} = \frac{1}{2\pi\sqrt{L_P C_{DS}}} \quad (2)$$

$$t_{DLY} = \frac{\pi\sqrt{L_P C_{DS}}}{2} \quad (3)$$

After determining the delay time, t_{DLY} can be implemented by setting R_{DLY} according to the following equation:

$$R_{DLY} = K_{DLY}(t_{DLY} - 105ns) \quad (4)$$

where

- K_{DLY} = 32MΩ/ns is a constant

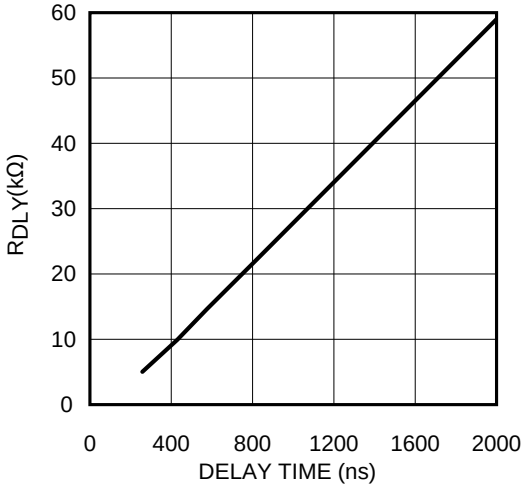


Figure 17. Delay Time Setting

Protection Features

OUTPUT OPEN CIRCUIT PROTECTION

The open circuit protection can be trigger through ZCD pin or VCC pin. If the LED string is disconnected from the output of the TPS92314/14A, The secondly output voltage (V_{LED}) and AUX wiring voltage $V_{ZCD-PEAK}$ will increases. IF $V_{ZCD-PEAK}$ is greater than $V_{ZCD-OVP}$ for 3 continues switching cycles or VCC voltage higher than V_{CCOVP} threshold, Over Voltage Protection (OVP) protection will be trigger. At the meantime, switching of Q_1 will stop and V_{CC} will decreases until it drops below the falling threshold of $V_{CC-UVLO}$, the controller will restarts automatically and enter into startup state (Figure 19).

VCC OVP PROTECTION

The TPS92314/14A has a built-in over voltage protection feature. It can be trigger through the VCC pin when over V_{CC-OVP} threshold. Once the V_{CC-OVP} triggered, the output gate signal will pull low and VCC will decrease until it drops below the $V_{CC-UVLO}$, the controller will restarts automatically.

OUTPUT SHORT CIRCUIT PROTECTION

If the LED string is shorted, the voltage of AUX wiring ($V_{ZCD-PEAK}$) will decrease, and as $V_{ZCD-PEAK}$ voltage decrease below $V_{ZCD-TRIG}$, the TPS92314/14A will enter low switching frequency operation. During low switching frequency operation, power supplied from L_{AUX} to V_{CC} is not enough to maintain V_{CC}. If the short remains V_{CC} will drop below the falling threshold of $V_{CC-UVLO}$, the TPS92314/14A will attempt to restart at this time (Figure 18). When the short is removed the TPS92314/14A will restore to steady state operation.

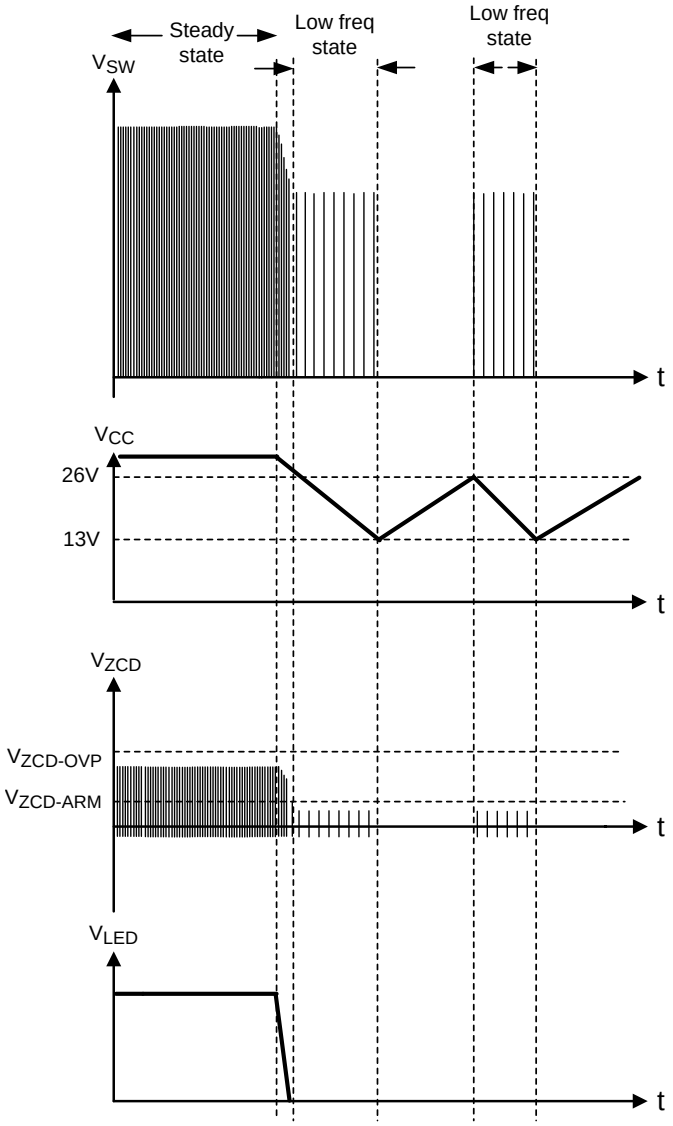


Figure 18. Output Short Circuit waveforms

OVER CURRENT PROTECTION

Over Current Protection (OCP) limits the drain current of MOSFET and prevents inductor / transformer saturation. When V_{ISNS} reaches a threshold, OCP function will be triggered, controller gate drive will pull low and OFF time will extends to 233μs, also C_{COMP} capacitor will be discharged by internal switch and gate drive ON time will force to minimum in next cycle.

THERMAL PROTECTION

Thermal protection is implemented by an internal thermal shutdown circuit, which activates at 165°C (typically). In this case, the switching power MOSFET will turn off. Capacitor C_{VCC} will discharge until UVLO. If the junction temperature of the TPS92314/14A falls back below 145°C, the TPS92314/14A resumes normal operation.

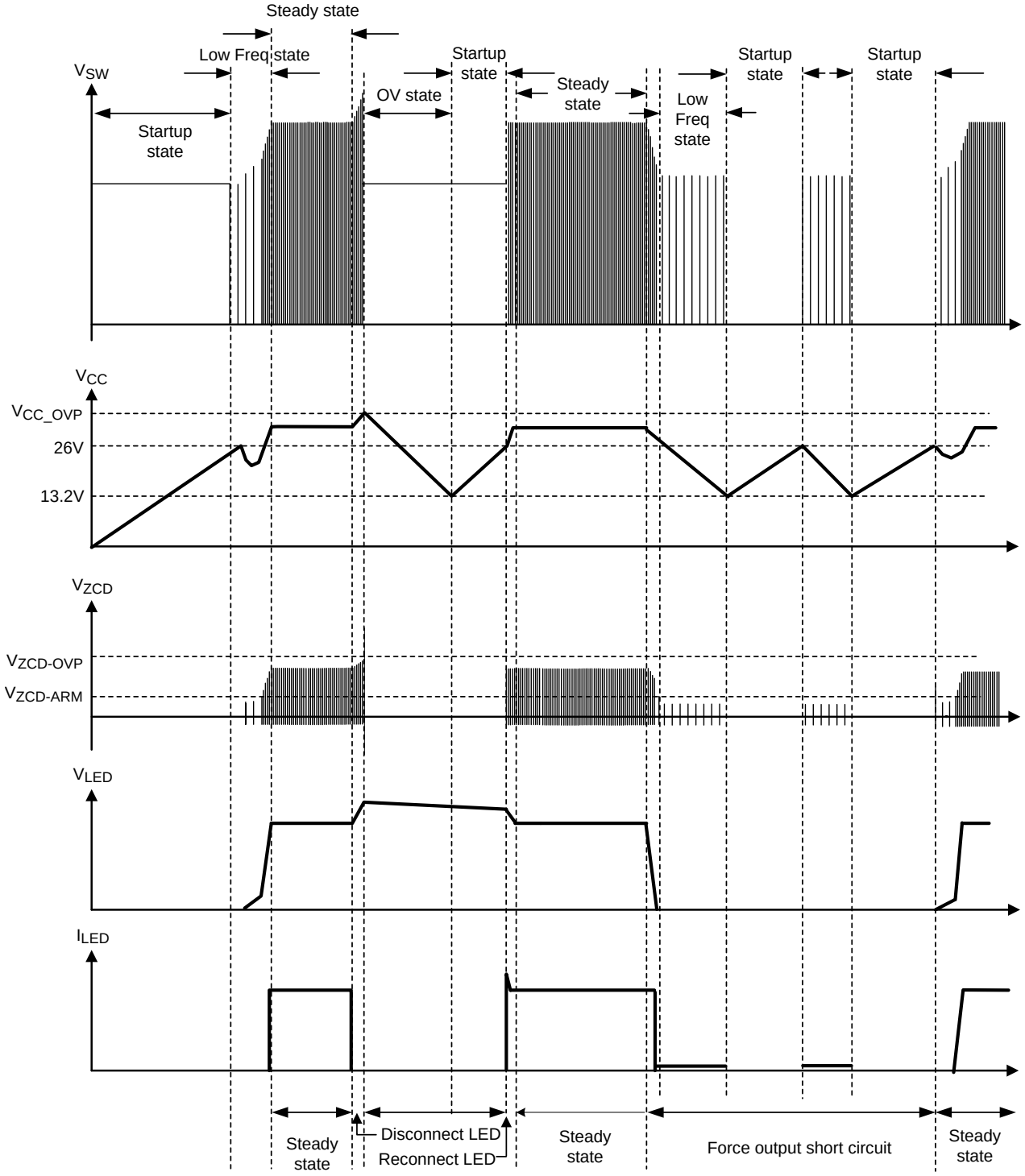


Figure 19. Auto Restart Operation

Design Example

The following design example illustrates the procedures to calculate the external component values for the TPS92314/14A isolated single stage fly-back LED driver with PFC.

- **Design Specifications:**
  - Input voltage range, V_{AC_RMS} = 85VAC – 132VAC
  - Nominal input voltage, $V_{AC\_RMS(NOM)}$ = 110VAC
  - Number of LED in serial =7
  - LED current, I_{LED} = 350mA
  - Forward voltage drop of single LED = 3.0V
  - Forward voltage of LED stack, V_{LED} = 21V
- **Key operating Parameters:**
  - Converter minimum switching frequency, f_{SW} = 75kHz
  - Output rectifier maximum reverse voltage, $V_{DOUT(MAX)}$ = 100V
  - Power MOSFET rating, $V_{Q1(MAX)}$ =800V
  - Power MOSFET Output Capacitance, C_{DS} = 37pF (estimated)
  - Nominal output power, P_{OUT} = 8W

START UP BIAS RESISTOR

During start up, the V_{CC} will be powered by the rectified line voltage through external resistor, R_1. The V_{CC} start up current, $I_{VCC(SU)}$ must set in the range $I_{VCC(MIN)} > I_{VCC(SU)} > I_{STARTUP(MAX)}$ to ensure proper restart operation during OVP fault at maximum voltage input. In this example, a value of 0.88mA is suggested. The resistance of R_1 can be calculated by dividing the nominal input voltage in RMS by the start up current suggested.

So, R_{AC} = 132V / 0.88mA = 150KΩ is recommended.

TRANSFORMER TURN RATIO

The transformer winding turn ratio, n is governed by the MOSFET Q1 maximum rated voltage, ($V_{Q1(MAX)}$), highest line input peak voltage ($V_{AC\text{-}PEAK}$) and output diode maximum reverse voltage rating ($V_{OUT(MAX)}$). The output diode rating limits the lower bound of the turn ratio and the power MOSFET rating provide the upper bound of the turn ratio. The transformer turn ratio must be selected in between the bounds. If the maximum reverse voltage of D_{OUT} ($V_{DOUT(MAX)}$) is 100V. the minimum transformer turn ratio can be calculated with the equation in below.

$$n > \frac{V_{AC\text{-}PEAK}}{\left(V_{DOUT(MAX)} - V_{LED}\right)}$$

$$n > \frac{132 \times \sqrt{2}}{100 - 30} = 2.33 \tag{5}$$

In operation, the voltage at the switching node, V_{SW} must be small than the MOSFET maximum rated voltage $V_{Q1(MAX)}$, For reason of safety, 10% safety margin is recommended. Hence, 90% of $V_{Q1(MAX)}$ is used in the following equation.

$$n < \frac{V_{Q1(MAX)} \times 0.9 - V_{AC\text{-}PEAK} - V_{os}}{V_{LED(MAX)}}$$

$$n < \frac{800 \times 0.9 - 132\sqrt{2} - 50}{30} = 18.8 \tag{6}$$

where

- V_{OS} is the maximum switching node overshoot voltage allowed, in this example, 50V is assumed. (7)

As a rule of thumb, lower turn ratio of transformer can provide a better line regulation and lower secondly side peak current. In here, turn ratio n = 3.8 is recommended.

SWITCHING FREQUENCY SELECTION

TPS92314/14A can operate at high switching frequency in the range of 60kHz to 150kHz. In most off-line applications, with considering of efficiency degradation and EMC requirements, the recommended switching frequency range will be 60kHz to 80kHz. In this design example, switching frequency at 75kHz is selected.

SWITCHING ON TIME

The maximum power switch on-time, t_{ON} depends on the low line condition of $85V_{AC}$. At $85V_{AC}$ the switching frequency was chosen at 75kHz. This transformer design will follow the formulae as shown below.

$$t_{ON}=\frac{1}{f_{sw}\left(\frac{V_{AC\_MIN\_PEAK}}{n x V_{LED}}+1\right)}$$

$$t_{ON}=\frac{1}{75000\left(\frac{85\sqrt{2}}{3.8 \text{ x } 21}+1\right)}=5.3\,\mu s \quad (8)$$

TRANSFORMER PRIMARY INDUCTANCE

The primary inductance, L_P of the transformer is related to the minimum operating switching frequency f_{SW}, converter output power P_{OUT}, system efficiency η and minimum input line voltage $V_{AC\_RMS(MIN)}$. For CRM operation, the output power, P_{OUT} can be described by the equation in below.

$$P_{OUT}=\eta x\frac{1}{2}L_P x I_{LP\text{-}PEAK}{}^2 x f_{SW} \quad (9)$$

By re-arranging terms, the transformer primary inductance required in this design example can be calculated with the equation follows:

$$L_P=\frac{\eta x V_{AC\_RMS(MIN)}{}^2 t_{ON}{}^2}{2 x P_{OUT} x \frac{1}{f_{sw}}} \quad (10)$$

The converter minimum switching frequency is 75kHz, t_{ON} is 5.3µs, $V_{AC\_RMS(MIN)}$ = 85V and P_{OUT} = 8W, assume the system efficiency, η = 85%. Then,

$$L_P=\frac{0.85 x (85)^2 x (5.3\,\mu)^2}{2x8x13.3\,\mu}=0.81 mH \quad (11)$$

From the calculation in above, the inductance of the primary winding required is 0.81mH.

After the primary inductance and transformer turn ratio is determined, the current sensing resistor, R_{ISNS} can be calculated.

The resistance for R_{ISNS} is governed by the output current and transformer turn ratio, the equation in below can be used.

$$R_{ISNS}= n \text{ x } \left(\frac{v_{REF}}{I_{LED}}\right)$$

where

- V_{REF} is fixed to 0.14V internally. (12)

Transformer turn ratio, N_P : N_S is 3.8 : 1 and I_{LED} = 0.35A

$$R_{ISNS}=3.8\times\frac{0.14}{0.35}=1.52\,\Omega \quad (13)$$

In Figure 20, resistor R_{FILTER} is used to reduce the high frequency noise into ISNS pin. the typical value is 300 x R_{ISNS} .

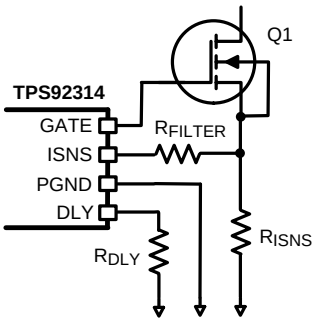


Figure 20. R_{ISNS} Resistor Interface

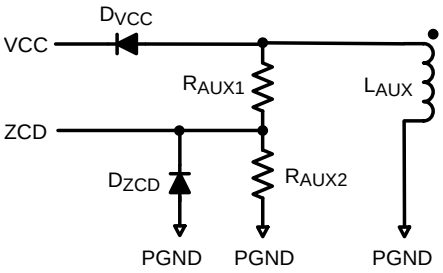


Figure 21. Auxiliary Winding Interface to ZCD

Auxiliary Winding Interface To ZCD

In Figure 21, R_{AUX1} and R_{AUX2} forms a resistor divider which sets the thresholds for over voltage protection of V_{LED}, $V_{ZCD-OVP}$, and $V_{ZCD-PEAK}$. Before the calculation, we need to set the voltage of the auxiliary winding, V_{LAUX} at open circuit.

- For example :
  - Assume the nominal forward voltage of LED stack (V_{LED}) is 21V.
  - To avoid false triggering ZCD_{OVP} voltage threshold at normal operation, select ZCD_{OVP} voltage at 1.3 times of the V_{LED} is typical in most applications. In case the transformer leakage is higher, the ZCD_{OVP} threshold can be set to 1.5 times of the V_{LED}.
  - In this design example, open circuit AUX winding OVP voltage threshold is set to 30V. Assume the current through the AUX winding is 0.4mA typical.
  - As a result, R_{AUX1} is 66kΩ and R_{AUX2} is 12kΩ.

Auxiliary Winding V_{cc} Diode Selection

The VCC diode D_{VCC} provides the supply current to the converter, low temperature coefficient , low reverse leakage and ultra fast diode is recommended.

Compensation Capacitor And Delay Timer Resistor Selection

To achieve PFC function with a constant on time flyback converter, a low frequency response loop is required. In most applications, a 4.7µF C_{COMP} capacitor is suitable for compensation.

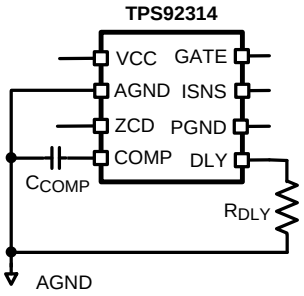


Figure 22. Compensation and DLY Timer connection

The resistor R_{DLY} connecting the DLY pin to ground is used to set the delay time between the ZCD trigger to power MOSFET turn on. The delay time required can be calculated with the parasitic capacitance at the drain of MOSFET to ground and primary inductance of the transformer. Equation 14 can be used to find the delay time and Figure 17 can help to find the resistance once the delay time is calculated

$$t_{DLY} = \frac{\pi\sqrt{L_P C_{DS}}}{2} \tag{14}$$

For example, using a transformer with primary inductance L_P = 1mH, and power MOSFET drain to ground capacitor C_{DS}=37pF, the t_{DLY} can be calculated by the upper equation. As a result, t_{DLY}=302ns and R_{DLY} is 6.31kΩ. The delay time may need to change according to the primary inductance of the transformer. The typical level of output current will shift if inappropriate delay time is chosen.

Output Flywheel Diode Selection

To increase the overall efficiency of the system, a low forward voltage schottky diode with appropriate rating should be used.

Primary Side Snubber Design

The leakage inductance can induce a high voltage spike when power MOSFET is turned off. Figure 23 illustrates the operation waveform. A voltage clamp circuit is required to protect the power MOSFET. The voltage of snubber clamp (V_{SN}) must be higher than the sum of over shoot voltage (V_{OS}), LED open load voltage multiplied by the transformer turn ratio (n). In this examples, the V_{OS} is 50V and LED maximum voltage, $V_{LED(MAX)}$ is 30V, transformer turn ratio is 3.8. The snubber voltage required can be calculated with following equations.

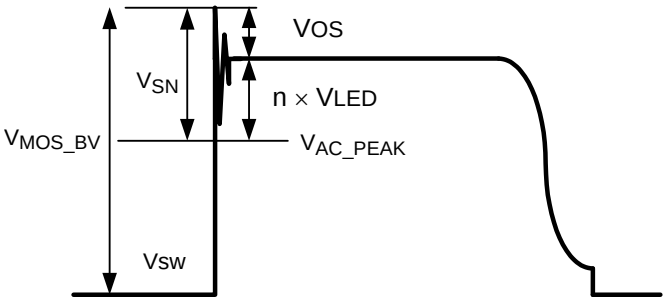


Figure 23. Snubber Waveform

$$V_{SN} > V_{OS} + V_{LED(MAX)} \times n \tag{15}$$

where n is the turn ratio of the transformer.

$$V_{SN} > 50V + 30V \times 3.8 = 164V \tag{16}$$

At the same time, sum of the snubber clamp voltage and V_{AC} peak voltage (V_{AC_PEAK}) must be smaller than the MOSFET breakdown voltage (V_{MOS_BV}). By re-arranging terms, equation in below can be used.

$$V_{SN} < V_{MOS\_BV} - V_{AC}\sqrt{2}$$
$$V_{SN} < 800 - 132 \times \sqrt{2} = 614V \quad (17)$$

In here, snubber clamp voltage, V_{SN} = 250V is recommended.

Output Capacitor

The capacitance of the output capacitor is determined by the equivalent series resistance (ESR) of the LED, R_{LED} and the ripple current allowed for the application. The equation in below can be used to calculate the required capacitance.

$$C_{OUT} = \frac{\sqrt{\left(2\frac{I_{LED}}{\Delta I_{LED}}\right)^2 - 1}}{4 \times \pi \times f_{AC} R_{LED}} \quad (18)$$

Assume the ESR of the LED stack contains 7 LEDs and is 2.6Ω, AC line frequency f_{AC} is 60Hz.

In this example, LED current I_{LED} is 350mA and output ripple current is 30% of I_{LED}:

$$C_{OUT} = \frac{\sqrt{\left(\frac{2x0.35}{0.3x0.35}\right)^2 - 1}}{4x\pi x60x7x2.6} \quad (19)$$

Then, C_{OUT} = 480µF.

In here, a 470µF output capacitor with 10µF ceramic capacitor in parallel is suggested.

PCB Layout Considerations

The performance of any switching power supplies depend as much upon the layout of the PCB as the component selection. Good layout practices are important when constructing the PCB. The layout must be as neat and compact as possible, and all external components must be as close as possible to their associated pins. High current return paths and signal return paths must be separated and connect together at single ground point. All high current connections must be as short and direct as possible with thick traces. The drain voltage of the MOSFET should be connected close to the transformer pin with short and thick trace to reduce potential electromagnetic interference. For off-line applications, one more consideration is the safety requirements. The clearance and creepage to high voltage traces must be complied to all applicable safety regulations.

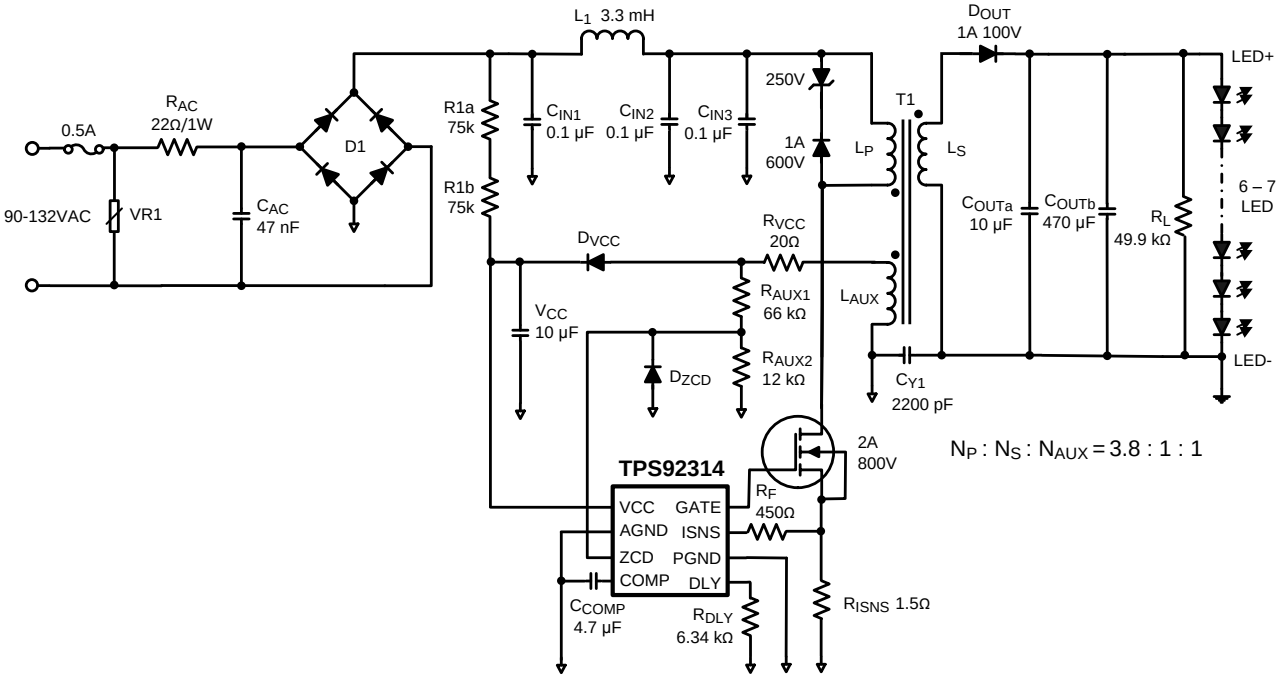


Figure 24. Isolated Topology Schematic

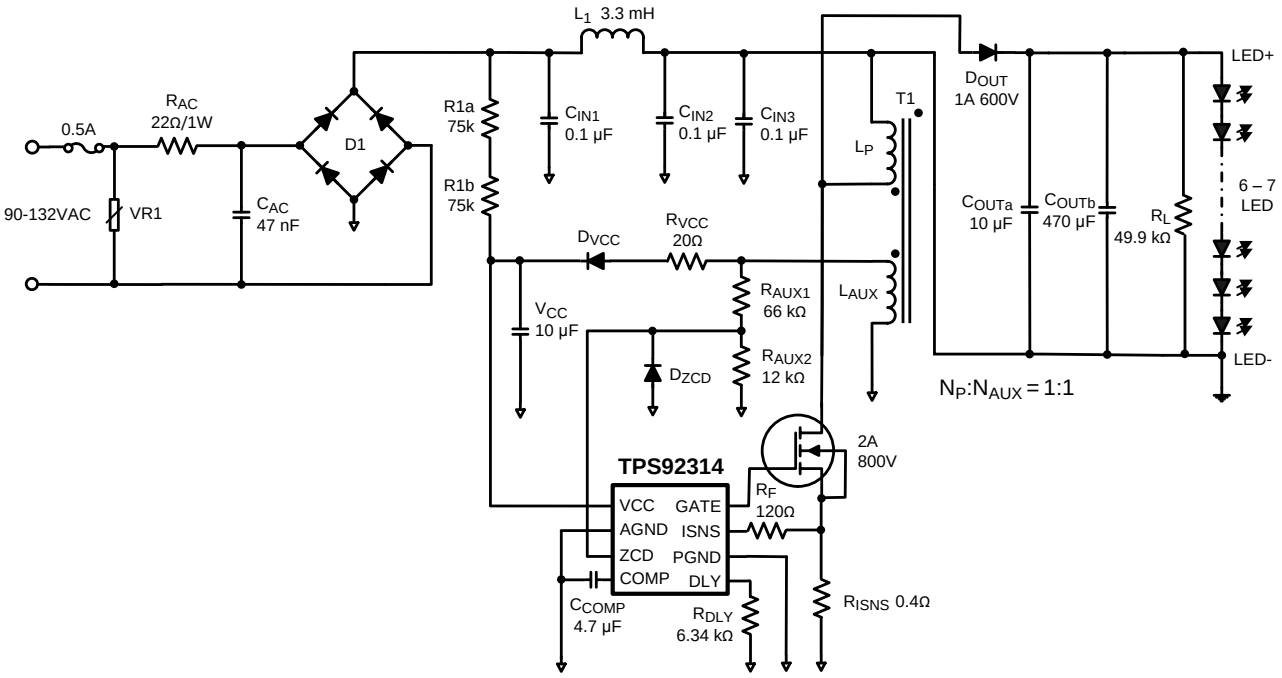


Figure 25. Non-isolated Topology Schematic

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92314AD/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T92314 A	Samples
TPS92314ADR/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T92314 A	Samples
TPS92314D/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T92314	Samples
TPS92314DR/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T92314	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

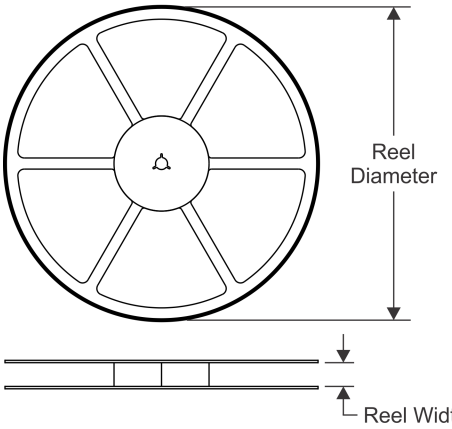
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

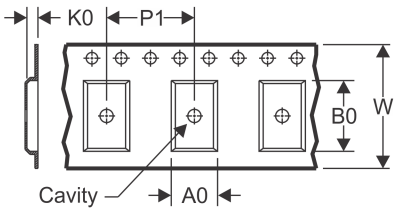
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

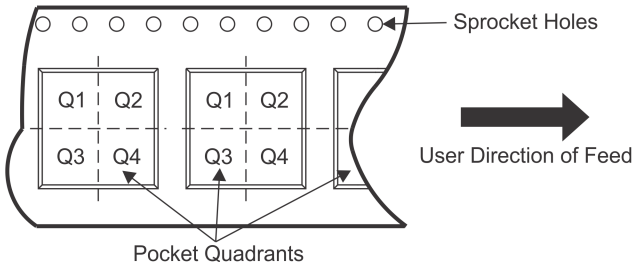


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

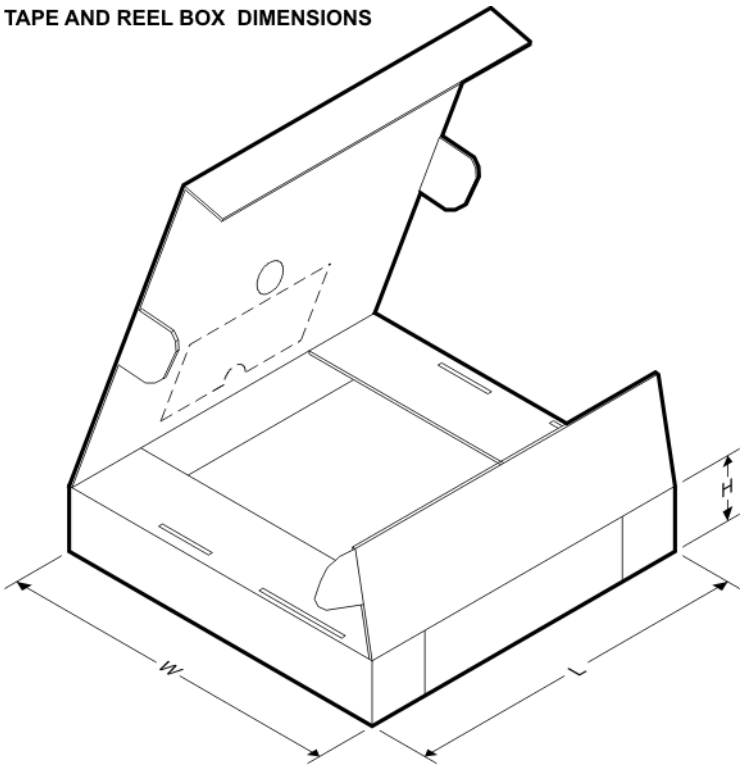
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92314ADR/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
TPS92314DR/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

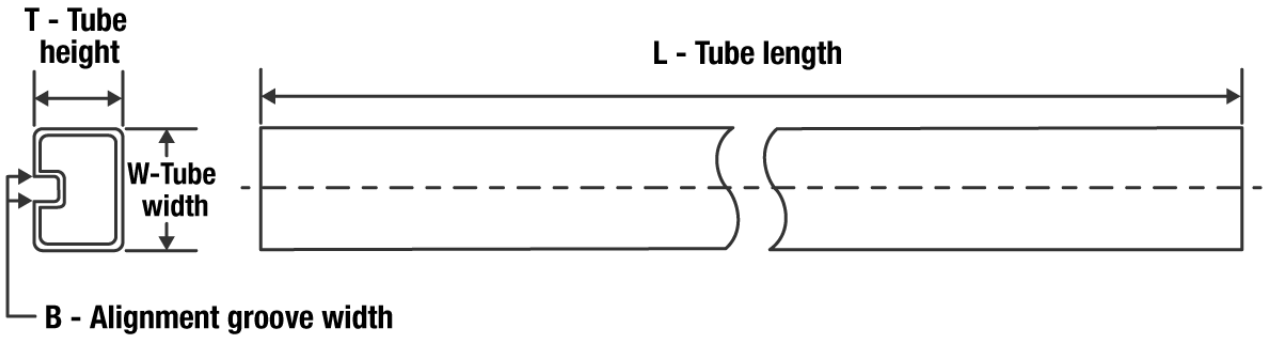
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

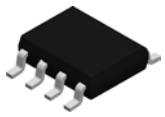
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92314ADR/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
TPS92314DR/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS92314AD/NOPB	D	SOIC	8	95	495	8	4064	3.05
TPS92314D/NOPB	D	SOIC	8	95	495	8	4064	3.05

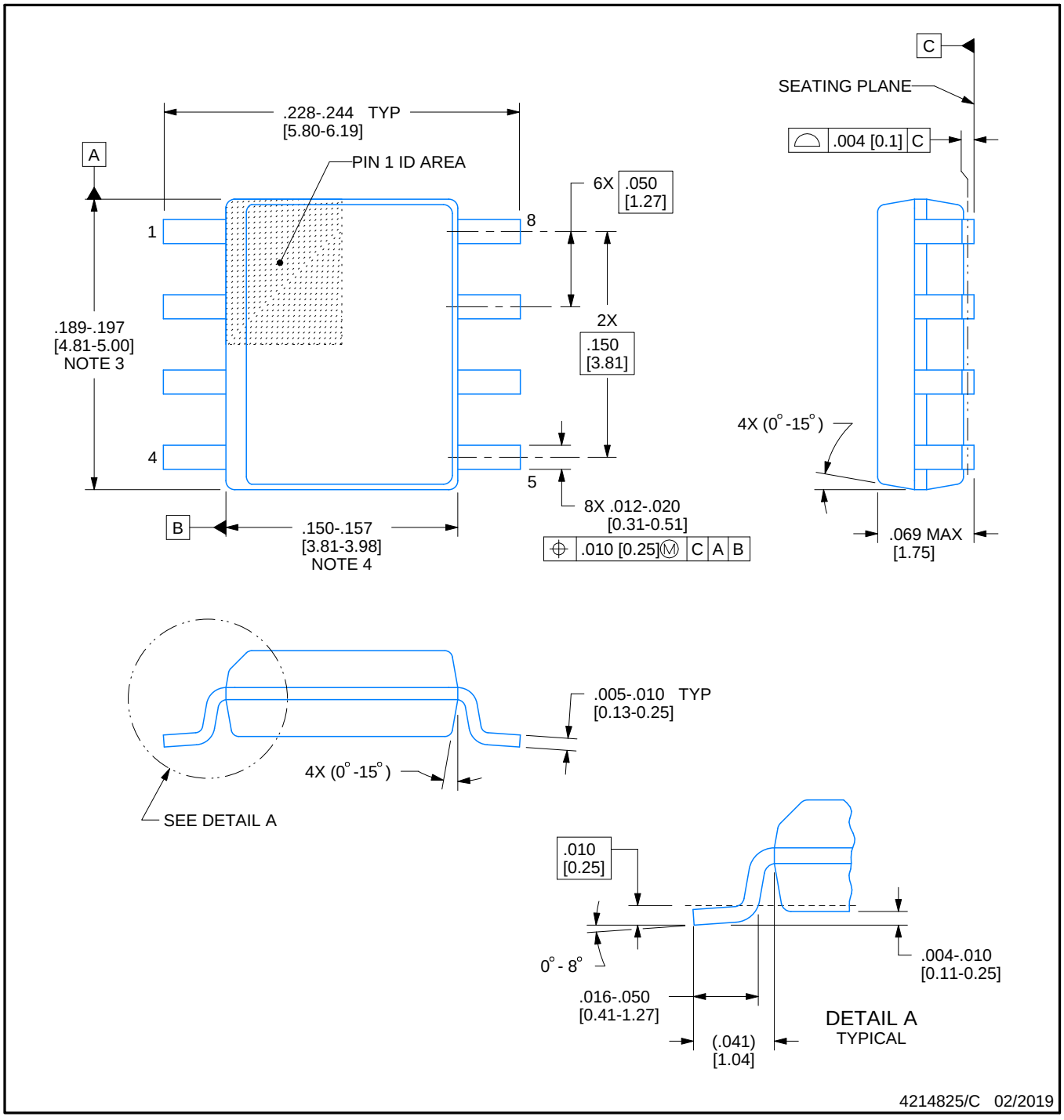


PACKAGE OUTLINE

D0008A

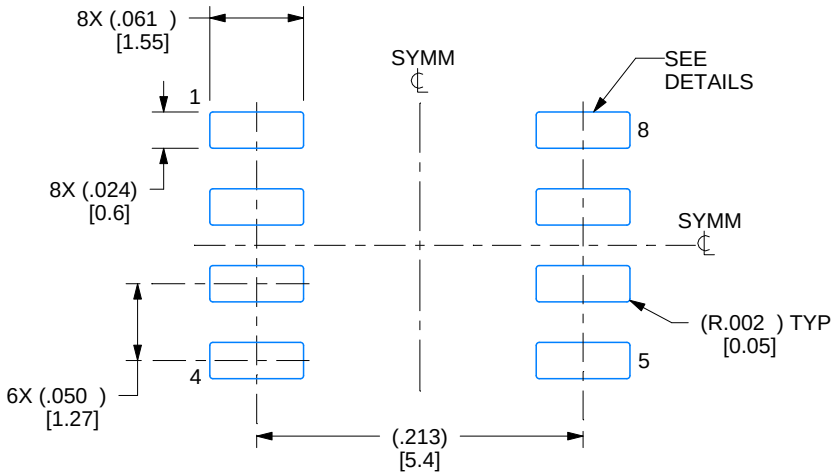
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

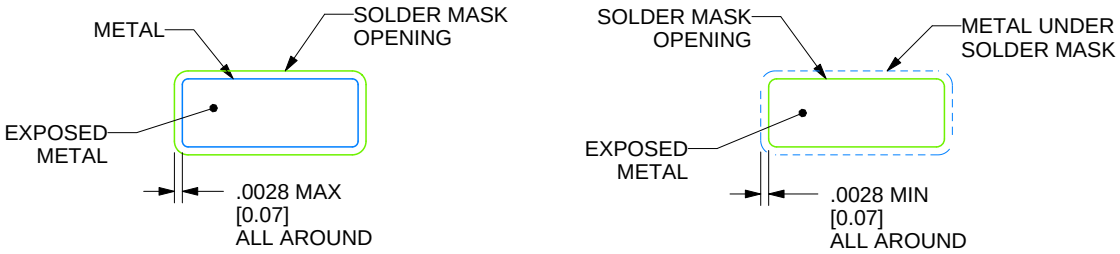


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

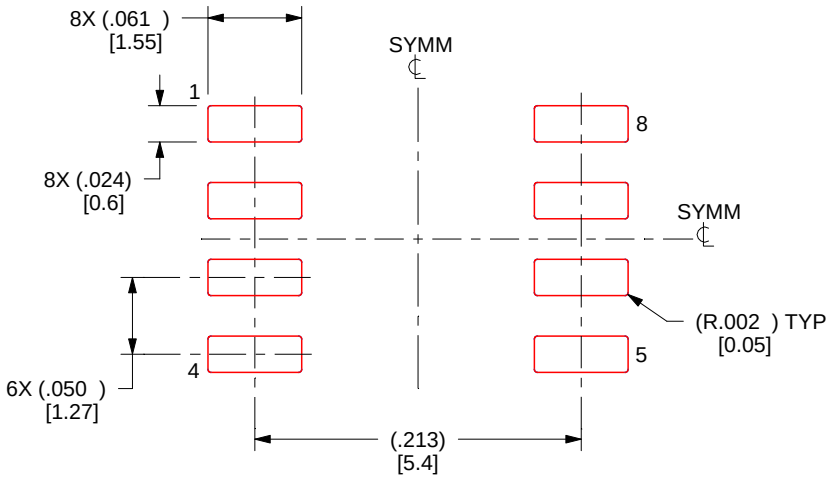
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for LED Lighting Drivers ***category:***

Click to view products by Texas Instruments ***manufacturer:***

Other Similar products are found below :

LV5235V-MPB-H AP5726WUG-7 IS31BL3228B-UTLS2-TR IS31BL3506B-TTLS2-TR AP5725FDCG-7 AP5726FDCG-7 SLG7NT4082V SLG7NT4082VTR AP5725WUG-7 BD1604MVV-E2 MAX16840ATB+ CAT4004BHU2-GT3 TLE4242EJ IS31LT3172-GRLS4-TR IS32LT3174-GRLA3-TR ZXLD1374QESTTC NCV78825DQ0R2G MP4425AGQB-P MP3367GR-P MPQ3369GR-P MPQ7220GF-AEC1-P MP3362GJ-Z DIO5662ST6 IS31BL3508A-TTLS2-TR DIO5661TST6 NJW4617DL3-TE1 BD2802GU-E2 BD6583MUV-E2 NCV7693DB0R2G LV52207NXA-VH NCL30076AADR2G NCL30486B2DR2G NCL30488B4DR2G NCV78763MW4AR2G BD18353EFV-ME2 A6217KLJTR-T LT3761EMSE#TRPBF TLD2132-1EP TLD2331-3EP MPM6010GQV-AEC1-Z MPQ4425MGQB-AEC1-Z MPQ3326GR-AEC1-Z MPQ7230GLE-AEC1-Z MP2341GTL-Z BCR602 IS31FL3236-TQLS2-TR TLD700216ESXUMA1 LM3405AXMYX/NOPB LM36273YFFR MP46885DN-LF-Z