Off-Line Primary-Side Sensing Controller

Check for Samples: TPS92315

FEATURES

- **Primary-Side Regulation (PSR) eliminates opto-coupler**
- **±5% LED current regulation**
- **130 kHz maximum switching frequency enables high power density SSL drivers designs**
- **Quasi-resonant valley switching operation for highest overall efficiency**
- **Patent-pending frequency jitter scheme to ease EMI compliance**
- **Wide VCC range (35V) allows small bias capacitor**
- **Drive output for MOSFET**
- **Protection functions: over-voltage, low-line, and over-current**
- **SOT23-6 package**

APPLICATIONS

- **LED lighting driver applications**
- **Small form factor LED light bulbs (E14, GU-10)**

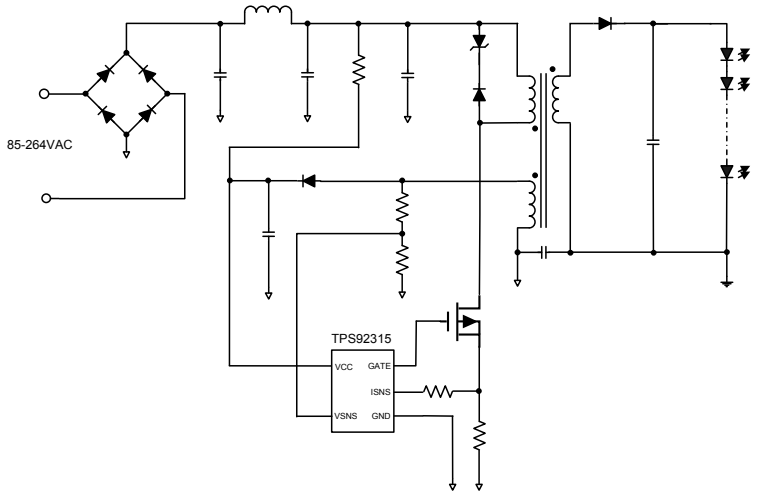
DESCRIPTION

The TPS92315 flyback power supply controller provides isolated output current regulation without the use of an optical coupler. The devices process operating information from the primary power switch and an auxiliary flyback winding to provide precise output current control. Low start-up current, dynamically controlled operating states and a tailored modulation profile support very low stand-by power without sacrificing start-up time or output transient response.

Control algorithms in the TPS92315 allow operating efficiencies to meet or exceed applicable standards. The drive output interfaces to a FET power switch. Discontinuous Conduction Mode (DCM) with valley switching is used to reduce switching losses. A combination of switching frequency and peak primary current amplitude modulation is used to keep conversion efficiency high across the full load and input voltage range.

The controller has a maximum switching frequency of 130 kHz and always maintains control of the peak primary current in the transformer. Protection features help keep secondary and primary component stress levels in check across the operation range.

SIMPLIFIED APPLICATION DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1) (2) (3)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VCC		38	V
Continuous gate current sink	I_{GATE}		50	mA
Continuous gate current source	I_{GATE}		Self-limiting	
Peak VSNS pin current	I_{VSNS}		-1.2	
Gate-drive voltage at GATE	I_{GATE}	-0.5	Self-limiting	V
Voltage range	VSNS	–0.75	7	
	ISNS	–0.5	5	
Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2000	V
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	
Junction temperature range, T_J		-55	150	°C
Storage temperature range, T_{stg}		-65	150	
Lead temperature 0.6 mm from case for 10 seconds			260	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VCC	Bias supply operating voltage	9		35	V
C_{VCC}	VCC bypass capacitor	0.047		1	µF
R_{LC}	ISNS pin line compensation programming resistor	0			kΩ
I_{VSNS}	VSNS pin current	-1			mA
T_J	Operating junction temperature	−20		125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TPS92315 DBV 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	180.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	71.2	
θ_{JB}	Junction-to-board thermal resistance(4)	44.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	5.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	43.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, VCC = 25V, -20°C ≤ T_A ≤ 125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Bias Supply Input						
I_{RUN}	Supply current, run	I_{GATE} = 0, run state		2.1	3.0	mA
I_{START}	Supply current, start	V_{VCC} = 18V, I_{GATE} = 0, start state		1.0	3.0	µA
I_{FAULT}	Supply current, fault	I_{GATE} = 0, fault state		2.1	2.8	mA
Under-Voltage Lockout						
V_{VCCON}	VCC turn-on threshold	V_{VCC} low to high	18	21	24	V
V_{VCCOFF}	VCC turn-off threshold	V_{VCC} high to low	7.70	8.10	8.45	
VSNS Input						
V_{VSNSR}	Regulating level	Measured at no-load condition, T_J = 25°C	4.0	4.05	4.1	V
V_{VSNSNC}	Negative clamp level	I_{VSNS} = -300 µA, volts below ground	190	250	325	mV
I_{VSNSB}	Input bias current	V_{VSNS} = 4V	-0.5	0	0.5	µA
ISNS Input						
$V_{ISNSTMAX}$	Max ISNS threshold voltage	V_{VSNS} = 3.7V(1)	715	750	775	mV
$V_{ISNSTMIN}$	Min ISNS threshold voltage	V_{VSNS} = 4.35V(1)	230	250	270	
K_{AM}	AM control ratio	$V_{ISNSTMAX}$ / $V_{ISNSTMIN}$	2.75	3.0	3.15	V/V
V_{CCR}	constant-current regulating level	CC regulation constant	310	319	329	mV
K_{LC}	Line compensating current ratio	I_{VSNSLS} = -300 µA, I_{VSNSLS} / current out of ISNS pin	23	25	28	A/A
$T_{ISNSLEB}$	Leading-edge blanking time	GATE output duration, V_{ISNS} = 1 V	195	235	275	ns
GATE						
I_{GATE}	GATE source current	V_{GATE} = 8V, V_{VCC} = 9V	20	25		mA
R_{GATELS}	GATE low-side drive resistance	I_{GATE} = 10 mA		6	12	Ω
V_{GATECL}	GATE clamp voltage	V_{VCC} = 35V		14	16	V
R_{GATESS}	GATE pull-down in start state		150	200	230	kΩ
Timing						
$F_{SW(max)}$	Maximum switching frequency	V_{VSNS} = 3.7V(1)	120	130	140	kHz
$F_{SW(min)}$	Minimum switching frequency	V_{VSNS} = 4.35V(1)	875	1000	1100	Hz
T_{ZTO}	Zero-crossing timeout delay		1.80	2.10	2.45	µs

(1) These devices automatically vary the control frequency and current sense thresholds to improve EMI performance, these threshold voltages and frequency limits represent average levels.

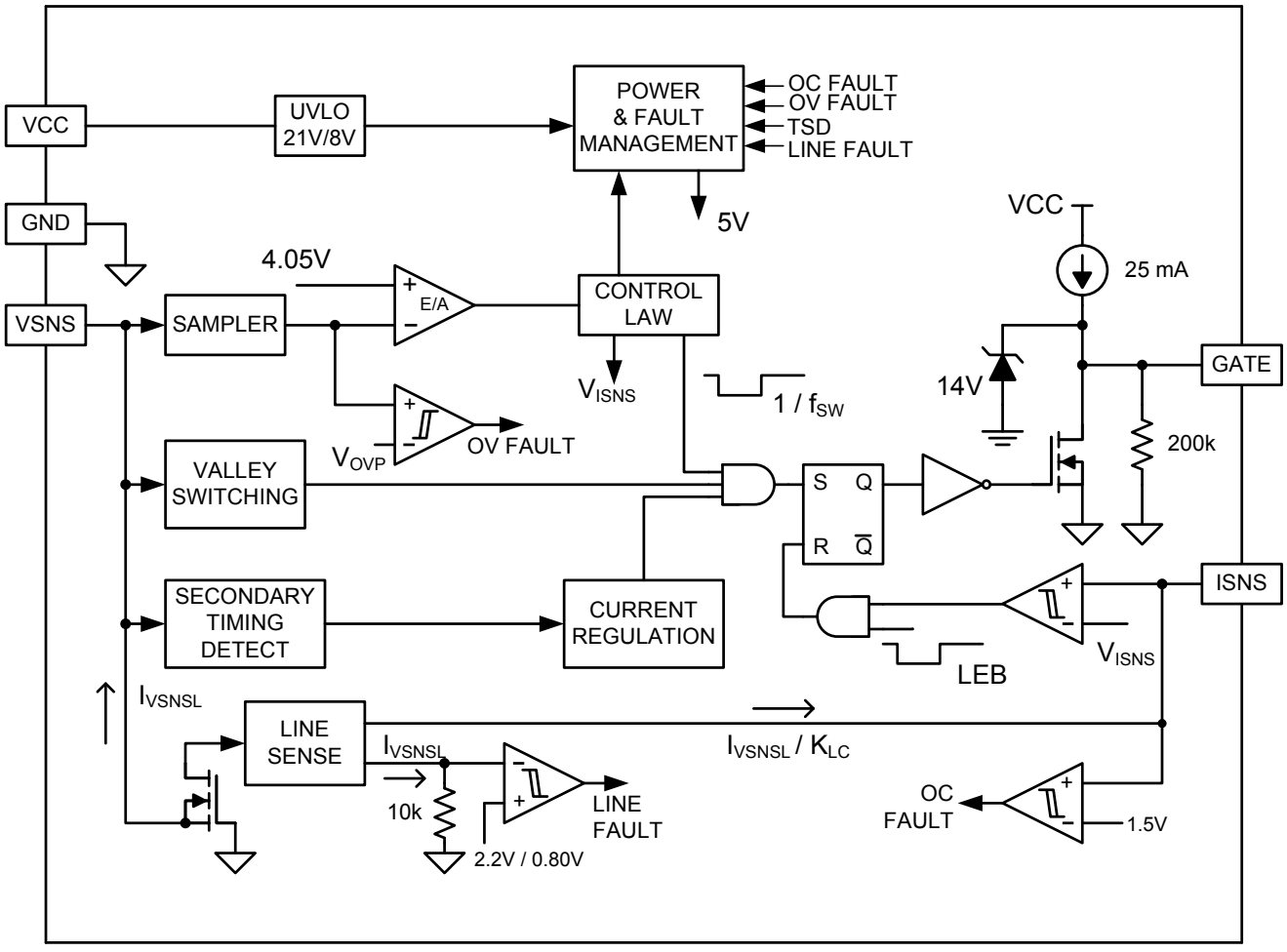
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, VCC = 25V, -20°C ≤ T_A ≤ 125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Protection						
V_{OVP}	Over-voltage threshold	At VSNS input, T_J = 25°C	4.52	4.6	4.68	V
V_{OCP}	Over-current threshold	At ISNS input	1.4	1.5	1.6	
$I_{VSNSL(run)}$	VSNS line-sense run current	Current out of VSNS pin – increasing	190	220	260	µA
$I_{VSNSL(stop)}$	VSNS line-sense stop current	Current out of VSNS pin – decreasing	70	80	95	
K_{VSNSL}	VSNS line-sense ratio	$I_{VSNSL(run)}$ / $I_{VSNSL(stop)}$	2.5	2.8	3.05	A/A
$T_{J(stop)}$	Thermal shut-down temperature	Internal junction temperature		165		°C

DEVICE INFORMATION

Functional Block Diagram



DBV PACKAGE
6 PIN
(TOP VIEW)

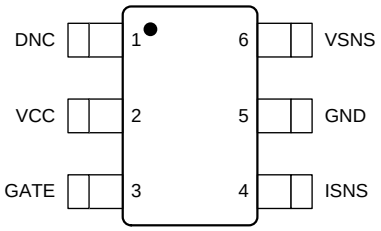


Table 1. TERMINAL FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
DNC	1	—	**DNC**, the **D**o **N**ot **C**onnect pin is only for device testing. For all end applications, this pin should left un-connected.
VCC	2	P	**VCC** is the supply pin to the controller. A carefully placed bypass capacitor to GND is required on this pin. The turn on threshold is 21V and turn off threshold is 8V.
GATE	3	O	**GATE** is an output used to drive the gate of an external high voltage MOSFET switching transistor. The driver output is limited to 14V with a 25 mA current source turn on and 6Ω turn off internal resistance.
ISNS	4	I	**ISNS**, current sense input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage is used to monitor and control the peak primary current. A series resistor can be added to this pin to compensate the peak switch current levels as the AC-mains input varies. The current sense voltage range is 0.25V to 0.75V for the peak primary current range.
GND	5	P	The **GND** pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal return paths.
VSNS	6	I	**VSNS**, voltage sense is an input used to provide voltage and timing feedback to the controller. This pin is connected to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider is used to program low line shutdown thresholds and compensate the current sense threshold at the ISNS pin across the AC input range.

Detailed Pin Description

VCC (Device Bias Voltage Supply): The VCC pin is connected to a bypass capacitor to ground and a start-up resistance to the input bulk capacitor (+) terminal. The VCC turn-on UVLO threshold is 21 V and turn-off UVLO threshold is 8.1 V, with an available operating range up to 35 V.

GND (Ground): This is a single ground reference external to the device for the gate drive current and analog signal reference. Place the VCC bypass capacitor close to GND and VCC with short traces to minimize noise on the VSNS and ISNS signal pins.

VSNS (Voltage-Sense): The VSNS pin is connected to a resistor divider from the auxiliary winding to ground. The output-voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. Timing information to achieve valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VSNS pin. Avoid placing a filter capacitor on this input which would interfere with accurate sensing of this waveform.

The VSNS pin also senses the bulk capacitor voltage to provide for AC-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. This information is sensed during the MOSFET on-time. For the AC-input run/stop function, the run threshold on VSNS is 220 µA and the stop threshold is 80 µA. The values for the auxilliary voltage divider upper-resistor R_{AUX1} and lower-resistor R_{AUX2} can be determined by the equations below.

$$R_{AUX1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSNS(run)}} \quad (1)$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- $V_{IN(run)}$ is the AC RMS voltage to enable turn-on of the controller (run),
- $I_{VSNSL(run)}$ is the run-threshold for the current pulled out of the VSNS pin during the MOSFET on-time. (see ELECTRICAL CHARACTERISTICS)

$$R_{AUX2} = \frac{R_{AUX1} \times V_{VSNSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSNSR}} \quad (2)$$

where

- V_{OCV} is the converter regulated output voltage
- V_F is the output rectifier forward drop at near-zero current
- N_{AS} is the transformer auxiliary to secondary turns ratio
- R_{AUX1} is the VSNS divider high-side resistance
- V_{VSNSR} is the CV regulating level at the VSNS input (see ELECTRICAL CHARACTERISTICS)

GATE (Gate Drive): The GATE pin is connected to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14V. The turn-on characteristic of the driver is a 25 mA current source which limits the turn-on dv/dt of the MOSFET drain and reduces the leading-edge current spike, but still provides gate-drive current to overcome the Miller plateau. The gate-drive turn-off current is determined by the low-side driver $R_{DS(on)}$ and any external gate-drive resistance. The user can reduce the turn-off MOSFET drain dv/dt by adding external gate resistance.

ISNS (Current Sense): The current-sense pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{ISNS}). The series resistor R_{LC} provides the function of feed-forward line compensation to eliminate change in I_{PP} (primary side peak current) due to change in di/dt and the propagation delay of the internal comparator and MOSFET turn-off time. There is an internal leading-edge blanking time of 235 ns to eliminate sensitivity to the MOSFET turn-on current spike. It should not be necessary to place a bypass capacitor on the ISNS pin. The value of R_{ISNS} is determined by the target output current in constant-current (CC) regulation. The values of R_{ISNS} and R_{LC} can be determined by the equations below. The term η_{XFMR} is intended to account for the energy stored in the transformer but not delivered to the secondary. This includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

Example: With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias power to output power ratio of 1.5%. The η_{XFMR} value is approximately: 1 - 0.05 - 0.035 - 0.015 = 0.9.

$$R_{ISNS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \eta_{XFMR}$$

where

- V_{CCR} is a current regulation constant (see ELECTRICAL CHARACTERISTICS),
- N_{PS} is the transformer primary-to-secondary turns ratio (a ratio of 7 to 8 is recommended for a 9V output),
- I_{OCC} is the target output current in constant-current regulation,
- η_{XFMR} is the transformer efficiency. (3)

$$R_{LC} = \frac{K_{LC} \times R_{AUX1} \times R_{ISNS} \times T_D \times N_{PA}}{L_P}$$

where

- R_{AUX1} is the VSNS pin high-side resistor value,
- R_{ISNS} is the current-sense resistor value,
- T_D is the current-sense delay including MOSFET turn-off delay, add ~50 ns to MOSFET delay,
- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant (see ELECTRICAL CHARACTERISTICS). (4)

TYPICAL CHARACTERISTICS

At VCC = 25 V, unless otherwise noted.

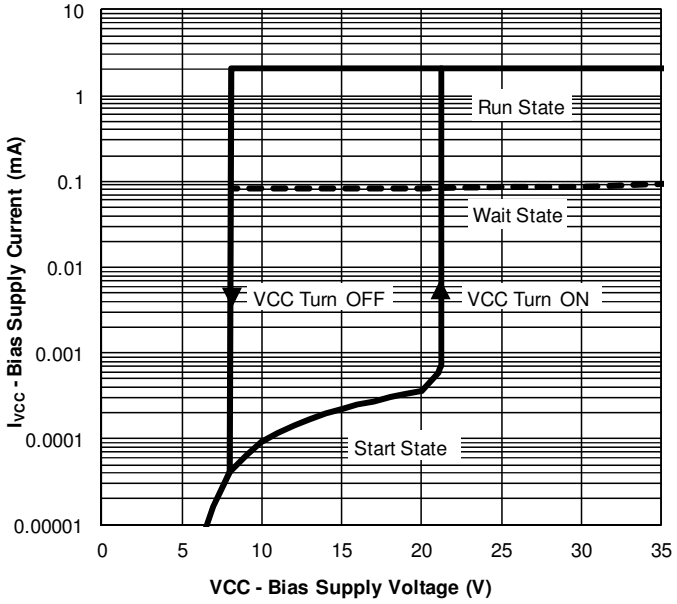


Figure 1. Bias Supply Current vs. Bias Supply Voltage

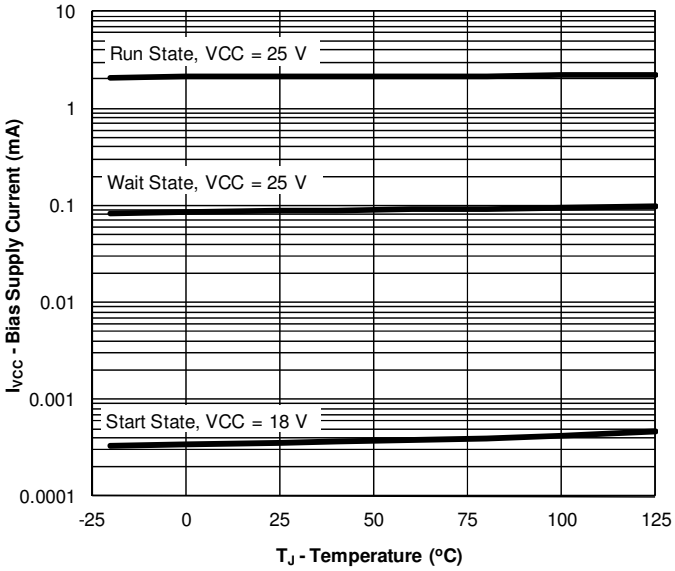


Figure 2. Bias Supply Current vs. Temperature

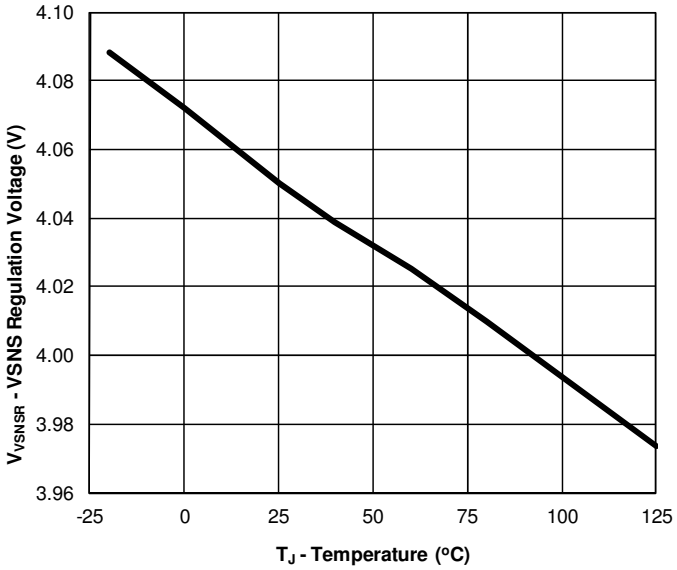


Figure 3. VSNS Regulation Voltage vs. Temperature

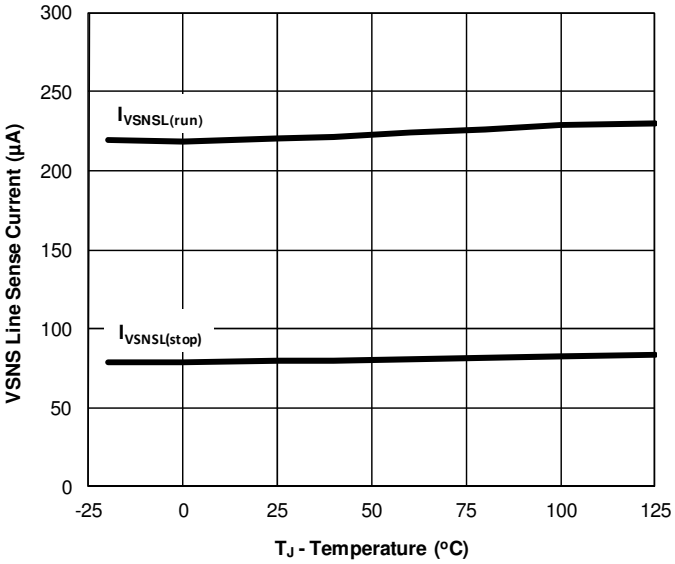


Figure 4. Line-Sense Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

At VCC = 25 V, unless otherwise noted.

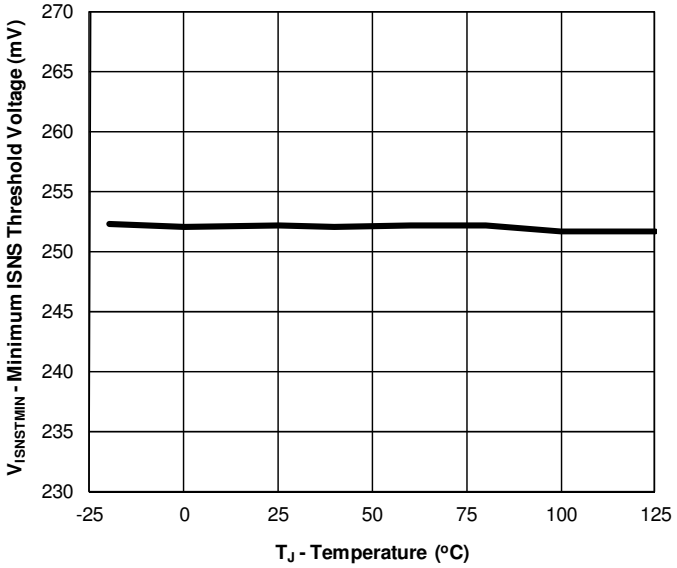


Figure 5. Minimum ISNS Threshold Voltage vs. Temperature

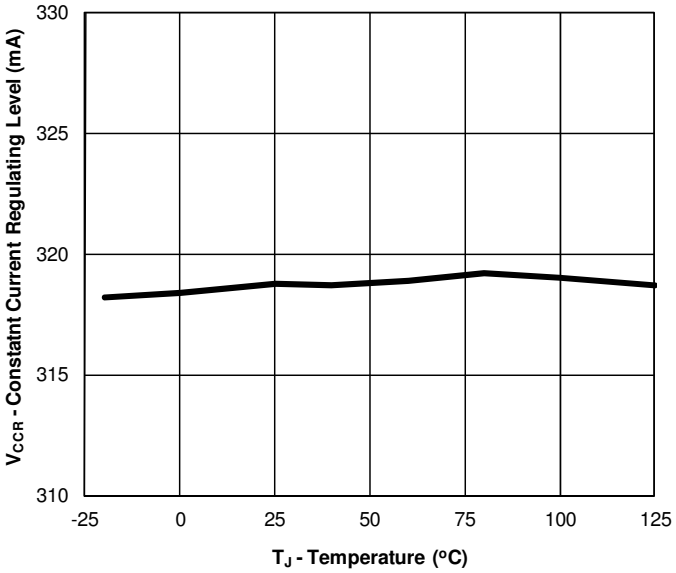


Figure 6. Constant-Current Regulating Level vs. Temperature

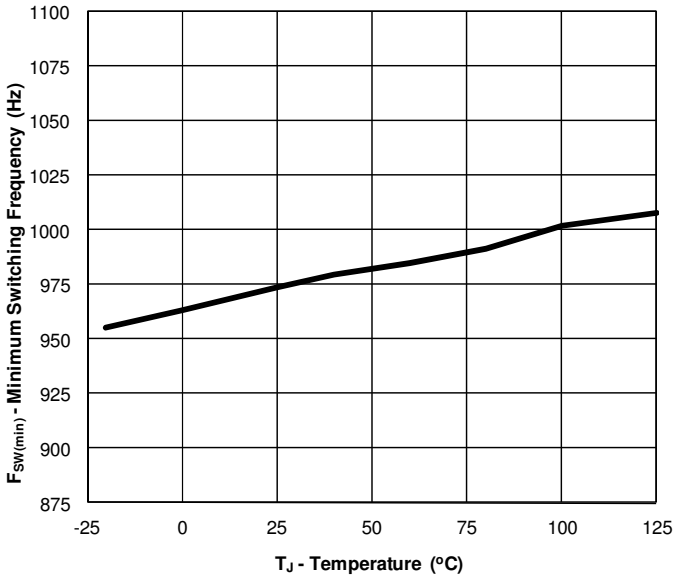


Figure 7. Minimum Switching Frequency vs. Temperature

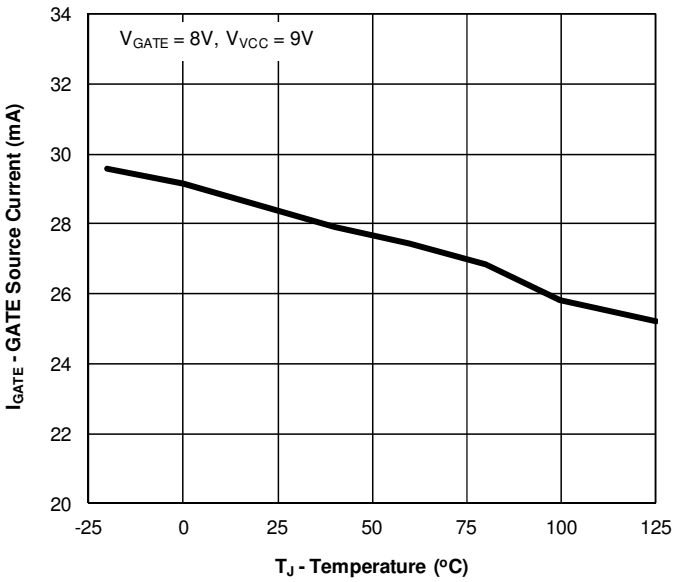


Figure 8. GATE Source Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

At VCC = 25 V, unless otherwise noted.

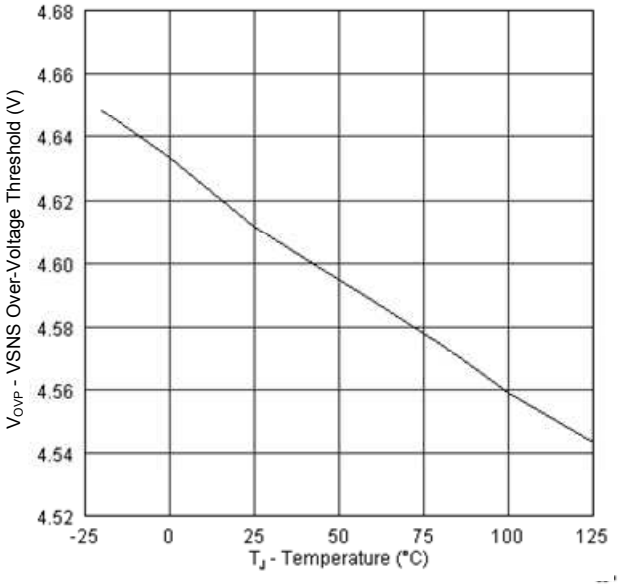


Figure 9. Over-Voltage Threshold vs. Temperature

FUNCTIONAL DESCRIPTION

The TPS92315 is a flyback power supply controller which provides accurate voltage and constant current regulation with primary-side feedback, eliminating the need for opto-coupler feedback circuits. The controller operates in discontinuous conduction mode with valley-switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversion efficiency across the load range.

Another feature beneficial to achieve low quescient power without excessive start-up time is a wide operating VCC range to allow a high-value VCC start-up resistance and low-value VCC capacitance. During low-power operating ranges the device has power management features to reduce the device operating current at operating frequencies below 44 kHz. The TPS92315 controller includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. Accurate voltage and constant current regulation, fast dynamic response, and fault protection are achieved with primary-side control. A complete LED driver solution can be realized with a straightforward design process, low cost and low component count.

Primary-Side Voltage Regulation

Figure 10 illustrates a simplified flyback convertor with the main voltage regulation blocks of the device shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary-side control.

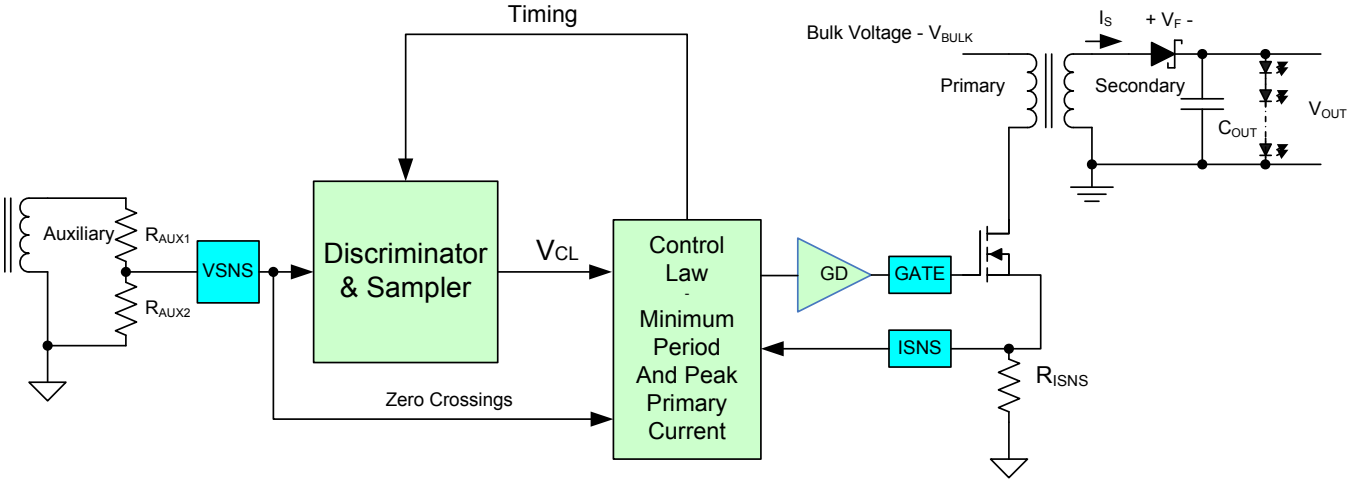


Figure 10. Simplified Flyback Convertor (with the main voltage regulation blocks)

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. As shown in Figure 11 it is clear there is a down slope representing a decreasing total rectifier V_F and resistance voltage drop ($I_S R_S$, where I_S and R_S are the current and equivalent resistance of the secondary winding) as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VSNS is 4.05 V; the resistor divider is selected as outlined in the VSNS pin description.

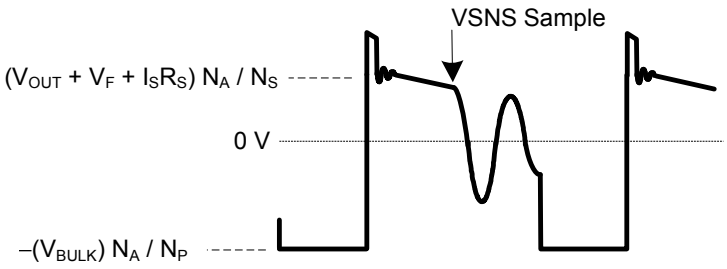


Figure 11. Auxiliary Winding Voltage

The TPS92315 VSNS signal sampler includes signal discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are however some details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to Figure 12 below for a detailed illustration of waveform criteria to ensure a reliable sample on the VSNS pin. The first detail to examine is the duration of the leakage inductance reset pedestal, T_{LK_RESET} in Figure 12. Since this can mimic the waveform of the secondary current decay, followed by a sharp downslope, it is important to keep the leakage reset time less than 500 ns for I_{PRI} minimum, and less than 1.5 µs for I_{PRI} maximum. The second detail is the amplitude of ringing on the V_{AUX} waveform following T_{LK_RESET}. The peak-to-peak voltage at the VSNS pin should be less than approximately 100 mV_{p-p} at least 200 ns before the end of the demagnetization time, t_{DM}. If there is a concern with excessive ringing, it usually occurs during light or no-load conditions, when t_{DM} is at the minimum. The tolerable ripple on VSNS is scaled up to the auxiliary winding voltage by R_{AUX1} and R_{AUX2}, and is equal to 100 mV x (R_{AUX1} + R_{AUX2}) / R_{AUX2}.

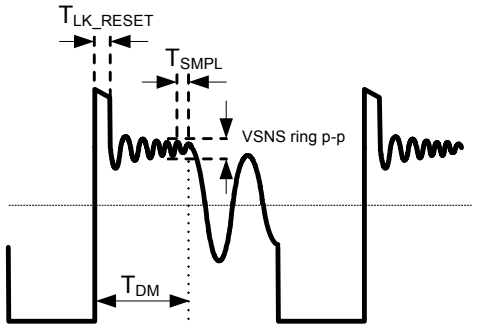


Figure 12. Auxiliary Waveform Details

During voltage regulation, the controller operates in frequency modulation mode and amplitude modulation mode as illustrated in Figure 13 below. The internal operating frequency limits of the device are 130 kHz maximum and 1 kHz minimum. The transformer primary inductance and primary peak current chosen sets the maximum operating frequency of the converter. The output preload resistor and efficiency at low power determines the converter minimum operating frequency. There is no stability compensation required for the TPS92315 controller.

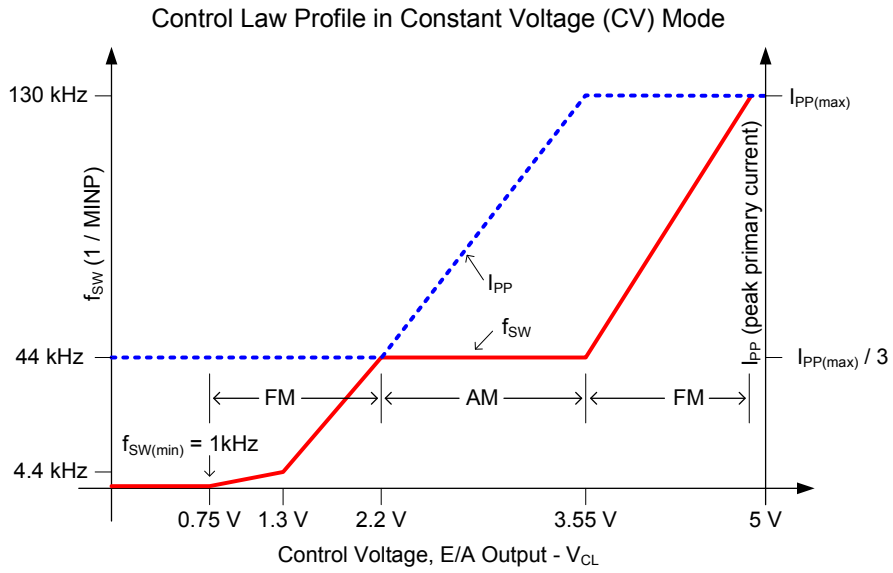


Figure 13. Frequency and Amplitude Modulation Modes (during voltage regulation)

Primary-Side Current Regulation

Timing information at the VSNS pin and current information at the ISNS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current is at $I_{PP(max)}$. Referring to Figure 14 below, the primary-peak current, turns ratio, secondary demagnetization time (t_{DM}), and switching period (T_{SW}) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by Equation 5. When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VCC above the UVLO turn-off threshold.

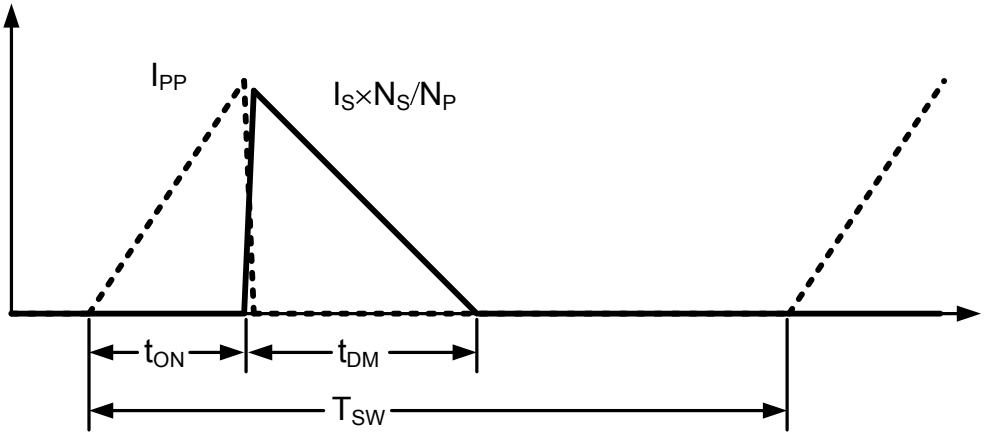


Figure 14. Transformer Currents

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{T_{SW}} \quad (5)$$

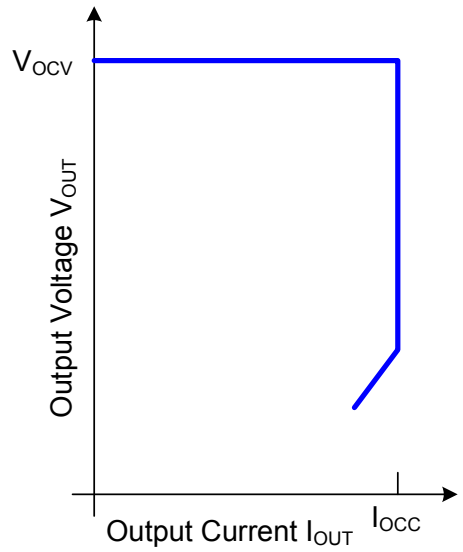


Figure 15. Typical Target Output V-I Characteristic

Valley-Switching

The TPS92315 utilizes valley-switching to reduce switching losses in the MOSFET, to reduce induced-EMI, and to minimize the turn-on current spike at the sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing has diminished.

Referring to Figure 16 below, the TPS92315 operates in a valley-skipping mode in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

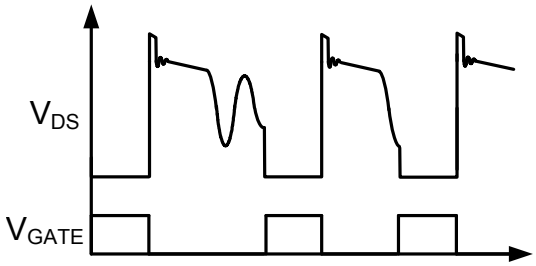


Figure 16. Valley-Skipping Mode

Start-Up Operation

Upon application of input voltage to the converter, the start-up resistor connected to VCC from the bulk capacitor voltage (V_{BULK}) charges the VCC capacitor. During charging of the VCC capacitor the device bias supply current is less than 1.5 µA. When VCC reaches the 21V UVLO turn-on threshold, the controller is enabled and the converter starts switching. The initial three cycles are limited to $I_{PP(min)}$. This allows sensing any initial input or output faults with minimal power delivery. After the initial three cycles at minimum $I_{PP(min)}$, the controller responds to the condition dictated by the control law. The converter remains in discontinuous mode during charging of the output capacitor(s), maintaining a constant output current until the output voltage is in regulation.

Fault Protection

There is comprehensive fault protection incorporated into the TPS92315. Protection functions include:

- Output Over Voltage
- Input Under Voltage
- Internal Over Temperature

- Primary Over-current fault
- ISNS pin fault
- VSNS pin fault

An UVLO reset and restart sequence applies for all fault protection events.

The output over-voltage function is determined by the voltage feedback on the VSNS pin. If the voltage sample on VSNS exceeds 115% of the nominal V_{OUT}, the device stops switching and keeps the internal circuitry enabled to discharge the VCC capacitor to the UVLO turn-off threshold. After that, the device returns to the start state and a start-up sequence ensues.

The TPS92315 always operates with cycle-by-cycle primary peak current control. The normal operating range of the ISNS pin is 0.75V to 0.25V. There is additional protection if the ISNS pin reaches 1.5V. This results in a UVLO reset and restart sequence. There is no leading-edge blanking on the 1.5V threshold on ISNS.

The line input run and stop thresholds are determined by current information at the VSNS pin during the MOSFET on-time. While the VSNS pin is clamped close to GND during the MOSFET on-time, the current through R_{AUX1} is monitored to determine a sample of the bulk capacitor voltage. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. The run current threshold is 220 µA and the stop current threshold is 80 µA.

The internal over-temperature protection threshold is 165°C. If the junction temperature reaches this threshold the device initiates a UVLO reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VSNS pin. If complete loss of feedback information on the VSNS pin occurs, the controller stops switching and restarts.

DESIGN PROCEDURE

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the TPS92315 family of controllers. Refer to the Figure 17 for component names and network locations. The design procedure equations use terms that are defined below.

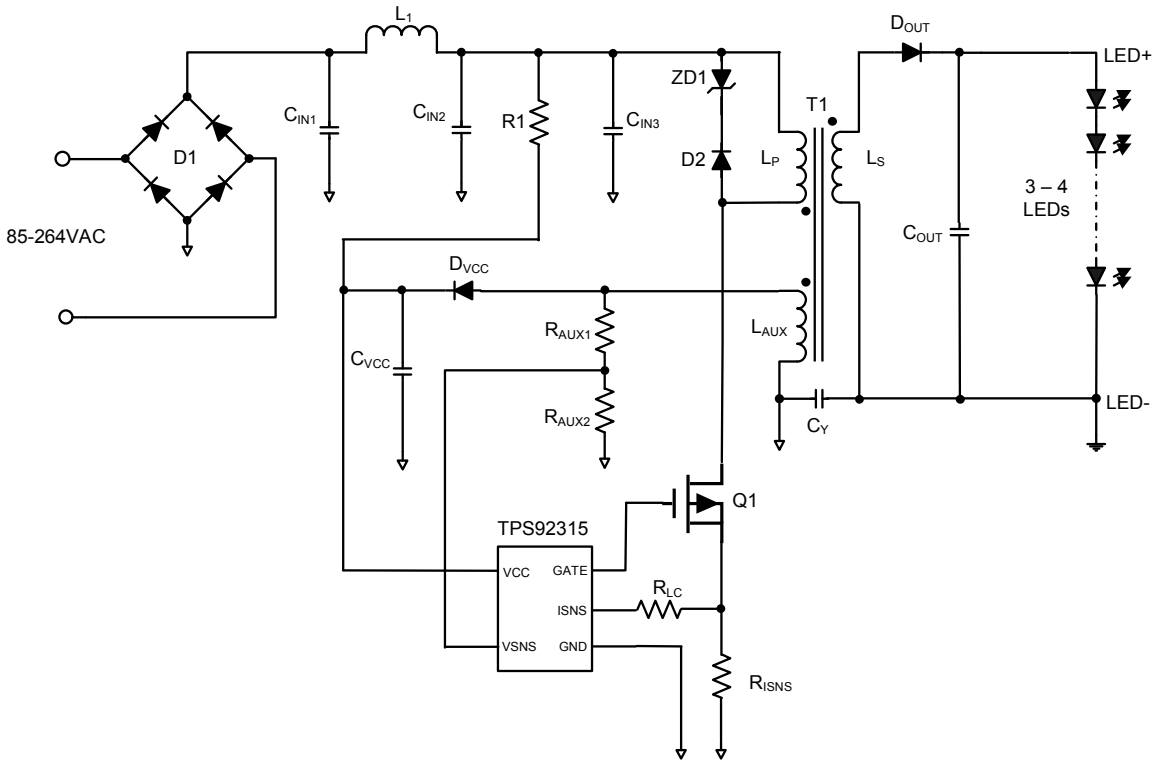


Figure 17. Design Procedure Application Example

Definition of Terms

Capacitance Terms in Farads

- **C_{BULK}:** total input capacitance of C_{IN1}, C_{IN2} and C_{IN3}.
- **C_{VCC}:** minimum required capacitance on the VCC pin.
- **C_{OUT}:** minimum output capacitance required.

Duty Cycle Terms

- **D_{MAGCC}:** secondary diode conduction duty cycle in CC, 0.425.
- **D_{MAX}:** MOSFET maximum on-time duty cycle.

Frequency Terms in Hertz

- **f_{LINE}:** minimum line frequency.
- **f_{MAX}:** target full-load maximum switching frequency of the converter.
- **f_{MIN}:** minimum switching frequency of the converter, add 15% margin over the $f_{SW(min)}$ limit of the device.
- **$f_{SW(min)}$:** minimum switching frequency (see ELECTRICAL CHARACTERISTICS).

Current Terms in Amperes

- **I_{OCC}:** converter output constant-current target.
- **$I_{PP(max)}$:** maximum transformer primary current.
- **I_{START}:** start-up bias supply current (see ELECTRICAL CHARACTERISTICS).
- **I_{TRAN}** : required positive load-step current.

- **$I_{VSNSL(run)}$:** VSNS pin run current (see ELECTRICAL CHARACTERISTICS).

Current and Voltage Scaling Terms

- **K_{AM}:** maximum-to-minimum peak primary current ratio (see ELECTRICAL CHARACTERISTICS).
- **K_{LC}:** current-scaling constant (see ELECTRICAL CHARACTERISTICS).

Transformer Terms

- **L_P:** transformer primary inductance.
- **N_{AS}:** transformer auxiliary-to-secondary turns ratio.
- **N_{PA}:** transformer primary-to-auxiliary turns ratio.
- **N_{PS}:** transformer primary-to-secondary turns ratio.

Power Terms in Watts

- **P_{IN}:** converter maximum input power.
- **P_{OUT}:** full-load output power of the converter.
- **P_{R1}:** VCC start-up resistor power dissipation.

Resistance Terms in Ω

- **R_{ISNS}:** primary current programming resistance.
- **R_{ESR}:** total ESR of the output capacitor(s).
- **R_{AUX1}:** high-side VSNS pin resistance.
- **R_{AUX2}:** low-side VSNS pin resistance.
- **R_1:** maximum start-up resistance to achieve the turn-on time target.

Timing Terms in Seconds

- **T_D:** current-sense delay including MOSFET turn-off delay; add 50 ns to MOSFET delay.
- **$T_{DMAG(min)}$:** minimum secondary rectifier conduction time.
- **$T_{ON(min)}$:** minimum MOSFET on time.
- **T_R:** the reciprocal of resonant frequency during the DCM (discontinuous conduction mode) operation.
- **T_{STR}:** converter start-up time requirement.

Voltage Terms in Volts

- **V_{BULK}:** highest bulk capacitor voltage for quescient power measurement.
- **$V_{BULK(min)}$:** minimum voltage on C_{B1} and C_{B2} at full power.
- **V_{CCR}:** constant-current regulating voltage (see ELECTRICAL CHARACTERISTICS).
- **$V_{ISNSTMAX}$:** ISNS pin maximum current-sense threshold (see ELECTRICAL CHARACTERISTICS).
- **$V_{ISNSTMIN}$:** ISNS pin minimum current-sense threshold (see ELECTRICAL CHARACTERISTICS).
- **V_{VCCOFF}:** UVLO turn-off voltage (see ELECTRICAL CHARACTERISTICS).
- **V_{VCCON}:** UVLO turn-on voltage (see ELECTRICAL CHARACTERISTICS).
- **$V_{O\Delta}$:** output voltage drop allowed during the load-step transient.
- **V_{DSPK}:** peak MOSFET drain-to-source voltage at high line.
- **V_F:** secondary rectifier forward voltage drop at near-zero current.
- **V_{FA}:** auxiliary rectifier forward voltage drop.
- **V_{LK}:** estimated leakage inductance energy reset voltage.
- **V_{OCV}:** pre-set output voltage of the converter.
- **V_{OUT}:** LED string voltage.
- **V_{OCC}:** target lowest converter output voltage in constant-current regulation.
- **V_{REV}:** peak reverse voltage on the secondary rectifier.
- **V_{RIPPLE}:** output peak-to-peak ripple voltage at full-load.
- **V_{VSNSR}:** CV regulating level at the VSNS input (see ELECTRICAL CHARACTERISTICS).

AC Voltage Terms in V_{RMS}

- **$V_{IN(max)}$:** maximum input voltage to the converter.
- **$V_{IN(min)}$:** minimum input voltage to the converter.
- **$V_{IN(run)}$:** converter input start-up (run) voltage.

Efficiency Terms

- **η_{SB}:** estimated efficiency of the converter at no-load condition, not including start-up resistance or bias losses. For a E14 or GU-10 application, 70% to 75% is a good initial estimate.
- **η:** converter overall efficiency.
- **η_{XFMR}:** transformer primary-to-secondary power transfer efficiency.

Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input capacitance, C_{IN1} and C_{IN2} total, in order to determine the maximum Np to Ns turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

Maximum input power is determined based on V_{OCV}, I_{OCC}, and the full-load efficiency target.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \tag{6}$$

The below equation provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{2P_{IN} \times \left\{ 0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right\}}{\left(2V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE}} \tag{7}$$

Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM quasi-resonant time.

Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period, or 1 µs assuming 500 kHz resonant frequency. D_{MAX} can be determined using the equation below.

$$D_{MAX} = 1 - \left(\frac{T_R}{2} \times f_{MAX} \right) - D_{MAGCC} \tag{8}$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with the equation below. D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant-current, CC, operation. It is set internally by the TPS92315 at 0.425. The total voltage on the secondary winding needs to be determined; which is the sum of V_{OCV} and the secondary rectifier V_F. For the E14 or GU-10 applications with V_{OUT} of around 10V at an I_{OCC} of 350 mA, a turns ratio range of 7 to 8 is typically used.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F)} \tag{9}$$

Once an optimum turns ratio is determined from a detailed transformer design, use this ratio for the following parameters.

The TPS92315 controller constant-current regulation is achieved by maintaining a maximum D_{MAG} (the secondary diode conduction duty cycle) of 0.425 at the maximum primary current setting. The transformer turns ratio and constant-current regulating voltage determine the current sense resistor for a target constant current.

Since not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power. For a typical E14 or GU-10 application, bias power of 1.5% is a good estimate. An overall transformer efficiency of 0.9 is a good estimate to include 3.5% leakage inductance, 5% core and winding loss, and 1.5% bias power.

$$R_{ISNS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \eta_{XFMR} \quad (10)$$

The primary transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency and output current and transformer power losses are included in the equation below. Initially determine transformer primary current.

Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{ISNSTMAX}}{R_{ISNS}} \quad (11)$$

$$L_P = \frac{2(V_{OCV} + V_F) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \quad (12)$$

The secondary winding to auxiliary winding transformer turns ratio (N_{AS}) is determined by the lowest target operating output voltage in constant-current regulation and the V_{VCCOFF} of the TPS92315. There is additional energy supplied to VCC from the transformer leakage inductance energy which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{VCCOFF} + V_{FA}}{V_{OCC} + V_F} \quad (13)$$

Transformer Parameter Verification

The transformer turns ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage so these should be reviewed. The TPS92315 controller requires a minimum on time of the MOSFET (T_{ON}) and minimum D_{MAG} time (T_{DMAG}) of the secondary rectifier in the high line, minimum load condition. The selection of F_{MAX}, L_P and R_{ISNS} affects the minimum T_{ON} and T_{DMAG}.

The secondary rectifier and MOSFET voltage stress can be determined by the equations below.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} \quad (14)$$

For the MOSFET V_{DS} voltage stress, an estimated leakage inductance voltage spike (V_{LK}) needs to be included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + (V_{OCV} + V_F) \times N_{PS} + V_{LK} \quad (15)$$

The following equations are used to determine if the minimum T_{ON} target of 300 ns and minimum T_{DMAG} target of 1.1 µs is achieved.

$$T_{ON(min)} = \frac{L_P}{\left(V_{IN(max)} \times \sqrt{2}\right)} \times \frac{I_{PP(max)} \times V_{ISNSTMIN}}{V_{ISNSTMAX}} \quad (16)$$

$$T_{DMAG(min)} = \frac{T_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times (V_{OCV} + V_F)} \quad (17)$$

Output Capacitance

The output capacitance value is typically determined by the current ripple requirement of the LED current. For example, some E14 or GU-10 applications requires the current ripple to be 30% of the LED current. Then the equation below assumes that the switching frequency can be at the TPS92315 minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{0.3 \times I_S \left(\frac{1}{f_{SW(min)}} + 150\,\mu s \right)}{V_{O\Delta}} \quad (18)$$

Another consideration of the output capacitor(s) is the ripple voltage requirement which is reviewed based on secondary peak current and ESR. A margin of 20% is added to the capacitor ESR requirement in the equation below.

$$R_{ESR} = \frac{V_{RIPPLE} \times 0.8}{I_{PP(max)} \times N_{PS}} \quad (19)$$

VCC Capacitance, C_{VCC}

The capacitance on VCC needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. At this time the auxiliary winding can sustain the voltage to the TPS92315. The total output current available to the load and to charge the output capacitors is the constant-current regulation target. The equation below assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved. There is an estimated 1 mA of gate-drive current in the equation and 1V of margin added to VCC.

$$C_{VCC} = \frac{(I_{RUN} + 1mA) \times \frac{C_{OUT} \times C_{OCC}}{I_O}}{(V_{VCCON} - V_{VCCOFF}) - 1V} \quad (20)$$

VCC Start-Up Resistance, R_1

Once the VCC capacitance is known, the start-up resistance from V_{BULK} to achieve the turn-on time target can be determined.

$$R_1 = \frac{\sqrt{2} \times V_{IN(max)}}{I_{START} + \frac{V_{VCCON} \times C_{VCC}}{T_{STR}}} \quad (21)$$

VSNS Resistor Divider

The VSNS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{AUX1}) determines the line voltage at which the controller enables continuous GATE operation. R_{AUX1} is initially determined based on transformer auxiliary to primary turns ratio and desired input voltage operating threshold.

$$R_{AUX1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSNS(run)}} \quad (22)$$

The low-side VSNS pin resistor is selected based on desired V_{OUT} regulation voltage.

$$R_{AUX2} = \frac{R_{AUX1} \times V_{VSNSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSNSR}} \quad (23)$$

The TPS92315 can maintain tight constant-current regulation over input line by utilizing the line compensation feature. The line compensation resistor (R_{LC}) value is determined by current flowing in R_{AUX1} and expected gate drive and MOSFET turn-off delay. Assume a 50 ns internal delay in the TPS92315.

$$R_{LC} = \frac{K_{LC} \times R_{AUX1} \times R_{ISNS} \times T_D \times N_{PA}}{L_P} \quad (24)$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92315DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T315	Samples
TPS92315DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T315	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

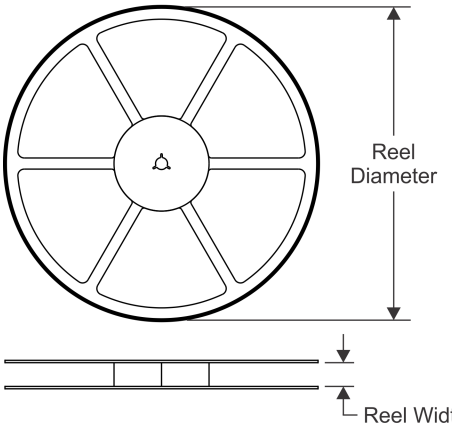
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

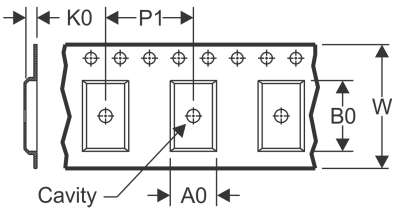
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

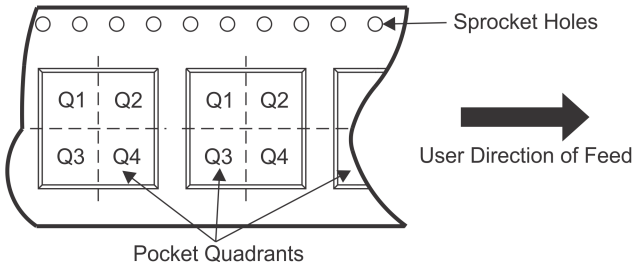


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

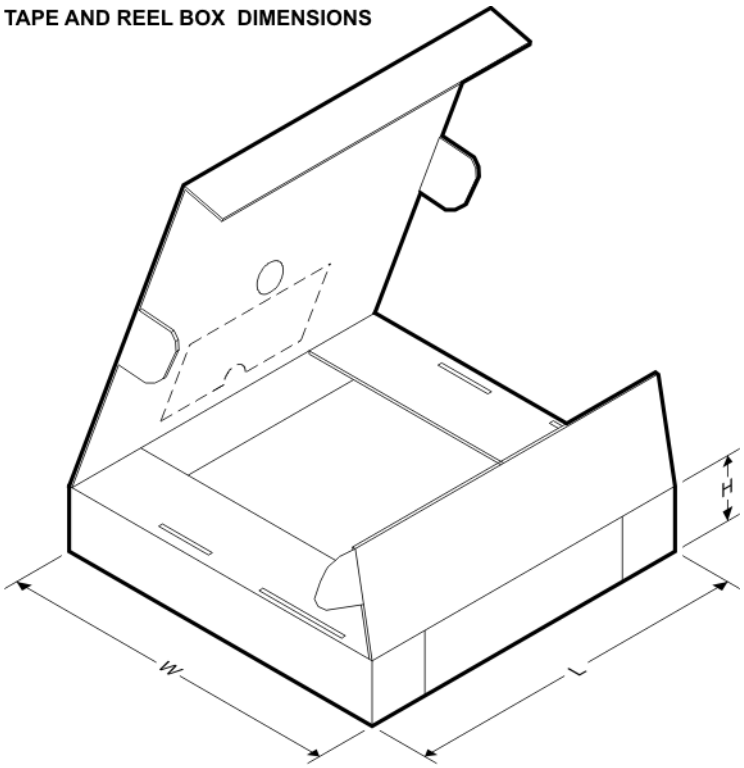
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92315DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS92315DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

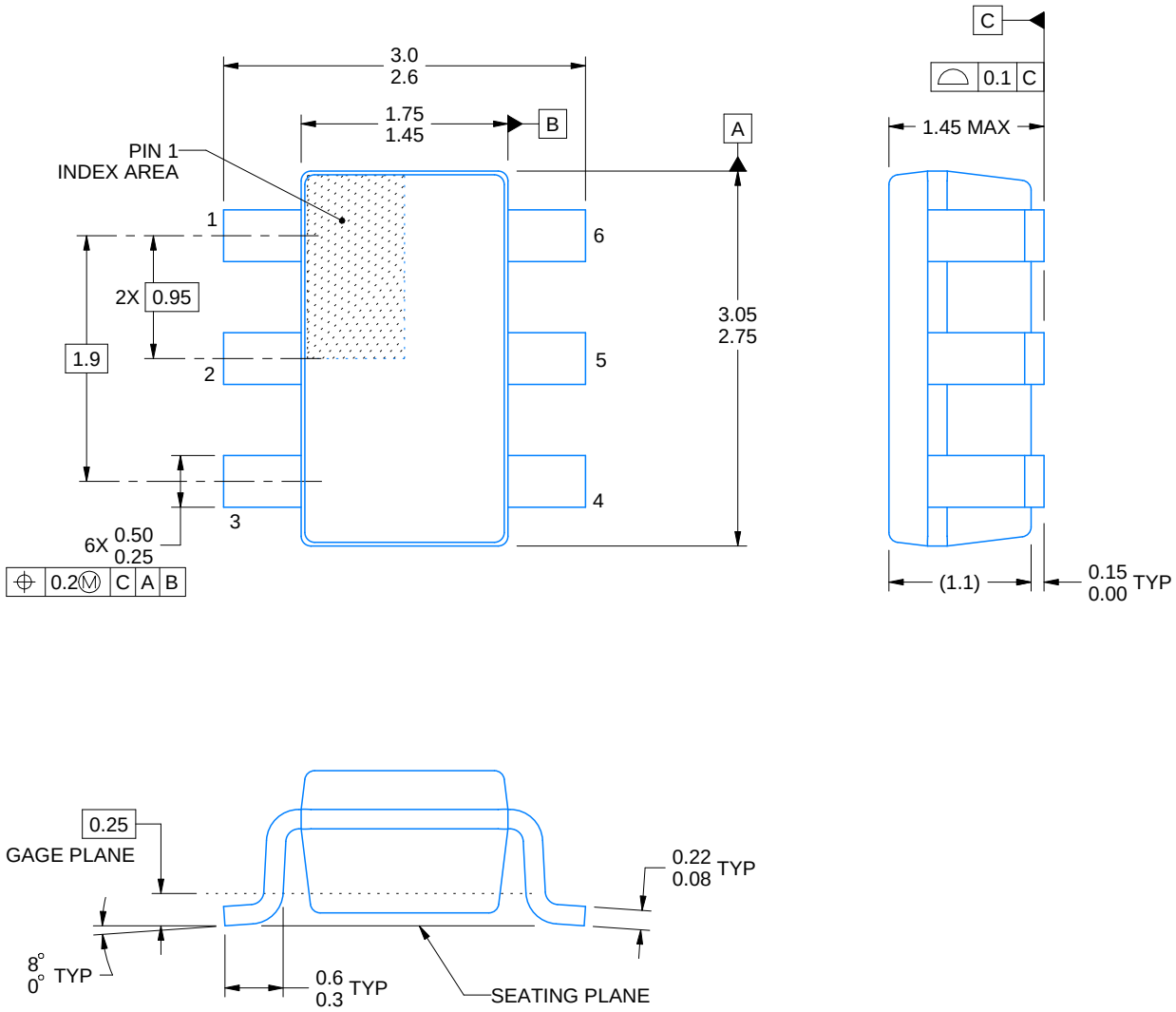
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92315DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS92315DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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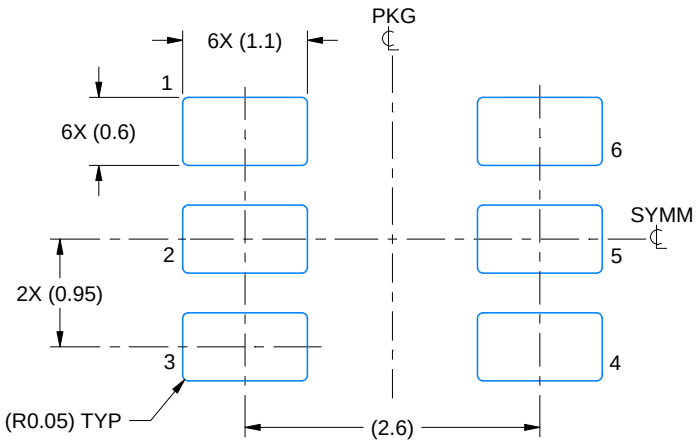
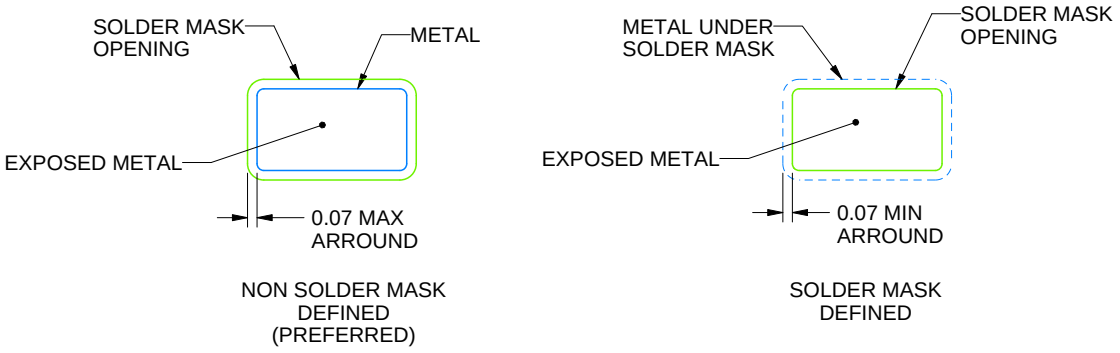
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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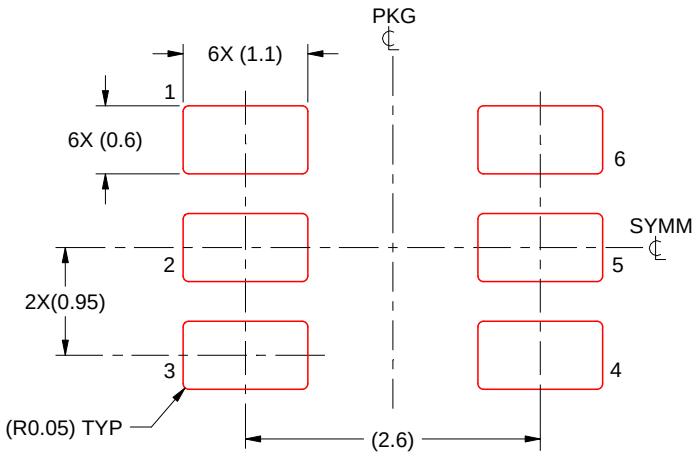
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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