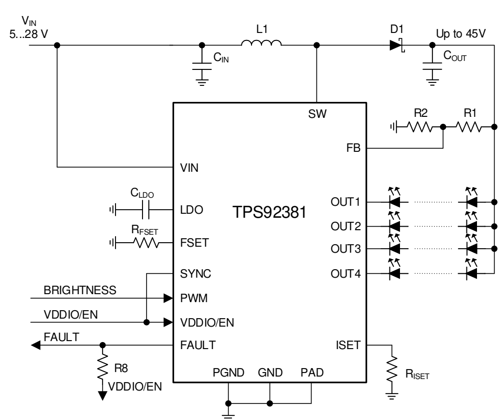
TPS92380、TPS92381 具有 3、4 通道的 45V LED 背光灯驱动器

1 特性

- 3 通道、4 通道 120mA 灌电流
  - 在 100Hz 时具有 10 000:1 的高调光比
  - 电流匹配度为 1%(典型值)
  - LED 灯串电流高达 120mA/通道
  - 可以在外部组合输出,以便为每个灯串提供更高的电流
- 用于 LED 灯串电源的集成式升压和 SEPIC 转换器
  - 输入电压工作范围:4.5V 至 40V
  - 输出电压最高达 45V
  - 集成式 3.3A 开关 FET
  - 开关频率为 300kHz 至 2.2MHz
  - 开关同步输入
  - 扩频,以实现更低的 EMI
- 故障检测和保护
  - 故障输出
  - 输入电压过压保护 (OVP)、欠压锁定 (UVLO) 和过流保护 (OCP)
  - 升压块 SW OVP 和输出 OVP
  - LED 开路和短路故障检测
  - 热关断



简化版原理图

2 应用

- 适用于中型面板的工业背光
- 适用于中型面板的消费类背光
- 适用于 LED 面板的工业照明

3 说明

TPS92380、TPS92381 是一款具有直流/直流转换器的高度集成、高输出功率且易于使用的 LED 驱动器。直流/直流转换器支持升压和 SEPIC 工作模式。此器件具有四个或三个高精度灌电流,可以将这些电流组合在一起以获得更高的电流能力。

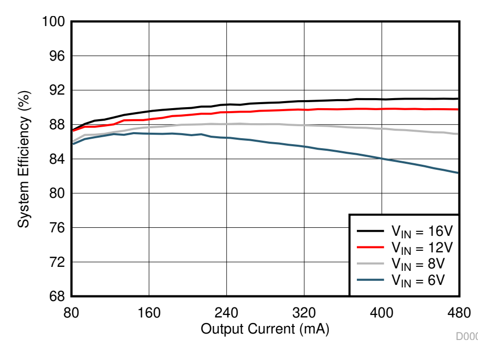
直流/直流转换器可基于 LED 正向电压提供自适应输出电压控制。该特性可在所有条件下将电压调节到能够满足需要的最低水平,从而更大限度降低功耗。为了降低 EMI,直流/直流转换器支持针对开关频率进行扩频以及使用专用引脚实现外部同步。凭借宽范围可调频率,TPS9238x 可避免敏感频段的干扰。

TPS9238x 的输入电压范围为 4.5V 至 40V。TPS9238x 集成了丰富的故障检测功能。

器件信息(1)

器件型号	封装	封装尺寸(标称值)
TPS92380	HTSSOP (20)	6.50mm × 4.40mm
TPS92381		

(1) 如需了解所有可用封装,请参阅数据表末尾的可订购产品附录。



LED 背光效率

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
May 2021	*	Initial Release

5 Device Comparison Table

	TPS92380	TPS92381
Number of LED channels	3	4
LED current / channel	120 mA	120 mA

6 Pin Configuration and Functions

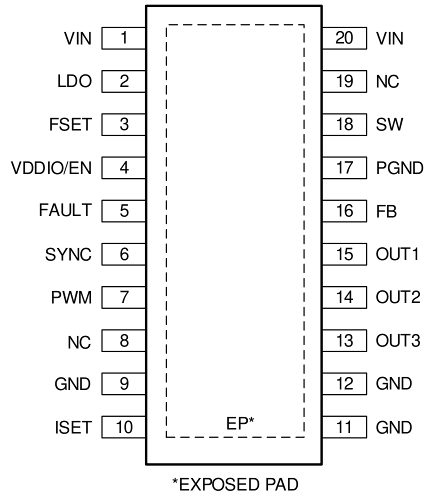


图 6-1. TPS92380 PWP Package 20-Pin HTSSOP with Exposed Thermal Pad Top View

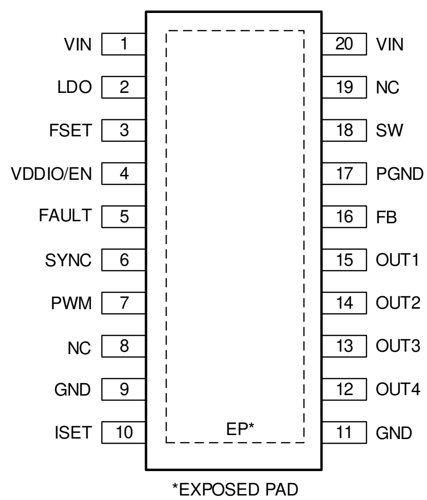


图 6-2. TPS92381 PWP Package 20-Pin HTSSOP with Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VIN	A	Input power pin; input voltage OVP detection pin; input current sense positive input pin.
2	LDO	A	Output of internal LDO; connect a 1-µF decoupling capacitor between this pin and noise-free ground. Put the capacitor as close to the chip as possible.
3	FSET	A	DC-DC (boost or SEPIC) switching frequency setting resistor; for normal operation, resistor value from 24 kΩ to 219 kΩ must be connected between this pin and ground.
4	VDDIO/EN	I	Enable input for the device as well as supply input (VDDIO) for digital pins.
5	FAULT	OD	Fault signal output. If unused, the pin may be left floating.
6	SYNC	I	Input for synchronizing DC-DC converter. If synchronization is not used, connect this pin to ground to disable spread spectrum or to VDDIO/EN to enable spread spectrum.
7	PWM	I	PWM dimming input.
8	NC	-	No connect.
9	GND	G	Ground.

表 6-1. Pin Functions (continued)

PIN		TYPE[(1)]	DESCRIPTION
NO.	NAME		
10	ISET	A	LED current setting resistor; for normal operation, resistor value from 20 kΩ to 129 kΩ must be connected between this pin and ground.
11	GND	G	Ground.
12	OUT4/GND	A	Current sink output for TPS92381 This pin must be connected to ground if not used. GND pin for TPS92380.
13	OUT3	A	Current sink output. This pin must be connected to ground if not used.
14	OUT2	A	Current sink output. This pin must be connected to ground if not used.
15	OUT1	A	Current sink output. This pin must be connected to ground if not used.
16	FB	A	DC-DC (boost or SEPIC) feedback input; for normal operation this pin must be connected to the middle of a resistor divider between V_{OUT} and ground using feedback resistor values greater than 5 kΩ.
17	PGND	G	DC-DC (boost or SEPIC) power ground.
18	SW	A	DC-DC (boost or SEPIC) switch pin.
19	NC	-	No connect.
20	VIN	A	Input power pin and pin for input voltage detection for OVP protection.

(1) A: Analog pin, G: Ground pin, P: Power pin, I: Input pin, I/O: Input/Output pin, O: Output pin, OD: Open Drain pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
Voltage on pins	VIN, SD, SW, FB	–0.3	50	V
	OUT1, OUT2, OUT3, OUT4	–0.3	45	
	LDO, SYNC, FSET, ISET, PWM, VDDIO/EN, FAULT	–0.3	5.5	
Continuous power dissipation[(3)]		Internally Limited		
Ambient temperature, T_A [(4)]		–40	125	°C
Junction temperature, T_J [(4)]		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 145°C (typical).
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 150°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, all pins [(1)]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner pins (1, 10, 11 and 20)	±750	
			All pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	NOM	MAX	UNIT
Voltage on pins	VIN	4.5	12	45	V
	SW	0		45	
	OUT1, OUT2, OUT3, OUT4	0		40	
	FB, FSET, LDO, ISET, VDDIO/EN, FAULT	0		5.25	
	SYNC, PWM	0		VDDIO/EN	

(1) All voltages are with respect to the potential at the GND pins.

7.4 Thermal Information

THERMAL METRIC[(1)]		TPS9238x PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[(2)]	44.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.2	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

7.5 Electrical Characteristics

Limits apply over the full operation temperature range −40°C ≤ T_A ≤ +125°C , unless otherwise specified, V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Standby supply current	Device disabled, $V_{VDDIO/EN}$ = 0 V, V_{IN} = 12 V		4.5	20	μA
	Active supply current	V_{IN} = 12 V, V_{OUT} = 26 V, output current 80 mA/ channel, converter f_{SW} = 300 kHz		5	12	mA
V_{BG}	Bandgap Voltage		1.18	1.2	1.24	V

7.6 Internal LDO Electrical Characteristics

Limits apply over the full operation temperature range −40°C ≤ T_A ≤ +125°C , unless otherwise specified, V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LDO}	Output voltage	V_{IN} = 12 V	4.15	4.3	4.55	V
V_{DR}	Dropout voltage		120	300	430	mV
I_{SHORT}	Short circuit current			50		mA
I_{EXT}	Current for external load				5	mA

7.7 Protection Electrical Characteristics

Limits apply over the full operation temperature range −40°C ≤ T_A ≤ +125°C , unless otherwise specified, V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	VIN OVP threshold voltage		41	43	45	V
V_{UVLO}	VIN UVLO Falling threshold		3.7	3.85	4	V
V_{UVLO_HYST}	VIN UVLO Rising threshold - VIN UVLO Fallling threshold			150		mV
V_{FB_OVP}	FB threshold for BST_OVP fault			2.3		V
T_{TSD}	Thermal shutdown Rising threshold		150	165	175	℃
T_{TSD_HYS}	Thermal shutdown Rising threshold - Thermal shutdown Falling threshold			20		℃

7.8 Current Sinks Electrical Characteristics

Limits apply over the full operation temperature range −40°C ⩽ T_A ⩽ +125°C , unless otherwise specified, V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs OUT1 to OUT4 , V_{OUTx} = 45 V, EN = L		0.1	5	µA
I_{MAX}	Maximum current	OUT1, OUT2, OUT3, OUT4, R_{ISET} = 20 kΩ		120		mA
I_{OUT}	Output current accuracy	I_{OUT} = 120 mA	−5%		5%	
I_{MATCH}	Output current matching(1)	I_{OUT} = 100 mA, PWM duty =100%		1%	5%	
V_{LOW_COMP}	Low comparator threshold			0.9		V
V_{MID_COMP}	Mid comparator threshold			1.9		V
V_{HIGH_COMP}	High comparator threshold		5.5	6	7	V

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUTx), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Matching number is calculated: (MAX-MIN)/AVG. The typical specification provided is the most likely norm of the matching figure for all parts. LED current sinks were characterized with 1-V headroom voltage. Note that some manufacturers have different definitions in use.

7.9 PWM Brightness Control Electrical Characteristics

Limits apply over the full operation temperature range −40°C ⩽ T_A ⩽ +125°C , unless otherwise specified, V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM}	PWM input frequency		100		20 000	Hz
$t_{ON/OFF}$	Minimum on/off time(1)			1		µs

(1) This specification is not ensured by ATE.

7.10 Boost and SEPIC Converter Characteristics

Limits apply over the full operation temperature range −40°C ⩽ T_A ⩽ +125°C , unless otherwise specified, V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5		40	V
V_{OUT}	Output voltage		6		45	
f_{SW_MIN}	Minimum switching frequency	Defined by R_{FSET} resistor		300		kHz
f_{SW_MAX}	Maximum switching frequency	Defined by R_{FSET} resistor		2 200		kHz
t_{OFF}	Minimum switch OFF time(1)	f_{SW} ⩾ 1.15 MHz			55	ns
I_{SW_MAX}	SW current limit first triggerred		3.3	3.7	4.1	A
t_{SW_MAX}	SW current limit first triggerred period			1.6		s
I_{SW_LIM}	SW current limit		3	3.35	3.7	A
R_{DSON}	FET R_{DSON}			240	400	mΩ
f_{SYNC}	External SYNC frequency		300		2 200	kHz
t_{SYNC_ON}	External SYNC on time(1)		150			ns
t_{SYNC_OFF}	External SYNC off time(1)		150			ns

(1) This specification is not ensured by ATE.

7.11 Logic Interface Characteristics

Limits apply over the full operation temperature range −40°C ⩽ T_A ⩽ +125°C , unless otherwise specified, V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT VDDIO/EN						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.65			
I_{EN}	Input DC current		−1	5	30	µA
	Input transient current during VDDIO/EN powering up				1.2	mA
LOGIC INPUT SYNC, PWM						

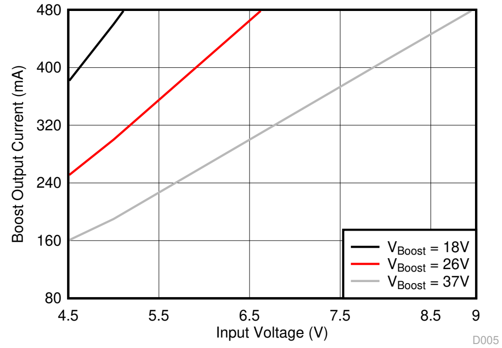
7.11 Logic Interface Characteristics (continued)

Limits apply over the full operation temperature range −40°C ⩽ T_A ⩽ +125°C , unless otherwise specified, V_{IN} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low level				0.2 × VDDIO/EN	V
V_{IH}	Input high level		0.8 × VDDIO/EN			V
I_I	Input current		−1		1	µA
LOGIC OUTPUT FAULT						
V_{OL}	Output low level	Pullup current 3 mA		0.3	0.5	V
$I_{LEAKAGE}$	Output leakage current	V = 5.5 V			1	µA

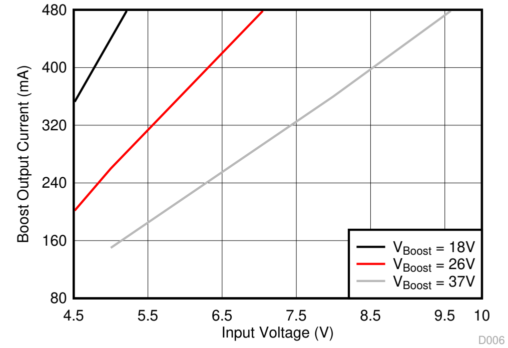
7.12 Typical Characteristics

Unless otherwise specified: D = NRVB460MFS, T_A = 25°C



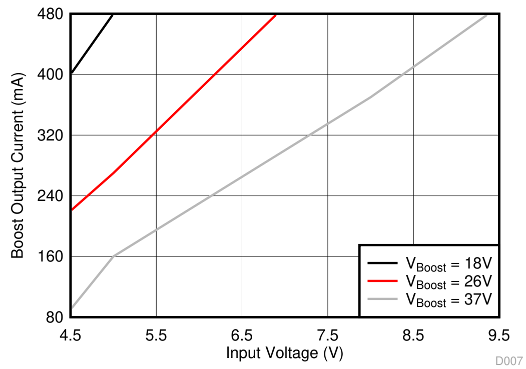
f_{SW} = 400 kHz L = 33 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 33 µF (electrolytic) + 2 × 10 µF (ceramic)

图 7-1. Maximum Boost Current



f_{SW} = 1.1 MHz L = 15 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 33 µF (electrolytic) + 10 µF (ceramic)

图 7-2. Maximum Boost Current



f_{SW} = 2.2 MHz L = 10 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 3 × 10 µF (ceramic)

图 7-3. Maximum Boost Current

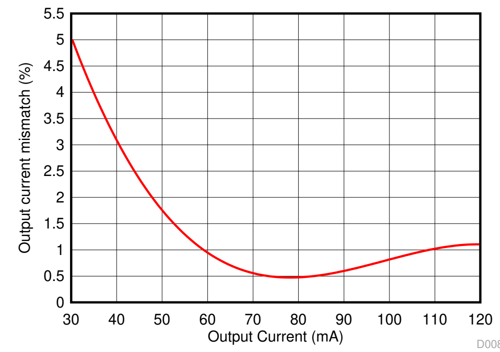
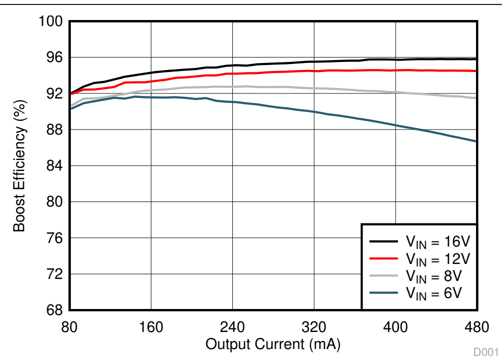
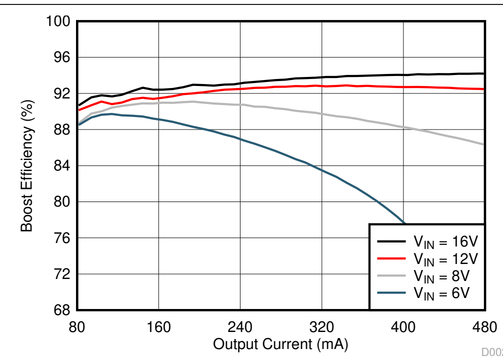


图 7-4. LED Current Sink Matching



f_{SW} = 400 kHz L = 22 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 33 µF (electrolytic) V_{BOOST} = 18 V
+ 2 × 10 µF (ceramic)

图 7-5. Boost Efficiency

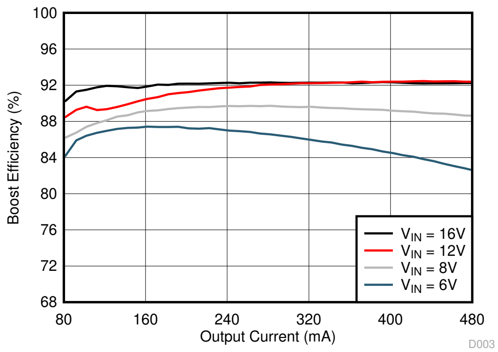


f_{SW} = 400 kHz L = 22 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 33 µF (electrolytic) V_{BOOST} = 30 V
+ 2 × 10 µF (ceramic)

图 7-6. Boost Efficiency

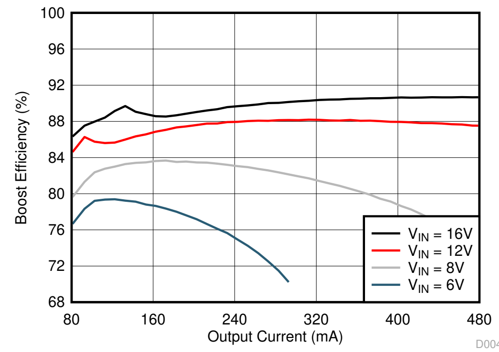
7.12 Typical Characteristics (continued)

Unless otherwise specified: D = NRVB460MFS, T_A = 25°C



f_{SW} = 2.2 MHz L = 4.7 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 3 × 10 µF (ceramic) V_{BOOST} = 18 V

图 7-7. Boost Efficiency



f_{SW} = 2.2 MHz L = 4.7 µH DC Load (PWM = 100%)
C_{IN} and C_{OUT} = 3 × 10 µF (ceramic) V_{BOOST} = 30 V

图 7-8. Boost Efficiency

8 Detailed Description

8.1 Overview

The TPS92380, TPS92381 is a highly integrated LED driver for medium-size LCD backlight applications. It includes a DC-DC with an integrated FET, supporting both boost and SEPIC modes, an internal LDO enabling direct connection to battery without need for a pre-regulated supply, and 3 or 4 LED current sinks. The VDDIO/EN pin provides the supply voltage for digital IOs (PWM and SYNC inputs) and at the same time enables the device.

The switching frequency on the DC-DC converter is set by a resistor connected to the FSET pin. The maximum voltage of the DC-DC is set by a resistive divider connected to the FB pin. For the best efficiency, the output voltage is adapted automatically to the minimum necessary level needed to drive the LED strings. This is done by monitoring LEDs' cathode voltage in real time. For EMI reduction, two optional features are available:

- Spread spectrum, which reduces EMI noise around the switching frequency and its harmonic frequencies
- DC-DC can be synchronized to an external frequency connected to SYNC pin

The 3 or 4 constant current outputs OUT1, OUT2, OUT3, and OUT4 provide LED current up to 120 mA. Value for the current per OUT pin is set with a resistor connected to ISET pin. Current sinks that are not used must be connected to ground. Grounded current sink is disabled and excluded from boost adaptive voltage detection loop.

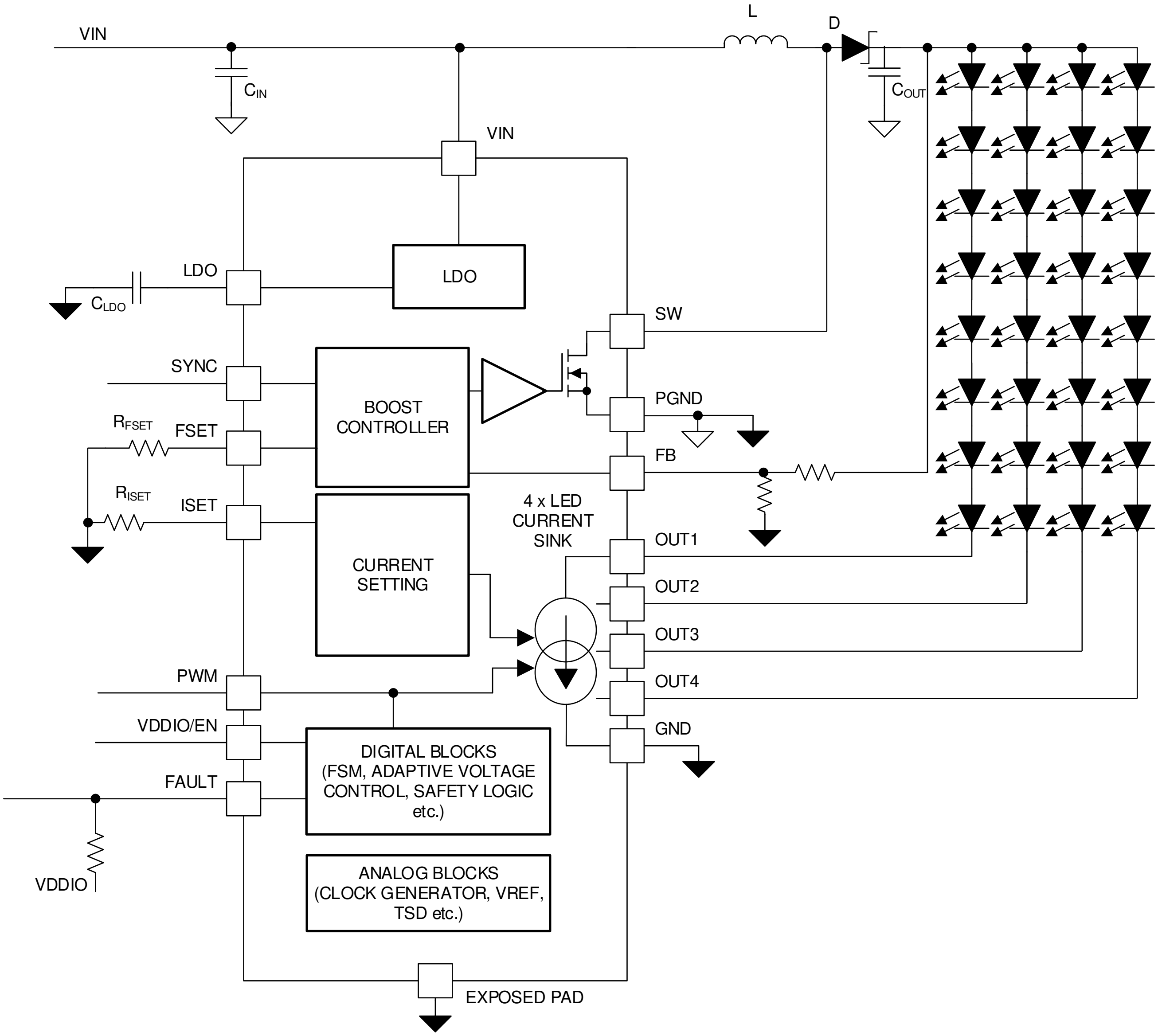
Brightness is controlled with the PWM input. Frequency range for the input PWM is from 100 Hz to 20 kHz. LED output PWM behavior follows the input PWM so the output frequency is equal to the input frequency.

TPS9238x has extensive fault detection features:

- LED open and short detection
- V_{IN} input overvoltage protection
- V_{IN} input undervoltage protection
- V_{Boost} output overvoltage protection
- SW overvoltage protection
- Thermal shutdown in case of chip overheated

Fault condition is indicated through the FAULT output pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Integrated DC-DC Converter

The TPS9238x DC-DC converter generates supply voltage for the LEDs and can operate in boost mode or in SEPIC mode. The output voltage, switching frequency are all configured by external resistors.

For detailed boost application, refer to *Typical Application for 4 LED Strings*.

For detailed SEPIC application, refer to *SEPIC Mode Application*.

8.3.1.1 DC-DC Converter Parameter Configuration

The TPS9238x converter is a current-peak mode DC-DC converter, where the switch FET's current and the output voltage feedback are measured and controlled. The block diagram is shown in 图 8-1.

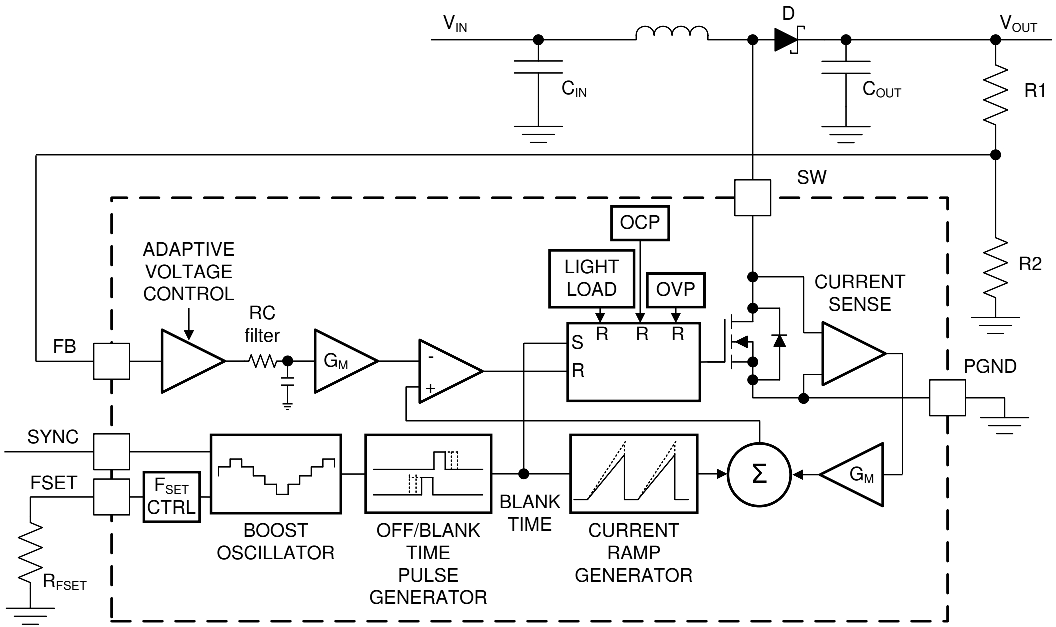


图 8-1. DC-DC Converter in Boost Application

8.3.1.1.1 Switching Frequency

Switching frequency is adjustable between 300 kHz and 2.2 MHz with R_{FSET} resistor as 方程式 1:

$$f_{SW} = 67600 / (R_{FSET} + 6.4) \quad (1)$$

where

- f_{SW} is switching frequency, kHz
- R_{FSET} is frequency setting resistor, kΩ

For example, if R_{FSET} is set to 163 kΩ, f_{SW} will be 400 kHz.

In most cases, lower switching frequency has higher system efficiency and lower internal temperature increase.

8.3.1.1.2 Spread Spectrum and External SYNC

TPS9238x has an optional spread spectrum feature (±3% from central frequency, 1-kHz modulation frequency) which reduces EMI noise at the switching frequency and its harmonic frequencies. If SYNC pin level is low, spread spectrum function is disabled. If SYNC pin level is high, spread spectrum function is enabled.

TPS9238x DC-DC converter can be driven by an external SYNC signal between 300 kHz and 2.2 MHz. When external synchronization is used, spread spectrum is not available. If the external synchronization input disappears, DC-DC continues operation at the frequency defined by R_{FSET} resistor and spread spectrum function will be enabled/disabled depending on the final SYNC pin level.

External SYNC frequency must be close to the frequency defined by R_{FSET} resistor. In external SYNC configuration, minimum frequency setting with R_{FSET} could go as low as 250 kHz to support 300-kHz switching with external clock.

表 8-1. DC-DC Synchronization Mode

SYNC PIN INPUT	MODE
Low	Spread spectrum disabled
High	Spread spectrum enabled
300 to 2200-kHz frequency	Spread spectrum disabled, external synchronization mode

8.3.1.1.3 Recommended Component Value and Internal Parameters

The TPS9238x DC-DC converter has an internal compensation network to ensure the stability. There's no external component needed for compensation. It's strongly recommended that the inductance value and the boost input and output capacitors value follow the requirement of 表 8-2. Also, the DC-DC internal parameters are chosen automatically according to the selected switching frequency (see 表 8-2) to ensure stability.

表 8-2. Boost Converter Parameters(1)

RANGE	FREQUENCY (kHz)	TYPICAL INDUCTANCE (µH)	TYPICAL BOOST INPUT AND OUTPUT CAPACITORS (µF)	MINIMUM SWITCH OFF TIME (ns)(2)	BLANK TIME (ns)
1	300 to 480	22 or 33	2 ×10 (cer.) + 33 (electr.)	150	95
2	480 to 1150	15	10 (cer.) + 33 (electr.)	60	95
3	1150 to 1650	10	3 × 10 (cer.)	40	95
4	1650 to 2200	4.7 or 10	3 × 10 (cer.)	40	70

(1) Parameters are for reference only.
(2) Due to current sensing comparator delay the actual minimum off time is 6 ns (typical) longer than in the table.

8.3.1.1.4 DC-DC Converter Switching Current Limit

The TPS9238x DC-DC converter has an internal SW FET inside chip's SW pin. The internal FET current is limited to 3.35 A (typical). The DC-DC converter will sense the internal FET current, and turn off the internal FET cycle-by-cycle when the internal FET current reaches the limit.

To support start transient condition, the current limit could be automatically increased to 3.7 A for a short period of 1.6 seconds when a 3.35-A limit is reached.

Note

Application condition where the 3.35-A limit is exceeded continuously is not allowed. In this case the current limit would be 3.35 A for 1.6 seconds followed by 3.7-A limit for 1.6 seconds, and this 3.2-second period repeats.

8.3.1.1.5 DC-DC Converter Light Load Mode

TPS9238x DC-DC converter will enter into light load mode in below condition:

- V_{IN} voltage is very close to V_{OUT}
- Loading current is very low
- PWM pulse width is very short

When DC-DC converter enters into light load mode, DC-DC converter stops switching occasionally to make sure boost output voltage won't rise up too much. It could also be called as PFM mode, since the DC-DC converter switching frequency will change in this mode.

8.3.1.2 Adaptive Voltage Control

The TPS9238x DC/DC converter generates the supply voltage for the LEDs. During normal operation, boost output voltage is adjusted automatically based on the LED cathode (OUTx pin) voltages. This is called adaptive boost control. Only the active LED outputs are monitored to control the adaptive boost voltage. Any LED strings with open or short faults are removed from the adaptive voltage control loop. The OUTx pin voltages are periodically monitored by the control loop. The boost voltage is raised if any of the OUTx voltage falls below the V_{LOW_COMP} threshold. The boost voltage is also lowered if all OUTx voltages are higher than V_{LOW_COMP} threshold. The boost voltage keeps unchanged when one of OUTx voltage touches the V_{LOW_COMP} threshold. In normal operation, the lowest voltage among the OUTx pins is around V_{LOW_COMP}, and boost voltage stays constant. V_{LOW_COMP} level is the minimum voltage which could guarantee proper LED current sink operation. See 图 8-2 for how the boost voltage automatically scales based on the OUT1-4 pin voltage.

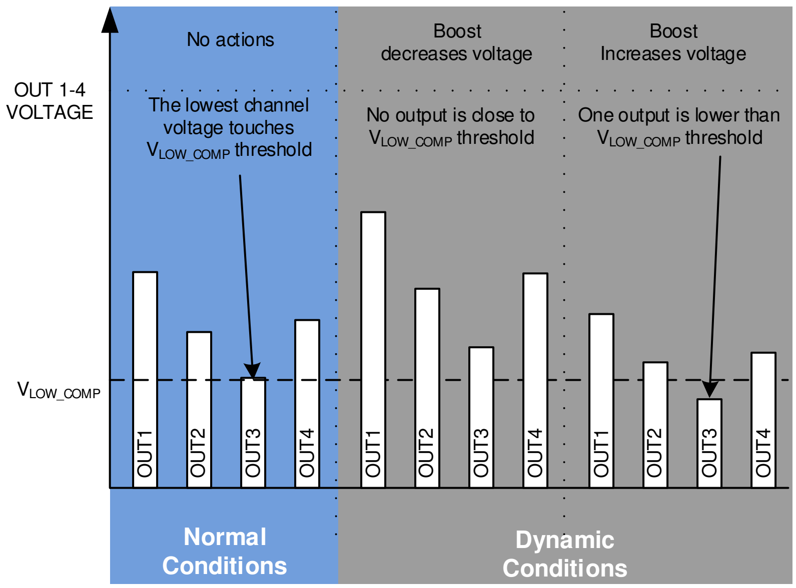


图 8-2. Adaptive Boost Voltage Control Loop Function

8.3.1.2.1 Using Two-Divider

V_{BOOST_MAX} voltage should be chosen based on the maximum voltage required for LED strings. Recommended maximum voltage is about 3 to 5-V higher than maximum LED string voltage. DC-DC output voltage is adjusted automatically based on LED cathode voltage. The maximum, minimum and initial boost voltages can be calculated with 方程式 2:

$$V_{BOOST} = \left(\frac{V_{BG}}{R2} + K \times 0.0387 \right) \times R1 + V_{BG} \tag{2}$$

where

- V_{BG} = 1.2 V
- R2 recommended value is 10 kΩ to 200 kΩ
- R1/R2 recommended value is 5 to 10
- K = 1 for maximum adaptive boost voltage (typical)
- K = 0 for minimum adaptive boost voltage (typical)
- K = 0.88 for initial boost voltage (typical)

For example, if R1 is set to 750 kΩ and R2 is set to 130 kΩ, V_{BOOST} will be in the range of 8.1 V to 37.1 V.

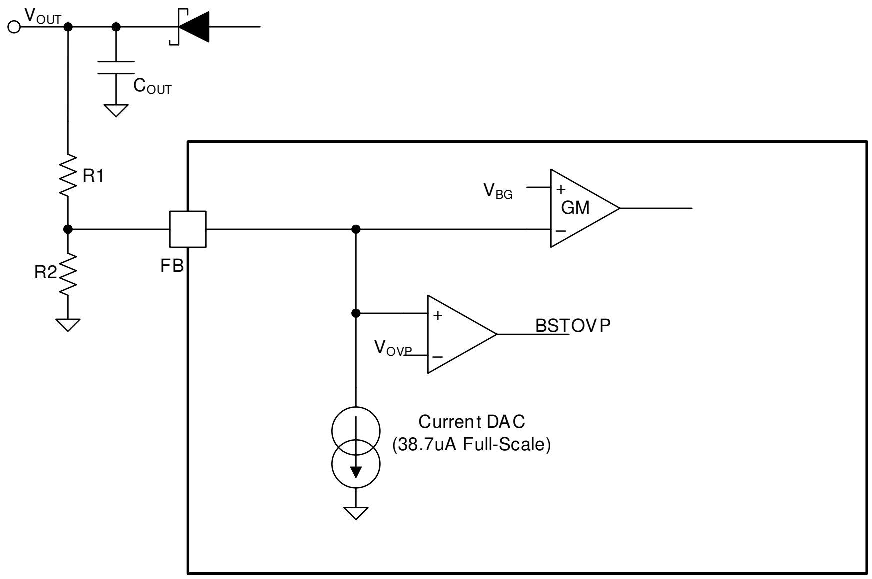


图 8-3. FB External Two-Divider Resistors

8.3.1.2.2 Using T-Divider

Alternatively, a T-divider can be used if resistance less than 100 kΩ is required for the external resistive divider. Then the maximum, minimum and initial boost voltages can be calculated with

$$V_{BOOST} = \left(\frac{R1 \times R3}{R2} + R1 + R3\right) K \times 0.0387 + \left(\frac{R1}{R2} + 1\right) \times V_{BG} \tag{3}$$

where

- V_{BG} = 1.2 V
- R2 recommended value is 10 kΩ to 200 kΩ
- R1/R2 recommended value is 5 to 10
- K = 1 for maximum adaptive boost voltage (typical)
- K = 0 for minimum adaptive boost voltage (typical)
- K = 0.88 for initial boost voltage (typical)

For example, if R1 is set to 100 kΩ, R2 is set to 10 kΩ and R3 is set to 60 kΩ, V_{BOOST} will be in the range of 13.2 V to 42.6 V.

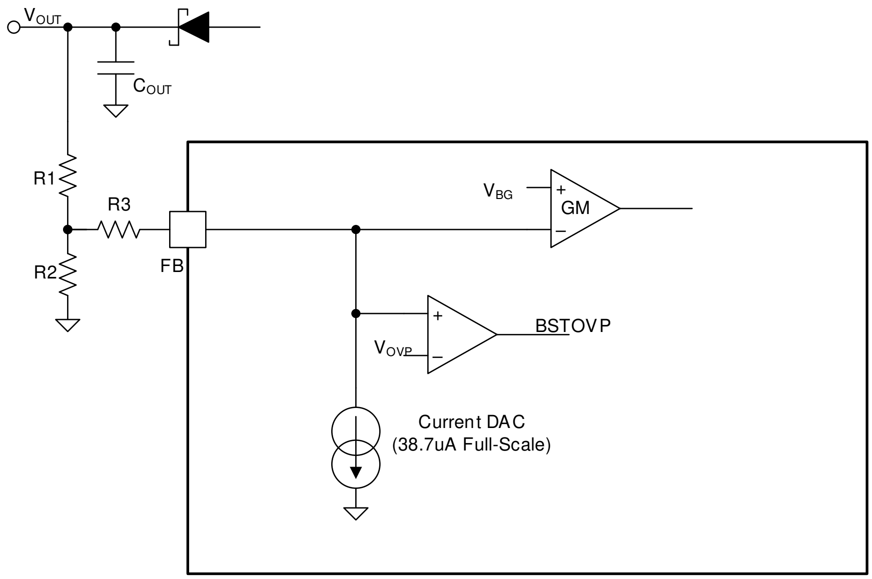


图 8-4. FB External T-divider Resistors

8.3.1.2.3 External Compensation

The device has internal compensation network to keep the DC-DC control loop in good stability in most cases. However, an additional external compensation network could also be added on FB-pin to offer more flexibility in loop design or solving some extreme use-cases.

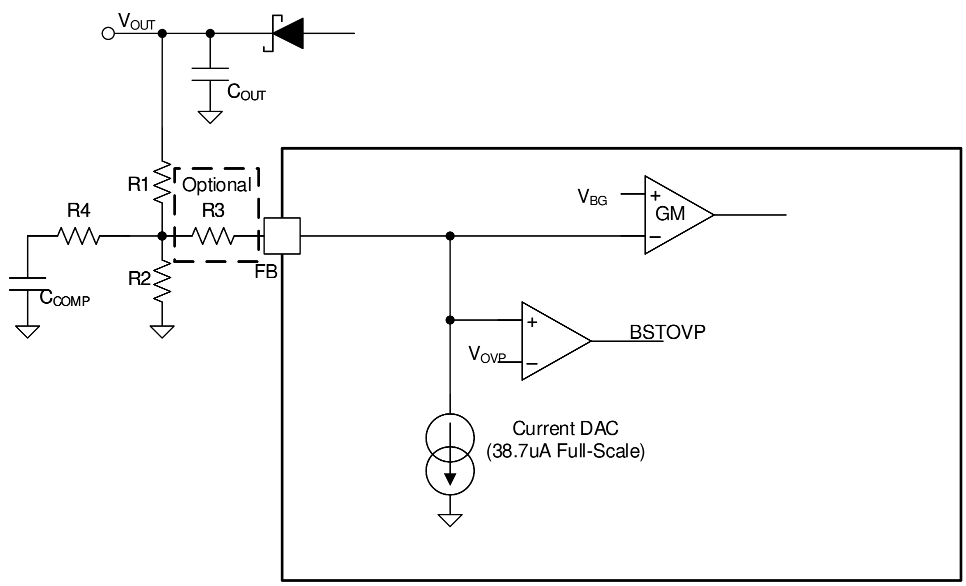


图 8-5. External Compensation Network

This network will create one additional pole and one additional zero in the loop.

$$f_{POLE\_COMP} = \frac{1}{2\pi[(R_1 \| R_2) + R_4]C_{COMP}}$$

$$f_{ZERO\_COMP} = \frac{1}{2\pi R_4 C_{COMP}}$$

It could be noted that R_3 doesn't take part in the compensation. So this external compensation network could be both used in two-divider netwrok and T-divider network with no equation change.

In real application, for example, when DC-DC loop has stability concern, putting the additional pole in 1 kHz and the additional zero in 2 kHz will suppress the loop gain by approximately 6dB after 2 kHz. This will benefit gain margin and phase margin a lot.

8.3.2 Internal LDO

The internal LDO regulator converts the input voltage at VIN to a 4.3-V output voltage for internal use. Connect a minimum of 1-µF ceramic capacitor from LDO pin to ground, as close to the LDO pin as possible.

8.3.3 LED Current Sinks

8.3.3.1 LED Output Configuration

TPS9238x detects LED output configuration during start-up. Any current sink output connected to ground is disabled and excluded from the adaptive voltage control of the DC-DC converter and fault detections.

If more current is needed, TPS9238x's output could also be connected together to support the high current LED.

8.3.3.2 LED Current Setting

The output current of the LED outputs is controlled with external R_{ISET} resistor. R_{ISET} value for the target LED current per channel can be calculated using 方程式 4:

$$I_{LED} = 2000 \times \frac{V_{BG}}{R_{ISET}} \tag{4}$$

where

- V_{BG} = 1.2 V
- R_{ISET} is current setting resistor, kΩ
- I_{LED} is output current per OUTx pin, mA

For example, if R_{ISET} is set to 20 kΩ, I_{LED} will be 120 mA per channel.

8.3.3.3 Brightness Control

TPS9238x controls the brightness of the display with conventional PWM. Output PWM directly follows the input PWM. Input PWM frequency can be in the range of 100 Hz to 20 kHz.

8.3.4 Fault Detections and Protection

The TPS9238x has fault detection for LED open and short, VIN input overvoltage protection (VIN_OVP), VIN undervoltage protection (VIN_UVLO), VIN overcurrent protection (VIN_OCP), Boost output overvoltage protection (BST_OVP), SW overvoltage protection (SW_OVP) and thermal shutdown (TSD).

8.3.4.1 Supply Fault and Protection

8.3.4.1.1 VIN Undervoltage Fault (VIN_UVLO)

The TPS9238x device supports VIN undervoltage protection. The VIN undervoltage falling threshold is 3.85-V typical and rising threshold is 4-V typical. If during operation of the TPS9238x device, the VIN pin voltage falls below the VIN undervoltage falling threshold, the boost, LED outputs, and power-line FET will be turned off, and the device will enter FAULT RECOVERY mode. The FAULT pin will be pulled low. The TPS9238x will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. VIN_UVLO fault detection is available in SOFT START, BOOST START, and NORMAL state.

8.3.4.1.2 VIN Overvoltage Fault (VIN_OVP)

The TPS9238x device supports VIN overvoltage protection. The VIN overvoltage threshold is 43-V typical. If during TPS9238x operation, VIN pin voltage rises above the VIN overvoltage threshold, the boost, LED outputs and the power-line FET will be turned off, and the device will enter FAULT RECOVERY mode. The FAULT pin will be pulled low. The TPS9238x will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. VIN_OVP fault detection is available in SOFT START, BOOST START and NORMAL state.

8.3.4.2 Boost Fault and Protection

8.3.4.2.1 Boost Overvoltage Fault (BST_OVP)

The TPS9238x device supports boost overvoltage protection. If during TPS9238x operation, the FB pin voltage exceeds the V_{FB_OVP} threshold, which is 2.3-V typical, the boost, LED outputs and the power-line FET will be turned off, and the device will enter FAULT RECOVERY mode. The FAULT pin will be pulled low. The TPS9238x will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. BST_OVP fault detection is available in NORMAL state.

Calculating back from FB pin voltage threshold to boost output OVP voltage threshold, the value is not a static threshold, but a dynamic threshold changing with the current target boost adaptive voltage:

$$V_{BOOST\_OVP} = V_{BOOST} + \left(\frac{R1}{R2} + 1\right) \times (V_{FB\_OVP} - V_{BG}) \tag{5}$$

where

- V_{BOOST} is the current target boost adaptive voltage, which in most time is the current largest LED string forward voltage among multiple strings + 0.9 V in steady state
- V_{FB_OVP} = 2.3 V
- V_{BG} = 1.2 V
- R_1 and R_2 is the resistor value of FB external network in *Using Two-Divider* and *Using T-Divider*

For example, if R_1 is set to 750 kΩ and R_2 is set to 130 kΩ, V_{BOOST} will report OVP when the boost voltage is 7.4 V above target boost voltage.

This equation holds true in both two-divider FB external network and T-divider FB external network.

8.3.4.2.2 SW Overvoltage Fault (SW_OVP)

Besides boost overvoltage protection, the TPS9238x supports SW pin overvoltage protection to further protect the boost system from overvoltage scenario. If during TPS9238x operation, the SW pin voltage exceeds the V_{SW_OVP} threshold, which is 49-V typical, the boost, LED outputs and the power-line FET are turned off, and the device will enter FAULT RECOVERY mode. The FAULT pin will be pulled low. The TPS9238x will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. SW_OVP fault detection is available in SOFT START, BOOST START and NORMAL state.

8.3.4.3 LED Fault and Protection (LED_OPEN and LED_SHORT)

Every LED current sink has 3 comparators for LED fault detections.

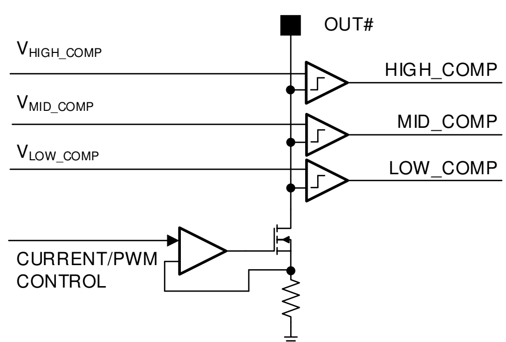


图 8-6. Comparators for LED Fault Detection

图 8-7 shows cases which generates LED faults. Any LED faults will pull the Fault pin low.

During normal operation, boost voltage is raised if any of the used LED outputs falls below the V_{LOW_COMP} threshold. Open LED fault is detected if boost output voltage has reached the maximum and at least one LED output is still below the threshold. The open string is then disconnected from the boost adaptive control loop and its output is disabled.

Shorted LED fault is detected if one or more LED outputs are above the V_{HIGH_COMP} threshold (typical 6 V) and at least one LED output is inside the normal operation window (between V_{LOW_COMP} and V_{MID_COMP}, typical 0.9 V and 1.9 V). The shorted string is disconnected from the boost adaptive control loop and its output is disabled.

LED Open fault detection and LED Short fault detection are available only in NORMAL state.

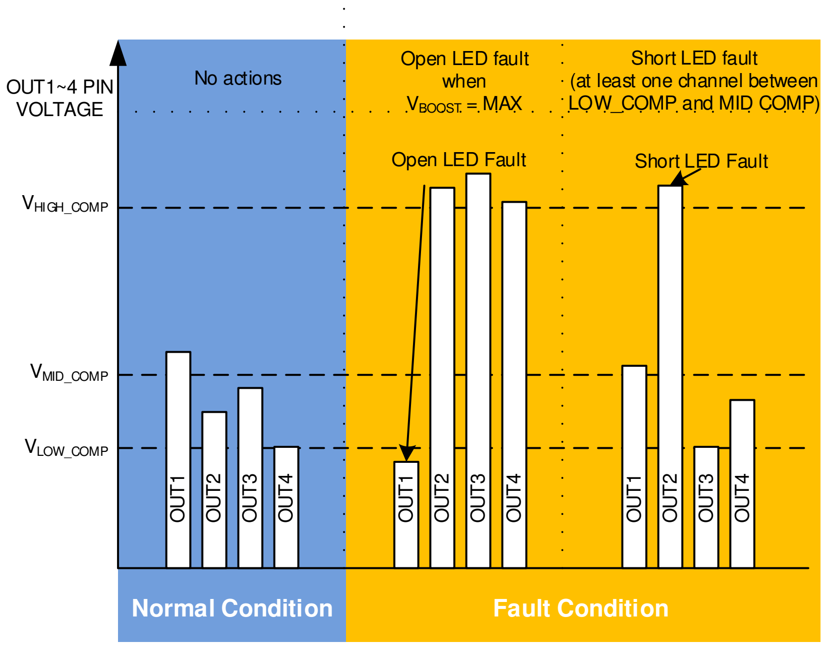


图 8-7. Protection and DC-DC Voltage Adaptation Algorithms

If LED fault is detected, the device continues normal operation and only the faulty string is disabled. The fault is indicated via the FAULT pin which can be released by toggling VDDIO/EN pin low for a short period of 2 µs to 20 µs. LEDs are turned off for this period but the device stays in NORMAL state. If VDDIO/EN is low longer, the device goes to STANDBY and restarts when EN goes high again.

This means if the system doesn't want to simply disable the device because of LED faults. It could clear the LED faults by toggling VDDIO/EN pin low for a short period of 2 µs to 20 µs.

8.3.4.4 Thermal Fault and Protection (TSD)

If the die temperature of TPS9238x reaches the thermal shutdown threshold T_{TSD}, which is 165°C typical, the boost, power-line FET and LED outputs are turned off to protect the device from damage. The FAULT pin will be pulled low. The TPS9238x will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. Only if the die temperature drops lower than T_{TSD} - T_{TSD_HYS}, which is 145°C typical, the device could start-up normally. TSD fault detection is available in SOFT START, BOOST START and NORMAL state.

8.3.4.5 Overview of the Fault and Protection Schemes

A summary of the TPS9238x fault detection behavior is shown in 表 8-3. Detected faults (excluding LED open or short) cause device to enter FAULT RECOVERY state. In FAULT_RECOVERY the DC-DC and LED current sinks of the device are disabled, and the FAULT pin is pulled low. The device will exit FAULT RECOVERY mode after 100 ms and try the start-up sequence again. When recovery is successful and device enters into NORMAL state, the FAULT pin is released high.

表 8-3. Fault Detections

FAULT/ PROTECTION	FAULT NAME	CONDITION	FAULT PIN	Enter FAULT_ RECOVERY STATE	ACTIVE STATE	ACTION
VIN overvoltage protection	VIN_OVP	VIN > 43 V	Yes	Yes	SOFT START, BOOST START, NORMAL	Device enters into FAULT RECOVERY state, and restarts after 100 ms.
VIN undervoltage protection	VIN_UVLO	Effective when VIN < 3.85 V Released when VIN > 4 V	Yes	Yes	SOFT START, BOOST START, NORMAL	Device enters into FAULT RECOVERY state, and restarts after 100 ms.
Open LED fault	LED _OPEN	Adaptive Voltage is max. and any OUTx voltage < 0.9 V	Yes	No	NORMAL	Open string is removed from the DC-DC voltage control loop and output is disabled. Fault pin low could be released by toggling VDDIO/EN pin, If VDDIO/EN is low for a period of 2 µs to 20 µs, LEDs are turned off for this period but device stays in NORMAL.
Shorted LED fault	LED_SHORT	One of OUTx voltage is [0.9 V, 1.9 V] and any OUTx voltage > 6 V	Yes	No	NORMAL	Short string is removed from the DC-DC voltage control loop and output is disabled. Fault pin low could be released by toggling VDDIO/EN pin, If VDDIO/EN is low for a period of 2 µs to 20 µs, LEDs are turned off for this period but device stays NORMAL.
Boost overvoltage protection	BST_OVP	V_{FB} > 2.3 V	Yes	Yes	NORMAL	Fault is detected if boost overvoltage condition duration is more than 560 ms. Device enters into FAULT RECOVERY state, and restarts after 100 ms.
SW overvoltage protection	SW_OVP	V_{SW} > 49 V	Yes	Yes	SOFT START, BOOST START, NORMAL	Device enters into FAULT RECOVERY state, and restarts after 100 ms.
Thermal protection	TSD	Effective when Tj > 165 °C Released when Tj < 145 °C	Yes	Yes	SOFT START, BOOST START, NORMAL	Device enters into FAULT RECOVERY state, and restarts until TSD fault is released.

8.4 Device Functional Modes

8.4.1 STANDBY State

The TPS9238x enters STANDBY state when the VIN voltage powers on and voltage is higher than VINUVLO rising threshold, which is 4-V typical. In STANDBY state, the device is able to detect VDDIO/EN signal. When VDDIO/EN is pulled high, the internal LDO wakes up and the device enters into SOFT START state. The device will re-enter the STANDBY state when VDDIO/EN is pulled low for more than 50 µs.

8.4.2 SOFT START State

In SOFT START state, VIN_OVP, VIN_UVLO, SW_OVP and TSD fault are active. After 65 ms, the device enters into BOOST START state.

8.4.3 BOOST START State

In BOOST START state, DC-DC controller is turned on and boost voltage is ramped to initial boost voltage level with reduced current limit. VIN_OVP, VIN_UVLO, SW_OVP and TSD fault are active in this state. After 50 ms, LED outputs do a one-time detection on grounded outputs. Grounded outputs are disabled and excluded from the adaptive voltage control loop. Then the device enters into NORMAL state.

8.4.4 NORMAL State

In NORMAL state, LED drivers are enabled when PWM signal is high. All faults are active in this state. Fault pin will be released high in the start of NORMAL state if recovering from FAULT RECOVERY state and no fault is available.

8.4.5 FAULT RECOVERY State

Non-LED faults can trigger fault recovery state. LED drivers and boost converter are both disabled. After 100 ms, the device attempts to restart from SOFT START state if VDDIO/EN is still high.

8.4.6 State Diagram and Timing Diagram for Start-up and Shutdown

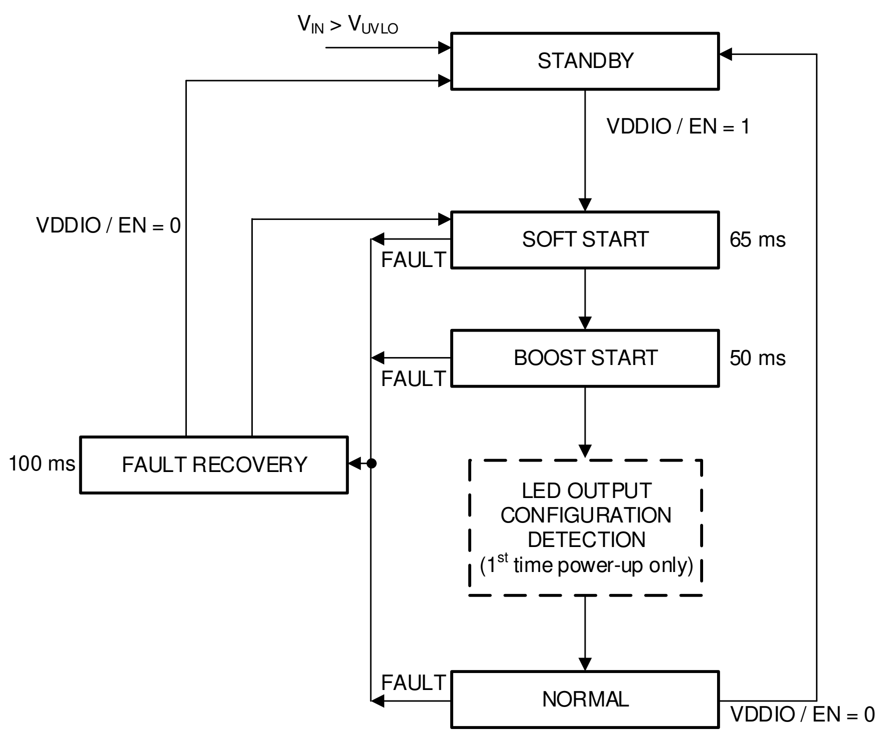


图 8-8. State Diagram

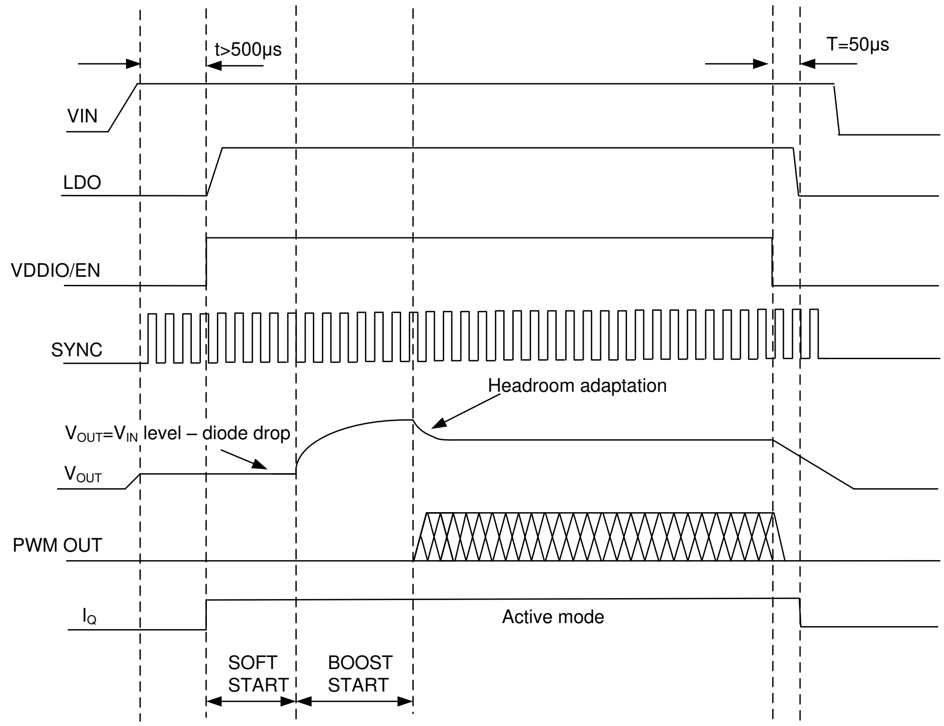


图 8-9. Timing Diagram for the Typical Start-Up and Shutdown

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS9238x is designed for medium power backlight applications. The input voltage (V_{IN}) is intended to be connected to the system DC supply directly, which supports voltage range from 4.5 V to 40 V. Device internal circuitry is powered from the integrated LDO.

The TPS9238x uses a simple four-wire control:

- VDDIO/EN for enable
- PWM input for brightness control
- SYNC pin for boost synchronisation (optional)
- FAULT output to indicate fault condition (optional)

9.2 Typical Applications

9.2.1 Typical Application for 4 LED Strings

图 9-1 shows the typical application for TPS9238x which supports 4 LED strings, 100 mA per string with a boost switching frequency of 400 kHz.

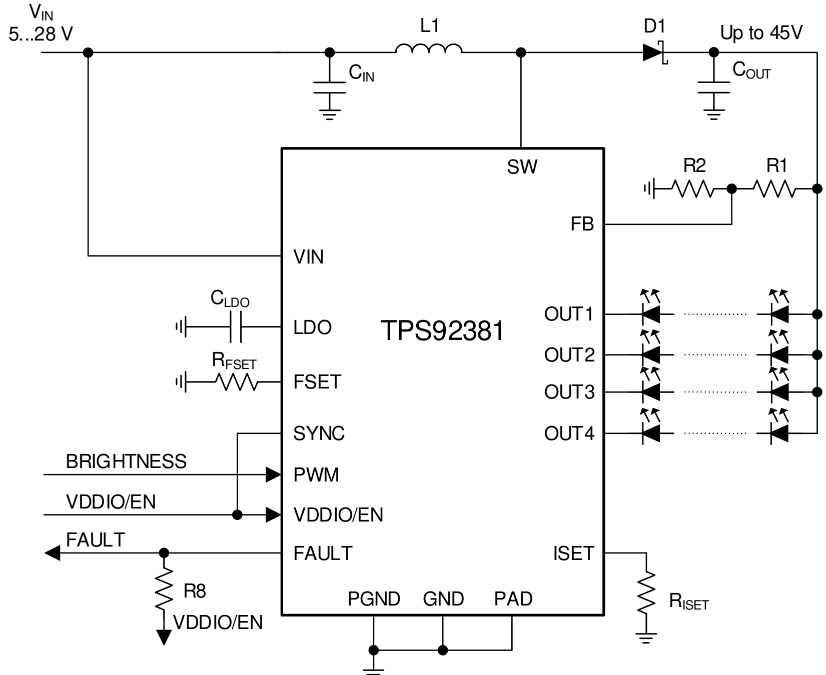


图 9-1. Four Strings 100 mA per String Configuration

9.2.2 Design Requirements

表 9-1. Design Requirements Table

DESIGN PARAMETER	VALUE
V_{IN} voltage range	5 V – 28 V
LED string	4P8S LEDs (30-V max)
LED string current	100 mA
Maximum boost voltage	34 V
Boost switching frequency	400 kHz
External boost sync	not used
Boost spread spectrum	enabled
L1	33 µH
C_{IN}	100 µF, 50 V
$C_{IN\ BOOST}$	2 × (10 µF, 50-V ceramic) + 33 µF, 50-V electrolytic
C_{OUT}	2 × (10 µF, 50-V ceramic) + 33 µF, 50-V electrolytic
C_{LDO}	1 µF, 10 V
R_{ISET}	24 kΩ
R_{FSET}	160 kΩ
R1	685 kΩ
R2	130 kΩ

9.2.3 Detailed Design Procedure

9.2.3.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor must not saturate, and the inductor current ripple must be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and are preferred. The saturation current must be greater than the sum of the maximum load current, and the worst case average-to-peak inductor current. 方程式 6 shows the worst case conditions

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE} \quad \text{For Boost}$$
$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$
$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1 - D) \tag{6}$$

- I_{RIPPLE} - peak inductor current
- I_{OUTMAX} - maximum load current
- V_{IN} - minimum input voltage in application
- L - min inductor value including worst case tolerances
- f - minimum switching frequency
- V_{OUT} - output voltage
- D - Duty Cycle for CCM Operation

As a result, the inductor should be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit. A saturation current rating of at least 4.1 A is recommended for most applications. See 表 8-2 for recommended inductance value for the different switching frequency ranges. The inductor's resistance should be less than 300 mΩ for good efficiency.

See detailed information in *Understanding Boost Power Stages in Switch Mode Power Supplies*.
Power Stage DesingerTool can be used for the boost calculation.

9.2.3.2 Output Capacitor Selection

A ceramic capacitor with 2 × $V_{MAX\ BOOST}$ or more voltage rating is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. If the selected ceramic capacitors' voltage rating is less than 2 × $V_{MAX\ BOOST}$, an alternative way is to increase the number of ceramic capacitors. Capacitance recommendations for different switching frequencies are shown in 表 8-2. To minimize audible noise of ceramic capacitors their physical size should typically be minimized.

9.2.3.3 Input Capacitor Selection

A ceramic capacitor with 2 × $V_{IN\ MAX}$ or more voltage rating is recommended for the input capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. If the selected ceramic capacitors' voltage rating is less than 2 × $V_{MAX\ BOOST}$, an alternative way is to increase the number of ceramic capacitors. Capacitance recommendations for different boost switching frequencies are shown in 表 8-2.

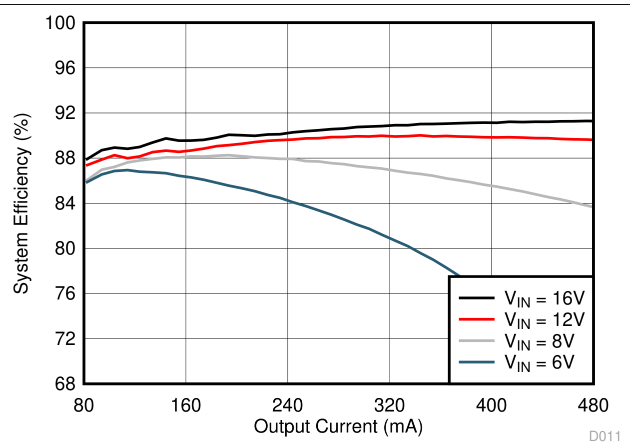
9.2.3.4 LDO Output Capacitor

A ceramic capacitor with at least 10-V voltage rating is recommended for the output capacitor of the LDO. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically a 1-µF capacitor is sufficient.

9.2.3.5 Diode

A Schottky diode should be used for the boost output diode. Do not use ordinary rectifier diodes, because slow switching speeds and long recovery times degrade the efficiency and the load regulation. Diode rating for peak repetitive current should be greater than inductor peak current (up to 4.1 A) to ensure reliable operation in boost mode. Average current rating should be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. Choose a reverse breakdown voltage of the Schottky diode significantly larger than the output voltage. The junction capacitance of Schottky diodes are also very important. Big junction capacitance leads to huge reverse current and big noise when boost is switching. A < 500-pF junction capacitance at V_R = 0.1 V Schottky diode is recommended.

9.2.4 Application Curves



Load 4 strings, V_{Boost} = 30 V f_{sw}=400 kHz, 22 μH

图 9-2. LED Backlight Efficiency

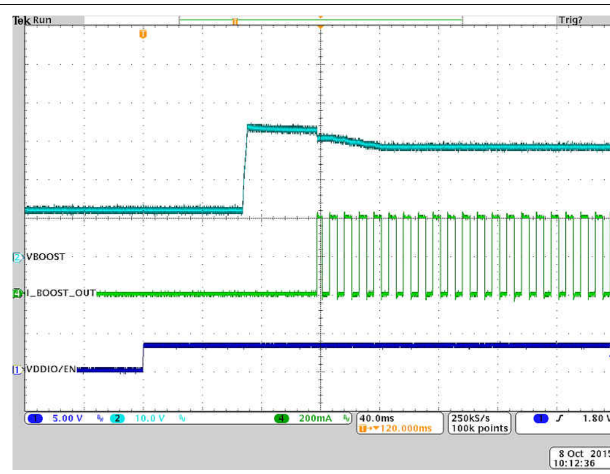


图 9-3. Typical Start-Up

9.2.5 SEPIC Mode Application

When LED string voltage can be above or below V_{IN} voltage, SEPIC configuration can be used. In this example, two separate coils or coupled coil could both be used for SEPIC. Separate coils can enable lower height external components to be used, compared to a coupled coil solution. On the other hand, coupled coil typically maximizes the efficiency. Also, in this example, an external clock is used to synchronize SEPIC switching frequency. External clock input can be modulated to spread switching frequency spectrum.

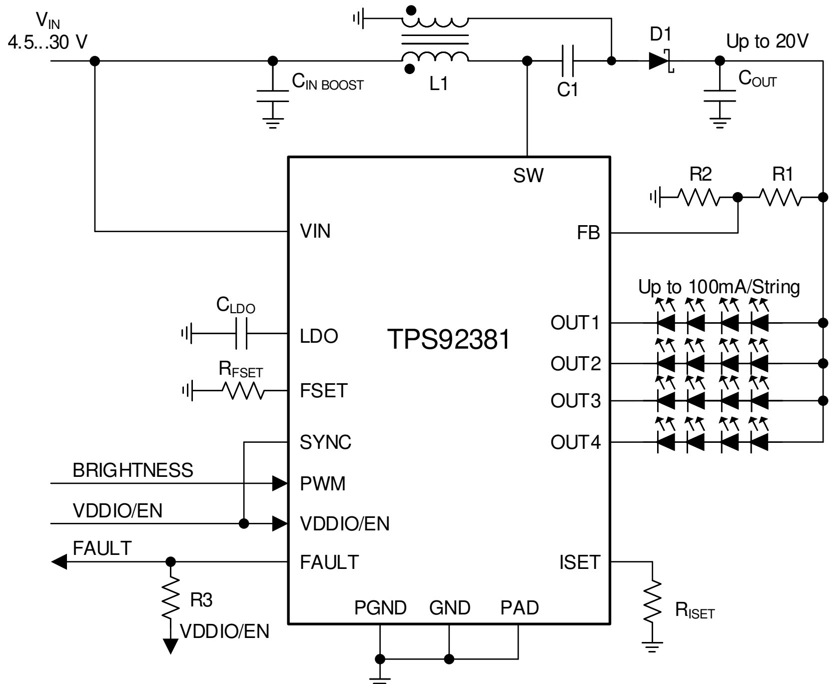


图 9-4. SEPIC Mode, 4 Strings 100 mA per String Configuration

9.2.5.1 Design Requirements

表 9-2. Design Requirements Table

DESIGN PARAMETER	VALUE
V_{IN} voltage range	4.5 V – 30 V
LED string	4P4S LEDs (15-V max)
LED string current	100 mA
Maxmum output voltage	20 V
SEPIC switching frequency	2.2 MHz
External sync for SEPIC	used
Spread spectrum	Internal spread spectrum disabled (external sync used)
L1, L2	4.7 µH
C_{IN}	10 µF 50 V
$C_{IN\ SEPIC}$	2 × 10 µF, 50-V ceramic + 33 µF, 50-V electrolytic
C1	10-µF 50-V ceramic
C_{OUT}	2 × 10 µF, 50-V ceramic + 33 µF, 50-V electrolytic
C_{LDO}	1 µF, 10 V
R_{ISET}	24 kΩ
R_{FSET}	24 kΩ
R1	265 kΩ
R2	37 kΩ
R3	10 kΩ

9.2.5.2 Detailed Design Procedure

In SEPIC mode the maximum voltage at the SW pin is equal to the sum of the input voltage and the output voltage. Because of this, the maximum sum of input and output voltage must be limited below 49 V. See the *Detailed Design Procedure* section for general external component guidelines. Main differences of SEPIC compared to boost are described below.

Power Stage Designer™ Tool can be used for modeling SEPIC behavior. For detailed explanation on SEPIC see Texas Instruments Analog Applications Journal *Designing DC/DC Converters Based on SEPIC Topology*.

9.2.5.2.1 Inductor

In SEPIC mode, currents flowing through the coupled inductors or the two separate inductors L1 and L2 are the input current and output current, respectively. Values can be calculated using *Power Stage Designer™ Tool* or using equations in *Designing DC/DC Converters Based on SEPIC Topology*.

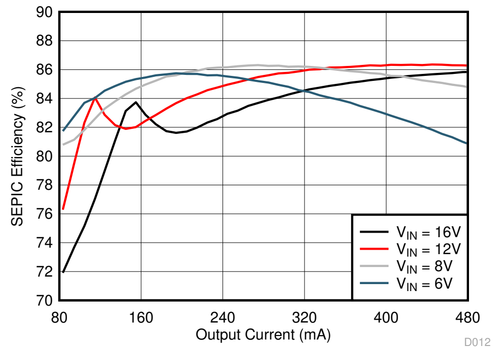
9.2.5.2.2 Diode

In SEPIC mode diode peak current is equal to the sum of input and output currents. Diode rating for peak repetitive current should be greater than SW pin current limit (up to 4.1 A for transients) to ensure reliable operation in boost mode. Average current rating should be greater than the maximum output current. Diode voltage rating must be higher than sum of input and output voltages.

9.2.5.2.3 Capacitor C1

TI recommends a ceramic capacitor with low ESR. Capacitor voltage rating must be higher than maximum input voltage.

9.2.5.3 Application Curves

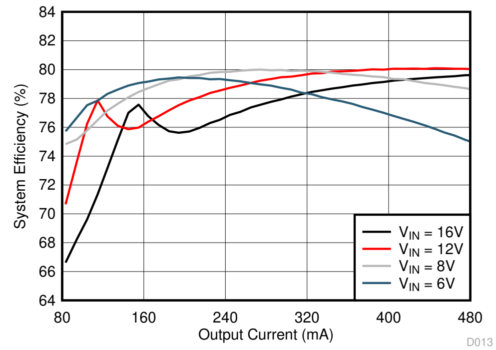


4 strings, 4 LEDs per string

f_{sw} = 2.2 MHz

IHCL-4040DZ-5A 4.7 μH

图 9-5. SEPIC Efficiency



4 strings, 4LEDs per string

f_{sw} = 2.2 MHz

IHCL-4040DZ-5A 4.7 μH

图 9-6. LED Backlight Efficiency

10 Power Supply Recommendations

The device is designed to operate from a direct DC supply. The resistance of the input supply rail must be low enough so that the input current transient does not cause a high drop at TPS9238x VIN pin. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to the ceramic bypass capacitors in the V_{IN} line.

11 Layout

11.1 Layout Guidelines

图 11-1 is a layout recommendation for TPS9238x used to demonstrate the principles of a good layout. This layout can be adapted to the actual application layout if or where possible. It is important that all boost components are close to the chip, and the high current traces must be wide enough. By placing boost components on one side of the chip it is easy to keep the ground plane intact below the high current paths. This way other chip pins can be routed more easily without splitting the ground plane. Bypass LDO capacitor must be placed as close as possible to the device.

Here are some main points to help the PCB layout work:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close as possible to the SW and PGND pins. Input and output capacitor grounds must be close to each other to minimize current loop size.
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High-frequency return currents find a route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the **positive** current route in the ground plane if the ground plane is intact under the route. To minimize the current loop for high frequencies:
    - The inductor's pin in SW node needs to be as near as possible to chip's SW pin.
    - Put a small capacitor as near as possible to the diode's pin in boost output node and arrange vias to PGND plane close to the capacitor's GND pin.
- Use separate power and noise-free grounds. PGND is used for boost converter return current and noise-free ground is used for more sensitive signals, such as LDO bypass capacitor grounding as well as grounding the GND pin of the device.
- Boost output feedback voltage to LEDs must be taken out *after* the output capacitors, not straight from the diode cathode.
- Place LDO 1-μF bypass capacitor as close as possible to the LDO pin.

- Input and output capacitors require strong grounding (wide traces, many vias to GND plane).

11.2 Layout Example

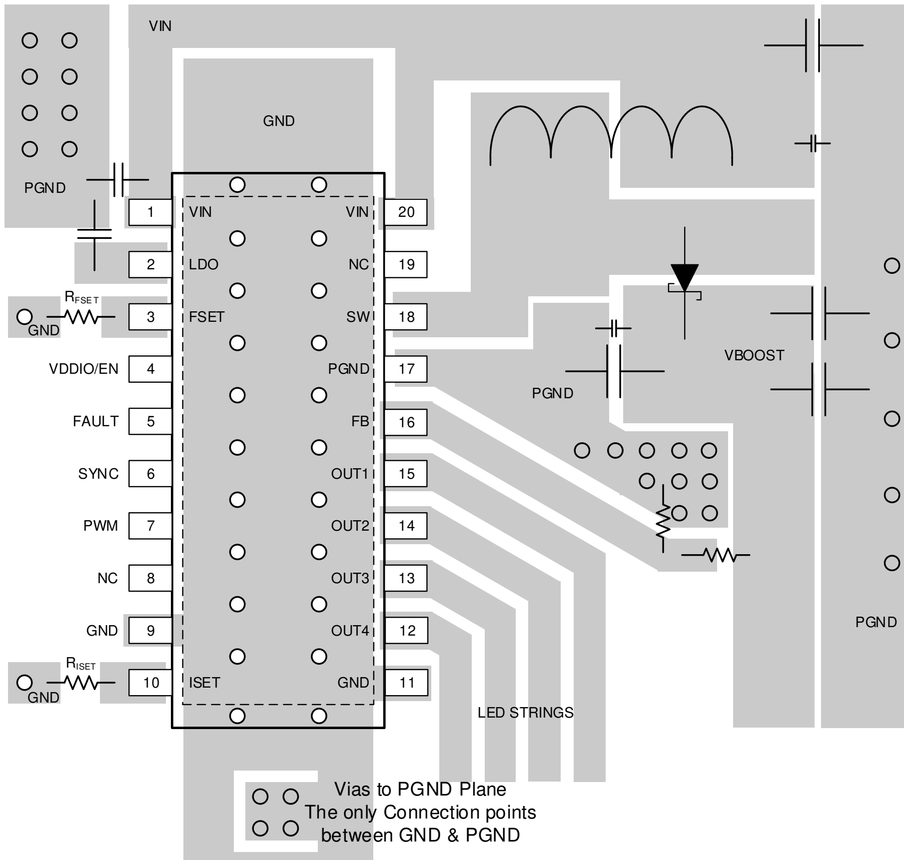


图 11-1. TPS9238x Boost Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Power Stage Designer™ Tool can be used for both boost and SEPIC: *Power Stage Designer™ Tool*

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package*
- *Understanding Boost Power Stages in Switch Mode Power Supplies*
- *Designing DC-DC Converters Based on SEPIC Topology*
- *TI E2E™ support forums*

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

Power Stage Designer™ is a trademark of TI.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92380PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	92830	Samples
TPS92381PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	92831	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

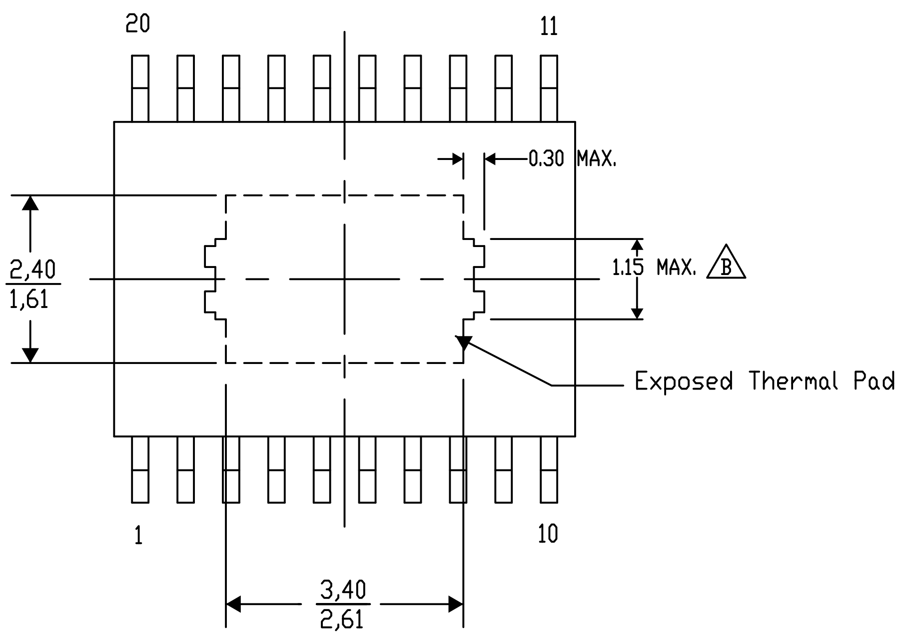
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

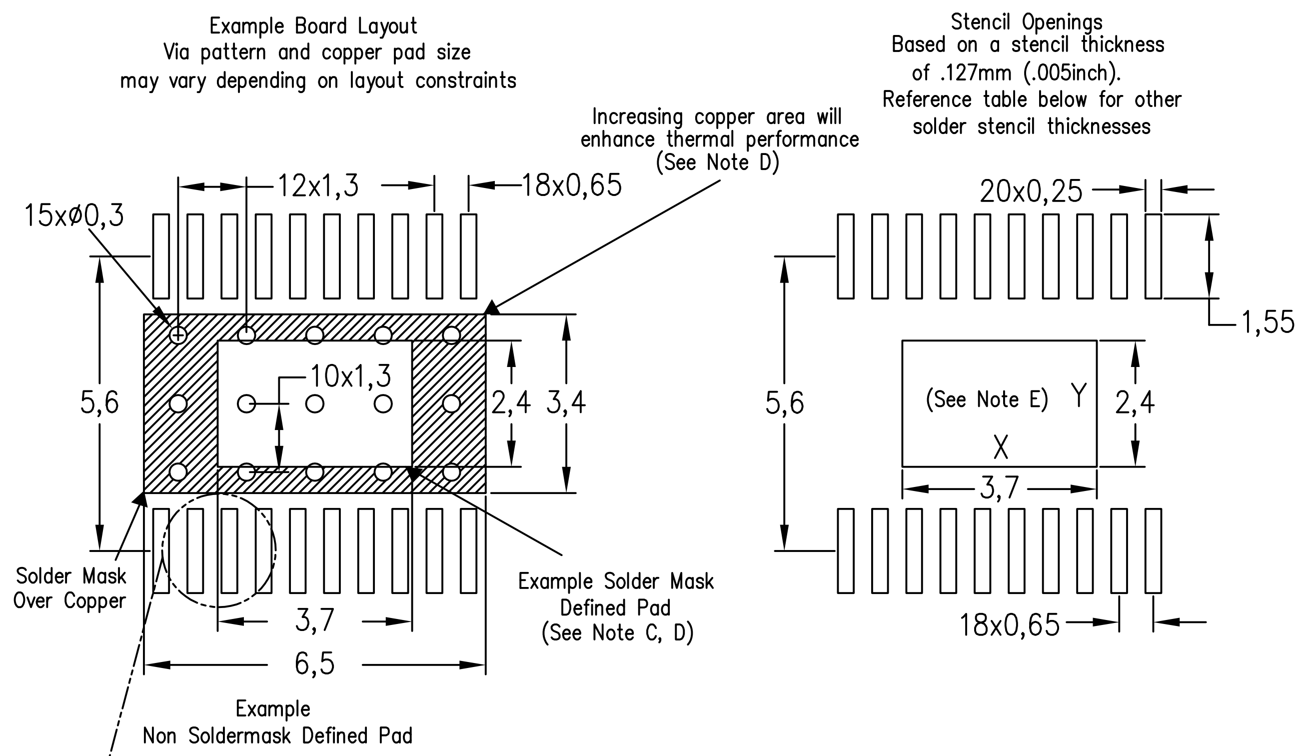
4206332-15/AO 01/16

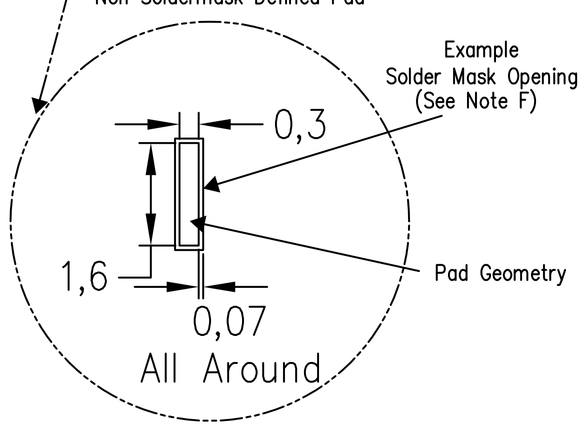
NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609-8/W 09/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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