具有 SPI 控制功能的 TPS92520-Q1 4.5V 至 65V、双路、1.6A 同步降压 LED 驱动器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 1 级：–40°C 至 125°C 的工作环境温度范围
  - 器件 HBM 分类等级 H1C
  - 器件 CDM 分类等级 C5
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 4.5V 至 65V 的宽输入电压范围
- 持续输出电流最高为 1.6A，且精度为 4%
- 自适应导通时间平均电流控制
- 可编程开关频率范围为 100kHz 至 2.2MHz
- 高级调光操作
  - 10 位精密模拟调光
  - 10 位精密内部 PWM 调光
  - 支持外部 PWM 调光输入
  - 为外部分流调光（包括 LED 矩阵管理器）而优化
- 开关逐周期过流保护
- 开关过热保护
- 串行外设接口 (SPI)
  - 可配置模拟基准、开关频率和 PWM 调光占空比
  - 故障监控和报告
- 支持跛行回家 (LH) 和独立模式运行

2 应用

- 汽车前照灯和自适应 LED 驱动模块

3 说明

TPS92520-Q1 是一款单片双路同步降压 LED 驱动器，具有 4.5V 至 65V 宽工作输入电压范围，可独立为两串串联的 LED 供电。TPS92520-Q1 实施自适应导通时间平均电流模式控制功能，经设计可与分流 FET 调光技术和基于 LED 矩阵管理器的动态光束前照灯兼容。自适应导通时间控制功能可提供近乎恒定的开关频率，频率设置范围为 100kHz 至 2.2MHz。电感器电流感应和闭环反馈功能可在较宽的输入电压、输出电压和环境温度范围内实现 ±4% 以上的精度。

高性能 LED 驱动器可使用模拟调光或 PWM 调光技术来单独调制 LED 电流。通过 SPI 对 10 位 IADJ 数值进行编程可获得高于 16:1 的线性模拟调光响应。通过借助所需占空比直接调制相应的 UDIM 输入引脚或通过启用内部 PWM 发生器电路，来实现 LED 电流的 PWM 调光。通过比较 10 位 PWM 寄存器与可编程数字计数器的数值，PWM 发生器可将 10 位 PWM 寄存器值转化为相应的占空比。

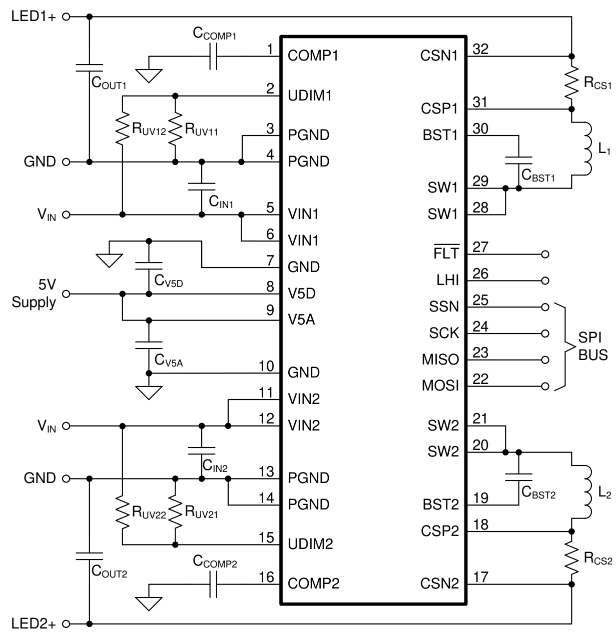
TPS92520-Q1 整合了高级 SPI 可编程诊断和故障保护功能，其中涉及：逐周期电流限制、自举欠压保护、LED 开路、LED 短路、热警告和热关断功能。板载 10 位 ADC 对监测和诊断系统运行状况所需的重要输入参数进行采样。

TPS92520-Q1 采用 8.1mm x 11mm 热增强型 32 引脚 HTSSOP 封装（具有 2.75mm x 3.45mm 的顶部外露散热焊盘和底部外露散热焊盘）。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
TPS92520-Q1	HTSSOP	8.1mm × 11mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (June 2020) to Revision D (February 2021) — **Page**

- 更新了整个文档的表、图和交叉参考的编号格式 ... 1
- Updated the minimum on-time specification from 90-ns typical to 105-ns typical ... 5
- Added "SWx to PGND (< 10 µs)" row to *Absolute Maximum Ratings* table ... 5
- Added "CSPx to CSNx (< 100 µs)" row to *Absolute Maximum Ratings* table ... 5
- Updated $t_{ONx(MIN)}$ MIN value from "75" to "87" ... 5
- Updated $t_{ONx(MIN)}$ TYP value from "90" to "105" ... 5
- Updated $t_{ONx(MIN)}$ MAX value from "105" to "123" ... 5
- Updated 图 6-17 ... 10
- Updated the *Functional Block Diagram* ... 15
- Updated "90 ns" to 105 ns" in *Minimum On-Time, Off-Time, and Inductor Ripple* section ... 17
- Updated "1.24 V" to "1.22 V" in the *External PWM Dimming and Input Undervoltage Lockout* section ... 19
- Updated "!~ 220 µA" to "10 µA" in the *External PWM Dimming and Input Undervoltage Lockout* section ... 19
- Updated "2.8 V" to "2.95 V" in the BSTx Undervoltage Lockout description ... 23
- Updated "2.8 A" to "2.7 A" in the High-Side Switch Current Limit description ... 23
- Updated "2.5 A" to "1.5 A" in the Low-Side Switch Current Limit description ... 23
- Updated "4 ms" to "3.6 ms" in the *Faults and Diagnostics* section ... 23
- Updated "32 ms" to "28.8 ms" in the *Faults and Diagnostics* section ... 23

Changes from Revision B (May 2020) to Revision C (June 2020) — **Page**

- 增加了 DAP 封装 ... 1

Changes from Revision A (January 2020) to Revision B (May 2020) — **Page**

- 将器件状态从“预告信息”更改为“量产数据” ... 1

5 Pin Configuration and Functions

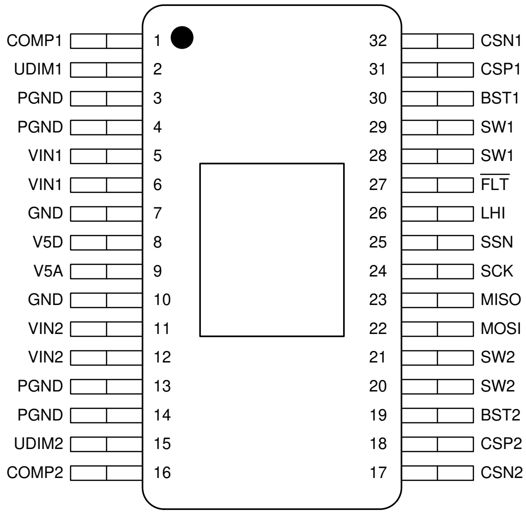


图 5-1. DAD Package 32-Pin HTSSOP (Top-Exposed PAD) Top View

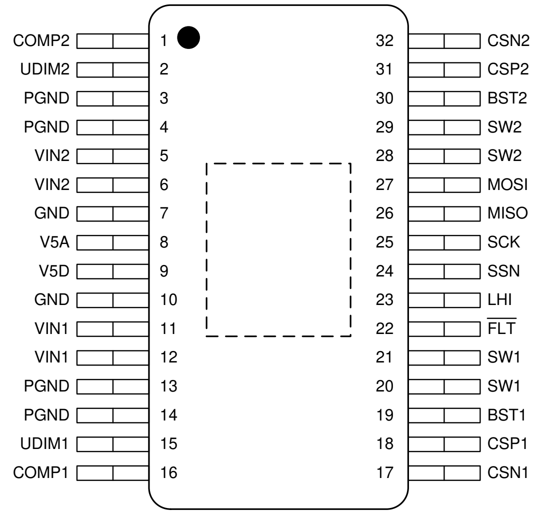


图 5-2. DAP Package 32-Pin HTSSOP (Top-Exposed PAD) Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DAD	DAP		
BST1	30	19	P	Supply input for high-side MOSFET gate drive circuit. Connect a ceramic capacitor between BSTx and SWx pins. An internal diode is connected between V5D and BSTx.
BST2	19	30	P	
COMP1	1	16	I/O	Output of internal transconductance error amplifier. Connect an integral compensation network to ensure stability.
COMP2	16	1	I/O	
CSN1	32	17	I	Negative input (–) of internal rail-to-rail transconductance error amplifier. Connect directly to the negative node of the LED current sense resistor, R_{CS}.
CSN2	17	32	I	
CSP1	31	18	I	Positive input (+) of internal rail-to-rail transconductance error amplifier. Connect directly to the positive node of the LED current sense resistor, R_{CS}.
CSP2	18	31	I	
FLT	27	22	O	Open-drain fault indicator. Connect to V5D with a resistor to create an active low fault signal output.
GND	7, 10	7, 10	G	Signal ground. Return for the internal voltage reference and analog circuits. Connect to circuit ground to complete return path.
LHI	26	23	I	Limp-home and standalone mode LED current reference set point. The voltage can be used instead of SPI registers to set LED current. The operation is configured through the LHCFG1 register. Setting voltage below 148 mV disables both channels and setting the voltage above 200 mV enables both channels.
MISO	23	26	O	Open-drain SPI slave data output. Connect a 4.7-kΩ resistor to V5D digital supply voltage.
MOSI	22	27	I	SPI slave data input
PGND	3, 4, 13, 14	3, 4, 13, 14	G	Ground returns for low-side MOSFETs
SCK	24	25	I	SPI clock input
SSN	25	24	I	SPI chip select input
SW1	28, 29	20, 21	P	Switching output of the regulator. Internally connected to both power MOSFETs. Connect to the power inductor.
SW2	20, 21	28, 29	P	

表 5-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	NO.			
	DAD	DAP		
UDIM1	2	15	I	Undervoltage lockout and external PWM dimming input. Connect to VIN through a resistor divider to implement input undervoltage protection. Diode couple external PWM signal to enable dimming. Do not float.
UDIM2	15	2	I	
V5A	9	8	P	Analog supply voltage. Locally decouple to GND using a 100-nF to 1-µF ceramic capacitor located close to the controller.
V5D	8	9	P	Digital supply voltage. Locally decouple to GND using a 2.2-µF to 4.7-µF ceramic capacitor located close to the controller.
VIN1	5, 6	11, 12	P	Power inputs and connections to high-side MOSFET drain node. Connect to the power supply and bypass capacitors C_{IN}. The path from the VIN pin to high frequency bypass C_{IN} and PGND must be as short as possible.
VIN2	11, 12	5, 6	P	

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage	V5A, V5D to GND	–0.3	5.5	V
Boot voltage	BSTx to SWx	–0.3	5.5	V
	BSTx to PGND	–0.3	70	V
Switch node voltage	SWx to PGND	–0.5	65	V
	SWx to PGND (< 10 µs)	–0.75		V
	SWx to PGND (< 10 ns)	–3.5		V
Drain node voltage	VINx to PGND	–0.3	65	V
Current	CSNx to VINx (< 10 µs)		1.5	A
	GND to CSPx, GND to CSNx (< 10 µs)		430	mA
Inputs	CSNx - VINx		0.5	V
	CSPx, CSNx to GND	–0.5	65	V
	CSPx to CSNx	–0.3	0.3	V
	CSPx to CSNx (< 100 µs)	–0.5	0.5	V
	UDIMx to GND	–0.3	60	V
	COMPx, LHI to GND	–0.3	5.5	V
	MOSI, SCK, SSN to GND	–0.3	5.5	V
Outputs	MISO, $\overline{\text{FLT}}$ to GND	–0.3	5.5	V
Junction temperature	T_J		150	°C
Lead temperature	Soldering, 10 s		260	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 16, 17, and 32)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	4.5		63	V
V_{5A}, V_{5D}	Bias supply	4.5	5	5.3	V
$\Delta V_{(CSP-CSN)}$	Sensed inductor current ripple	20			mV
dv_{CSP}/dt	CSP slew-rate			5	V/µs
I_{LED}	LED current			1.6	A
f_{SW}	Switching frequency	100		2200	kHz

6.3 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{UDIM}	External PWM dimming frequency			1000	Hz
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		DEVICE		UNIT
		DAD (HTSSOP)	DAP (HTSSOP)	
		32	32	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2] [3]	56.7	26.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.8	16.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.1	8.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	27.8	8.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The package thermal impedance is calculated in accordance with JESD51-7 standard with a 4-layer board and 2 W power dissipation.
(3) A heatsink or airflow would yield a much better $R_{\theta JA}$.

6.5 Electrical Characteristics

-40°C ≤ T_J ≤ 150°C, V_{5D} = V_{5A} = 5 V, V_{IN} = 24 V, V_{UDIMx} = 5 V, C_{V5D} = C_{V5A} = 4.7 µF C_{BSTx} = 0.1 µF, C_{COMPx} = 1 nF, R_{CSx} = 100 mΩ, no load on SWx, LHI pin floating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL ANALOG AND GATE DRIVE SUPPLIES (V5D, V5A)						
$V_{V5D,A(UVLO)}$	V_{5D} and V_{5A} UVLO threshold	Rising		4.10	4.26	V
		Falling	3.84	4.00		V
		Hysteresis		100		mV
$I_{V5A(STBY)}$	Analog supply stand-by current	V_{UDIM1} = V_{UDIM2} = 0 V		4	5	mA
$I_{V5D(STBY)}$	Gate drive supply stand-by current	V_{UDIM1} = V_{UDIM2} = 0 V		0.9	1.3	mA
$I_{V5A(SLEEP)}$	Analog supply sleep state current			16	300	nA
$I_{V5D(SLEEP)}$	Gate drive supply sleep state current			17	24	µA
$I_{VINx(SLEEP)}$	VIN pin sleep state current	V_{INx} = 15 V		2	4	µA
$I_{V5D(SW)}$	Gate drive supply switching current	V_{V5D} = 5 V, f_{SW} = 1 MHz, CH1 and CH2 switching		12	20	mA
HIGH-SIDE FET (SWx, BOOTx)						
$R_{DSx(ON-HS)}$	High-side MOSFET on resistance	V_{INx} = 6 V, V_{BSTx} = 11 V, I_{HSx} = 100 mA		227	440	mΩ
$V_{BSTx(UV)}$	Bootstrap UVLO threshold	Falling, V_{INx} = 6 V, V_{SWx} = 0 V	2.60	2.95	3.30	V
		Hysteresis, V_{INx} = 6 V, V_{SWx} = 0 V	120	184	250	mV
$I_{Q(xBST)}$	Bootstrap pin quiescent current	V_{BSTx} = 5 V, V_{SWx} = 0 V	200	250	300	µA
LOW-SIDE FET (SWx)						
$R_{DSx(ON-LS)}$	Low-side MOSFET on resistance	V_{INx} = 6 V, I_{LSx} = 100 mA		227	440	mΩ
HIGH-SIDE FET CURRENT LIMIT						
$I_{HSx(ILIM)}$	High-side current limit threshold	V_{INx} = 6 V	2.1	2.7	3.5	A

6.5 Electrical Characteristics (continued)

-40°C ≤ T_J ≤ 150°C, V_{5D} = V_{5A} = 5 V, V_{IN} = 24 V, V_{UDIMx} = 5 V, C_{V5D} = C_{V5A} = 4.7 µF C_{BSTx} = 0.1 µF, C_{COMPx} = 1 nF, R_{CSx} = 100 mΩ, no load on SWx, LHI pin floating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HSx(LEB)}$	High-side current sense leading-edge blanking period	V_{INx} = 6 V	35	60	80	ns
$t_{HSx(RES)}$	Current limit response time	V_{INx} = 6 V		20		ns
LOW-SIDE FET CURRENT LIMIT						
$I_{LSx(ILIM)}$	Low-side sinking current limit threshold	V_{INx} = 6 V	1.00	1.50	2.15	A
$t_{LSx(LEB)}$	Low-side current sense leading-edge blanking period	V_{INx} = 6 V		76		ns
OSCILLATOR						
f_{OSC}	Oscillator frequency		9.2	10.8	12.4	MHz
ANALOG TO DIGITAL CONVERTER (VDD, VIN1, VIN2, VCSN1, VCSN2, LHI, TEMP)						
t_{CONV}	ADC conversion time			18		µs
$V_{ADC(FS)}$	ADC full scale		2.38	2.45	2.52	V
q_{ADC}	ADC LSB			2.4		mV
ADC_{INL}	Integral nonlinearity		–2		2	LSB
ADC_{DNL}	Differential nonlinearity		–2		2	LSB
q_{TEMP}	Temperature LSB			1.4		count
ADC_{TEMP}	ADC measurement output	T_J = 25 °C		414		count
		T_J = 125 °C		553		count
K_{VINx}	VINx sense resistor divider ratio			0.037		
K_{V5D}	V5D sense resistor divider ratio			0.45		
K_{LHI}	LHI sense resistor divider ratio			1		
ANALOG ADJUST SETTING AND CURRENT SENSE AMPLIFIER (CSPx, CSNx)						
$V_{DACx(FS)}$	DAC full scale		2.38	2.45	2.52	V
q_{DAC}	DAC resolution		2.33	2.40	2.47	mV
$DACx_{INL}$	Integral nonlinearity		–1		1	LSB
$DACx_{DNL}$	Differential nonlinearity	CHxADJ stepped (63-64, 127-128, 255-256, 511-512, 1022-1023)	–0.85		0.85	LSB
$V_{(CSPx-CSNx)}$	Current sense threshold	V_{CSPx} = 6 V, ILED_REF_DACx = 1023	167.5	173.0	178.5	mV
		V_{CSPx} = 6 V, ILED_REF_DACx = 512	83.0	88.5	94.0	mV
		V_{CSPx} = 6 V, ILED_REF_DACx = 192	29.0	34.5	40.0	mV
		V_{CSPx} = 6 V, ILED_REF_DACx = 63	6.5	12.5	18.5	mV
$g_{mx(LV)}$	Level shift amplifier transconductance	V_{INx} = 63 V, V_{CSNx} = 5 V		50		µA/V
$V_{CSPx(SHT)}$	Output short circuit detection threshold	Rising		2.65		V
		Falling		2.45		V
VALLEY CURRENT COMPARATOR (CSPx, CSNx)						
$V_{VALx(OS)}$	Systematic comparator offset voltage	V_{CSNx} < 2.4 V		17		mV
ON-TIME GENERATOR						
$t_{ONx(MIN)}$	Minimum on-time.	V_{INx} = 4.5 V	87	105	123	ns

6.5 Electrical Characteristics (continued)

-40°C ≤ T_J ≤ 150°C, V_{5D} = V_{5A} = 5 V, V_{IN} = 24 V, V_{UDIMx} = 5 V, C_{V5D} = C_{V5A} = 4.7 µF C_{BSTx} = 0.1 µF, C_{COMPx} = 1 nF, R_{CSx} = 100 mΩ, no load on SWx, LHI pin floating (unless noted otherwise)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ONx}	Programmed on-time	V_{INx} = 50 V, V_{CSPx} = 38 V, tonx_DAC = 39	295	375	460	ns
		V_{INx} = 50 V, V_{CSPx} = 25 V, tonx_DAC = 7	900	1155	1400	ns
OFF-TIME GENERATOR						
$t_{OFFx(MIN)}$	Minimum off-time	V_{INx} = 4.5 V	44	57	68	ns
PWM DIMMING and PROGRAMMABLE UVLO INPUT (DIMx)						
$V_{UDIMx(EN)}$	UDIM input threshold	Rising		1.22	1.27	V
		Falling	1.075	1.120		V
$I_{UDIMx(UVLO)}$	UDIM source current (UVLO hysteresis)	V_{UDIMx} = 1.5 V	8	10	12	µA
ERROR AMPLIFIER (COMPx)						
g_M	Transconductance	V_{INx} = 63 V		450		µA/V
$I_{COMPx(SRC)}$	COMPx current source capacity	V_{INx} = 63 V, $V_{(CSPx-CSNx)}$ = 0 V, CHxIADJ = 578		45		µA
$I_{COMPx(SINK)}$	COMPx current sink capacity	V_{INx} = 63 V, $V_{(CSPx-CSNx)}$ = 200 mV, CHxIADJ = 578		45		µA
$EA_{x(BW)}$	Bandwidth	Unity gain		3		MHz
$EA_{(VD)}$	Input differential sense range		–225		225	mV
$EA_{(CM)}$	Input common mode range	V_{INx} = 63 V	0		V_{INx} – 0.5	V
$I_{COMPx(LKG)}$	COMPx leakage current	V_{UDIMx} = 0 V		2.5		nA
$V_{COMPx(ST)}$	COMPx startup threshold	Rising		2.45		V
		Hysteresis		250		mV
$V_{COMPx(OV)}$	COMPx over-voltage detection threshold	Rising	3.0	3.2		V
		Hysteresis		60		mV
$R_{COMPx(DCH)}$	COMPx discharge FET resistance			230		Ω
$V_{COMPx(RST)}$	Reset voltage	Falling		100		mV
LIMP HOME CURRENT SET POINT (LHI)						
I_{LHI}	Source current	V_{IN} = 6 V	8	10	12	µA
$V_{LHI(SD)}$	Shutdown threshold	Rising, V_{IN} = 6 V	174	200	227	mV
		Falling, V_{IN} = 6 V	119	148	176	mV
FAULT INDICATOR ($\overline{FLT}$)						
$R_{(\overline{FLT})}$	Fault pin pull-down resistance			3	7	Ω
T_{OC}	Hiccup retry delay time			3.6		ms
SERIAL PERIPHERAL INTERFACE (MOSI, MISO, SCK, SSN)						
$V_{OL-MISO}$	Output low voltage threshold	I_{MISO} = 10 mA		0.5		V
$R_{DS-MISO}$		I_{MISO} = 10 mA		50		Ω
$V_{INPUT(RISE)}$	Logic threshold (SSN, SCK, MOSI)	Rising			1.8	V
$V_{INPUT(FALL)}$		Falling	0.8			V
t_{SS-SU}	SSN setup time	Falling edge of SSN to 1st SCK rising edge	500			ns
t_{SS-H}	SSN hold time	Falling edge of 16th SCK to SSN rising edge	250			ns
t_{SS-HI}	SSN high time	Time SSN must remain high between transactions	1000			ns
t_{SCK}	SCK period	Clock period	500			ns

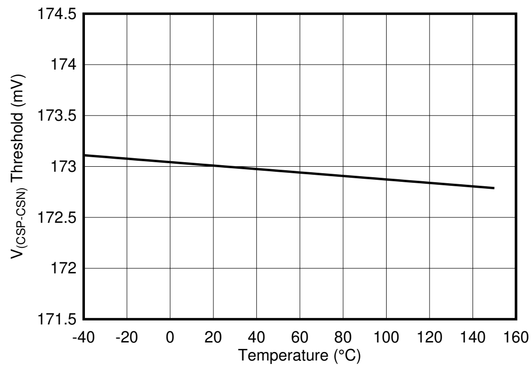
6.5 Electrical Characteristics (continued)

-40°C ≤ T_J ≤ 150°C, V_{5D} = V_{5A} = 5 V, V_{IN} = 24 V, V_{UDIMx} = 5 V, C_{V5D} =C_{V5A} = 4.7 µF C_{BSTx} = 0.1 µF, C_{COMPx} = 1 nF, R_{CSx} = 100 mΩ, no load on SWx, LHI pin floating (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D_{SCK}	SCK duty cycle	Clock duty cycle	40		60	%
t_{SU}	MOSI setup time	MOSI valid to rising edge SCK	125			ns
t_H	MOSI hold time	MOSI valid after rising edge SCK	140			ns
t_{HI_Z}	MISO tri-state time	Time to tri-state MISO after SSN rising edge	110		320	ns
t_{MISO_HL}	MISO valid high-to-low	Time to place valid "0" on MISO after falling SCK edge			320	ns
t_{MISO_LH}	MISO valid low-to-high	Time to tri-state MISO after falling SCK edge			320+t_{RC}	ns
t_{ZO_HL}	MISO drive time high-to-low	SSN Falling Edge to MISO falling			320	ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			175		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			16		°C

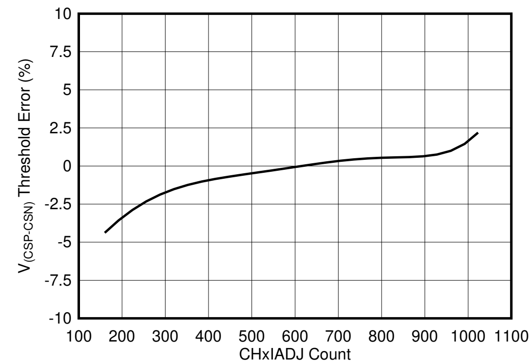
6.6 Typical Characteristics

$T_A = T_J = 25°C$, $V_{5D} = V_{5A} = 5$ V, $V_{IN} = 24$ V, $V_{UDIMx} = 5$ V, $C_{V5D} = C_{V5A} = 4.7$ µF $C_{BSTx} = 0.1$ µF, $C_{COMPx} = 1$ nF, $R_{CSx} = 100$ mΩ, no load on SWx, LHI pin floating (unless otherwise noted)



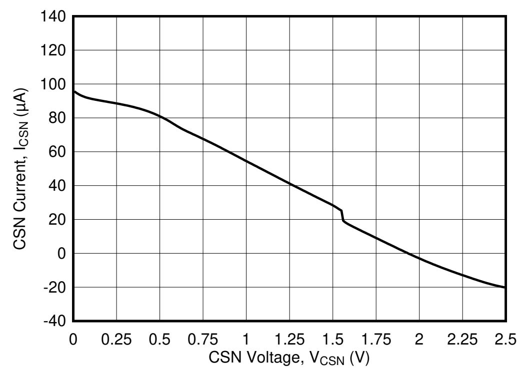
$V_{CSN} = 3$ V

图 6-1. $V_{(CSP-CSN)}$ Current Sense Threshold vs Temperature



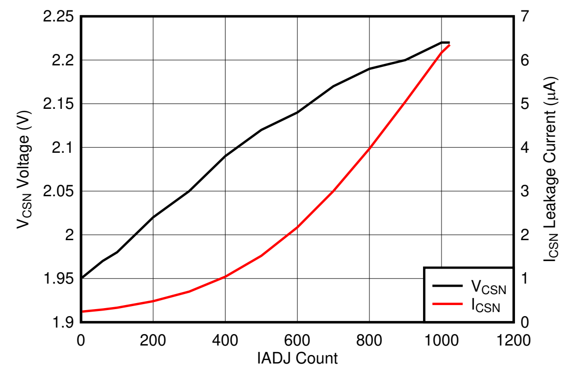
$V_{CSN} = 3$ V $V_{IN} = 60$ V

图 6-2. $V_{(CSP-CSN)}$ Current Sense Error vs IADJ Count



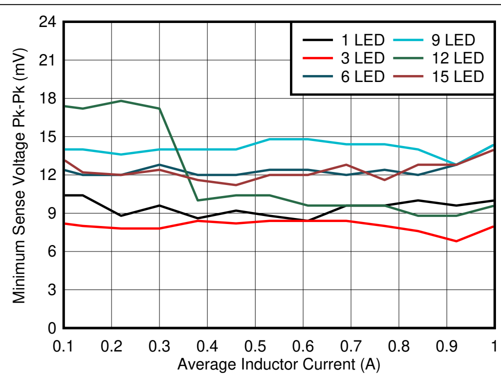
CHxEN = 0, CHxIADJ = 0 0 V < V_{CSN} < 2.5 V

图 6-3. CSN Source Current vs CSN Voltage



ChxEN = 0

图 6-4. CSN Voltage and Leakage Current vs IADJ Count



L = 68 µH $V_{IN} = 60$ V

图 6-5. Minimum Ripple Voltage vs Average Inductor Current

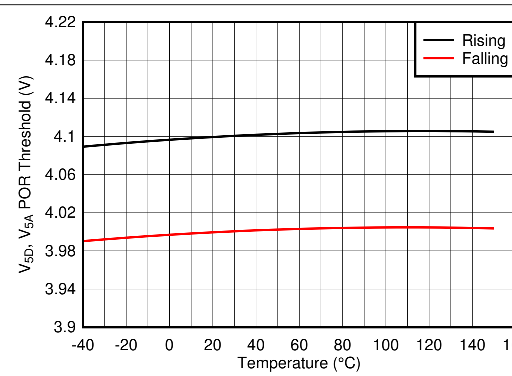


图 6-6. $V_{5D,A}$ POR Threshold vs Temperature

6.6 Typical Characteristics (continued)

$T_A = T_J = 25°C$, $V_{5D} = V_{5A} = 5$ V, $V_{IN} = 24$ V, $V_{UDIMx} = 5$ V, $C_{V5D} = C_{V5A} = 4.7$ µF $C_{BSTx} = 0.1$ µF, $C_{COMPx} = 1$ nF, $R_{CSx} = 100$ mΩ, no load on SWx, LHI pin floating (unless otherwise noted)

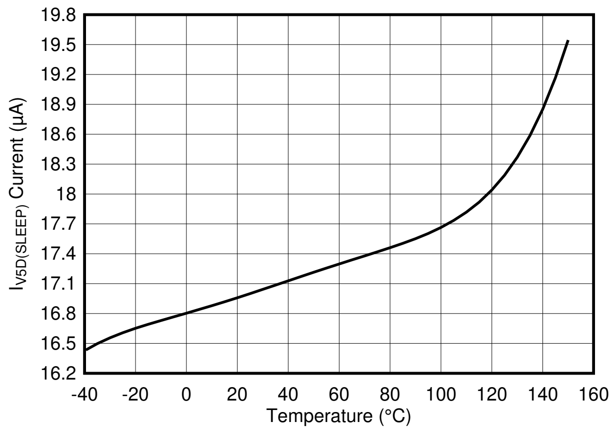


图 6-7. V5D Sleep Current vs Temperature

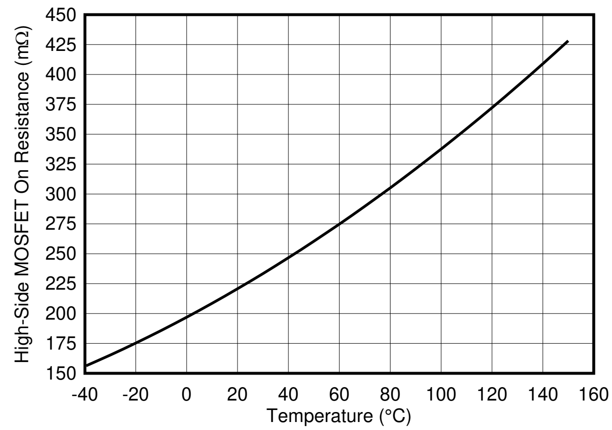


图 6-8. High Side MOSFET On Resistance vs Temperature

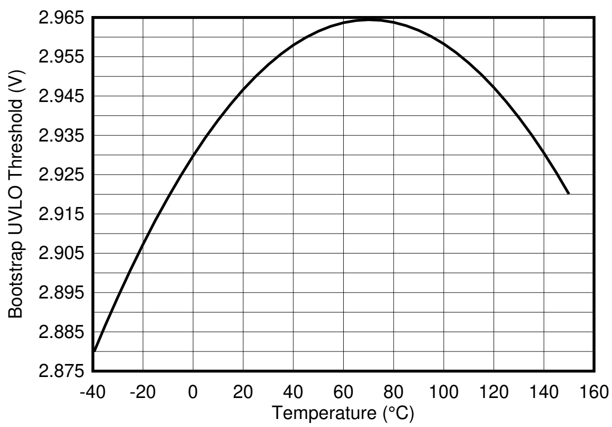


图 6-9. Bootstrap UVLO Threshold vs Temperature

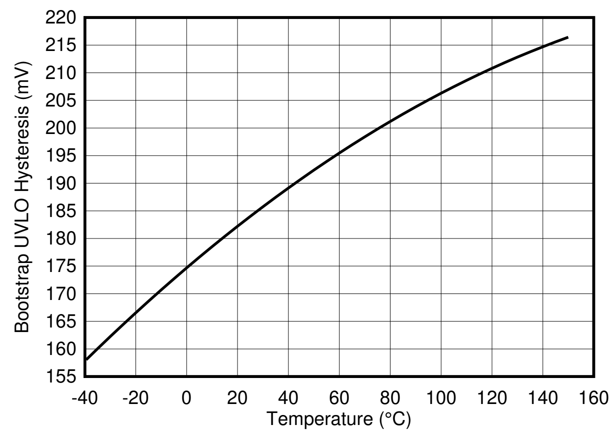


图 6-10. Bootstrap UVLO Hysteresis vs Temperature

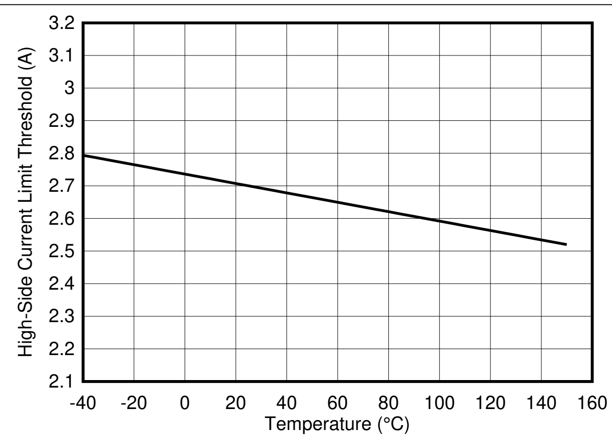


图 6-11. High-Side Current Limit Threshold vs Temperature

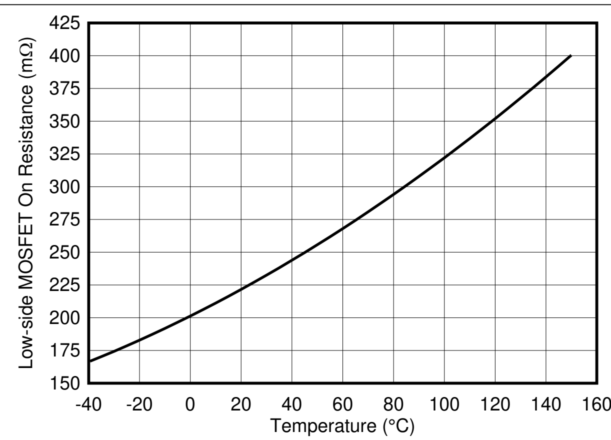


图 6-12. Low-Side MOSFET On Resistance vs Temperature

6.6 Typical Characteristics (continued)

$T_A = T_J = 25°C$, $V_{5D} = V_{5A} = 5$ V, $V_{IN} = 24$ V, $V_{UDIMx} = 5$ V, $C_{V5D} = C_{V5A} = 4.7$ µF $C_{BSTx} = 0.1$ µF, $C_{COMPx} = 1$ nF, $R_{CSx} = 100$ mΩ, no load on SWx, LHI pin floating (unless otherwise noted)

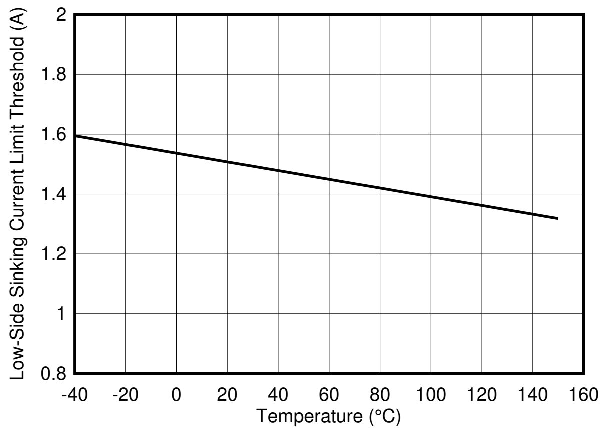


图 6-13. Low-Side Sinking Current Limit Threshold vs Temperature

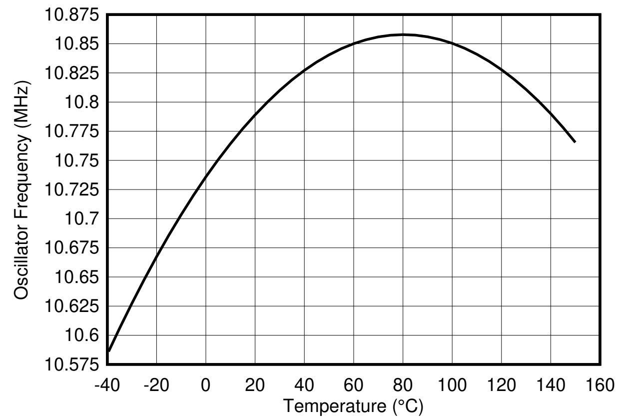


图 6-14. Oscillator Frequency vs Temperature

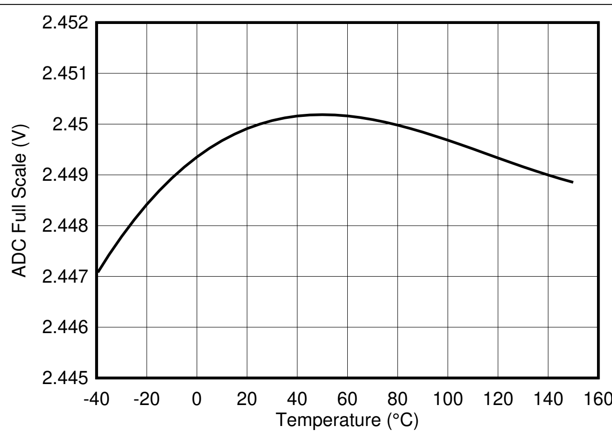


图 6-15. ADC Full Scale vs Temperature

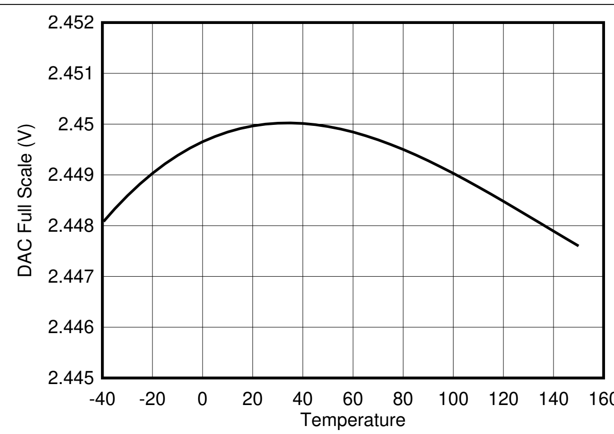


图 6-16. DAC Full Scale vs Temperature

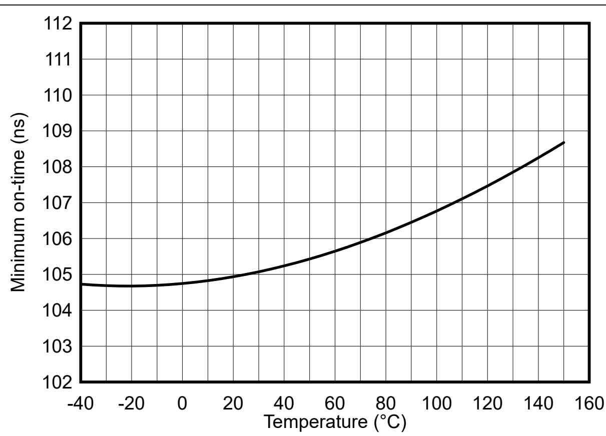


图 6-17. Minimum On-time vs Temperature

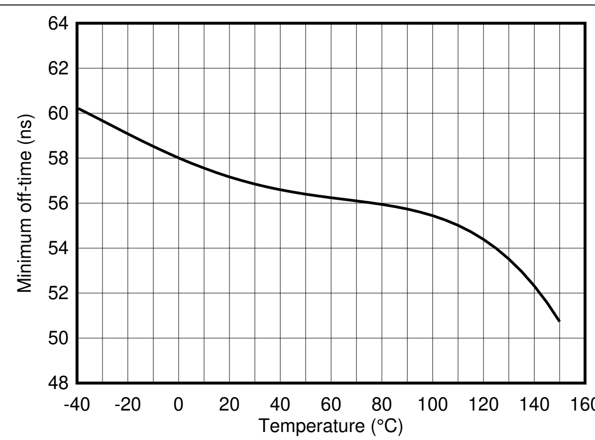


图 6-18. Minimum Off-time vs Temperature

6.6 Typical Characteristics (continued)

$T_A = T_J = 25°C$, $V_{5D} = V_{5A} = 5$ V, $V_{IN} = 24$ V, $V_{UDIMx} = 5$ V, $C_{V5D} = C_{V5A} = 4.7$ µF $C_{BSTx} = 0.1$ µF, $C_{COMPx} = 1$ nF, $R_{CSx} = 100$ mΩ, no load on SWx, LHI pin floating (unless otherwise noted)

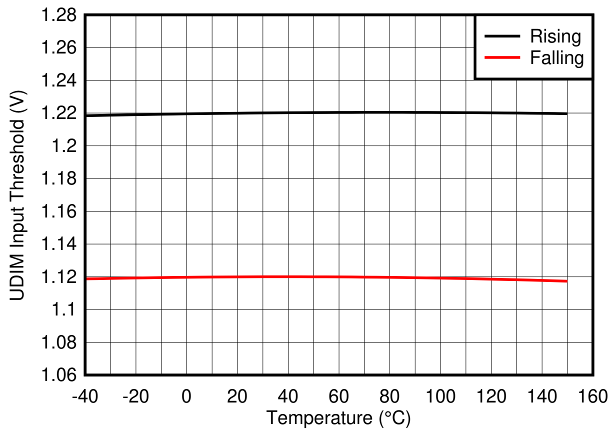


图 6-19. UDIM Input Threshold vs Temperature

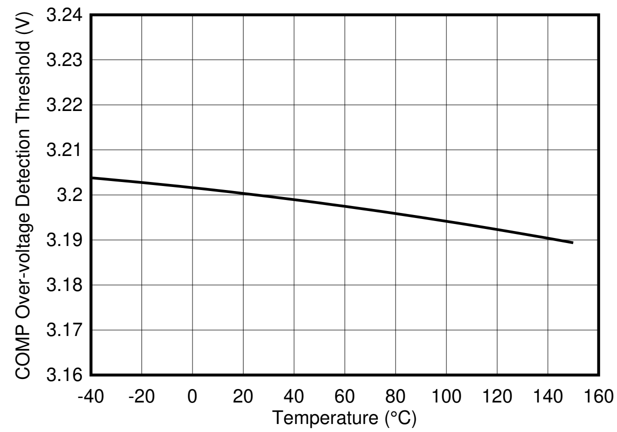


图 6-20. COMP Overvoltage Detection Threshold vs Temperature

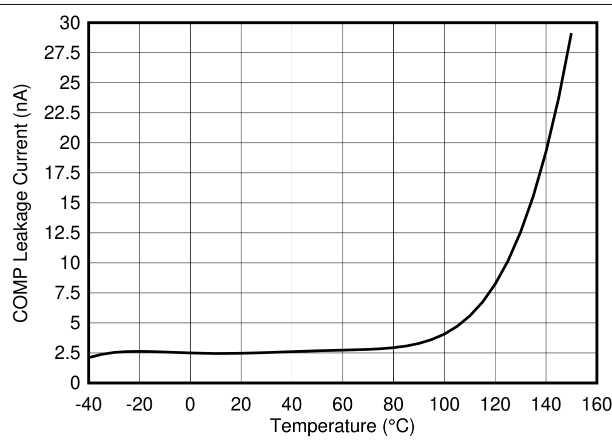
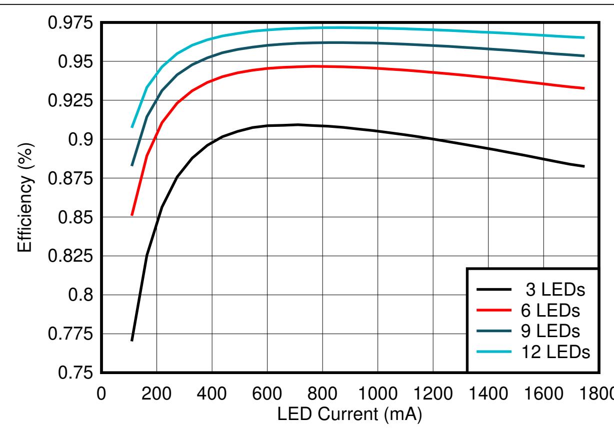
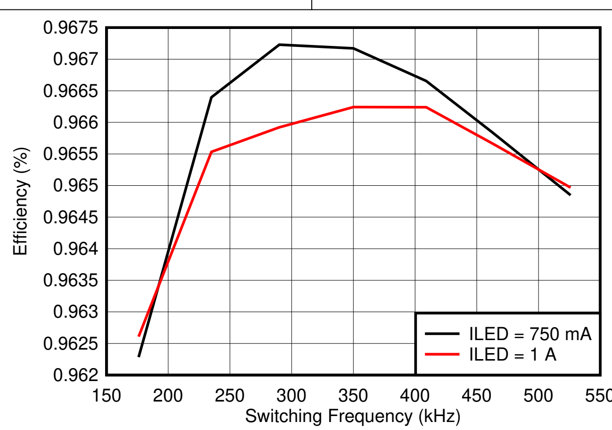


图 6-21. COMP Leakage Current vs Temperature



V_{IN} = 60 V f_{SW} = 437 kHz

图 6-22. Efficiency vs LED Current



V_{CSN} = 45 V V_{IN} = 60 V

图 6-23. Efficiency vs Switching Frequency

7 Detailed Description

7.1 Overview

The TPS92520-Q1 is a dual synchronous buck LED driver with a 4.5-V to 65-V input voltage range. It can deliver up to 1.6 A of continuous current per channel and power two independent strings of one to 16 series-connected LEDs. The device implements an adaptive on-time current regulation control technique to achieve fast transient response. This architecture uses a comparator and a one-shot on-timer that varies inversely with input and output voltage to maintain a near-constant frequency. The integrated low offset rail-to-rail error amplifier enables closed-loop regulation of LED current and ensures better than 4% accuracy over a wide input, output, and temperature range.

The LED current reference is set by the 10-bit IADJ DAC and is programmed by the CHxIADJ register to achieve over a 16:1 linear analog dimming range. Pulse width modulation (PWM) dimming of the LED current is achieved by either programming the internal PWM generator or by modulating the duty cycle of external voltage signal at UDIMx input. When enabled, the internal PWM generator sets the LED current duty cycle based on the 10-bit CHxPWM command. The external UDIMx input acts as an enable and directly controls the LED current. This device optimizes the inductor current response and is capable of achieving over a 1000:1 PWM dimming ratio.

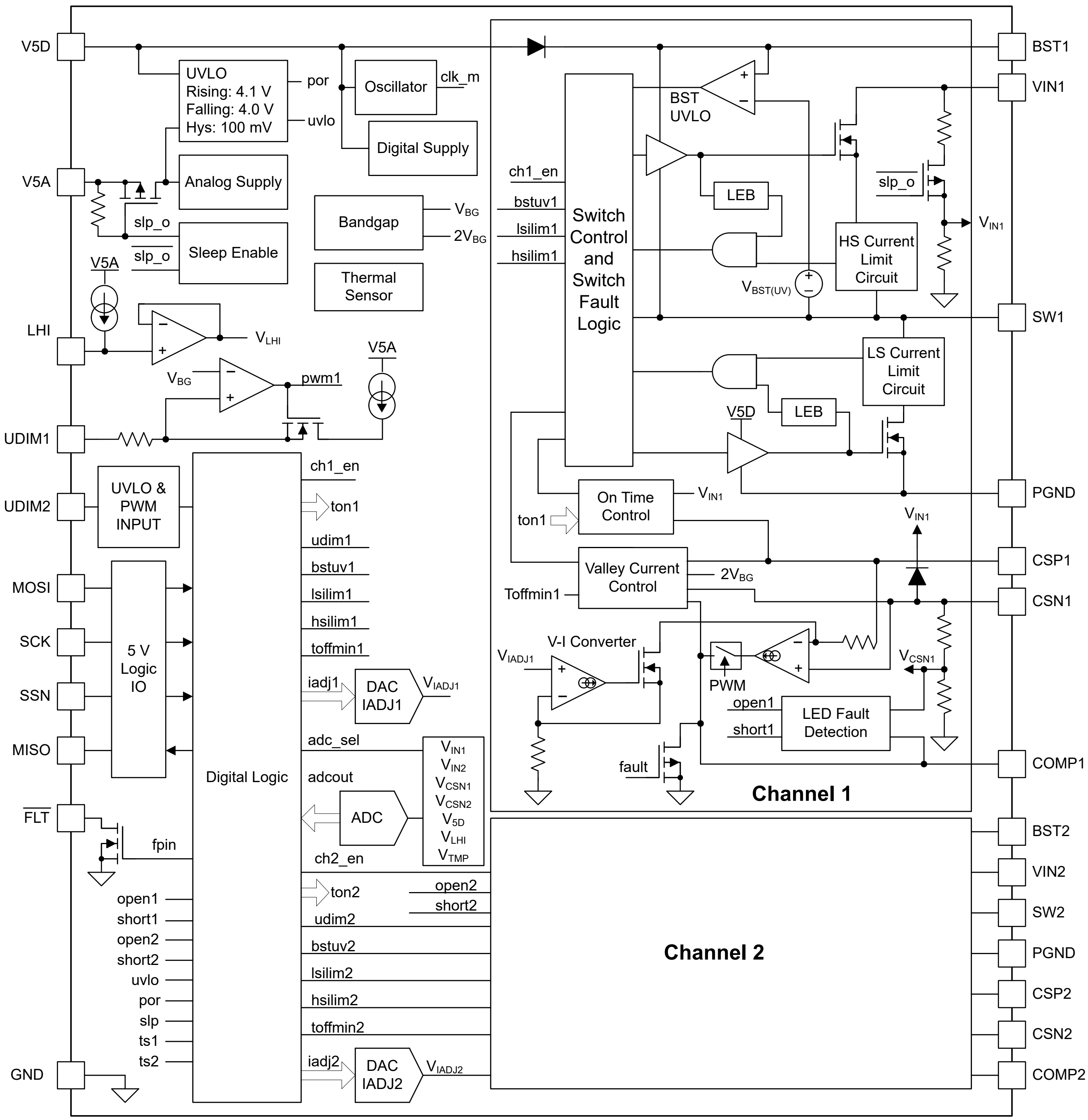
The device incorporates an enhanced programmable fault feature including the following:

- Cycle-by-cycle switch overcurrent limit
- Input undervoltage protection
- Boot undervoltage protection
- Comp overvoltage warning
- Thermal warning
- LED short circuit indication

In addition, thermal shutdown (TSD) protection is implemented to limit the junction temperature at 175°C (typical). For each fault, there is an associated fault read-bit in the status registers that can be easily accessed via SPI read commands.

The TPS92520-Q1 includes a communication watchdog timer that enables standalone and limp-home (LH) function. When enabled, the watchdog timer monitors the SPI communication during start-up and normal operation. Communication failure at start-up forces the device in stand-alone mode operation. In this mode, the operation of each channel is controlled by UDIMx and LHI inputs while the SPI communication is disabled. Limp-home (LH) mode is activated on detection of communication failure during normal operation. In LH mode, the device operation is controlled by the limp-home registers that are initialized and loaded during the device start-up sequence.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Buck Converter Switching Operation

The following operating description of the TPS92520-Q1 refers to the *Functional Block Diagram* and the waveforms in 图 7-1. The main control loop of the TPS92520-Q1 is based on an adaptive on-time pulse width modulation (PWM) technique that combines a constant on-time control with an inductor valley current sense circuit for pseudo-fixed frequency operation. This proprietary control technique enables closed-loop regulation of LED current and fast dynamic response necessary to meet the requirements for LED pixel control and LED matrix beam applications.

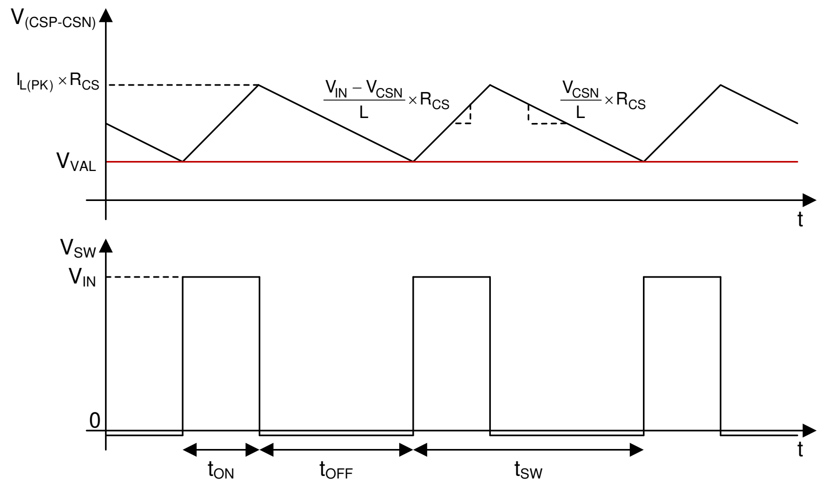


图 7-1. Adaptive On Time Control Buck Converter Waveforms

In steady state, the high-side MOSFET is turned on at the beginning of each cycle. The on-time duration of this MOSFET is controlled by an internal one-shot timer and the high-side MOSFET is turned off after the timer expires. The one-shot timer duration is set by the output voltage measured at the CSP pin, V_{CSP}, and the input voltage measured at the VIN pin, V_{IN}, to maintain a pseudo-fixed frequency. During the on-time interval, the inductor current increases with a slope proportional to the voltage applied across its terminals (V_{IN} – V_{CSP}).

The low-side MOSFET is turned on after a fixed deadtime and the inductor current then decreases with the constant slope proportional to the output voltage, V_{CSP}. Inductor current measured by the external sense resistor is compared to the valley threshold, V_{VAL}, by an internal high-speed comparator. This MOSFET is turned off and the one-shot timer is initiated when the sensed inductor current falls below the valley threshold voltage. The high-side MOSFET is turned on again after a fixed deadtime.

The internal rail-to-rail error amplifier sets the valley threshold voltage and regulates the average inductor current based on a reference value set by CHxIADJ-DAC. A simple integral loop compensation circuit consisting of a capacitor connected from the COMP pin to GND provides a stable and high-bandwidth response. As the inductor current is directly sensed by an external resistor, the device operation is not sensitive to the ESR of the output capacitors and is compatible with common multi-layered ceramic capacitors (MLCC).

7.3.2 Switching Frequency and Adaptive On-Time Control

The TPS92520-Q1 uses an adaptive on-time control scheme and does not have a dedicated on-board oscillator. The one-shot timer incorporates a 6-bit current steering DAC and is programmed by the CHxTON registers. The on-time is calculated internally using 方程式 1 and is inversely proportional to the measured input voltage, V_{IN}, and proportional to the measured CSP voltage, V_{CSP}.

$$t_{ON} = \frac{4 \times 10^{-8} \times CHxTON[5:0] + 18 \times 10^{-6}}{CHxTON[5:0] + 1} \times \frac{V_{CSP}}{V_{IN}} \tag{1}$$

Given the duty ratio of the buck converter is V_{CSP} / V_{IN}, the switching period, T_{SW}, remains nearly constant over all operating points. Use 方程式 2 to calculate the switching period.

$$T_{SW} = t_{ON} \times \frac{V_{IN}}{V_{CSP}} = \frac{4 \times 10^{-8} \times CHxTON[5:0] + 18 \times 10^{-6}}{CHxTON[5:0] + 1} \tag{2}$$

Use 方程式 3 to calculate the switching frequency.

$$f_{SW} = \frac{CHxTON[5:0]+1}{4\times10^{-8}\times CHxTON[5:0]+18\times10^{-6}} \quad (3)$$

TI recommends a switching frequency setting between 110 kHz and 2.2 MHz, corresponding to a decimal value of the CHxTON register ranging from 1 to 43.

7.3.3 Minimum On-Time, Off-Time, and Inductor Ripple

Buck converter operation is impacted by minimum on-time, minimum off-time, and minimum peak-to-peak inductor ripple limitations. The converter reaches the minimum on-time of 105 ns (typ) when operating with high input voltage and low-output voltage. In this control scheme, the off-time continues to increase and the switching frequency reduces to regulate the inductor current and LED current to the desired value.

$$f_{SW(MIN)} = \frac{V_{OUT(MIN)}}{t_{ON(MIN)}\times V_{IN(MAX)}};\ t_{ON} = t_{ON(MIN)} \quad (4)$$

The converter reaches the minimum off-time of 57 ns (typ) when operating in dropout (low input voltage and high output voltage). As the on-time and off-time are fixed, the duty cycle is constant and the buck converter operates in open-loop mode. The inductor current and LED current are not in regulation. The CHxTOFFMIN bit is set to indicate operation at maximum duty cycle. The converter continues to switch unless disabled by resetting the CHxEN bit. Upon detection of a minimum off-time operation, the device disables the error amplifier and disconnects the COMP pin to maintain charge on the compensation network. This ensures fast response with minimum LED current overshoot as the converter recovers from dropout condition.

The behavior and response of valley comparator is dependent on sensed peak-to-peak voltage ripple, $\Delta V_{(CSP-CSN)}$, and is a function of current sense resistor, R_{CS}, and peak-to-peak inductor current ripple, $\Delta i_{L(PK-PK)}$. To ensure periodic switching, the sensed peak-to-peak ripple needs to exceed the minimum value, specified in Minimum Ripple Voltage vs Average Inductor Current. At high (near 100%) or low (near 0%) duty cycles, the inductor current ripple may not be sufficient to ensure periodic switching. Under such operating conditions, the converter transitions from periodic switching to a burst sequence, forcing multiple on-time and off-time cycles at a rate higher than the programmed frequency. Although the converter may not operate in a periodic manner, the closed-loop control continues regulating the average LED current with a larger ripple value corresponding to higher peak-to-peak inductor ripple. TI recommends choosing an inductor, output capacitor, and switching frequency to ensure minimum sensed peak-to-peak ripple voltage under nominal operating condition is greater than 20 mV. The *Application and Implementation* section summarizes the detailed design procedure.

7.3.4 LED Current Regulation and Error Amplifier

The reference voltage, V_{IADJ}, set by the 10-bit CHxIADJ-DAC, is internally scaled by a gain factor of 1/14 via a resistor network. An internal rail-to-rail error amplifier generates an error signal proportional to the difference between the scaled reference voltage (V_{IADJ} / 14) and the inductor current measured by the differential voltage drop between CSP and CSN, $V_{(CSP-CSN)}$. This error drives the COMP pin voltage, V_{COMP}, and directly controls the valley threshold of the inductor current. Zero average DC error and closed-loop regulation is achieved by implementing an integral compensation network consisting of a capacitor connected from the output of the error amplifier to GND. As a good starting point, TI recommends a capacitor value between 1 nF and 10 nF between the COMP pin and GND. The choice of compensation network must ensure a minimum of 60° of phase margin and 10 dB of gain margin. The *Application and Implementation* section summarizes the detailed design procedure.

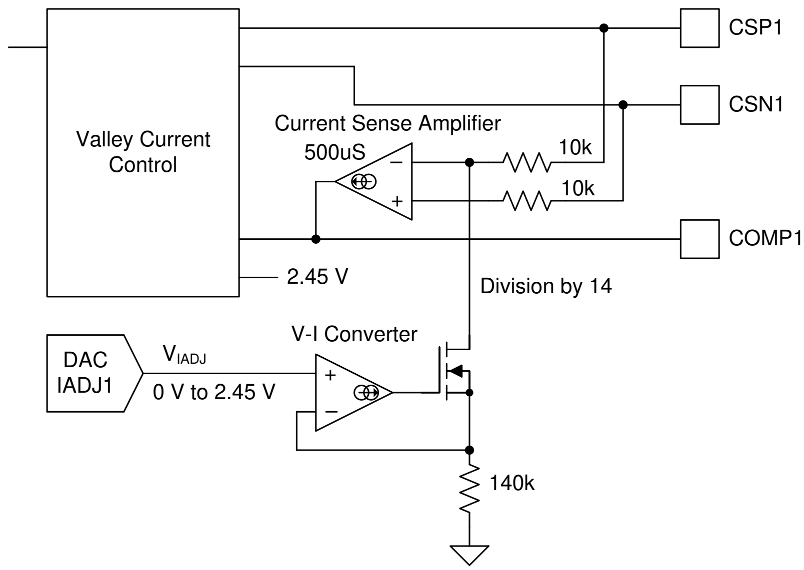


图 7-2. Closed-loop LED Current Regulation

LED current is dependent on the current sense resistor, R_{CS}. Use 方程式 5 to calculate the LED current.

$$I_{LED} = \frac{V_{(CSP-CSN)}}{R_{CS}} = \frac{V_{IADJ}}{14 \times R_{CS}} = \frac{V_{DAC(FS)}}{1024} \times \frac{CHxIADJ[9:0]}{14 \times R_{CS}} \quad (5)$$

LED current accuracy is a function of the tolerance of the external sense resistor, R_{CS}, and the variation in the sense threshold, $V_{(CSP-CSN)}$, caused by internal mismatch and temperature dependency of the analog components. The TPS92520-Q1 incorporates low offset rail-to-rail amplifiers, and is capable of achieving LED current accuracy of ±4% over common-mode range and a junction temperature range of –40°C to 150°C. The internal offset of the device can be measured and compensated using the lower LSBs of the 10-bit CHxIADJ-DAC. Therefore, the error can be further reduced and the LED current accuracy can be improved to be better than ±3%.

7.3.5 Start-up Sequence

The start-up circuit allows the COMP pin voltage to gradually increase, thus reducing the LED current overshoot and current surges. The switching operation is initiated after the COMP pin voltage exceeds 2.45 V. A 250-mV hysteresis window allows the device to operate when COMP voltage is within the expected operating range of 2.2 V to 2.7 V. Switching is disabled on detection of low COMP voltage to avoid excessive negative inductor current.

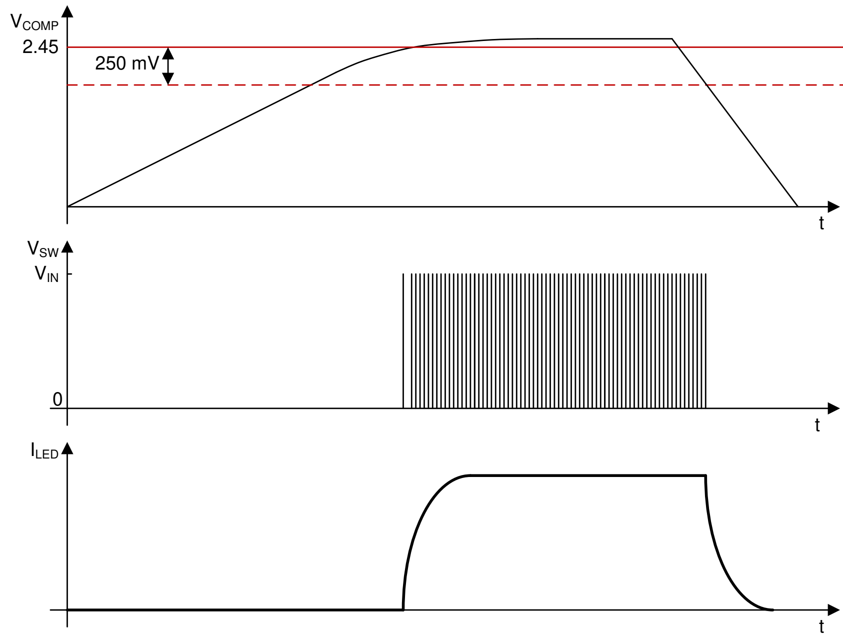


图 7-3. Soft-Start Sequence

The duration of soft start, t_{SS}, depends on the size of the compensation capacitor and the error amplifier source current, $I_{COMP(SRC)}$.

$$t_{SS} = \frac{2.45 \times C_{COMP}}{I_{COMP(SRC)}} \quad (6)$$

The source current, $I_{COMP(SRC)}$ is a function of the transconductance, g_M, of the error amplifier and error generated between the reference and the current sensed voltage.

$$I_{COMP(SRC)} = g_M \times \left(\frac{V_{IADJ}}{14} - V_{(CSP-CSN)} \right) \quad (7)$$

With no current flowing through the LEDs, the soft start duration depends on the choice of compensation capacitor, C_{COMP}, and the reference voltage, V_{IADJ}.

The CHxCOMPOV bit in the STATUS1 register is set when the COMP voltage deviates from the nominal range and exceeds 3.2 V. This indicates a fault condition where the converter is operating in open-loop and the LED current is out of regulation. The corresponding channel can be disabled by resetting the CHxEN bit via a SPI command or controlling the UDIMx input.

7.3.6 Analog Dimming and Forced Continuous Conduction Mode

Analog dimming is accomplished by the SPI interface through the adjustment of the 10-bit CHxIADJ registers. The TPS92520-Q1 improves the linear range of analog dimming by supporting forced continuous conduction mode of operation. With synchronous MOSFETs, the inductor current is allowed to go negative for part of the switching cycle, thus enabling linear dimming with over 16:1 dimming range.

7.3.7 External PWM Dimming and Input Undervoltage Lockout (UVLO)

The UDIM pin is a dual-function input that features an accurate 1.22-V threshold with programmable hysteresis as shown in 图 7-4. This pin functions as both the external PWM dimming input for the LEDs and as a VIN UVLO. When the rising pin voltage exceeds the 1.22-V threshold, 10 μA (typical) of current is driven out of the UDIM pin into the resistor divider providing programmable hysteresis.

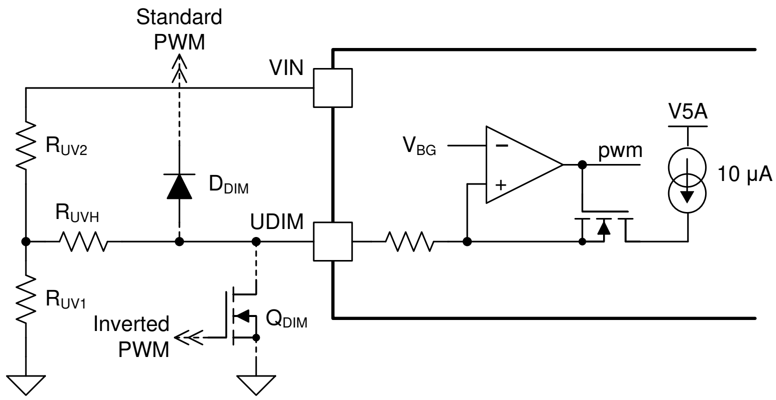


图 7-4. External PWM Dimming

The brightness of LEDs can be varied by modulating the duty cycle of the signal directly connected to the UDIM input. In addition, either an n-channel MOSFET or a Schottky diode can be used to couple an external PWM signal when using UDIM input in conjunction with UVLO functionality. With an n-channel MOSFET, the brightness is proportional to the negative duty cycle of the external PWM signal. With an Schottky diode, the brightness is proportional to the positive duty cycle of the external PWM signal.

When using the UDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra resistor to set the hysteresis. This allows the standard resistor divider to have smaller values, minimizing PWM delays. TI recommends at least 1 V of hysteresis when PWM dimming if you are operating near the UVLO threshold. Use 方程式 8 to define the rising threshold.

$$V_{IN(RISE)} = V_{UDIM(RISE)} \times \frac{R_{UV1} + R_{UV2}}{R_{UV1}} \tag{8}$$

Use 方程式 9 to define the hysteresis.

UVLO only:

$$V_{HYS} = I_{UDIM(UVLO)} \times R_{UV2} \tag{9}$$

PWM and UVLO:

$$V_{HYS} = I_{UDIM(UVLO)} \times \left(R_{UV2} + \frac{R_{UVH} \times (R_{UV1} + R_{UV2})}{R_{UV1}} \right) \tag{10}$$

7.3.8 Internal PWM Dimming

The TPS92520-Q1 incorporates an internal 10-bit counter to independently configure PWM dimming for each channel. To use the internal PWM, set the CHxINTPWM bit in the SYSCFG1 register. The duty cycle of the internal PWM can be set using a 10-bit value in the CHxPWML and CHxPWMH registers. Since CHxPWM is a 10-bit value, a PWM duty cycle update can require two SPI writes, one to the CHxPWMH and another to the CHxPWML register. In order to prevent transferring unintentional values, the contents of the two registers are only transferred to the CHxPWM counter upon the write to the CHxPWML register. Therefore, to update the PWM duty cycle, it is required to write a value to the CHxPWMH first, and in a consecutive command, write a value to the CHxPWML register. In addition, to avoid corrupting the progress of the current PWM duty cycle, the update from the CHxPWM register to the CHxPWM counter occurs two PWM_{CLK} counts before the end of each PWM period (at the count of 1022).

The clock to the 10-bit PWM counter is set by a 3-bit value in the PWMDIV register. 方程式 11 and 方程式 12 show the relationship between the PWM_{CLK} and PWM frequency with a 10.8-MHz oscillator, CLK_M.

$$PWM_{CLK} = \frac{CLK_M}{PWM_{DIV}} \quad (11)$$

$$PWM_{FREQ} = \frac{PWM_{CLK}}{1024} \quad (12)$$

For example, a PWMDIV[2:0] register setting of decimal value 5 sets the division ratio to 24 and results in a PWM frequency of 439 Hz. Refer to 节 7.6.3.7 for more details.

The device can be controlled through the input of the UDIM independent of the internal PWM setting. The signal at the UDIM input is ANDed with the internal PWM to generate a combined output which controls the switching operation. Therefore, each channel can be independently disabled based on the external UDIM signal, even when the device is configured to operate based on internal PWM settings.

7.3.9 Shunt FET Dimming or Matrix Beam Application

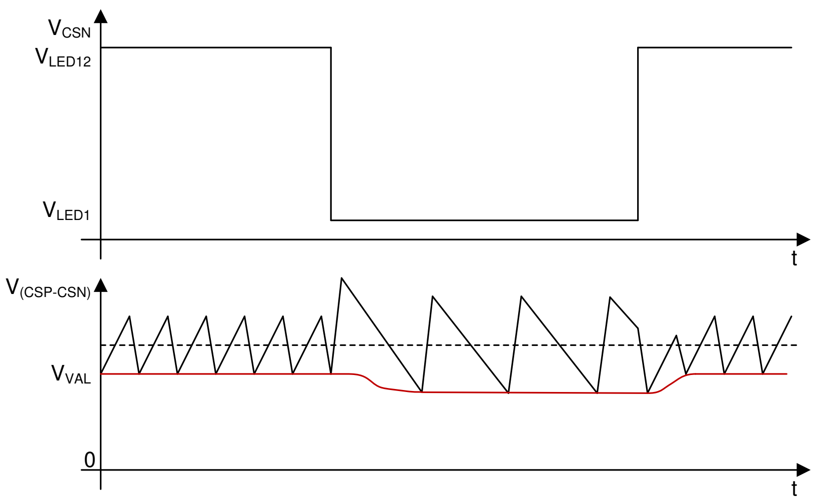


图 7-5. Shunt FET Dimming Transient Response

The TPS92520-Q1 is compatible with shunt FET dimming and LED Matrix Manager devices. The fast dynamic response and adaptive on-time control topology ensure near ideal current source behavior with minimum inductor current overshoot or undershoot. In contrast to constant off-time control, the control loop is able to maintain LED current regulation under shorted output condition. The off-time of the converter naturally adapts to the inductor slope and valley command while keeping the average LED current constant. 图 7-5 shows the shunt-FET dimming transient with all LEDs switched from on to off.

The device behavior is impacted by the falling slew-rate of CSN node, V_{CSN}. A large slew-rate in conjunction with the parasitic capacitances from CSP and CSN to GND results in differential voltage forcing the converter to burst with minimum on-time and minimum off-time. To avoid switch node bursting TI recommends a maximum slew-rate (dv/dt) of 5 V/µs.

7.3.10 Bias Supply

The device is powered by an external 5-V supply connected to V5D and V5A pins. Operation is enabled when V5D and V5A exceed the 4.1-V (typ) rising threshold and is disabled when either V5D or V5A drops below the 4-V (typ) falling threshold. The comparator provides 100-mV of hysteresis to avoid chatter during transitions. The V5D supply powers the internal digital logic, a 10.8-MHz oscillator, and the high-side and low-side gate driver circuits. The V5A supply powers the analog-to-digital converter (ADC), the digital-to-analog converters (DACs), and the sensitive analog circuits. The two bias pins can be connected together on the PCB or through a series 10-Ω resistor between V5D and V5A with 5-V external supply connected directly to the V5D pin. TI recommends a capacitor from each pin to GND . The recommended range for the bypass capacitor from V5D pin to ground is between 1 µF and 4.7 µF. The recommended range from the V5A pin to ground is between 100 nF and 1 µF.

The bypass capacitor from V5D to GND must be 10 times larger than the bootstrap capacitor, C_{BST}, to support proper operation during PWM dimming. The voltage on V5D and V5A must never exceed 5.5 V.

The power cycle (PC) bit indicates a fault condition when both V5D and V5A are below the 4 V. At power up, the PC bit is set and must be cleared before enabling the operation of individual channels. Reading the STATUS3 register clears the PC bit.

In device sleep state, the V5A input is internally disconnected to reduce power consumption. As the internal voltage drops below the 4-V threshold, the V5AUV bit is set in the STATUS3 register to indicate bias undervoltage condition. The fault clears when the device is programmed to exit the sleep state and assumes normal operation. See the *Device Functional Modes* section for more details.

7.3.11 Bootstrap Supply

The TPS92520-Q1 contains both high-side and low-side N-channel MOSFETs. The high-side gate driver works in conjunction with an internal bootstrap diode and an external bootstrap capacitor, C_{BST}. During the on-time of the low-side MOSFET, the SW pin voltage is approximately 0 V and C_{BST} is charged from the V5D supply through the internal diode. TI recommends a 0.1-μF to 1-μF capacitor connected with short traces between the BST and SW pins. A larger capacitor is required to prevent a bootstrap undervoltage fault when operating at low PWM dimming frequencies.

7.3.12 ADC

The TPS92520-Q1 incorporates a 10-bit successive approximation register (SAR) ADC. The single ADC is multiplexed to sample the following signals:

- VINx
- CSNx
- V5D
- LHI
- Internal temperature sensor nodes

The SAR ADC sampling and conversion require 18 μs typical. Priority is given to CSNx inputs to ensure accurate output voltage measurement when operating at low PWM duty cycles. The ADC scheduler samples CSN1 and CSN2 inputs four times consecutively followed by other input parameters. The complete round-robin sampling sequence is illustrated in 图 7-6.

1	2	3	4	5	6	7	8	9	10	11 18	19	20 27	28	29 36	37	38 45	46	47
VIN1	CSN1	CSN2	CSN1	CSN2	CSN1	CSN2	CSN1	CSN2	V5D	CSN1 ---- CSN2	VIN2	CSN1 ---- CSN2	LHI	CSN1 ---- CSN2	TEMP	CSN1 ---- CSN2	VIN1	CSN1

图 7-6. ADC Sampling Sequence

The CSN1 and CSN2 inputs are sampled at an interval of 36 μs with an additional delay occurring every 9^{th} sample. All other parameters are sampled at a rate of 810 μs. For example, VIN1 input is sampled after 45 ADC conversion cycles. The round robin sampling scheme ensures an adequate sampling speed to allow for very fast failure detection without data link loss, even when PWM dimming.

7.3.12.1 Input Voltage Measurement: VINx

The VINx ADC input is a measurement of the V_{INx} pin voltage. The VINx pin voltage is internally attenuated by 0.037 to achieve an 8-bit conversion ratio of 65/255 (V/dec). The CHxVIN register is updated based on the 8 MSBs of ADC conversion. The last 2 LSBs are ignored. The contents of the register provide diagnostics of input power supply or, in many applications, the pre-regulator boost converter output voltage.

7.3.12.2 LED Voltage Measurement: CSNx

The ADC updates the CHxVLED register every time after sampling the CSNx input. The CSNx pin voltage is internally attenuated by 0.037 to achieve an 8-bit conversion ratio of 65/255 (V/dec). Since the sampling interval is asynchronous to the PWM operation, the logic incorporates two additional registers, CHxVLEDON and CHxVLEDOFF, to save the output voltage information based on the PWM operation. The contents of the CHxVLED register are copied to CHxVLEDON on the falling edge of the PWM signal to record the CSNx voltage when the PWM input was high. Similarly, the CHxVLED register is copied to CHxVLEDOFF on the rising edge of the PWM signal to record the CSNx voltage when the PWM input was low. This ensures the most consistent LED voltage reading during PWM operation.

7.3.12.3 Bias Supply Measurement: V5D

The V5D pin measurement indicates the status of the external bias converter. The V5D pin voltage is internally attenuated by 0.45 to achieve an 8-bit conversion ratio of 5.33/255 (V/dec).

7.3.12.4 External Limp-Home Input Measurement: LHI

The ADC monitors the LHI pin and sets the internal current reference in limp-home mode. The LHI input voltage is digitized to achieve a 10-bit reference with resolution of 2.45/1023 (V/dec). The LHIL and LHIH registers are updated based on the ADC output.

7.3.12.5 Junction Temperature Measurement: TEMP

The combined TEMPL and TEMPH register values represent the 10-bit junction temperature measurement with a resolution of 1°C/LSB. The register is only updated when TEMPL is read. Therefore, TEMPL must be read first followed by TEMPH to read the junction temperature. Use 方程式 13 to calculate the junction temperature.

$$T_J = 0.7168 \times TEMP[9:0] - 271.51 \tag{13}$$

7.3.13 Faults and Diagnostics

表 7-1 summarizes the device behavior under fault conditions.

表 7-1. Fault Description

FAULT	DETECTION	DESCRIPTION
Thermal Warning	$T_J > T_{J(LMT)}$	Thermal warning (TW) bit is set in the STATUS3 register when the junction temperature exceeds the threshold programmed by TWLMT[9:2].
Thermal Protection	$T_J > 175°C$	Each channel is protected by an individual thermal sensor located close to the switching MOSFETs. The thermal protection is activated in the event the maximum MOSFET temperature exceeds the typical value of 175°C. The corresponding channel is forced into shutdown mode and the CHxTS bit is set in the STATUS2 register. This feature is designed to prevent overheating and damage to the internal switching MOSFETs.
SPI Error	—	A communication error is indicated by the SPE bit and it is set high. The device enters stand-alone mode or LIMP-HOME mode of operation when the watchdog timer duration expires (CMWTAP register) and the watchdog timeout event counter (CMWTO[1:0] in the STATUS3 register).
V5D Undervoltage Lockout	$V_{5D(RISE)} < 4.1$ V $V_{5D(FALL)} > 4$ V	The device enters the undervoltage lockout (UVLO). The switching operation is disabled, the COMP capacitor is discharged, and the digital logic is reset to default values. The power cycle (PC) bit is set in the STATUS3 register.
V5A Undervoltage Lockout	$V_{5A(RISE)} < 4.1$ V $V_{5A(FALL)} > 4$ V	In SLEEP mode, the internal V5A node is disconnected to reduce the current consumption. The switching operation is disabled and the COMP capacitor is discharged. The V5AUV bit is set in the STATUS3 register.
VINx Undervoltage Lockout	$V_{UDIMx} < 1.12$ V	The device disables switching operation for the corresponding channel. Switching is enabled when the input voltage rises above the turnon threshold, $V_{IN(RISE)}$.
BSTx Undervoltage Lockout	$V_{BSTx(RISE)} > 3.14$V $V_{BSTx(FALL)} < 2.95$ V	The device turns off the high-side MOSFET and turns on the low-side MOSFET for the corresponding channel. The CHxBSTUV bit is set in the STATUS2 register. Normal switching operation is resumed once the bootstrap voltage exceeds 2.95 V.

表 7-1. Fault Description (continued)

FAULT	DETECTION	DESCRIPTION
COMPx Overvoltage	V_{COMPx} > 3.2 V	The CHxCOMPOV bit in the STATUS1 register is set to indicate that the COMP voltage exceeded the normal operating range. This information is provided for device diagnostics.
Short CHx Output	V_{CSNx} < 2.45 V	The CHxSHORT bit is set in the STATUS1 register to indicate an output short circuit condition based on sensed CSNx voltage.
High-Side Switch Current Limit	I_{HS} > 2.7 A	The device turns off the high-side MOSFET and discharges the COMP capacitor when the drain current exceeds 2.7 A typical. The low-side switch is turned on to discharge the inductor and output capacitor. The CHxHSILIM bit is set in the STATUS1 register. The fault recovery is based on the device configuration.
Low-Side Switch Current Limit	I_{LS} > 1.5 A	The device turns off both high-side and low-side MOSFETs and discharges the COMP capacitor when the drain current exceeds 1.5 A typical. The CHxLSILIM bit is set in the STATUS1 register. The fault recovery is based on the device configuration.
Minimum Off-Time	—	The CHxTOFFMIN bit is set in the STATUS2 register when the corresponding channel reaches the maximum possible duty cycle. This usually occurs during dropout condition or PWM dimming operation. The compensation network is disconnected from the output of the error amplifier to prevent COMP voltage from exceeding the normal operating range. Normal operation is resumed once the off-time increases above the minimum limit.

All the faults and diagnostics features, except V_{5D} UVLO and V_{INx} UVLO, have an associated Fault-Read bit in the STATUS1, STATUS2, and STATUS3 registers. Upon occurrence of a fault, the associated Fault-Read bit is set in the register map. Reading these registers clears the bits if the condition no longer exists. The clearing of the Fault-Read bits happens at the end of the SPI transfer read response, not at the end of the read command.

The TPS92520-Q1 can be configured to auto-restart or latch-off on detection of the thermal shutdown, high-side, or low-side current limit faults. The device enters the latched-off state when the bit associated with the fault and channel is set high in the SYSCFG2 register. This forces the device to disable the channel and remain off upon the detection of the fault condition. The channel can be turned back on by clearing the fault bit in STATUS1 and by re-setting the CHxEN bit in the SYSCFG1 register.

If the fault is configured as non-latched (the CHxTS, CHxHSILIMFL, or CHxLSILIMFL bit is set to 0 in the SYSCFG2 register), a restart sequence is initiated to attempt recovery from the fault condition. In the case of thermal shutdown fault, the restart is initiated after the MOSFET temperature decreases by the fixed hysteresis of 10°C. A soft-start sequence is initiated and switching operation is enabled. For a high-side or low-side current limit fault, a fixed timer is initiated on detection of the fault. The fault timer is programmable with a range of 3.6 ms to 28.8 ms by IFT[1:0] bits in SYSCFG2 register. A restart is initiated by the expiration of the fault timer and switching operation is enabled.

The TPS92520-Q1 logic has a communication watchdog timer that is based on the system clock (CLK). The watchdog timer is enabled by default upon power-up (the CMWEN bit is set to 1 in the SYSCFG1 register). The communications watchdog timer tap point is programmed by writing the desired value to the CMWTAP register.

The tap point defines the timing of the communication watchdog timer (a 25-bit counter). By default, the tap point is set to bit 24 corresponding to 1.67 s of duration. The communication watchdog monitors the status of SPI bus and defines the device operation in case of SPI communication error (SPE bit set to 1). See the *Device Functional Modes* for more details.

The high-side current limit, low-side current limit, and thermal protection faults force the $\overline{FLT}$ pin low when biased through an external resistor and connected to a 5-V supply. The $\overline{FLT}$ output can be used in conjunction with a microcontroller or system basis chip (SBC) as an interrupt and can be used to aid in fault diagnostics. Setting the FPINRST bit to one in SYSCFG1 register resets the $\overline{FLT}$ pin out when no active faults are detected by the device.

表 7-2. Faults and Diagnostics Summary

LIST	DESCRIPTION	FAULT OR DIAGNOSTIC	FAULT READ BIT	ENABLE FAULT TIMER	$\overline{FLT}$ INDICATION	ENABLE LATCH
TW	Thermal Warning	Diagnostics	Yes	No	No	No
CHxTP	Thermal Protection	Fault	Yes	No	Yes	Yes
$VINx_{(UVLO)}$	VIN Supply Undervoltage Lockout	Fault	No	No	No	No
CHxBSTUV	BST Supply Undervoltage Lockout	Fault	Yes	No	No	No
CHxCOMPOV	COMP Overvoltage	Diagnostics	Yes	No	No	No
CHxSHORT	Short Circuit Detected	Diagnostics	Yes	No	No	No
CHxHSILIM	High-side Current Limit	Fault	Yes	Yes	Yes	Yes
CHxLSILIM	Low-side Current Limit	Fault	Yes	Yes	Yes	Yes
CHxTOFFMIN	Minimum Off Time	Diagnostics	Yes	No	No	No
V5AUV	V5A Undervoltage	Diagnostics	Yes	No	No	No
PC	Power On Reset (Power Cycle)	Fault	Yes	No	Yes	Yes
SPE	SPI Communication Error	Diagnostics	Yes	No	No	No
LHSW	Limp-Home Mode (Communication Error)	Fault	Yes	No	No	No

7.3.14 Output Short Circuit Fault

The TPS92520-Q1 monitors the CSNx voltage to detect output short circuit faults. A short failure is indicated when the CSNx voltage drops below 2.45 V. The corresponding CHxSHORT bit is set in the STATUS1 register. The device continues to regulate current and operate without interruption in case of short circuit. The microcontroller can detect short circuit either by reading the STATUS1 register or by reading the CSNx voltage measured by the ADC (CHxVLED register). Upon detection of a short, the microcontroller is required to take action by writing to SYSCFG1 register via SPI. A short circuit fault in standalone mode or limp-home mode does not impact the device behavior. The device continues to operate and regulate current without interruption.

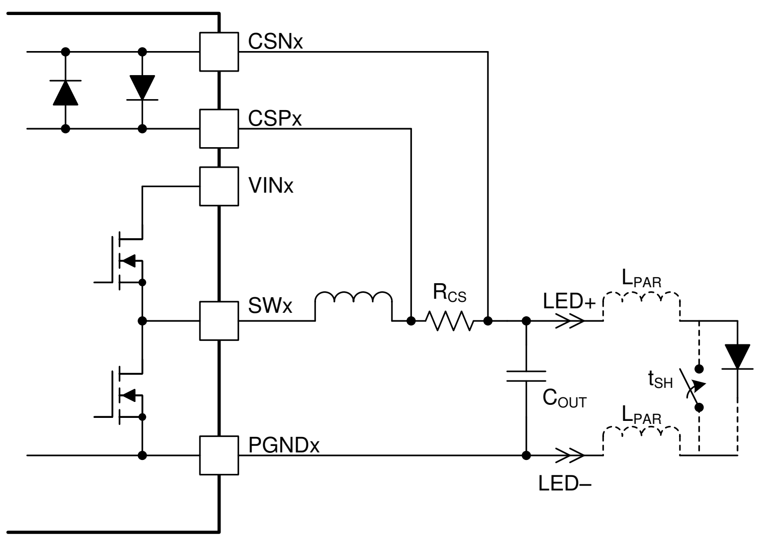


图 7-7. Cable harness parasitic inductance

The voltage transient imposed on CSPx and CSNx inputs during short circuit is dependent on the output capacitance and is influenced by the cable harness impedance. The inductance associated with a long cable harness resonates with the charge stored on the output capacitor and forces CSPx and CSNx voltage to ring below ground. The negative voltage and current are dependent on the parasitic cable harness inductance and resistance.

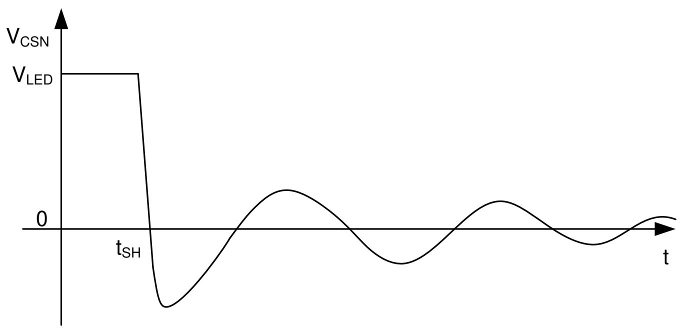


图 7-8. Short Circuit Fault Transient Behavior

When using a long cable harness, a diode is recommended to clamp the negative voltage across CSPx and CSNx input, as shown in 图 7-9. TI recommends a low forward voltage Schottky diode or a fast recovery silicon diode with reverse blocking voltage rating greater than the maximum output voltage. The diode is required to be placed close to the output capacitor and should ensure that the current flowing through CSP and CSN nodes under negative transient condition is below the absolute maximum rating of the device.

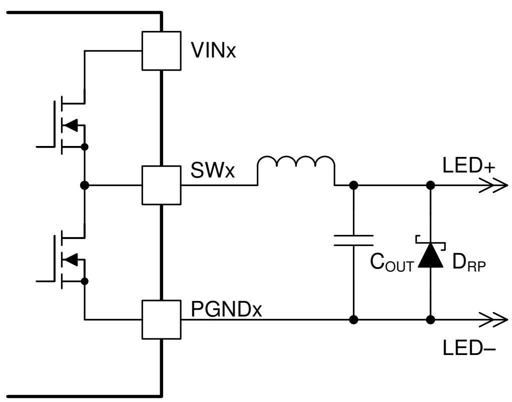


图 7-9. CSP and CSN Transient Protection Using an External Diode

7.3.15 Output Open Circuit Fault

An LED open circuit fault ultimately causes the output voltage to increase and settle close to the input voltage. When this occurs, the TPS92520-Q1 switching operation is then controlled by the fixed on-time and minimum off-time resulting in a duty cycle close to 100%. However during open circuit, the dynamic behavior of the device and buck converter is influenced by the input voltage, V_{IN}, and the output capacitor, C_{OUT}, value. The device response to open circuit can be categorized into the following three distinct cases.

Case 1: For a Buck converter design with a small output capacitor, the switching operation in open load condition excites the inductor and the output capacitor resonance, forcing the output voltage to oscillate. The frequency and amplitude of the oscillation are based on the resonant frequency and Q-factor of the tank. The open-circuit is detected by checking the CHxCOMPOV, CHxTOFFMIN bits in STATUS1 and STATUS2 registers and by polling the CHxVLED register to verify the output voltage measured by internal ADC.

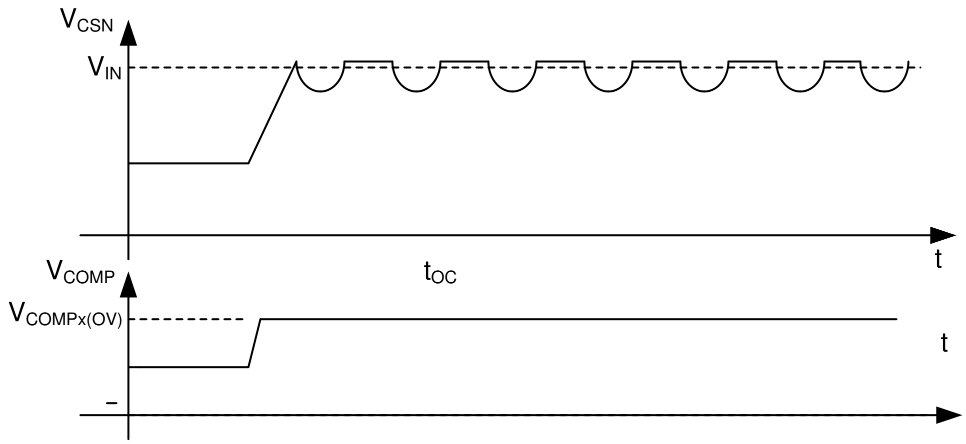


图 7-10. Open Circuit Condition with Output Voltage Oscillation

Case 2: For a buck converter design with larger output capacitor, the inductor Q-factor and resonant frequency are much lower than the switching frequency. In this case, output voltage rises to input voltage and the converter continues to switch with minimum off-time. The open-circuit fault is detected by checking the CHxTOFFMIN bit in STATUS2 register and by polling the CHxVLED register to verify the output voltage measured by internal ADC.

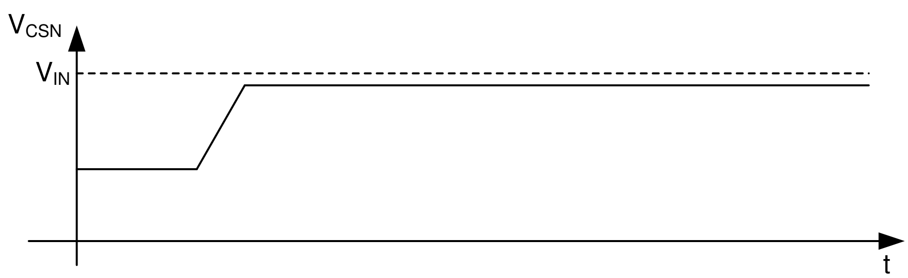


图 7-11. Open circuit Condition with Minimum Off-time Operation

Case 3: When operating at higher input voltage, the larger gate-to-drain charge depletes the bootstrap capacitor and triggers bootstrap UVLO protection. When bootstrap voltage is below 2.95 V, undervoltage protection is triggered. Due to insufficient gate drive supply, the high-side MOSFET RDS_{ON} is larger than typical value tripping the high side current limit circuit. On detection of high-side current limit, the low-side FET is turned on, causing the output capacitor to discharge and trip the low-side current limit. Further attempts to restart the converter cause the low-side protection to trigger and the sequence continues until the output capacitor is discharged to ground. The operation is illustrated in 图 7-12.

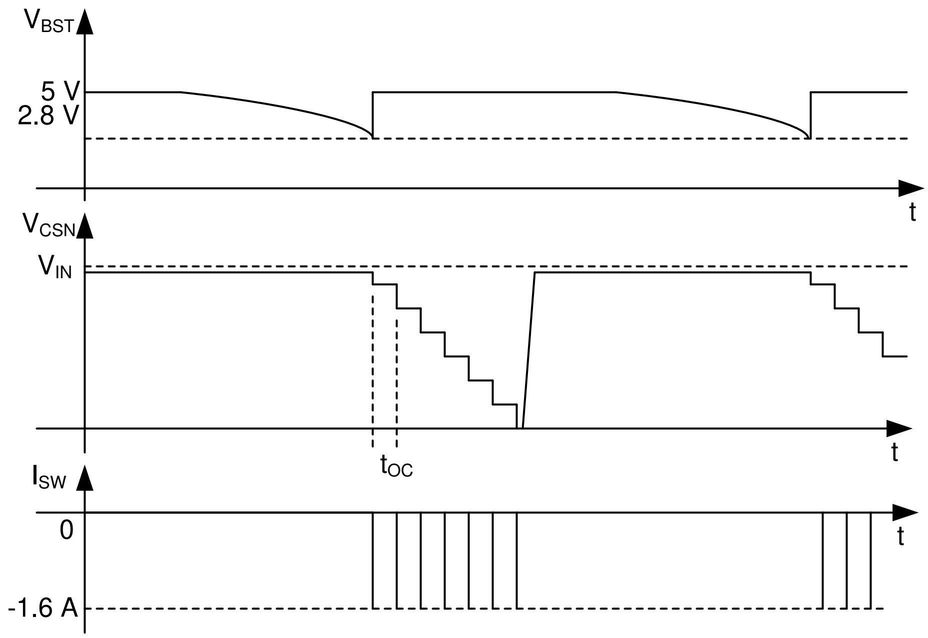


图 7-12. Open Circuit Condition with Bootstrap Undervoltage Lockout Fault

The open circuit can be detected by reading the CHxHSILIM, CHxLSILIM bits in the STATUS1 register and CHxBSTUV bit in the STATUS2 register in conjunction with the CHxTOFFMIN and CHxVLED register. The microcontroller can detect and respond to open circuit by polling CHxVLED register in conjunction with reading CHxTOFFMIN, CHxLSILIM, and CHxBSTUV bits.

表 7-3 summarizes the device response to open circuit faults. The device can transition between different modes near the input voltage range of 40 V to 50 V. TI recommends polling STATUS1, STATUS2, and STATUS3 registers to correctly identify an open circuit fault based on the specified input voltage range and choice of output capacitor.

表 7-3. Open Circuit Fault Detection Summary

	VCSNx ADC	CHxCOMPOV	CHxTOFFMIN	CHxBSTUV	CHxHSILIM	CHxLSILIM	CHxSHORT
Case 1	Read CSNx ADC measurement	1	1	0	0	0	0
Case 2	Read CSNx ADC measurement	0	1	0	0	0	0
Case 3	Ignore CSNx ADC measurement	x	x	1	1	1	1

7.4 Device Functional Modes

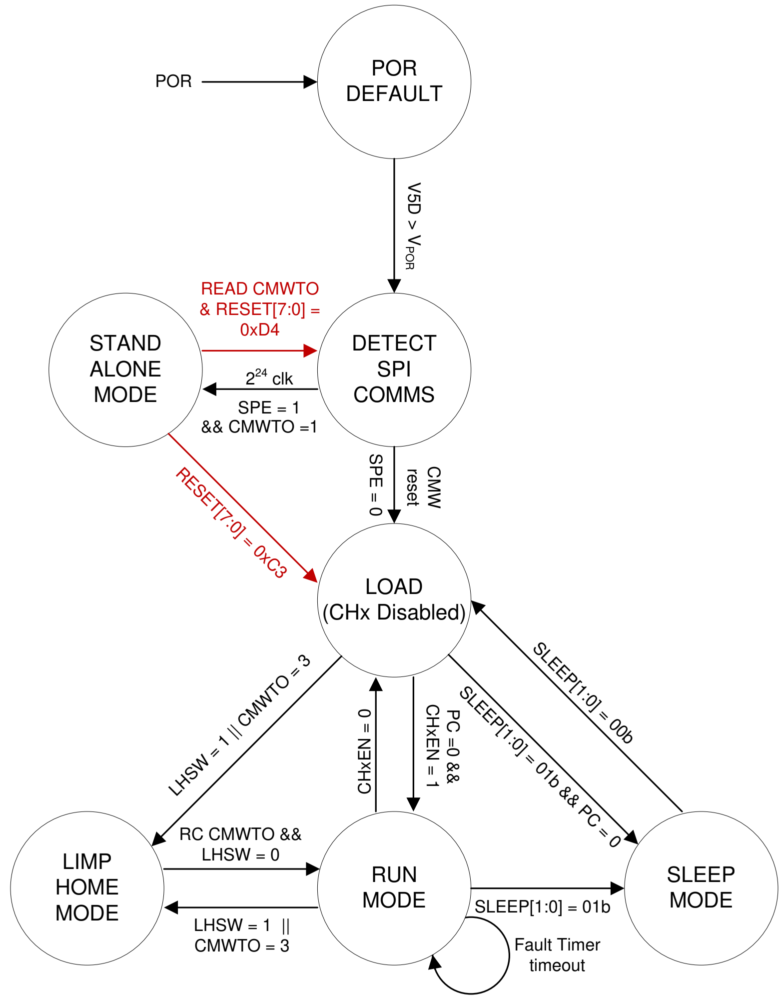


图 7-13. TPS92520-Q1 Functional Modes

7.4.1 Power On Reset (POR)

The device is in POR state when V5A or V5D input is below the undervoltage lockout threshold. In POR, all of the register settings are reset to the default values and both channels are turned off. The device exits POR and enters functional modes when the V5D supply exceeds 4.1 V.

7.4.2 Detect SPI Communication

After the existing POR state, the device waits for an SPI transaction. If no transaction with an correct SPI frame is received for 2^{24} system clock cycles (approximately 1.55 s), the communication watchdog timer times out and the device enters stand-alone mode of operation. Receiving a valid SPI frame before the watchdog timeout resets the timer and the device transitions to LOAD mode.

7.4.3 Standalone Mode

The TPS92520-Q1 is designed to operate in stand-alone mode without the need for an external microcontroller or SPI-based communication. In this mode, the watchdog timer circuit is disabled and each channel is individually controlled by external inputs. The reference current is set based on the LHI pin voltage and the outputs are enabled using the UDIM inputs. The default value for the on-timer is selected and the channels operate at a fixed switching frequency of 437 kHz. The device also defaults to auto-restart mode for all faults with the fault timer set to 3.6 ms typical. Connecting the LHI pin to GND (below 148-mV threshold) disables both channels and turns off both outputs. If the logic is in Standalone Mode, writing 0xC3 to the RESET register sets all values to default and returns the state machines to the LOAD state. Likewise, if the logic is in Standalone Mode, reading STATUS3 register first to clear the CMWTO bits and then writing 0xD4 to the RESET register sets all values to default and returns the state machine to the DETECT state.

7.4.4 Load Mode

The device operation in normal-run mode and limp-home mode is programmed by loading information into the configuration and control registers via SPI. The CHxEN bit is set low to prevent the converters from turning on and operating with default system parameters. The PC bit in the STATUS3 register must be cleared by sending a read command in order to exit this mode. Writing "01" bits to the SLEEP register skips the run mode and the device directly enters a low-power sleep state.

7.4.5 Run Mode

The device advances to run mode when the CHxEN bit is set to "1" in the SYSCFG1 register. In this mode, all the necessary conditions for initiating the soft-start sequence are checked. The LHSW bit in the SYSCFG1 register must be "0" and cannot have any active latched faults present to initiate switching operation. If a latched fault occurs in this state, the CHxEN bit is reset and the COMP capacitor is discharged, thus forcing the device back to load mode. Otherwise, the device attempts to resume operation after waiting for the fault timer to timeout.

In the event of SPI communication failure, the device transitions to limp-home mode. For this to occur, the watchdog timer must be enabled (the CMWEN bit equals 1 in the SYSCFG1 register). The device enters limp-home mode after counting three consecutive watchdog timeout events. Alternatively, the device can be forced into limp-home mode by setting the LHSW bit high in the SYSCFG1 register.

Transition to sleep mode is initiated by writing "01" bits to the SLEEP register via SPI. This causes the device to enter a low-power state.

7.4.6 Sleep Mode

In sleep mode, the following occurs:

1. The internal regulators are disconnected from the V5A pin.
2. The oscillator is disabled.
3. The CHxEN bit is set low.
4. The channels are disabled.
5. ADC and DAC operation are disabled.
6. The MOSFETs are turned off.

In addition, the resistor divider networks for VINx measurements and V5D measurement are disconnected to conserve power. Only the SPI communication logic, powered by V5D supply, is active and the SPI bus is monitored to check command writes to the SLEEP register. Upon receiving the wake command (writing "00" to SLEEP[1:0] bits in SLEEP register), the device transitions from sleep mode to load mode. In sleep mode, the output voltage will rise above 3 V as all internal loads are switched off and the leakage current associated with high-side gate drive is forced through the switch node, SWx.

7.4.7 Limp-Home Mode

The TPS92520-Q1 enters the limp-home mode after detecting three consecutive watchdog timeout events or when the LHSW bit is set high in the SYSCFG1 register. In limp-home mode, the device sets the operation based on the SPI-programmable LH-registers (register address 0x1E to 0x2D). The limp-home registers must be programmed upon the initialization of the device in load mode.

The LED current reference can be programmed through the LHxIADJ registers or set by external voltage measured at the LHI pin by the ADC. To enable LED control by the LHI pin, set the LHEXTIADJ bit in the LHCFG1 register to "1". 方程式 14 expresses the relationship between the LED current and voltage at the LHI pin, V_{LHI}.

$$I_{LED} = \frac{V_{LHI}}{14 \times R_{CS}} \quad (14)$$

The LHI voltage measured by the ADC is converted to a 10-bit value and stored in the LHI registers. An internal digital low pass filter attenuates any switching noise coupled to the LHI pin. The output of the filter is stored in the LHIFILT registers.

When the external LHI pin is selected as the LED current reference, an LHI pin voltage below 148 mV disables both channels and turns off the LEDs. In this condition, the device ensures that no light output is generated for the associated channels. The LHI pin voltage has to exceed 200 mV to enable both channels. The hysteresis rejects external noise on LHI pin and avoids light flickering.

To exit limp-home mode, the contents of STATUS3 register must be read to clear the CMWTO bits followed by a write command to set the LHSW bit in the SYSCFG1 register to "0".

7.5 Programming

The programming of the TPS92520-Q1 registers can be performed via a serial interface communication. The 4-wire control interface in TPS92520-Q1 is compatible with the Serial Peripheral Interface (SPI) bus. A microcontroller unit (MCU) can write to and read from the device registers to configure the channel operation and enable or disable a specific channel.

7.5.1 Serial Interface

The SPI bus consists of four signals:

- SSN
- SCK
- MOSI
- MISO

The SSN, SCK, and MOSI pins are TTL inputs into the TPS92520-Q1 while the MISO pin is an open-drain output. The SPI bus can be configured for both star-connect and daisy-chain network.

A bus transaction is initiated by an MCU on a falling edge of SSN. While SSN is low, the input data present on the MOSI pin is sampled on the rising edge of SCK with the MS-bit first. The output data is asserted on the MISO pin at the falling edge of the SCK. 图 7-14 shows the data transition and sampling edges of SCK.

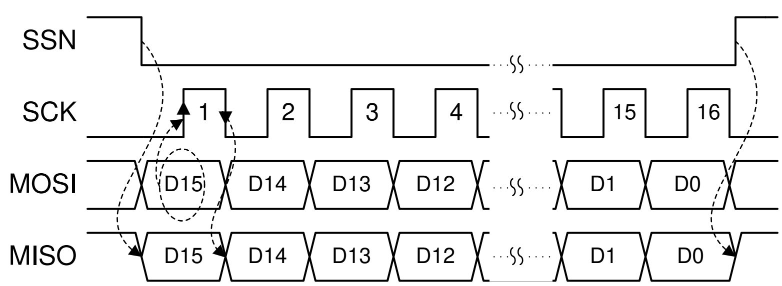


图 7-14. SPI Data Format

A valid transfer requires a non-zero integer multiple of 16 SCK cycles (that is 16, 32, 48, and so forth). If SSN is pulsed low and no SCK pulses are issued before SSN rises, a SPI error is reported. Similarly, if SSN is raised before the 16th rising edge of SCK, the transfer is aborted and a SPI error is reported. If SSN is held low after the 16th falling edge of SCK and additional SCK edges occur, the data continues to flow through the TP92520-Q1 shift register and out of the MISO pin. When SSN transitions from low to high, the internal digital block decodes the most recent 16 bits that were received prior to the SSN rising edge.

SSN must transition to high only after a multiple of 16 SCK cycles for a transaction to be valid. Otherwise a SPI error is reported. In the case of a write transaction, the TPS92520-Q1 logic performs the requested operation when SSN transitions high as long as there was no SPI error. In the case of a read transaction, the read data is transferred during the next frame, regardless of whether an SPI error has occurred.

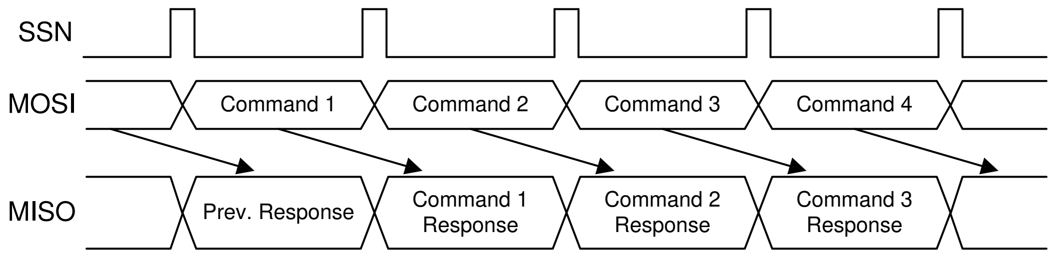


图 7-15. SPI Command and Response Sequence

The data bit on MOSI is shifted into an internal 16-bit shift register (MS-bit first) while data is simultaneously shifted out of the MISO pin. While SSN is high (bus idle), MISO is tri-stated by the open-drain driver. While SSN is low, MISO is driven according to the 16-bit data pattern being shifted out based on the prior received command. To begin a transaction at the falling edge of the SSN, MISO is driven to the MS-bit of the outbound data and is updated on each subsequent falling edge of SCK.

7.5.2 Command Frame

The command frames are the only defined frame-format that are sent from master to slave on MOSI. A command frame can be either a read command or a write command. A command frame consists of a CMD bit, six bits of ADDRESS, a PARITY bit (odd parity), and eight bits of DATA. 图 7-16 shows the format of the command frame. The bit sequence is as follows:

1. The COMMAND bit (CMD). CMD = 1 means the transfer is a write command; CMD = 0 means it is a read command.
2. Six bits of ADDRESS (A5:A0)
3. The PARITY bit (PAR). This bit is set by the following equation: PARITY = XNOR(CMD, A5..A0, D7..D0).
4. Eight bits of DATA (D7..D0). For read commands, set the DATA bits to zero.

Both the read and the write command follow the command frame format.

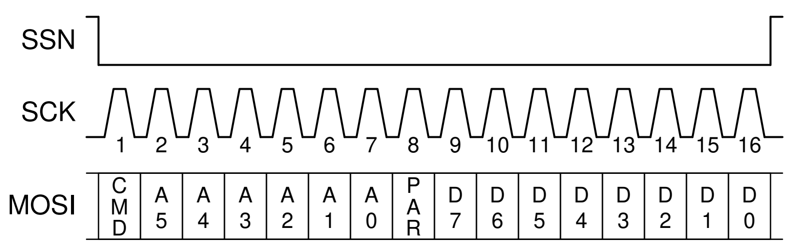


图 7-16. Command Frame Format

7.5.3 Response Frame

There are three possible response frame formats: read response, write response, and write error/POR. These formats are further described in *Write Response Frame Format* through *Write Error/POR Frame Format*.

7.5.3.1 Read Response Frame Format

The read response has the following format:

1. The SPI Error bit (SPE)
2. Five reserved bits (always '11000')
3. The Power-Cycled bit (PC)
4. The Thermal Warning bit (TW)
5. Eight bits of DATA (D7..D0) (only valid if SPE = 0)

图 7-17 shows the read response format. The frame is sent out by the TPS92520-Q1 following a read command.

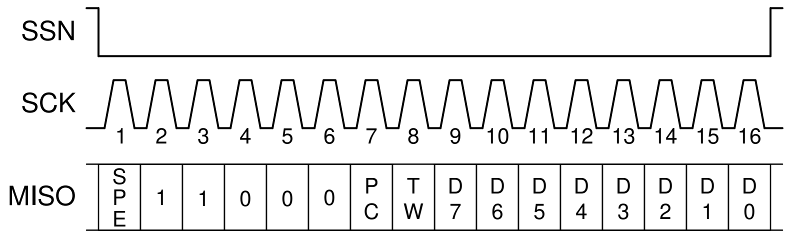


图 7-17. Read Response Frame Format

7.5.3.2 Write Response Frame Format

The write response frame has the following format:

1. The SPI Error bit (SPE)
2. The COMMAND bit (CMD)
3. Six bits of ADDRESS (A5..A0)
4. Eight bits of DATA read from the destination register (D7..D0)

图 7-18 shows the write response format. This frame is sent out following a write command if the previously received frame was a write command and no SPI error occurred during that frame.

The data bits in the write response are read back from the destination register that was just written. There is no need to issue a read command and evaluate the read response in order to check that the destination register was written correctly.

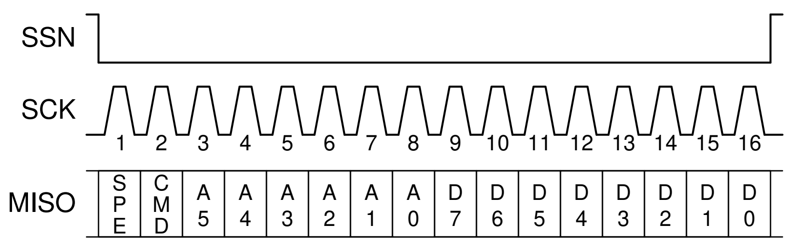


图 7-18. Write Response Frame Format

7.5.3.3 Write Error/POR Frame Format

The write error/POR frame is simply a '1' in the MSB followed by all zeroes (see 图 7-19). This frame is sent out by the TPS92520-Q1 internal digital block during the first SPI transfer following power-on reset, or following a write command with a SPI Error.

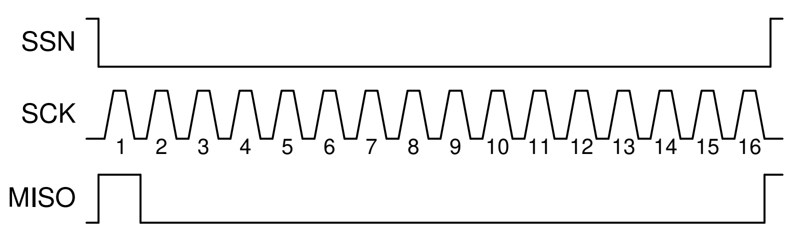


图 7-19. Write Error/POR Frame Format

7.5.4 SPI Error

The TPS92520-Q1 device records a SPI Error if any of the following conditions occur:

1. The SPI command has a non-integer multiple of 16 SCK pulses.
2. Any of the DATA bits during a read command are non-zero.
3. There is a parity error in the previously received command.

If any of these conditions are true, the TPS92520-Q1 sets the SPE bit high in the next response frame. A write command with a SPI error does not write to the register begin addressed. Similarly, a read command does not clear any active fault bits if the command has a SPI error. Additionally, if a read response has SPE = 1, the read data bits are invalid and must be disregarded.

7.5.5 SPI for Multiple Slave Devices in Parallel Configuration

The TPS92520-Q1 device can be connected in a star configuration where the SSN of each device is independently controlled by the microcontroller. 图 7-20 shows the topology when three devices are connected.

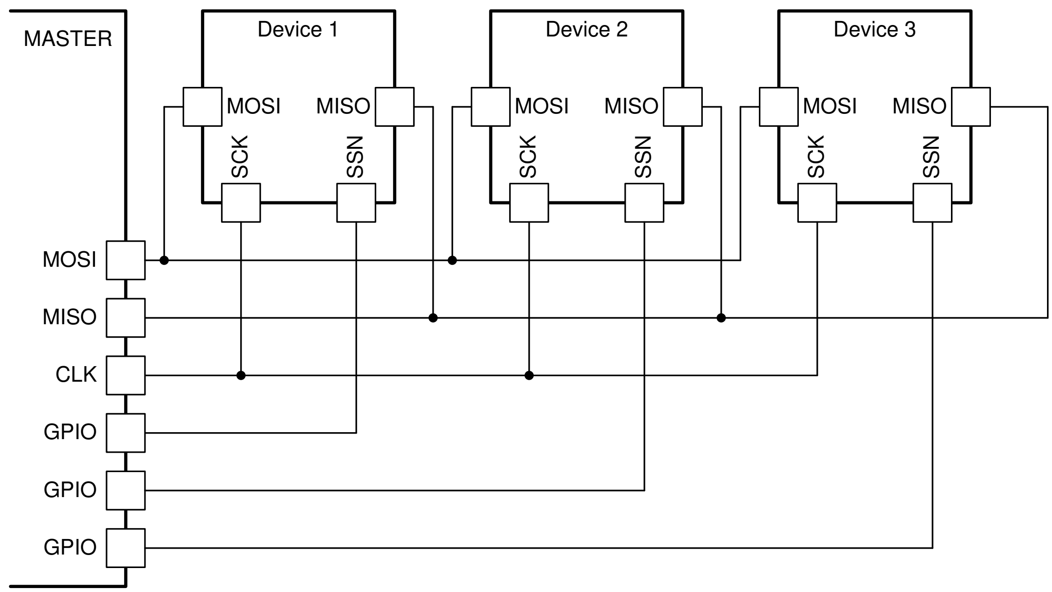


图 7-20. Parallel / Star Configuration

7.5.6 SPI for Multiple Slave Devices in Daisy Chain Configuration

The TPS92520-Q1 device can be connected in a daisy chain configuration to keep GPIO ports available when multiple devices are communicating to the same microcontroller. 图 7-21 shows the topology when three devices are connected.

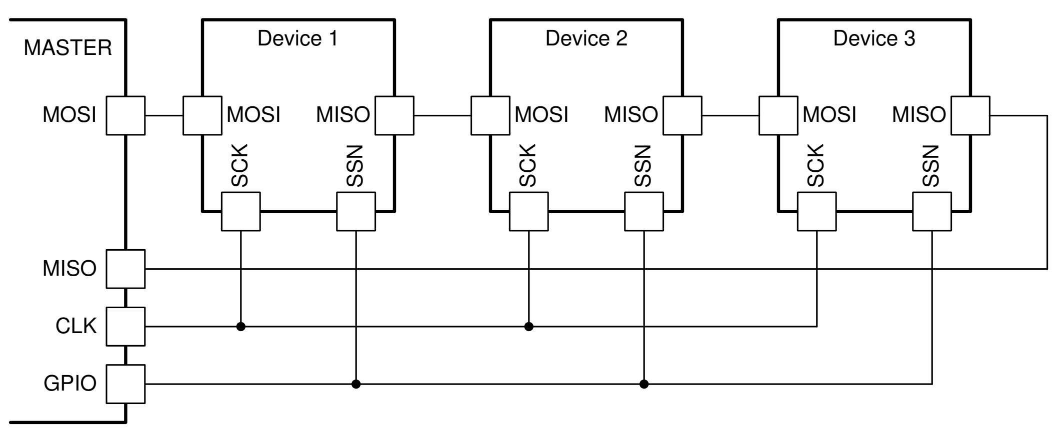


图 7-21. Daisy Chain Configuration

The data is shifted through each slave device, from MOSI input to MISO output through each device's internal 16-bit shift register. After 16 clock cycles, the data has been transferred from one device to another. The sequence continues until all data is passed through from first device, with MOSI connected to the microcontroller, to the last device, with MISO connected to the mircrontroller. On the rising edge of SSN, each device decodes the last 16 bits that were received and held in the internal shift register.

7.6 Register Maps

The SPI-accessible registers are each eight bits wide and exist in a six-bit addressable register array (0x00 through 0x3F). The registers in the TPS92520-Q1 device contain programmed information and operating status. Upon power up, the registers are reset to the default values. Writes to unlisted addresses are not permitted and can result in undesired operation. Reads of unlisted addresses return the zero value.

Reserved bits ("RESERVED") must be written with '0' values when writing. Registers are read or write unless indicated otherwise in the description of the register. 表 7-4 lists the TPS92520-Q1 register map.

表 7-4. TPS92520-Q1 Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0x00	SYSCFG1	FPINRST	PWMPH	LHSW	CMWEN	CH2INTPWM	CH2EN	CH1INTPWM	CH1EN	00010000
0x01	SYSCFG2	IFT[1:0]		CH2TSFL	CH2HSILIMFL	CH2LSILIMFL	CH1TSFL	CH1HSILIMFL	CH1LSILIMFL	00000000
0x02	CMWTAP	RESERVED				CMWTAP[3:0]				00001000
0x03	STATUS1	CH2LSILIM	CH2HSILIM	CH2SHORT	CH2COMPOV	CH1LSILIM	CH1HSILIM	CH1SHORT	CH1COMPOV	n/a
0x04	STATUS2	RESERVED		CH2TP	CH2BSTUV	CH2TOFFMIN	CH1TP	CH1BSTUV	CH1TOFFMIN	n/a
0x05	STATUS3	STANDALONE	V5AUV	CMWTO[1:0]		TW	PC	CH2STATUS	CH1STATUS	n/a
0x06	TWLMT	TWLMT[9:2]								10001010
0x07	SLEEP	RESERVED						SLEEP[1:0]		00000000
0x08	CH1IADJL	RESERVED						CH1IADJ[1:0]		00000000
0x09	CH1IADJH	CH1IADJ[9:2]								00000000
0x0A	CH2IADJL	RESERVED						CH2IADJ[1:0]		00000000
0x0B	CH2IADJH	CH2IADJ[9:2]								00000000
0x0C	PWMDIV	RESERVED					PWMDIV[2:0]			00000100
0x0D	CH1PWML	CH1PWM[7:0]								00000000
0x0E	CH1PWMH	RESERVED						CH1PWM[9:8]		00000000
0x0F	CH2PWML	CH2PWM[7:0]								00000000
0x10	CH2PWMH	RESERVED						CH2PWM[9:8]		00000000
0x11	CH1TON	RESERVED		CH1TON[5:0]						00000111
0x12	CH2TON	RESERVED		CH2TON[5:0]						00000111
0x13	CH1VIN	CH1VIN[7:0]								n/a
0x14	CH1VLED	CH1VLED[7:0]								n/a
0x15	CH1VLEDON	CH1VLEDON[7:0]								n/a
0x16	CH1VLEDOFF	CH1VLEDOFF[7:0]								n/a
0x17	CH2VIN	CH2VIN[7:0]								n/a
0x18	CH2VLED	CH2VLED[7:0]								n/a
0x19	CH2VLEDON	CH2VLEDON[7:0]								n/a
0x1A	CH2VLEDOFF	CH2VLEDOFF[7:0]								n/a
0x1B	TEMPL	RESERVED						TEMP[1:0]		n/a
0x1C	TEMPH	TEMP[9:2]								n/a
0x1D	V5D	V5D[7:0]								n/a
0x1E	LHCFG1	LHPWMPH	LHEXTIADJ	LH2100DC	LH2INTPWM	LH2EN	LH1100DC	LH1INTPWM	LH1EN	00000000
0x1F	LHCFG2	LHIFT[1:0]		LH2TSFL	LH2HSILIMFL	LH2LSILIMFL	LH1TSFL	LH1HSILIMFL	LH1LSILIMFL	00000000
0x20	LHIL	RESERVED						LHI[1:0]		n/a
0x21	LHIH	LHI[9:2]								n/a
0x22	LHIFILTL							LHIFILT[1:0]		n/a
0x23	LHIFILTH	LHIFILT[9:2]								
0x24	LH1IADJL	RESERVED						LH1IADJ[1:0]		00000000
0x25	LH1IADJH	LH1IADJ[9:2]								00000000
0x26	LH2IADJL	RESERVED						LH2IADJ[1:0]		00000000
0x27	LH2IADJH	LH2IADJ[9:2]								00000000
0x28	LHCH1PWML	LH1PWM[7:0]								00000000
0x29	LHCH1PWMH	RESERVED						LH1PWM[9:8]		00000000
0x2A	LHCH2PWML	LH2PWM[7:0]								00000000
0x2B	LHCH2PWMH	RESERVED						LH2PWM[9:8]		00000000
0x2C	LH1TON	RESERVED		LH1TON[5:0]						00000111
0x2D	LH2TON	RESERVED		LH2TON[5:0]						00000111

表 7-4. TPS92520-Q1 Register Map (continued)

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
0x2E	RESET	RESET[7:0]								00000000

Complex bit access types are encoded to fit into small table cells. 表 7-5 shows the codes that are used for access types in this section.

表 7-5. Access Type Codes

Access Type	Code	Description
W	W	Write
R	R	Read
R/W	R/W	Read and Write
RC	RC	Read to clear
-n		Value after reset or the default value

The following sections provide the descriptions for different registers.

7.6.1 Configuration Registers

The configuration registers are used to control the device operation and program the fault response. Configuration registers are read and write capable.

表 7-6. Configuration Registers

Address	Acronym	Register Name	Section
0x00	SYSCFG1	System Configuration Register 1	Section 7.6.1.1
0x01	SYSCFG2	System Configuration Register 2	Section 7.6.1.2
0x02	CMWTAP	Communication Watchdog Timer Tap Point Register	Section 7.6.1.3

7.6.1.1 SYSCFG1 Register (address = 0x00) [reset = 0x10]

The SYSCFG1 register is the first system configuration register and it contains bits associated with the enabling of channels and several device-related functions. 图 7-22 shows SYSCFG1. 表 7-7 describes SYSCFG1.

图 7-22. System Configuration Register 1 (SYSCFG1)

7	6	5	4	3	2	1	0
FPINRST	PWMPH	LHSW	CMWEN	CH2INTPWM	CH2EN	CH1INTPWM	CH1EN
W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-7. System Configuration Register 1 Field Description

Bit	Field	Type	Reset	Description
7	FPINRST	W	0	Reset open-drain fault output if there are no active faults in the system. Note that this bit is write-only. Any reads of this register return 0 in the FPINRST bit location. 0 = Do not care 1 = Reset open-drain fault output
6	PWMPH	R/W	0	PWM phase shift setting for internal PWM generator 0 = 180° phase shift between internally generated PWM signals 1 = 0° phase shift between internally generated PWM signals
5	LHSW	R/W	0	Software limp-home mode. The limp-home mode can be activated by writing to the register. The bit is also set high in case of communication failure. The bit has to be written to zero to return to normal operation. 0 = Normal Operation 1 = Operation in limp-home state
4	CMWEN	R/W	1	Communication watch dog timer 0 = Disable communication watch dog timer 1 = Enable communication watch dog timer

表 7-7. System Configuration Register 1 Field Description (continued)

Bit	Field	Type	Reset	Description
3	CH2INTPWM	R/W	0	This bit is used to enable internal PWM generator function for channel 2. 0 = LED current duty cycle of channel 2 controlled by the external signal connected to UDIM2 input 1 = LED current duty cycle of channel 2 controlled by the internal PWM generator (registers PWMDIV and CH2PWM). UDIM2 input must be above $V_{UDIM2(UVLO)}$.
2	CH2EN	R/W	0	CH2 enable. This bit controls the operation of channel 2. 0 = Disable LED channel 2 1 = Enable LED channel 2
1	CH1INTPWM	R/W	0	This bit is used to enable internal PWM generator function for channel 1. 0 = LED current duty cycle of channel 1 controlled by external signal connected to UDIM1 input 1 = LED current duty cycle of channel 1 controlled by internal PWM generator (registers PWMDIV and CH1PWM). UDIM1 input must be above $V_{UDIM1(UVLO)}$.
0	CH1EN	R/W	0	CH1 enable. This bit controls the operation of channel 1. 0 = Disable LED channel 1 1 = Enable LED channel 1

7.6.1.2 SYSCFG2 Register (address = 0x01) [reset = 0x00]

The SYSCFG2 register is the second system configuration register. This register contains bits associated with enabling fault handling for both channels and configuring the fault timer. 图 7-23 shows SYSCFG2. 表 7-8 describes SYSCFG2.

图 7-23. System Configuration Register 2 (SYSCFG2)

7	6	5	4	3	2	1	0
IFT		CH2TSFL	CH2HSILIMFL	CH2LSILIMFL	CH1TSFL	CH1HSILIMFL	CH1LSILIMFL
R/W - 00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-8. System Configuration Register 2 Field Description

Bit	Field	Type	Reset	Description
7-6	IFT	R/W	00	IFT sets the counter limit for the fault timer as shown below. 00 = 3.6 ms fault timer 01 = 7.2 ms fault timer 10 = 14.4 ms fault timer 11 = 28.8 ms fault timer
5	CH2TSFL	R/W	0	Channel 2 thermal shutdown fault response 0 = Channel 2 auto-restarts based on internal temperature hysteresis. 1 = Channel 2 is latched off; CH2EN bit is reset and channel 2 is disabled until the CH2EN bit is programmed high by SPI command.
4	CH2HSILIMFL	R/W	0	Channel 2 high-side FET current limit fault response 0 = Channel 2 auto-restarts after the ILIM fault timer has expired. 1 = Channel 2 is latched off; CH2EN bit is reset and channel 2 is disabled until the CH2EN bit is programmed high by SPI command.
3	CH2LSILIMFL	R/W	0	Channel 2 low-side FET current limit fault response 0 = Channel 2 auto-restarts after the ILIM fault timer has expired. 1 = Channel 2 is latched off; CH2EN bit is reset and channel 2 is disabled until the CH2EN bit is programmed high by SPI command.
2	CH1TSFL	R/W	0	Channel 1 thermal shutdown fault response 0 = Channel 1 auto-restarts based on internal temperature hysteresis. 1 = Channel 1 is latched off; CH1EN bit is reset and channel 1 is disabled until the CH1EN bit is programmed high by SPI command.
1	CH1HSILIMFL	R/W	0	Channel 1 high side FET current limit fault response 0 = Channel 1 auto-restarts after the ILIM fault timer has expired. 1 = Channel 1 is latched off; CH1EN bit is reset and channel 1 is disabled until the CH1EN bit is programmed high by SPI command.

表 7-8. System Configuration Register 2 Field Description (continued)

Bit	Field	Type	Reset	Description
0	CH1LSILIMFL	R/W	0	Channel 1 low side FET current limit fault response 0 = Channel 1 auto-restarts after the ILIM fault timer has expired. 1 = Channel 1 is latched off; CH1EN bit is reset and channel 1 is disabled until the CH1EN bit is programmed high by SPI command.

7.6.1.3 CMWTAP Register (address = 0x02) [reset = 0x08]

The CMWTAP register sets the tap point (that is the bit number, starting from 0) on the 25-bit communication watchdog timer to establish the timeout condition. By default, the tap point is set to bit 24. 图 7-24 shows CMWTAP. 表 7-9 describes CMWTAP.

图 7-24. Communication Watchdog Timer Tap Point Register (CMWTAP)

7	6	5	4	3	2	1	0
RESERVED				CMWTAP[3:0]			
R-0b				R/W-1000b			

表 7-9. CMWTAP-to-Tap Point Mapping

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	Reserved
3-0	CMWTAP	R/W	1000	Mapping of CMWTAP bits to the tap points 0000 = Tap point set to bit 16 corresponding to 6.1 ms (typical) watch dog period. 0001 = Tap point set to bit 17 corresponding to 12.1 ms (typical) watch dog period. 0010 = Tap point set to bit 18 corresponding to 24.3 ms (typical) watch dog period. 0011 = Tap point set to bit 19 corresponding to 48.5 ms (typical) watch dog period. 0100 = Tap point set to bit 20 corresponding to 97.1 ms (typical) watch dog period. 0101 = Tap point set to bit 21 corresponding to 194.2 ms (typical) watch dog period. 0110 = Tap point set to bit 22 corresponding to 388.3 ms (typical) watch dog period. 0111 = Tap point set to bit 23 corresponding to 776.7 ms (typical) watch dog period. 1000 through 1111 = Tap point set to bit 24 corresponding to 1.52 s (typical) watchdog period.

7.6.2 STATUS Registers

The status registers are used to report warning and fault conditions. Status registers are read-only registers. Reading the register clears the bits that are set if the condition that caused them no long exists. The clearing of the bits happens at the end of the read response SPI transfer, not at the end of the read command SPI transfer. All bits are active-high.

表 7-10. Status Registers

Address	Acronym	Register Name	Section
0x03	STATUS1	Status 1 Register (Read-Only)	Section 7.6.2.1
0x04	STATUS2	Status 2 Register (Read Only)	Section 7.6.2.2
0x05	STATUS3	Status 3 Register (Read Only)	Section 7.6.2.3

7.6.2.1 STATUS1 Register (address = 0x03)

图 7-25 shows STATUS1. 表 7-11 describes STATUS1.

图 7-25. Status 1 Register (Read-Only) (STATUS1)

7	6	5	4	3	2	1	0
CH2LSILIM	CH2HSILIM	CH2SHORT	CH2COMPOV	CH1LSILIM	CH1HSILIM	CH1SHORT	CH1COMPOV
RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 7-11. Status 1 Register Field Description

Bit	Field	Type	Reset	Description
7	CH2LSILIM	RC	0	Indicates low-side switch current limit fault on channel 2. Low-side switch current is greater than 1.5 A (typical).
6	CH2HSILIM	RC	0	Indicates high-side switch current limit fault on channel 2. High-side switch current is greater than 2.7 A (typical).
5	CH2SHORT	RC	0	Indicates output short circuit fault on channel 2. CSP pin voltage is below 2.45 V.
4	CH2COMPOV	RC	0	Indicates overvoltage condition on COMP2 pin. COMP2 pin voltage is greater than 3.2 V.
3	CH1LSILIM	RC	0	Indicates low-side switch current limit fault on channel 1. Low-side switch current is greater than 1.5 A (typical).
2	CH1HSILIM	RC	0	Indicates high-side switch current limit fault on channel 1. High-side switch current is greater than 2.7 A (typical).
1	CH1SHORT	RC	0	Indicates output short circuit fault on channel 1. CSP pin voltage is below 2.45 V.
0	CH1COMPOV	RC	0	Indicates overvoltage condition on COMP1 pin. COMP1 pin voltage is greater than 3.2 V.

7.6.2.2 STATUS2 Register (address = 0x04)

STATUS2 register is a read-only register. 图 7-26 shows STATUS2. 表 7-12 describes STATUS2.

图 7-26. Status 2 Register (Read Only) (STATUS2)

7	6	5	4	3	2	1	0
RESERVED		CH2TP	CH2BSTUV	CH2TOFFMIN	CH1TP	CH1BSTUV	CH1TOFFMIN
R-00b		RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b

表 7-12. Status 2 Register Field Description

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	Reserved
5	CH2TP	RC	0	Indicates overtemperature thermal protection for channel 2. The channel automatically restarts when the bit is cleared to 0.
4	CH2BSTUV	RC	0	Indicates bootstrap undervoltage fault condition on channel 2. BST2 pin voltage is less than 2.95 V.
3	CH2TOFFMIN	RC	0	Indicates channel 2 operation at maximum duty cycle.
2	CH1TP	RC	0	Indicates overtemperature thermal protection for channel 1. The channel automatically restarts when the bit is cleared to 0.
1	CH1BSTUV	RC	0	Indicates bootstrap undervoltage fault condition on channel 1. BST1 pin voltage is less than 2.95 V.
0	CH1TOFFMIN	RC	0	Indicates channel 1 operation at maximum duty cycle.

7.6.2.3 STATUS3 Register (address = 0x05)

STATUS3 register is a read-only register. 图 7-27 shows STATUS3. 表 7-13 describes STATUS3.

图 7-27. Status 3 Register (Read Only) (STATUS3)

7	6	5	4	3	2	1	0
STANDALONE	V5AUV	CMWTO[1:0]		TW	PC	CH2STATUS	CH1STATUS
R-0b	RC-0b	RC-00b		RC-0b	RC-1b	RC-0b	RC-0b

表 7-13. Status 3 Register Field Description

Bit	Field	Type	Reset	Description
7	STANDALONE	R	0	Indicates standalone mode. This bit can be cleared by issuing the RESET or DETECT command (see RESET register).
6	V5AUV	RC	0	Indicates V5A undervoltage fault condition.

表 7-13. Status 3 Register Field Description (continued)

Bit	Field	Type	Reset	Description
5-4	CMWTO	RC	00	Indicates the number of times the communication watchdog timer has expired. 00 = Default (normal operation) 01 = Watchdog has expired 1 time. 10 = Watchdog has expired 2 times. 11 = Watchdog has expired 3 times. Device transitions into limp-home mode.
3	TW	RC	0	Indicates overtemperature thermal warning
2	PC	RC	1	Power cycle bit is set at power up and is considered a fault. The PC bit must be cleared before the channels can be enabled.
1	CH2STATUS	RC	0	Logic OR of the fault bits for channel 2 excluding over temperature thermal warning.
0	CH1STATUS	RC	0	Logic OR of the fault bits for channel 1 excluding over temperature thermal warning.

7.6.3 Device Control Registers

The control registers are used to enable sleep mode and program the temperature warning threshold, LED current, and PWM duty cycle set points. The registers are read- and write-capable.

表 7-14. Device Control Registers

Address	Acronym	Register Name	Section
0x06	TWLMT[9:2]	Thermal Warning Limit	Section 7.6.3.1
0x07	SLEEP	Sleep Command Register	Section 7.6.3.2
0x08	CH1IADJL	Channel 1 Analog Current Control Register (LSB)	Section 7.6.3.3
0x09	CH1IADJH	Channel 1 Analog Current Control Register (MSB)	Section 7.6.3.4
0x0A	CH2IADJL	Channel 2 Analog Current Control Register (LSB)	Section 7.6.3.5
0x0B	CH2IADJH	Channel 2 Analog Current Control Register (MSB)	Section 7.6.3.6
0x0C	PWMDIV	Internal PWM Clock Divider Register	Section 7.6.3.7
0x0D	CH1PWML	Channel 1 PWM Width Register (LSB)	Section 7.6.3.8
0x0E	CH1PWMH	Channel 1 PWM Width Register (MSB)	Section 7.6.3.9
0x0F	CH2PWML	Channel 2 PWM Width Register (LSB)	Section 7.6.3.10
0x10	CH2PWMH	Channel 2 PWM Width Register (MSB)	Section 7.6.3.11
0x11	CH1TON	Channel 1 On-Time Register	Section 7.6.3.12
0x12	CH2TON	Channel 2 On-Time Register	Section 7.6.3.13

7.6.3.1 Thermal Warning Limit (address = 0x06) [reset = 0x8A]

图 7-28 shows TWLMT[9:2]. 表 7-15 describes TWLMT[9:2].

图 7-28. Thermal Warning Limit Register

7	6	5	4	3	2	1	0
TWLMT[9:2]							
R/W-10001010b							

表 7-15. Thermal Warning Limit Field Description

Bit	Field	Type	Reset	Description
7-0	TWLMT[9:2]	R/W	10001010	TWLMT[9:2] sets the Thermal Warning (TW) bit when the most significant 8 bits of the ADC reading of the TEMP value exceed the programmed value. The default value is 138 decimal, or 0x8Ah (corresponding to a temperature of 125°C).

7.6.3.2 SLEEP Command (address = 0x07) [reset = 0x00]

图 7-29 shows the SLEEP register. 表 7-16 describes the SLEEP register.

图 7-29. Sleep Command Register

7	6	5	4	3	2	1	0
RESERVED						SLEEP[1:0]	
R-000000b						R/W-00b	

表 7-16. Sleep Command Register Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	SLEEP	R/W	00	Device sleep mode. The low-power sleep mode can be activated by writing to the register. 00 = Exit sleep mode and return to normal operation (SLEEP OFF). 01 = Enter sleep mode (SLEEP ON). 10 = No effect 11 = No effect

7.6.3.3 CH1IADJL Control Register (address = 0x08) [reset = 0x00]

图 7-30 shows the CH1IADJL register. 表 7-17 describes the CH1IADJL register.

图 7-30. Channel 1 Analog Current Register (LSB)

7	6	5	4	3	2	1	0
RESERVED						CH1IADJ[1:0]	
R-000000b						R/W-00b	

表 7-17. Channel 1 Analog Current Control Register Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	CH1IADJ[1:0]	R/W	00	Channel 1 analog current control. The 2 LSBs of the 10-bit IADJ DAC for channel 1 can be programmed by writing to the register.

7.6.3.4 CH1IADJH Control Register (address = 0x09) [reset = 0x00]

图 7-31 shows the CH1IADJH register. 表 7-18 describes the CH1IADJH register.

图 7-31. Channel 1 Analog Current Control Register (MSB)

7	6	5	4	3	2	1	0
CH1IADJ[9:2]							
R/W-00000000b							

表 7-18. Channel 1 Analog Current Control Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH1IADJ[9:2]	R/W	00000000	Channel 1 analog current control. The 8 MSBs of the 10-bit IADJ DAC for channel 1 can be programmed by writing to the register.

7.6.3.5 CH2IADJL Control Register (address = 0x0A) [reset = 0x00]

图 7-32 shows the CH2IADJL register. 表 7-19 describes the CH2IADJL register.

图 7-32. Channel 2 Analog Current Control Register (LSB)

7	6	5	4	3	2	1	0
RESERVED						CH2IADJ[1:0]	
R-000000b						R/W-00b	

表 7-19. Channel 2 Analog Current Control Register Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-2	RESERVED	R	000000	Reserved
1-0	CH2IADJ[1:0]	R/W	00	Channel 2 analog current control. The 2 LSBs of the 10-bit IADJ DAC for channel 2 can be programmed by writing to the register.

7.6.3.6 CH2IADJH Control Register (address = 0x0B) [reset = 0x00]

图 7-33 shows the CH2IADJH register. 表 7-20 describes the CH2IADJH register.

图 7-33. Channel 2 Analog Current Control Register (MSB)

7	6	5	4	3	2	1	0
CH2IADJ[9:2]							
R/W-00000000b							

表 7-20. Channel 2 Analog Current Control Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH2IADJ[9:2]	R/W	00000000	Channel 2 analog current control. The 8 MSBs of the 10-bit IADJ DAC for channel 2 can be programmed by writing to the register.

7.6.3.7 PWMDIV Register (address = 0x0C) [reset = 0x04]

图 7-34 shows the PWMDIV register. 表 7-21 describes the PWMDIV register.

图 7-34. Internal PWM Clock Divider Register (LSB)

7	6	5	4	3	2	1	0
RESERVED					PWMDIV[2:0]		
R-00000b					R/W-100b		

表 7-21. Internal PWM Clock Divider Register Field Description

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000	Reserved
2-0	PWMDIV[2:0]	R/W	100	This 3-bit value selects the clock divider for the internal PWM generator. The PWM clock is derived based on typical oscillator frequency of 10.8 MHz. 000 = Divide oscillator clock by 7 (f_{PWM} = 1507 Hz). 001 = Divide oscillator clock by 8 (f_{PWM} = 1318 Hz). 010 = Divide oscillator clock by 10 (f_{PWM} = 1055 Hz). 011 = Divide oscillator clock by 12 (f_{PWM} = 879 Hz). 100 = Divide oscillator clock by 16 (f_{PWM} = 659 Hz). 101 = Divide oscillator clock by 24 (f_{PWM} = 439 Hz). 110 = Divide oscillator clock by 49 (f_{PWM} = 215 Hz). 111 = Divide oscillator clock by 98 (f_{PWM} = 108 Hz).

7.6.3.8 CH1PWML Register (address = 0x0D) [reset = 0x00]

图 7-35 shows the CH1PWML register. 表 7-22 describes the CH1PWML register.

图 7-35. Channel 1 PWM Width Register (LSB)

7	6	5	4	3	2	1	0
CH1PWM[7-0]							
R/W-00000000b							

表 7-22. Channel 1 PWM Width Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH1PWM[7:0]	R/W	00000000	Channel 1 PWM width control. The 8 LSBs of the 10-bit PWM WIDTH for channel 1 can be programmed by writing to the register.

7.6.3.9 CH1PWMH Register (address = 0x0E) [reset = 0x00]

图 7-36 shows the CH1PWMH register. 表 7-23 shows the CH1PWMH register.

图 7-36. Channel 1 PWM Width Register (MSB)

7	6	5	4	3	2	1	0
RESERVED						CH1PWM[9:8]	
R-000000b						R/W-00b	

表 7-23. Channel 1 PWM Width Register Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	CH1PWM[9:8]	R/W	00	Channel 1 PWM width control. The 2 MSBs of the 10-bit PWM WIDTH for channel 1 can be programmed by writing to the register.

7.6.3.10 CH2PWML Register (address = 0x0F) [reset = 0x00]

图 7-37 shows the CH2PWML register. 表 7-24 describes the CH2PWML register.

图 7-37. Channel 2 PWM Width Register (LSB)

7	6	5	4	3	2	1	0
CH2PWM[7:0]							
R/W-00000000b							

表 7-24. Channel 2 PWM Width Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH2PWM[7:0]	R/W	00000000	Channel 2 PWM width control. The 8 LSBs of the 10-bit PWM WIDTH for channel 2 can be programmed by writing to the register.

7.6.3.11 CH2PWMH Register (address = 0x10) [reset = 0x00]

图 7-38 shows the CH2PWMH register. 表 7-25 describes the CH2PWMH register.

图 7-38. Channel 2 PWM Width Register (MSB)

7	6	5	4	3	2	1	0
RESERVED						CH2PWM[9:8]	
R-000000b						R/W-00b	

表 7-25. Channel 2 PWM Width Register Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	CH2PWM[9:8]	R/W	00	Channel 2 PWM width control. The 2 MSBs of the 10-bit PWM WIDTH for channel 2 can be programmed by writing to the register.

7.6.3.12 CH1TON Register (address = 0x11) [reset = 0x07]

图 7-39 shows the CH1TON register. 表 7-26 describes the CH1TON register.

图 7-39. Channel 1 On-Time Register

7	6	5	4	3	2	1	0
RESERVED		CH1TON[5:0]					

图 7-39. Channel 1 On-Time Register (continued)

R-00b	R/W-000111b

表 7-26. Channel 1 On-Time Register Field Description

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	Reserved
5-0	CH1TON[5:0]	R/W	000111	Channel 1 on-time control. The pseudo-fixed switching frequency for channel 1 is set by writing to this register. Default value is set to ensure 437-kHz switching frequency.

7.6.3.13 CH2TON Register (address = 0x12) [reset = 0x07]

图 7-40 shows the CH1TON register. 表 7-27 describes the CH1TON register.

图 7-40. Channel 2 On-Time Register

7	6	5	4	3	2	1	0
RESERVED		CH2TON[5:0]					
R-00b		R/W-000111b					

表 7-27. Channel 2 On-Time Register Field Description

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	Reserved
5-0	CH2TON[5:0]	R/W	000111	Channel 2 on-time control. The pseudo-fixed switching frequency for channel 2 is set by writing to this register. Default value is set to ensure 437 kHz switching frequency.

7.6.4 ADC Measurements

The output of ADC conversion is stored in the ADC measurement registers. ADC measurement registers are read-only registers. Only the 8 MSBs from 10-bit ADC are used and the remaining 2 LSBs are ignored.

表 7-28. ADC Measurements

Address	Acronym	Register Name	Section
0x13	CH1VIN	CH1VIN Register	Section 7.6.4.1
0x14	CH1VLED	CH1VLED Register	Section 7.6.4.2
0x15	CH1VLEDON	CH1VLEDON Register	Section 7.6.4.3
0x16	CH1VLEDOFF	CH1VLEDOFF Register	Section 7.6.4.4
0x17	CH2VIN	CH2VIN Register	Section 7.6.4.5
0x18	CH2VLED	CH2VLED Register	Section 7.6.4.6
0x19	CH2VLEDON	CH2VLEDON Register	Section 7.6.4.7
0x1A	CH2VLEDOFF	CH2VLEDOFF Register	Section 7.6.4.8
0x1B	TEMPL	TEMPL Register	Section 7.6.4.9
0x1C	TEMPH	TEMPH Register	Section 7.6.4.10
0x1D	V5D	V5D Register	Section 7.6.4.11

7.6.4.1 CH1VIN Measurement (address = 0x13)

图 7-41 shows the CH1VIN register. 表 7-29 describes the CH1VIN register.

图 7-41. CH1VIN Register

7	6	5	4	3	2	1	0
CH1VIN[7:0]							
R-00000000b							

表 7-29. CH1VIN Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH1VIN	R	00000000	ADC measurement of the drain voltage node for channel 1. The VIN1 pin voltage is internally attenuated by 0.037 to achieve an 8-bit conversion ratio of 65/255 (V/dec). The full scale reading represents 65 V at VIN1 node.

7.6.4.2 CH1VLED Measurement (address = 0x14)

图 7-42 shows the CH1VLED register. 表 7-30 describes the CH1VLED register.

图 7-42. CH1VLED Register

7	6	5	4	3	2	1	0
CH1VLED[7:0]							
R-00000000b							

表 7-30. CH1VLED Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH1VLED	R	00000000	ADC measurement of the CSN1 node for channel 1. The CSN1 pin voltage is internally attenuated by 0.037 to achieve an 8-bit conversion ratio of 65/255 (V/dec). The full scale reading represents 65 V at CSN1 node.

7.6.4.3 CH1VLEDON Measurement (address = 0x15)

图 7-43 shows the CH1VLEDON register. 表 7-31 describes the CH1VLEDON register.

图 7-43. CH1VLEDON Register

7	6	5	4	3	2	1	0
CH1VLEDON[7:0]							
R-00000000b							

表 7-31. CH1VLEDON Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH1VLEDON	R	00000000	ADC measurement of the CSN1 node for channel 1 before falling edge of PWM signal.

7.6.4.4 CH1VLEDOFF Measurement (address = 0x16)

图 7-44 shows the CH1VLEDOFF register. 表 7-32 describes the CH1VLEDOFF register.

图 7-44. CH1VLEDOFF Register

7	6	5	4	3	2	1	0
CH1VLEDOFF[7:0]							
R-00000000b							

表 7-32. CH1VLEDOFF Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH1VLEDOFF	R	00000000	ADC measurement of the CSN1 node for channel 1 before rising edge of PWM signal.

7.6.4.5 CH2VIN Measurement (address = 0x17)

图 7-45 shows the CH2VIN register. 表 7-33 describes the CH2VIN register.

图 7-45. CH2VIN Register

7	6	5	4	3	2	1	0
CH2VIN[7:0]							

图 7-45. CH2VIN Register (continued)

R-00000000b

表 7-33. CH2VIN Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH2VIN	R	00000000	ADC measurement of the drain voltage node for channel 2. The VIN2 pin voltage is internally attenuated by 0.037 to achieve an 8-bit conversion ratio of 65/255 (V/dec). The full scale reading represents 65 V at VIN2 node.

7.6.4.6 CH2VLED Measurement (address = 0x18)

图 7-46 shows the CH2VLED register. 表 7-34 describes the CH2VLED register.

图 7-46. CH2VLED Register

7	6	5	4	3	2	1	0
CH2VLED[7:0]							
R-00000000b							

表 7-34. CH2VLED Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH2VLED	R	00000000	ADC measurement of the CSN2 node for channel 2. The CSN2 pin voltage is internally attenuated by 0.037 to achieve an 8-bit conversion ratio of 65/255 (V/dec). The full scale reading represents 65 V at CSN2 node.

7.6.4.7 CH2VLEDON Measurement (address = 0x19)

图 7-47 shows the CH2VLEDON register. 表 7-35 describes the CH2VLEDON register.

图 7-47. CH2VLEDON Register

7	6	5	4	3	2	1	0
CH2VLEDON[7:0]							
R-00000000b							

表 7-35. CH2VLEDON Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH2VLEDON	R	00000000	ADC measurement of the CSN2 node for channel 2 before falling edge of PWM signal.

7.6.4.8 CH2VLEDOFF Measurement (address = 0x1A)

图 7-48 shows the CH2VLEDOFF register. 表 7-36 describes the CH2VLEDOFF register.

图 7-48. CH2VLEDOFF Register

7	6	5	4	3	2	1	0
CH2VLEDOFF[7:0]							
R-00000000b							

表 7-36. CH2VLEDOFF Register Field Description

Bit	Field	Type	Reset	Description
7-0	CH2VLEDOFF	R	00000000	ADC measurement of the CSN2 node for channel 2 before rising edge of PWM signal.

7.6.4.9 TEMPL Measurement (address = 0x1B)

图 7-49 shows the TEMPL register. 表 7-37 describes the TEMPL register.

图 7-49. TEMPL Register (LSB)

7	6	5	4	3	2	1	0
RESERVED						TEMP[1:0]	
R-000000b						R-00b	

表 7-37. TEMPL Register Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	TEMP[1:0]	R	00	ADC measurement of the junction temperature. The register reports the 2 LSBs of the junction/exposed pad temperature.

7.6.4.10 TEMPH Measurement (address = 0x1C)

图 7-50 shows the TEMPH register. 表 7-38 describes the TEMPH register.

图 7-50. TEMPH Register

7	6	5	4	3	2	1	0
TEMP[9:2]							
R-00000000b							

表 7-38. TEMPH Register Field Description

Bit	Field	Type	Reset	Description
7-0	TEMP[9:2]	R	00000000	ADC measurement of the junction temperature. The register reports the 8 MSBs of the junction/exposed pad temperature.

7.6.4.11 V5D Measurement (address = 0x1D)

图 7-51 shows the V5D register. 表 7-39 describes the V5D register.

图 7-51. V5D Register

7	6	5	4	3	2	1	0
V5D[7:0]							
R-00000000b							

表 7-39. V5D Register Field Description

Bit	Field	Type	Reset	Description
7-0	V5D[7:0]	R	00000000	ADC measurement of the 5-V bias supply. The V5D pin voltage is internally attenuated by 0.45 to achieve an 8-bit conversion ratio of 5.33/255 (V/dec).

7.6.5 Limp-Home Configuration and Command Registers

The limp-home registers are used to control the device when operating in limp-home mode. Limp-home registers are read and write capable.

表 7-40. Limp-Home Configuration and Command Registers

Address	Acronym	Register Name	Section
0x1E	LHCFG1	Limp-Home Configuration Register 1	Section 7.6.5.1
0x1F	LHCFG2	Limp-Home Configuration Register 2	Section 7.6.5.2
0x20	LHIL	Limp-Home Mode External Current Reference (LSB)	Section 7.6.5.3
0x21	LHIH	Limp-Home Mode External Current Reference (MSB)	Section 7.6.5.4
0x22	LHIFILTL	Limp-Home Mode Filtered External Current Register (LSB)	Section 7.6.5.5

表 7-40. Limp-Home Configuration and Command Registers (continued)

Address	Acronym	Register Name	Section
0x23	LHIFILTH	Limp-Home Mode Filtered External Current Register (MSB)	Section 7.6.5.6
0x24	LH1IADJL	Channel 1 Limp-Home Mode Analog Current Register (LSB)	Section 7.6.5.7
0x25	LH1IADJH	Channel 1 Limp-Home Mode Analog Current Register (MSB)	Section 7.6.5.8
0x26	LH2IADJL	Channel 2 Limp-Home Mode Analog Current Register (LSB)	Section 7.6.5.9
0x27	LH2IADJH	Channel 2 Limp-Home Mode Analog Current Register (MSB)	Section 7.6.5.10
0x28	LH1PWML	Channel 1 Limp-Home Mode PWM Width Register (LSB)	Section 7.6.5.11
0x29	LH1PWMH	Channel 1 Limp-Home Mode PWM Width Register (MSB)	Section 7.6.5.12
0x2A	LH2PWML	Channel 2 Limp-Home Mode PWM Width Register (LSB)	Section 7.6.5.13
0x2B	LH2PWMH	Channel 2 Limp-Home Mode PWM Width Register (MSB)	Section 7.6.5.14
0x2C	LH1TON	Channel 1 Limp-Home Mode On-Time Register	Section 7.6.5.15
0x2D	LH2TON	Channel 2 Limp-Home Mode On-Time Register	Section 7.6.5.16

7.6.5.1 LHCFG1 Register (address = 0x1E) [reset =0x00]

The LHCFG1 register contains bits associated with the enabling of channels and several device-related functions when operating in limp-home mode. 图 7-52 shows the LHCFG1 register. 表 7-41 describes the LHCFG1 register.

图 7-52. Limp-Home Configuration Register 1 (LHCFG1)

7	6	5	4	3	2	1	0
LHPWMPH	LHEXTIADJ	LH2100D	LH2INTPWM	LH2EN	LH1100D	LH1INTPWM	LH1EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-41. Limp-Home Configuration Register 1 Field Description

Bit	Field	Type	Reset	Description
7	LHPWMPH	R/W	0	PWM phase shift setting for internal PWM generator in limp-home mode. 0 = 180° phase shift between internally-generated PWM signals 1 = 0° phase shift between internally generated PWM signals
6	LHEXTIADJ	R/W	0	This bit is used to select between internal or external current reference set point. The external reference is set by voltage on LHI pin and is converted to a 10-bit value by internal ADC. 0 = Use internal LHxIADJ register as the CHxIADJ setting in limp-home mode. 1 = Use external LHI reference as the CHxIADJ setting in limp-home mode.
5	LH2100D	R/W	0	Set channel 2 PWM duty cycle to 100% in limp-home mode. 0 = LED current duty cycle based on internal or external command 1 = LED current duty cycle set to 100%
4	LH2INTPWM	R/W	0	This bit is used to enable internal PWM generator function for channel 2 in limp-home mode. 0 = LED current duty cycle of channel 2 controlled by an external signal connected to UDIM2 input 1 = LED current duty cycle of channel 2 controlled by an internal PWM generator (registers PWMDIV and LH2PWM). UDIM2 input must be above $V_{UDIM2(UVLO)}$ threshold.

表 7-41. Limp-Home Configuration Register 1 Field Description (continued)

Bit	Field	Type	Reset	Description
3	LH2EN	R/W	0	CH2 enable. This bit controls the operation of channel 2 in limp-home mode. 0 = Disable LED channel 2. 1 = Enable LED channel 2.
2	LH1100D	R/W	0	Set channel 1 PWM duty cycle to 100% in limp-home mode. 0 = LED current duty cycle based on internal or external command 1 = LED current duty cycle set to 100%
1	LH1INTPWM	R/W	0	This bit is used to enable internal PWM generator function for channel 1 in limp-home mode. 0 = LED current duty cycle of channel 1controlled by external signal connected to UDIM1 input 1 = LED current duty cycle of channel 1 controlled by internal PWM generator (registers PWMDIV and LH1PWM). UDIM1 input must be above $V_{UDIM1(UVLO)}$ threshold.
0	LH1EN	R/W	0	CH1 enable. This bit controls the operation of channel 1 in limp-home mode. 0 = Disable LED channel 1. 1 = Enable LED channel 1.

7.6.5.2 LHCFG2 Register (address = 0x1F) [reset =0x00h]

The LHCFG2 register contains bits associated with enabling fault handling for both channels and configuring fault timer in limp-home mode. 图 7-53 shows the LHCFG2 register. 表 7-42 describes the LHCFG2 register.

图 7-53. Limp-Home Configuration Register 2 (LHCFG2)

7	6	5	4	3	2	1	0
LHIFT[1:0]		LH2TSFL	LH2HSILIMFL	LH2LSILIMFL	LH1TSFL	LH1HSILIMFL	LH1LSILIMFL
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-42. Limp-Home Configuration Register 2 Field Description

Bit	Field	Type	Reset	Description
7-6	LHIFT	R/W	00	LHIFT sets the counter limit for the ILIM fault timer in limp-home mode. 00 = 3.6 ms fault timer 01 = 7.2 ms fault timer 10 = 14.4 ms fault timer 11 = 28.8 ms fault timer
5	LH2TSFL	R/W	0	Channel 2 thermal shutdown fault response in limp-home mode 0 = Channel 2 auto-restarts based on internal temperature hysteresis. 1 = Channel 2 is latched off; CH2EN bit is reset and channel 2 is disabled until the CH2EN bit is programmed high by SPI command.
4	LH2HSILIMFL	R/W	0	Channel 2 high-side FET current limit fault response in limp-home mode 0 = Channel 2 auto-restarts after the ILIM fault timer has expired. 1 = Channel 2 is latched off; CH2EN bit is reset and channel 2 is disabled until the CH2EN bit is programmed high by SPI command.
3	LH2LSILIMFL	R/W	0	Channel 2 low-side FET current limit fault response in limp-home mode 0 = Channel 2 auto-restarts after the ILIM fault timer has expired. 1 = Channel 2 is latched off; CH2EN bit is reset and channel 2 is disabled until the CH2EN bit is programmed high by SPI command.
2	LH1TSFL	R/W	0	Channel 1 thermal shutdown fault response in limp-home mode 0 = Channel 1 auto-restarts based on internal temperature hysteresis. 1 = Channel 1 is latched off; CH1EN bit is reset and channel 1 is disabled until the CH1EN bit is programmed high by SPI command.
1	LH1HSILIMFL	R/W	0	Channel 1 high-side FET current limit fault response in limp-home mode 0 = Channel 1 auto-restarts after the ILIM fault timer has expired. 1 = Channel 1 is latched off; CH1EN bit is reset and channel 1 is disabled until the CH1EN bit is programmed high by SPI command.

表 7-42. Limp-Home Configuration Register 2 Field Description (continued)

Bit	Field	Type	Reset	Description
0	LH1LSILIMFL	R/W	0	Channel 1 low-side FET current limit fault response in limp-home mode 0 = Channel 1 auto-restarts after the ILIM fault timer has expired. 1 = Channel 1 is latched off; CH1EN bit is reset and channel 1 is disabled until the CH1EN bit is programmed high by SPI command.

7.6.5.3 LHIL Measurement (address = 0x20)

图 7-56 shows the LHI measurement register. 表 7-43 describes the LHI measurement register.

图 7-54. Limp-Home Mode External Current Reference (LSB)

7	6	5	4	3	2	1	0
RESERVED						LHI[1:0]	
R-000000b						R-00b	

表 7-43. Channel 1 Limp-Home Mode External Current Reference Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	LHI[1:0]	R	00	External current reference set point in limp-home mode. The LHI input voltage is digitized to achieve a 10-bit reference with resolution of 2.45/1023 (V/dec). The 2 LSBs of the 10-bit ADC measurement of LHI pin voltage.

7.6.5.4 LHIH Measurement (address = 0x21)

图 7-55 shows the LHIH register. 表 7-44 describes the LHIH register.

图 7-55. Limp-Home Mode External Current Reference (MSB)

7	6	5	4	3	2	1	0
LHI[9:2]							
R-00000000b							

表 7-44. Limp-Home Mode External Current Reference Field Description

Bit	Field	Type	Reset	Description
7-0	LHI[9:2]	R	00000000	External current reference in limp-home mode. The LHI input voltage is digitized to achieve a 10-bit reference with resolution of 2.45/1023 (V/dec). The 8 MSBs of the 10-bit ADC measurement of LHI pin voltage.

7.6.5.5 LHIFILTL Register (address = 0x22)

表 7-45 shows the LHIFILTL register. 表 7-46 describes the LHIFILTL register.

表 7-45. Limp-Home Mode Filtered External Current Register (LSB)

7	6	5	4	3	2	1	0
RESERVED						LHIFILT[1:0]	
R-000000b						R-00b	

表 7-46. Limp-Home Mode Filtered External Current Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	LHIFLT[1:0]	R	00	Filtered ADC measurement of LHI input. The register reports the 2-LSB of the low-pass filtered LHI input voltage. This register is only updated when LHIFILTH is read. This means that LHIFILTH must always be read first, then LHIFILTL (read LHIFILTL only if 10-bit resolution is desired).

7.6.5.6 LHIFILTH Register (address = 0x23)

表 7-47 shows the LHIFILTH register. 表 7-48 describes the LHIFILTH register.

表 7-47. Limp-Home Mode Filtered External Current Register (MSB)

7	6	5	4	3	2	1	0
LHIFILT[9:2]							
R-00000000b							

表 7-48. Limp-Home Mode Filtered External Current Register Field Description

Bit	Field	Type	Reset	Description
1-0	LHIFLT[9:2]	R	00000000	Filtered ADC measurement of LHI input. The register reports the 8-MSB of the low-pass filtered LHI input voltage. LHIFILTH register can be read repeatedly without reading LHIFILTL register if 8-bit resolution is sufficient.

7.6.5.7 LH1IADJL Register (address = 0x24) [reset = 0x00]

图 7-56 shows the LH1IADJL register. 表 7-49 describes the LH1IADJL register.

图 7-56. Channel 1 Limp-Home Mode Analog Current Register (LSB)

7	6	5	4	3	2	1	0
RESERVED						LH1IADJ[1:0]	
R-000000b						R/W-00b	

表 7-49. Channel 1 Limp-Home Mode Analog Current Register Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	LH1IADJ[1:0]	R/W	00	Channel 1 analog current control in limp-home mode. The 2 LSBs of the 10-bit IADJ DAC for channel 1 can be programmed by writing to the register.

7.6.5.8 LH1IADJH Register (address = 0x25) [reset = 0x00]

图 7-57 shows the LH1IADJH register. 表 7-50 describes the LH1IADJH register.

图 7-57. Channel 1 Limp-Home Mode Analog Current Register (MSB)

7	6	5	4	3	2	1	0
LH1IADJ[9:2]							
R/W-00000000b							

表 7-50. Channel 1 Limp-Home Mode Analog Current Register Field Description

Bit	Field	Type	Reset	Description
7-0	LH1IADJ[9:2]	R/W	00000000	Channel 1 analog current control in limp-home mode. The 8 MSBs of the 10-bit IADJ DAC for channel 1 can be programmed by writing to the register.

7.6.5.9 LH2IADJL Register (address = 0x26) [reset = 0x00]

图 7-58 shows the LH2IADJL register. 表 7-51 describes the LH2IADJL register.

图 7-58. Channel 2 Limp-Home Mode Analog Current Register (LSB)

7	6	5	4	3	2	1	0
RESERVED						LH2IADJ[1:0]	
R-000000b						R/W-00b	

表 7-51. Channel 2 Limp-Home Mode Analog Current Register Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved

表 7-51. Channel 2 Limp-Home Mode Analog Current Register Field Description (continued)

Bit	Field	Type	Reset	Description
1-0	LH2IADJ[1:0]	R/W	00	Channel 2 analog current control in limp-home mode. The 2 LSBs of the 10-bit IADJ DAC for channel 2 can be programmed by writing to the register.

7.6.5.10 LH2IADJH Register (address = 0x27) [reset = 0x00]

图 7-59 shows the LH2IADJH register. 表 7-52 describes the LH2IADJH register.

图 7-59. Channel 2 Limp-Home Mode Analog Current Register (MSB)

7	6	5	4	3	2	1	0
LH2IADJ[9:2]							
R/W-00000000b							

表 7-52. Channel 2 Limp-Home Mode Analog Current Register Field Description

Bit	Field	Type	Reset	Description
7-0	LH2IADJ[9:2]	R/W	00000000	Channel 2 analog current control in limp-home mode. The 8 MSBs of the 10-bit IADJ DAC for channel 2 can be programmed by writing to the register.

7.6.5.11 LH1PWML Register (address = 0x28) [reset = 0x00]

图 7-60 shows the LH1PWML register. 表 7-53 describes the LH1PWML register.

图 7-60. Channel 1 Limp-Home Mode PWM Width Register (LSB)

7	6	5	4	3	2	1	0
LH1PWM[7:0]							
R/W-00000000b							

表 7-53. Channel 1 Limp-Home Mode PWM Width Register Field Description

Bit	Field	Type	Reset	Description
7-0	LH1PWM[7:0]	R/W	00000000	Channel 1 PWM width control in limp-home mode. The 8 LSBs of the 10-bit PWM WIDTH for channel 1 can be programmed by writing to the register.

7.6.5.12 LH1PWMH Register (address = 0x29) [reset = 0x00]

图 7-61 shows the LH1PWMH register. 表 7-54 describes the LH1PWMH register.

图 7-61. Channel 1 Limp-Home Mode PWM Width Register (MSB)

7	6	5	4	3	2	1	0
RESERVED						LH1PWM[9:8]	
R-000000b						R/W-00b	

表 7-54. Channel 1 Limp-Home Mode PWM Width Register Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	LH1PWM[9:8]	R/W	00	Channel 1 PWM width control in limp-home mode. The 2 MSBs of the 10-bit PWM WIDTH for channel 1 can be programmed by writing to the register.

7.6.5.13 LH2PWML Register (address = 0x2A) [reset = 0x00]

图 7-62 shows the LH2PWML register. 表 7-55 describes the LH2PWML register.

图 7-62. Channel 2 Limp-Home Mode PWM Width Register (LSB)

7	6	5	4	3	2	1	0
LH2PWM[7:0]							

图 7-62. Channel 2 Limp-Home Mode PWM Width Register (LSB) (continued)

R/W-00000000b

表 7-55. Channel 2 Limp-Home Mode PWM Width Register Field Description

Bit	Field	Type	Reset	Description
7-0	LH2PWM[7:0]	R/W	00000000	Channel 2 PWM width control in limp-home mode. The 8 LSBs of the 10-bit PWM WIDTH for channel 2 can be programmed by writing to the register.

7.6.5.14 LH2PWMH Register (address = 0x2B) [reset = 0x00]

图 7-63 shows the LH2PWMH register. 表 7-56 describes the LH2PWMH register.

图 7-63. Channel 2 Limp-Home Mode PWM Width Register (MSB)

7	6	5	4	3	2	1	0
RESERVED						LH2PWM[9:8]	
R-000000b						R/W-00b	

表 7-56. Channel 2 Limp-Home Mode PWM Width Register Field Description

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	Reserved
1-0	LH2PWM[9:8]	R/W	00	Channel 2 PWM width control in limp-home mode. The 2 MSBs of the 10-bit PWM WIDTH for channel 2 can be programmed by writing to the register.

7.6.5.15 LH1TON Register (address = 0x2C) [reset = 0x07]

图 7-64 shows the LH1TON register. 表 7-57 describes the LH1TON register.

图 7-64. Channel 1 Limp-Home Mode On-Time Register

7	6	5	4	3	2	1	0
RESERVED		LH1TON[5:0]					
R-00b		R/W-000111b					

表 7-57. Channel 1 Limp-Home Mode On-Time Register Field Description

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	Reserved
5-0	LH1TON[5:0]	R/W	000111	Channel 1 on-time control in limp-home mode. The pseudo-fixed switching frequency for channel 1 is set by writing to this register. Default value is set to ensure 437-kHz switching frequency.

7.6.5.16 LH2TON Register (address = 0x2D) [reset = 0x07]

图 7-65 shows the LH2TON register. 表 7-58 describes the LH2TON register.

图 7-65. Channel 2 Limp-Home Mode On-Time Register

7	6	5	4	3	2	1	0
RESERVED		LH2TON[5:0]					
R-00b		R/W-000111b					

表 7-58. Channel 2 Limp-Home Mode On-Time Register Field Description

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	Reserved
5-0	LH2TON[5:0]	R/W	000111	Channel 2 on-time control in limp-home mode. The pseudo-fixed switching frequency for channel 2 is set by writing to this register. Default value is set to ensure 437-kHz switching frequency.

7.6.6 RESET Register (address = 0x2E) (Write-Only)

图 7-66 shows the RESET register. 表 7-59 describes the RESET register. RESET command does not reset the PC bit in the STATUS3 register to the power-on default value.

图 7-66. RESET Register

7	6	5	4	3	2	1	0
RESET[7:0]							
W-00000000b							

表 7-59. RESET Register Field Description

Bit	Field	Type	Reset	Description
7-0	RESET	W	00000000	Write 0xC3 to the RESET register to reset all writable registers to their default values. If the logic is in stand-alone mode, writing 0xC3 returns the channel enable state machines to the LOAD state. Watchdog timer is disabled.
				Write 0xD4 to the RESET register to reset all writable registers to their default values. If the logic is in stand-alone mode, reading the STATUS3 register to clear the CMWTO bits and then writing 0xD4 to the RESET register returns the channel enable state machines to the DETECT state. Watchdog timer is enabled.
				This register is write-only. Reads of this register return 0.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

图 8-1 shows a schematic of a typical application for the TPS92520-Q1.

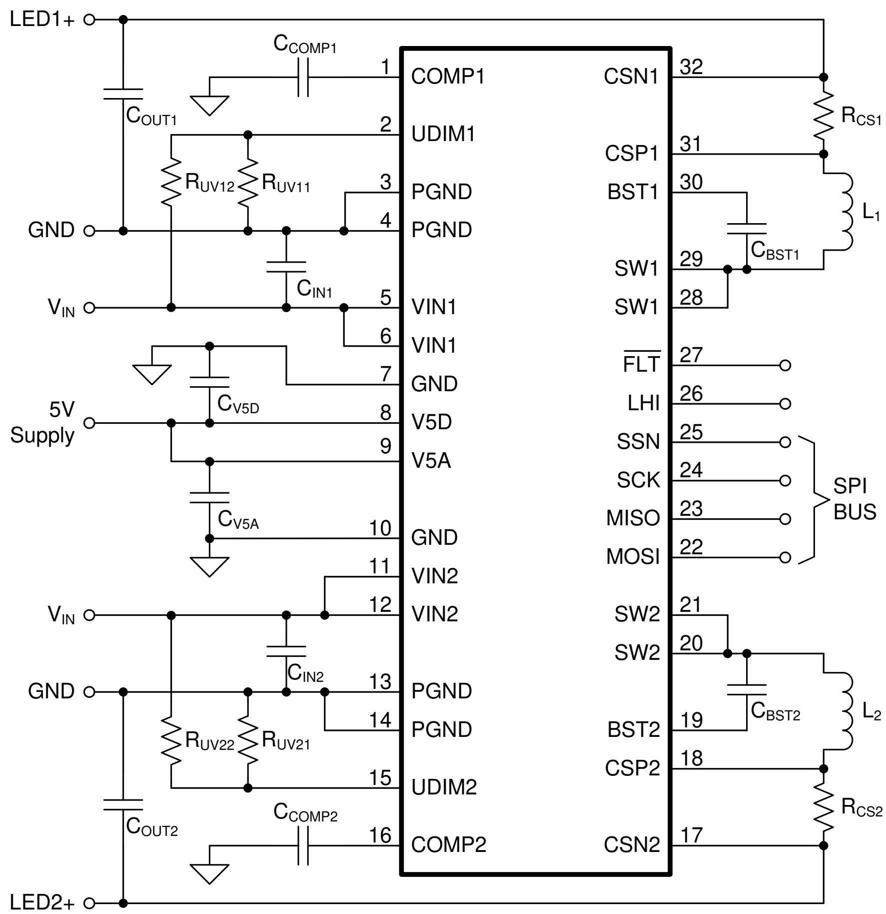


图 8-1. Buck LED Driver

8.1.1 Duty Cycle Consideration

The switch duty cycle, D, defines the converter operation and is a function of the input and output voltages. In steady state, the duty cycle is defined using 方程式 15:

$$D = \frac{V_{CSN}}{V_{IN}} \tag{15}$$

There is no limitation for small duty cycles, since at low duty cycles, the switching frequency is reduced as needed to always ensure current regulation. The maximum duty cycle attainable is limited by the minimum off-time duration and is a function of switching frequency.

8.1.2 Switching Frequency Selection

Nominal switching frequency (t_{ON} > $t_{ON(MIN)}$) is set by programming the CHxTON register. The switching varies slightly over operating range and temperature based on converter efficiency. 表 8-1 shows common switching frequencies and corresponding CHxTON register values.

表 8-1. Frequency Setting

FREQUENCY	CHxTON REGISTER VALUE (DECIMAL)	CHxTON REGISTER VALUE (BINARY)
220 kHz	3	000011
437 kHz	7	000111
1.064 MHz	19	010011
1.66 MHz	31	011111
2.23 MHz	43	101011

8.1.3 LED Current Set Point

The LED current is set by the external resistor, R_{CS}, and the CHxIADJ register value. The current sense resistor, R_{CS}, is selected to meet the maximum LED current specification and 90% of the full-scale range of CHxIADJ-DAC.

$$R_{CS} = \frac{0.9 \times V_{DAC(FS)}}{14 \times I_{LED(MAX)}} \quad (16)$$

The LED current can be varied between minimum and maximum specified limits by writing to the CHxIADJ register.

8.1.4 Inductor Selection

The inductor is sized to meet the ripple specification at 50% duty cycle. TI recommends a minimum of 30% peak-to-peak inductor ripple to ensure periodic switching operation. Use 方程式 17 to calculate the inductor value.

$$L = \frac{V_{IN(TYP)}}{4 \times \Delta i_L \times f_{SW}} \quad (17)$$

Use 方程式 18 and 方程式 19 to calculate the RMS and peak currents through the inductor. It is important that the inductor is rated to handle these currents.

$$i_{L(RMS)} = \sqrt{\left(I_{LED(MAX)}^2 + \frac{\Delta i_{L(MAX)}^2}{12}\right)} \quad (18)$$

$$i_{L(PK)} = I_{LED(MAX)} + \frac{\Delta i_{L(MAX)}}{2} \quad (19)$$

8.1.5 Output Capacitor Selection

The output capacitor value depends on the total series resistance of the LED string, r_D, and the switching frequency, f_{SW}. The capacitance required for the target LED ripple current is calculated using *方程式 20*.

$$C_{OUT} = \frac{\Delta i_{L(MAX)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED}} \quad (20)$$

For applications where the converter supports pixel beam or matrix LED loads, additional design considerations influence the selection of output capacitor. The size of the output capacitor depends on the slew-rate control of the LED bypass switches and must be carefully selected while considering the overshoot current created by the dv/dt of the bypass switch.

When choosing the output capacitors, it is important to consider the ESR and ESL characteristics since they directly impact the LED current ripple. Ceramic capacitors are the best choice due to the following:

- Low ESR
- High ripple current rating
- Long lifetime
- Good temperature performance

With ceramic capacitor technology, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions. TI recommends an X7R dielectric with a voltage rating greater than maximum LED stack voltage.

8.1.6 Input Capacitor Selection

The input capacitor buffers the input voltage for transient events and decouples the converter from the supply. TI recommends a 2.2-µF input capacitor across the VIN pin and PGND placed close to the device, and connected using wide traces. X7R-rated ceramic capacitors are the best choice due to the low ESR, high ripple current rating, and good temperature performance. Additional capacitance can be required to further limit the input voltage deviation during PWM dimming operation.

8.1.7 Bootstrap Capacitor Selection

The bootstrap capacitor biases the high-side gate driver during the high-side FET on-time. The required capacitance depends on the PWM dimming frequency, PWM_{FREQ}, and is sized to avoid boot undervoltage and fault during PWM dimming operation. The bootstrap capacitance, C_{BST}, is calculated using 方程式 21.

$$C_{BST} = \frac{I_{Q(BST)}}{\left(V_{5D} + V_{BST(HYS)} - V_{BST(UV)}\right) \times PWM_{FREQ}} \tag{21}$$

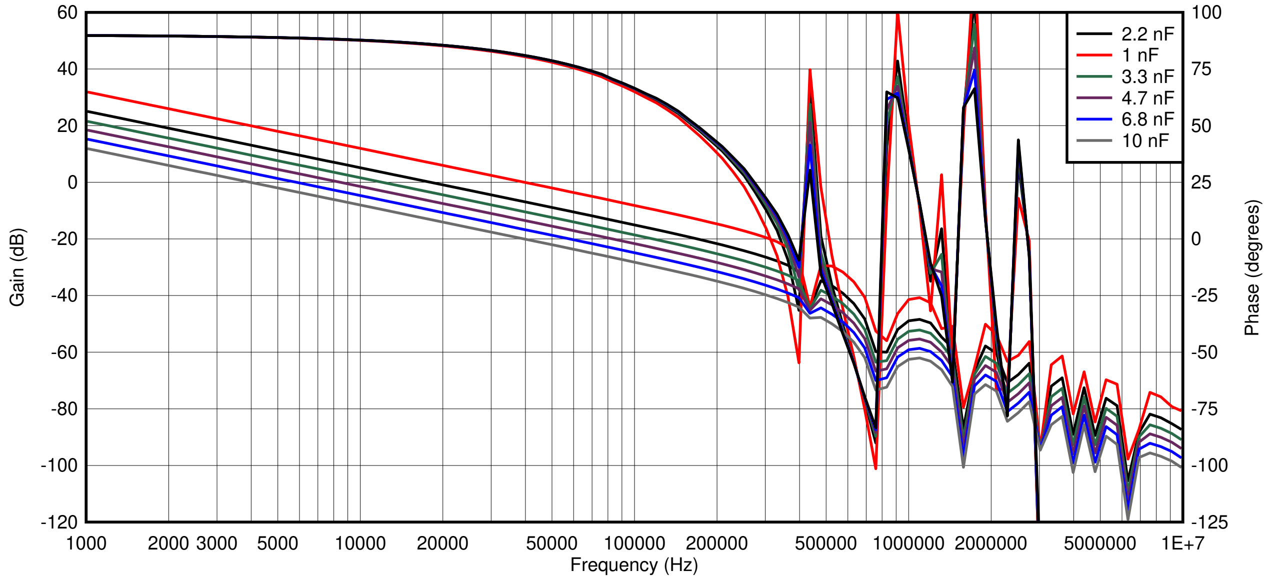
表 8-2 summarizes the TI recommended bootstrap capacitor value for different PWM dimming frequencies.

表 8-2. Bootstrap Capacitor Value

PWM DIMMING FREQUENCY (Hz)	BOOTSTRAP CAPACITOR (µF)
1507	0.1
1318	0.15
1055	0.22
879	0.22
659	0.33
439	0.47
215	1
108	2

8.1.8 Compensation Capacitor Selection

A simple integral compensator is recommended to achieve stable operation across the wide operating range. The bode plot of the loop gain with different compensation capacitors is shown in Simulated Bode Plot of Loop Gain. The buck converter behaves as a single pole system with additional phase lag caused by the switching behavior. The gain and phase margin is then determined by the choice of the switching frequency and is independent of other design parameters. TI recommends a 1-nF to 10-nF capacitor to achieve bandwidth between 4 kHz and 40 kHz. The choice of compensation capacitor impacts the transient response, the shunt FET dimming behavior and PWM dimming performance. A larger compensation capacitor (lower bandwidth) is recommended to limit the LED current overshoot on the rising edge of internal or external PWM signal. A smaller compensation capacitor (higher bandwidth) is recommend to improve shunt FET dimming response.



L = 68 µH, f_{SW} = 437 kHz

图 8-2. Simulated Bode Plot of Loop Gain

8.1.9 Input Undervoltage Protection

图 8-1 shows that the undervoltage protection threshold is programmed using a resistor divider, R_{UV1} and R_{UV2}, from the input voltage, V_{IN}, to ground. Use 方程式 22 and 方程式 23 to calculate the resistor values.

$$R_{UVx2} = \frac{V_{HYS}}{I_{UDIM(UVLO)}} \tag{22}$$

$$R_{UVx1} = \frac{V_{UDIM(RISE)}}{V_{INx(RISE)} - V_{UDIM(RISE)}} \times R_{UVx2} \tag{23}$$

8.1.10 CSN Protection Diode

An external Schottky diode is selected to protect the CSP / CSN node by clamping the negative voltage during short circuit transient. The Schottky diode should be selected based on the length of the cable harness and the choice of output capacitor. A Schottky diode with low forward voltage drop at room-temperature and non-repetitive peak surge current rating of 10 A for duration of 5 µs is recommended. The diode should be located close to the CSN pin.

8.2 Typical Application

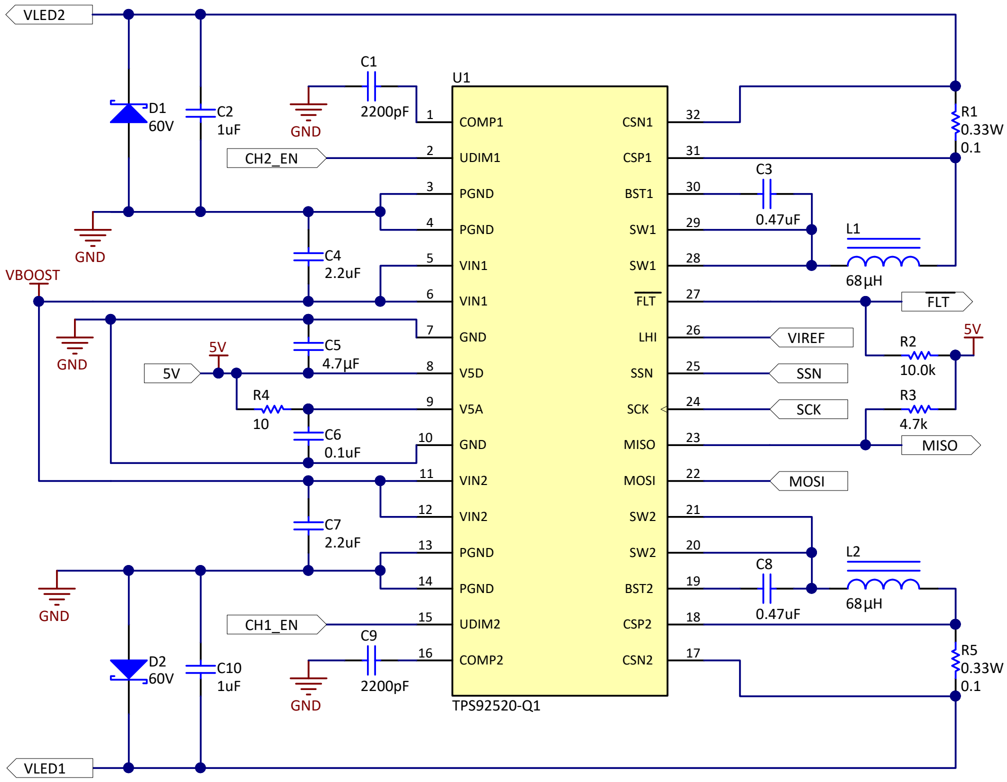


图 8-3. Application Schematic

8.2.1 Design Requirements

表 8-3. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage		58	60	62	V
N_S	Number of LEDs		1		16	
V_{FLED}	LED forward voltage drop		2.8	3	3.4	V
r_D	LED string series resistance	N x $r_{D(LED)}$	0.1		1.6	Ω
V_{OUT}	Output voltage	Ns x V_{FLED}	2.8		54.4	V
I_{LED}	LED current		100		1600	mA
Δi_{LED}	LED current ripple	Defined as percentage peak-to-peak at maximum LED current. 5 % of maximum LED current.			80	mA
Δi_L	Inductor current ripple	Defined as percentage peak-to-peak at maximum LED current		30		%
$V_{IN(RISE)}$	Start input voltage	Input voltage rising		54		V
$V_{IN(FALL)}$	Stop input voltage	Input voltage falling		52		V
f_{PWM}	PWM frequency			439		Hz
D_{PWM}	PWM dimming duty cycle		4		100	%
f_{SW}	Switching frequency			437		kHz
T_A	Ambient temperature			25		°C

8.2.1.1 Detailed Design Procedure

8.2.1.1.1 Calculating Duty Cycle

Solve for duty cycle D, D_{MAX}, and D_{MIN}:

$$D_{MAX} = \frac{V_{OUT(MAX)}}{V_{IN(MIN)}} = \frac{54.4}{58} = 0.938 \tag{24}$$

$$D_{MIN} = \frac{V_{OUT(MIN)}}{V_{IN(MAX)}} = \frac{2.8}{62} = 0.0452 \tag{25}$$

8.2.1.1.2 Calculating Minimum On-Time and Off-Time

Solve for minimum on-time, $t_{ON(DMIN)}$ at minimum duty cycle and minimum off-time, $t_{OFF(DMAX)}$ at maximum duty cycle:

$$t_{ON(DMIN)} = \frac{V_{OUT(MIN)}}{V_{IN(MAX)}} \times \frac{1}{f_{SW}} = \frac{2.8}{62} \times \frac{1}{437 \times 10^{3}} = 103.3 \times 10^{-9} \tag{26}$$

$$t_{ON(DMAX)} = \frac{V_{OUT(MAX)}}{V_{IN(MIN)}} \times \frac{1}{f_{SW}} = \frac{54.4}{58} \times \frac{1}{437 \times 10^{3}} = 142 \times 10^{-9} \tag{27}$$

8.2.1.1.3 Minimum Switching Frequency

Confirm minimum switching frequency at $t_{ON(DMIN)}$, $f_{SW(MIN)}$:

$$f_{SW(MIN)} = \frac{V_{OUT(MIN)}}{t_{ON(DMIN)} \times V_{IN(MAX)}} = \frac{2.8}{103.3 \times 10^{-9} \times 62} = 437.2 \times 10^{3} \tag{28}$$

For the design specification, $t_{ON(DMIN)} > t_{ON(MIN)}$ and $f_{SW(MIN)} = f_{SW}$.

8.2.1.1.4 LED Current Set Point

Solve for sense resistor, R_{CS}:

$$R_{CS} = \frac{0.9 \times V_{DAC(FS)}}{14 \times I_{LED(MAX)}} = \frac{0.9 \times 2.45}{14 \times 1.6} = 0.0984 \tag{29}$$

A standard resistor of 100 mΩ with tolerance better than 1 % and low temperature coefficient is selected.

8.2.1.1.5 Inductor Selection

The inductor is selected to meet the recommended 30% peak-to-peak inductor ripple specification:

$$L = \frac{V_{IN(TYP)}}{4 \times \Delta i_{L} \times f_{SW}} = \frac{V_{IN(TYP)}}{4 \times 0.3 \times I_{LED(MAX)} \times f_{SW}} = \frac{60}{4 \times 0.3 \times 1.6 \times 437x10^{3}} = 71.5 \times 10^{-6} \tag{30}$$

The closest standard capacitor is 68 μH.

- Lower inductor values increase the peak-to-peak inductor current, which minimizes size and cost at the expense of reduced efficiency and larger output capacitor.
- Higher inductance values decrease the peak-to-peak inductor current, which increases efficiency but reduces the operating range based on minimum sense voltage ripple, $\Delta V_{(CSP-CSN)}$ specification.

8.2.1.1.6 Output Capacitor Selection

The minimum output capacitance is selected to meet the LED current ripple specification:

$$C_{OUT} = \frac{\Delta i_{L(MAX)}}{8 \times f_{SW} \times r_{D(MAX)} \times \Delta i_{LED(MAX)}} = \frac{0.48}{8 \times 437 \times 10^{3} \times 1.6 \times 80 \times 10^{-3}} = 1.07 \times 10^{-6} \quad (31)$$

A standard 1-µF, 100-V X7R capacitor is selected.

8.2.1.1.7 Bootstrap Capacitor Selection

Referring to 表 8-2, a standard 470-nF, 16-V X7R capacitor is selected to support PWM frequency of 439 Hz.

8.2.1.1.8 Compensation Capacitor Selection

A compensation capacitor of 2.2 nF is selected to achieve balanced transient response between PWM dimming and shunt FET dimming.

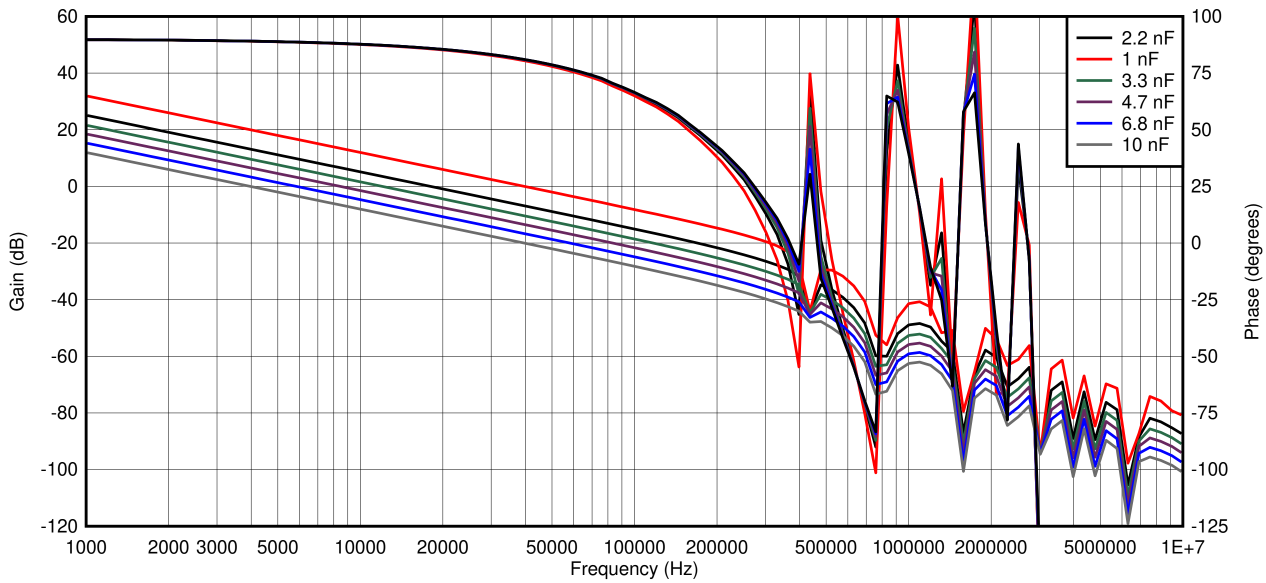
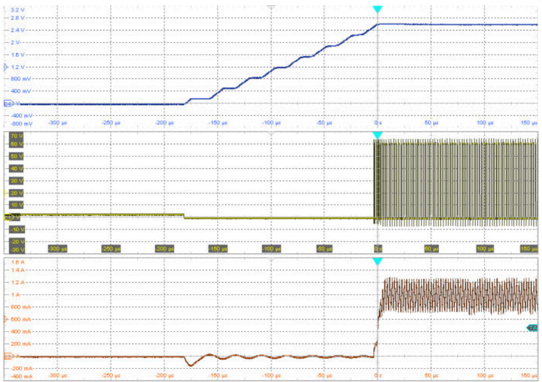


图 8-4. Simulated Buck Converter Bode Plot

8.2.1.1.9 External Channel Enable and PWM dimming

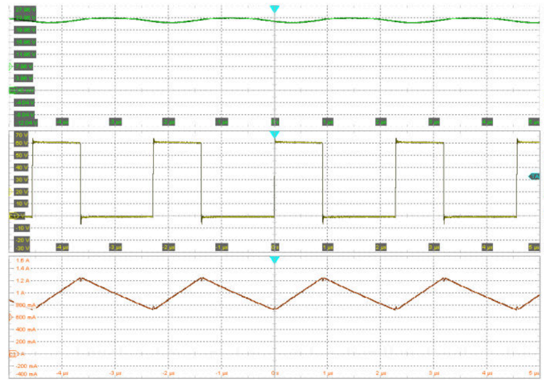
The device channel enable function and external PWM signal is achieved by controlling UDIM input via microcontroller. The device modulates the LED current based on the PWM duty cycle of the external signal. Input undervoltage lockout function is implemented by reading the VIN register value sampled by ADC. Refer to the 节 7.3.12 section for further details regarding ADC sampling and measurement.

8.2.2 Application Curves



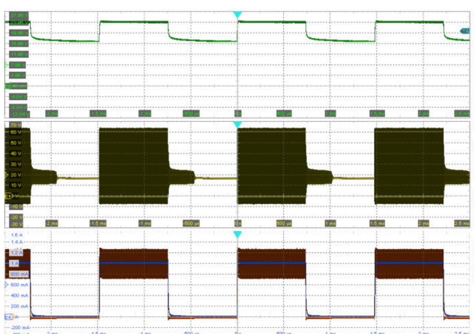
Ch1: SW voltage (10 V/div); Ch3: Inductor current (200 mA/div); Ch4: COMP voltage (400 mV/div); Time: 50 µs/div

图 8-5. Start-up Transient



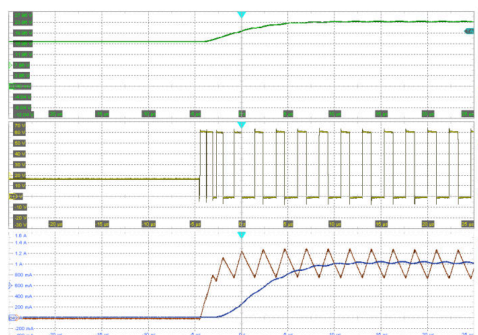
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Time: 1 µs/div

图 8-6. Normal Operation



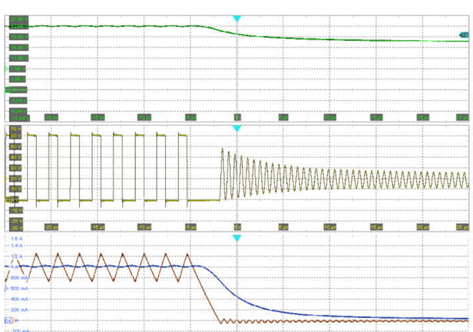
Ch1: SW voltage (10V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 500 µs/div

图 8-7. Internal PWM Dimming Transient



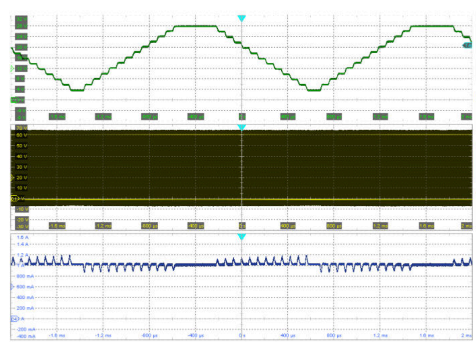
Ch1: SW voltage (10V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 5 µs/div

图 8-8. Internal PWM Dimming (Rising Edge)



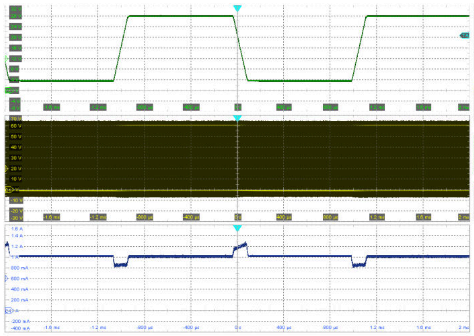
Ch1: SW voltage (10V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 5 µs/div

图 8-9. Internal PWM Dimming (Falling Edge)



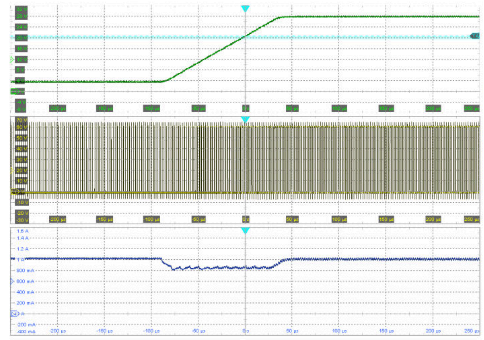
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch4: LED current (200 mA/div); Time: 400 µs/div

图 8-10. Shunt Dimming with Matrix Manager



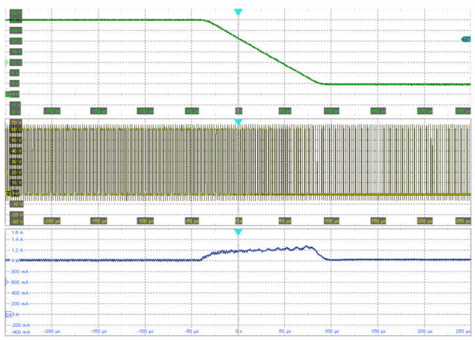
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch4: LED current (200 mA/div); Time: 400 µs/div

图 8-11. Shunt Dimming (LEDs ON-OFF Transient)



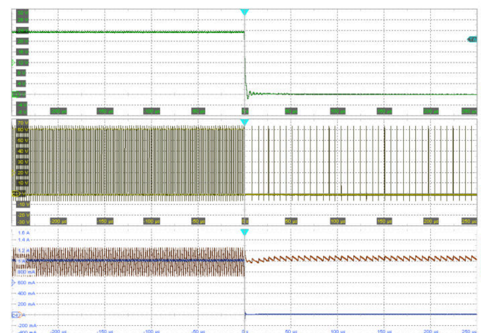
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch4: LED current (200 mA/div); Time: 50 µs/div

图 8-12. Shunt Dimming (LEDs OFF to LEDs ON)



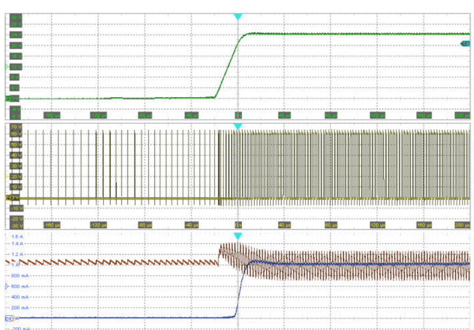
Ch1: SW voltage (10 V/div); Ch2: Output voltage (4 V/div); Ch4: LED current (200 mA/div); Time: 50 µs/div

图 8-13. Shunt Dimming (LEDs ON to LEDs OFF)



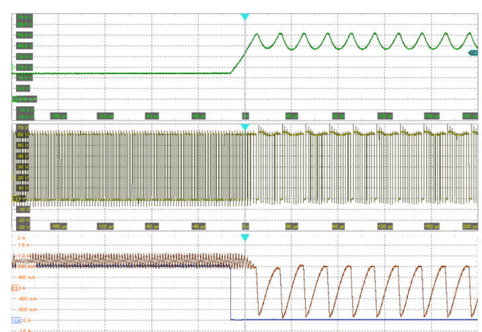
Ch1: SW voltage (10V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 50 µs/div

图 8-14. Output Short Circuit Fault



Ch1: SW voltage (10V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (200 mA/div); Ch4: LED current (200 mA/div); Time: 40 µs/div

图 8-15. Output Short Circuit Fault Recovery



Ch1: SW voltage (10V/div); Ch2: Output voltage (4 V/div); Ch3: Inductor current (400 mA/div); Ch4: LED current (200 mA/div); Time: 40 µs/div

图 8-16. Output Open Circuit Fault

8.3 Initialization Setup

The device is enabled with default watchdog timer on power up, $V_{5D} > V_{5D(POR)}$.

8.3.1 Initialize Device without Watchdog timer

The following steps must be implemented before the default watchdog timer times out in 1.55 s (typ).

1. Read register 0x05 to clear the PC (Power Cycle) bit (D2).
2. Write byte 0x00 to register 0x00. This will set bit D7 to 0 and reset $\overline{\text{FLT}}$ indicator. It also set bit D4 to 0 and disable the watchdog timer and bit .
3. Configure the device by writing to registers 0x00 to 0x02 and 0x06 to 0x12. The channels are disabled by setting CHxEN to 0 (register 0x00 bits D2 and D0).
4. Enable channels by setting ChxEN bits to 1. Write D2 and D0 bits to 1 in register 0x00.

If the watchdog timer is not disabled or the device does not receive a valid SPI command in 1.55 s after power up, the device will transition to standalone mode. The operation in standalone mode can be detected by reading register 0x05. If bit D7 is set then the device is operating in standalone mode. To exit standalone mode, write byte 0xC3.

8.3.2 Initialize Device with Watchdog Timer

The following steps must be implemented before the default watchdog timer times out in 1.55 s (typ).

1. Read register 0x05 to clear the PC (Power Cycle) bit (D2).
2. Write byte 0x10 to register 0x00. This will set bit D7 to 0 and reset the $\overline{\text{FLT}}$ indicator. Watchdog timer enabled by setting bit D4 to 1.
3. To change the default watchdog timeout value, modify the contents of register 0x02 to select the desired watchdog timeout period.
4. Repeatedly write or read a register within the specified period in step 2 in order to avoid triggering a watchdog timer time out event.
5. Configure the device by writing to registers 0x00 to 0x02 and 0x06 to 0x12. The channels are disabled by setting CHxEN to 0 (register 0x00 bits D2 and D0).
6. Enable channels by setting ChxEN bits to 1. Write D2 and D0 bits to 1 in register 0x00.

If the watchdog timer is not disabled or the device does not receive a valid SPI command in 1.55 s after power up, the device will transition to standalone mode. The operation in standalone mode can be detected by reading register 0x05. If bit D7 is set then the device is operating in standalone mode. To exit standalone mode, write byte 0xD4 to register 0x2E.

8.3.3 Limp-Home Mode

The following steps must be implemented to program the limp-home mode.

1. Enable limp-home mode by enabling watchdog timer by setting D4 bit to 1 in register 0x00.
2. Configure limp-home mode by writing to registers 0x1E to 0x2D.
3. Test limp-home configuration by toggling LHSW bit (D5) in register 0x00.

9 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 4.5 V and 65 V. The input can be a car battery or another preregulated power supply. Additional bulk capacitance or an input filter can be required in addition to the ceramic bypass capacitors to address converter stability, noise, and EMI concerns.

10 Layout

10.1 Layout Guidelines

The performance of any switching converter depends as much on the layout of the PCB as the component selection. The following guidelines can help you design a PCB with the best power converter performance.

- Place ceramic high-frequency bypass capacitors as close as possible to the TPS92520-Q1 VIN and PGND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the PGND pins.
- Place bypass capacitors for V5D and V5A close to the pins and ground the capacitors to device ground.
- Differentially route the CSP and CSN pins to sense resistor. Route the traces away from noisy nodes, preferably through a layer on the other side of a shielding/ground layer.
- Use ground plane in one of the middle layers for noise shielding.
- Make VIN and ground connection as wide as possible. This reduces any voltage drops on the input of the converter and maximizes efficiency.

10.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt from pulsing currents in switching converters. The larger the area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimize radiated EMI is to identify the pulsing current path and minimize the area of the path. In buck converters, the pulsing current path is from the VIN side of the input capacitors through the HS switch, through the LS switch, and then returns to the ground of the input capacitor.

High-frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic capacitors as close as possible to the VIN and PGND pins is the key to EMI reduction.

The PCB copper connection of the SW pin to the inductor must be as short as possible and just wide enough to carry the LED current without excessive heating. Short, thick traces or, copper pours (shapes), must be used for high current conduction path to minimize parasitic resistance. Place the output capacitor close to the CSN pin and grounded closely to the PGND pin.

10.1.1.1 Ground Plane

TI recommends using one of the middle layers as a solid ground plane. The ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. Connect the GND and PGND pins to the ground plane using vias right next to the bypass capacitors. PGND pins are connected to the source of the internal LS switch. They must be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations.

10.2 Layout Example

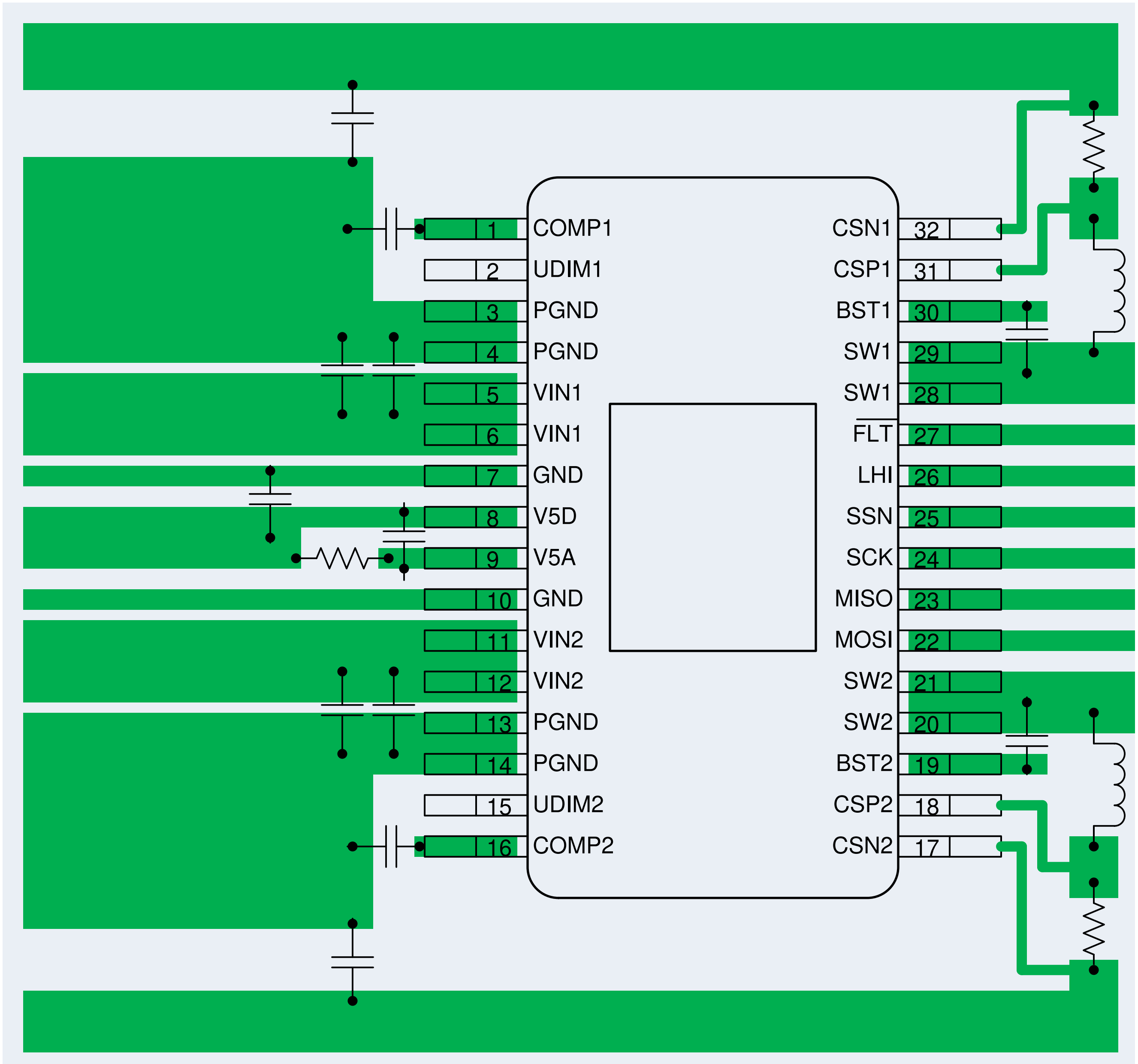


图 10-1. TPS92520-Q1 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS92520-Q1 Launchpad Evaluation Module User's Guide*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.4 Trademarks

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11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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