

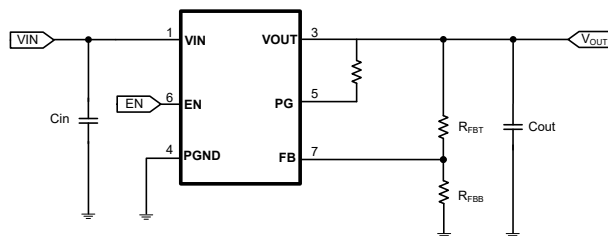
TPSM86325x 3-V to 17-V Input, 3-A, Synchronous Buck Module in QFN Package

1 Features

- Features and configured for a wide range of applications
 - 3-V to 17-V input voltage range
 - 0.6-V to 10-V output voltage range for TPSM863252
 - 0.6-V to 5.5-V output voltage range for TPSM863257
 - Fixed 3.3-V output voltage for TPSM863253
 - 0.6-V reference voltage
 - ± 1 % reference accuracy at 25°C
 - ± 1.5 % reference accuracy at –40°C to 125°C
 - Integrated 55-mΩ and 24-mΩ MOSFETs
 - 100-μA low quiescent current
 - 1.2-MHz switching frequency
 - Maximum 95 % large duty cycle operation
 - Precision EN threshold voltage
 - 1.6-ms fixed typical soft-start time
- Ease of use and small design size
 - TPSM863252 Eco-mode, TPSM863257 forced continuous conduction (FCCM) mode at light loading
 - Fast transient D-CAP3™ control mode
 - Easy layout with integrated bootstrap capacitor and inductor
 - Support start-up with prebiased output voltage
 - Open-drain power-good indicator
 - Non-latch for OV, OT, and UVLO protection
 - Hiccup mode in UV protection
 - Cycle-by-cycle OC and NOC protection
 - 40°C to 125°C operating junction temperature
 - 3.3-mm × 4-mm × 2-mm QFN package

2 Applications

- [Merchant network and server PSU](#)
- [Other AC/DC adapters/PSU](#)
- [Factory automation and control](#)
- [Test and measurement](#)



Simplified Schematic

3 Description

The TPSM86325x is a simple, easy-to-use, high-efficiency, high-power density, synchronous buck module with input voltage ranging from 3 V to 17 V and supports up to 3-A continuous current.

The TPSM86325x employs D-CAP3 control mode to provide a fast transient response and to support low-ESR output capacitors with no requirement for external compensation. The device can support up to 95% duty cycle operation.

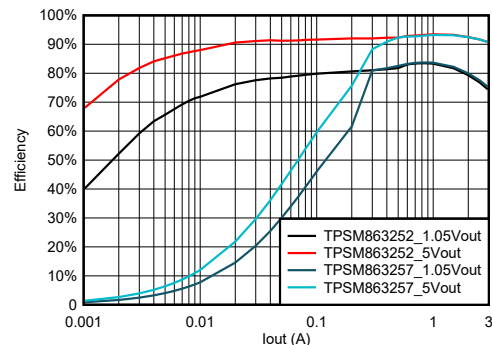
The TPSM863252 operates in Eco-mode, which maintains high efficiency during light loading. The TPSM863257 operates in FCCM mode, which keeps the same frequency and lower output ripple during all load conditions. TPSM863253 is fixed 3.3-V output voltage part with FCCM mode. The device integrates complete protection through OVP, OCP, UVLO, OTP, and UVP with hiccup.

The device is available in a QFN package. The junction temperature is specified from –40°C to 125°C.

Device Information

PART NUMBER ⁽⁴⁾	MODE	OUTPUT VOLTAGE	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TPSM863252	ECO	0.6 V to 10 V	RDX (QFN-FCMOD, 7)	4.00 mm × 3.30 mm
TPSM863257	FCCM	0.6 V to 5.5 V		
TPSM863253 ⁽³⁾	FCCM	3.3 V		

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- Advance information (not Production Data).
- See the [Family Devices](#) table.



TPSM86325x Efficiency at $V_{IN} = 12\text{ V}$



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2023) to Revision B (September 2023)	Page
• Added TPSM863253 to the document.....	1

Changes from Revision * (March 2023) to Revision A (June 2023)	Page
• Changed document status from Advance Information to Production Data.....	1

5 Family Devices

PART NUMBER	CURRENT (A)	OUTPUT VOLTAGE (V)	MODE
TPSM863252	0 to 3	0.6 to 10	Eco
TPSM863253 ⁽¹⁾	0 to 3	3.3	FCCM
TPSM863257	0 to 3	0.6 to 6	FCCM
TPSM861253	0 to 1	3.3	FCCM

(1) Advance information (not Production Data).

6 Pin Configuration and Functions

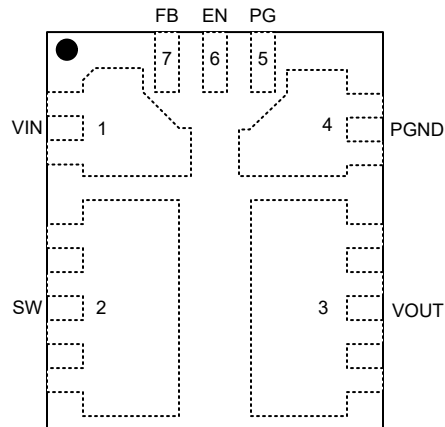


Figure 6-1. TPSM863252, TPSM863257 RDX Package, 7-Pin QFN-FCMOD (Top View)

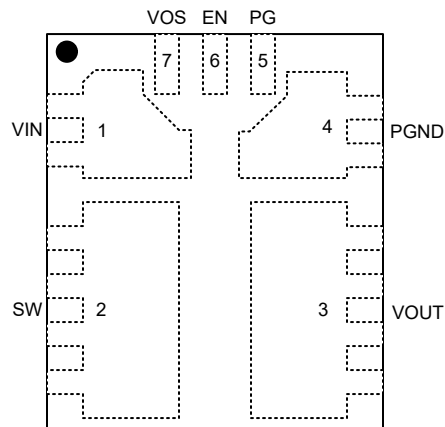


Figure 6-2. TPSM863253 RDX Package, 7-Pin QFN-FCMOD (Top View)

Table 6-1. Pin Functions

Pin		Type ⁽¹⁾	Description
Name	NO.		
VIN	1	P	Input voltage supply pin. Connect the input decoupling capacitors between VIN and GND.
SW	2	NC	Switch pin of the power stage. Do not connect, leave floating.
VOUT	3	P	Output connection. Connect recommended output capacitance from VOUT to PGND.
PGND	4	G	Power ground connection
PG	5	A	Power-good open drain output. PG pin can be floating.
EN	6	A	Enable pin of buck converter. Drive EN high to turn on the converter; drive EN low to turn off the converter. Internal pulldown to GND by a resistor.
FB	7	A	Converter feedback input. Connect to the center tap of the resistor divider between output voltage and ground.
VOS	7	A	TPSM863253: Converter feedback input. Connect to Vout directly.

(1) A = Analog, P = Power, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN	-0.3	18	V
Input voltage	FB, EN, PG	-0.3	6	V
Input voltage	GND	-0.3	0.3	V
Output voltage	VOUT(TPSM863252)	-0.3	11	V
Output voltage	VOUT(TPSM863257)	-0.3	6	V
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G
Operating Junction Temperature Range, TJ		-40	150	°C
Storage temperature, Tstg	Storage temperature, Tstg	-55	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	± 500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN	3		17	V
Input voltage	FB, EN, PG	-0.1		5.5	V
Input voltage	GND	-0.1		0.1	V
Output voltage	VOUT(TPSM863252)	-0.1		10	V
Output voltage	VOUT(TPSM863253)		3.3		V
Output voltage	VOUT(TPSM863257)	-0.1		5.5	V
Output current	IO	0		3	A
T _J	Operating junction temperature	-40		125	°C
Tstg	Storage temperature	-40		150	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPSM86325x		
		RDX		
		7 PINS		
				UNIT
R _{θJA}	Junction-to-ambient thermal resistance	61.3		°C/W
R _{θJA_effective}	Junction-to-ambient thermal resistance on EVM board	40 ⁽²⁾		°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	60.8		°C/W

7.4 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		TPSM86325x	
		RDX	
		7 PINS	
			UNIT
R _{θJB}	Junction-to-board thermal resistance	20.0	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	7.5	°C/W
Y _{JB}	Junction-to-board characterization parameter	19.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) This R_{θJA}_effective is tested on TPSM863252EVM board (4 layer board, copper thickness of top and bottom layer are 2 oz, and copper thickness of internal GND is 1 oz) at V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3 A, TA = 25°C.

7.5 Electrical Characteristics

Over operating T_J = -40°C - 125°C, V_{VIN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
V _{IN}	Input voltage range	V _{IN}	3		17	V
I _{VIN}	VIN Supply Current	No load, V _{EN} = 5 V, non-switching, PSM version		100		μA
		No load, V _{EN} = 5 V, non-switching, FCCM version		370		μA
I _{INSDN}	VIN Shutdown Current	No load, V _{EN} = 0 V		2		μA
UVLO						
UVLO	VIN Undervoltage Lockout	Wake up VIN voltage	2.8	2.9	3.0	V
UVLO	VIN Undervoltage Lockout	Shut down VIN voltage	2.6	2.7	2.8	V
UVLO	VIN Undervoltage Lockout	Hysteresis VIN voltage		200		mV
FEEDBACK VOLTAGE						
V _{FB}	FB voltage	T _J = 25°C	594	600	606	mV
V _{FB}	FB voltage	T _J = -40°C to 125°C	591	600	609	mV
V _{OUT} ⁽²⁾	TPSM863253 output voltage	T _J = 0°C to 65°C	3.27	3.3	3.33	V
V _{OUT} ⁽²⁾	TPSM863253 output voltage	T _J = -40°C to 125°C	3.25	3.3	3.35	V
MOSFET						
R _{DS(ON)HI}	High-side MOSFET R _{ds(on)}	T _J = 25°C, V _{VIN} ≥ 5 V		55		mΩ
		T _J = 25°C, V _{VIN} = 3 V ⁽¹⁾		68		mΩ
R _{DS(ON)LO}	Low-side MOSFET R _{ds(on)}	T _J = 25°C, V _{VIN} ≥ 5 V		24		mΩ
		T _J = 25°C, V _{VIN} = 3 V		30		mΩ
DUTY CYCLE and FREQUENCY CONTROL						
F _{SW}	Switching Frequency	T _J = 25°C, V _{VOUT} = 3.3 V		1.2		MHz
T _{OFF(MIN)} ⁽¹⁾	Minimum Off-time	V _{FB} = 0.5 V		110		ns
T _{ON(MIN)}	Minimum On-time			60		ns
CURRENT LIMIT						
I _{OCL_LS}	Over Current threshold	Valley current set point	3.1	4.1	5.1	A
I _{NOCL}	Negative Over Current threshold	Valley current set point	1.5	2.0	2.5	A
LOGIC THRESHOLD						
V _{EN(ON)}	EN Threshold High-level		1.15	1.20	1.25	V
V _{EN(OFF)}	EN Threshold Low-level		0.90	1.00	1.10	V

7.5 Electrical Characteristics (continued)

Over operating $T_J = -40^{\circ}\text{C} - 125^{\circ}\text{C}$, $V_{VIN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ENHYS}	EN Hysteresis			200		mV
REN1	EN Pull down resistor			2		M Ω
OUTPUT DISCHARGE and SOFT START						
t_{SS}	Internal Soft-start Time			1.6		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP Trip Threshold		110	115	120	%
t_{OVPDLY}	OVP Prop deglitch			24		us
V_{UVP}	UVP Trip Threshold		55	60	65	%
t_{UVPDLY}	UVP Prop deglitch			220		us
t_{UVPEN}	Output Hiccup enable delay relative to SS time	UVP detect		14		ms
PGOOD						
TPGDLY	PG Start-up Delay	PG from low to high		1		ms
TPGDLY	PG Start-up Delay	PG from high to low		28		us
VPGTH	PG Threshold	VFB falling (fault)	80	85	90	%
VPGTH	PG Threshold	VFB rising (good)	85	90	95	%
VPGTH	PG Threshold	VFB rising (fault)	110	115	120	%
VPGTH	PG Threshold	VFB falling (good)	105	110	115	%
VPG_L	PG Sink Current Capability	IOL = 4 mA			0.4	V
IPGLK	PG Leak Current	VPGOOD = 5.5 V			1	uA
THERMAL PROTECTION						
$T_{OTP}^{(1)}$	OTP Trip Threshold			155		$^{\circ}\text{C}$
$T_{OTPHSY}^{(1)}$	OTP Hysteresis			20		$^{\circ}\text{C}$

- (1) Specified by design
(2) Advance information (not Production Data).

7.6 Typical Characteristics

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

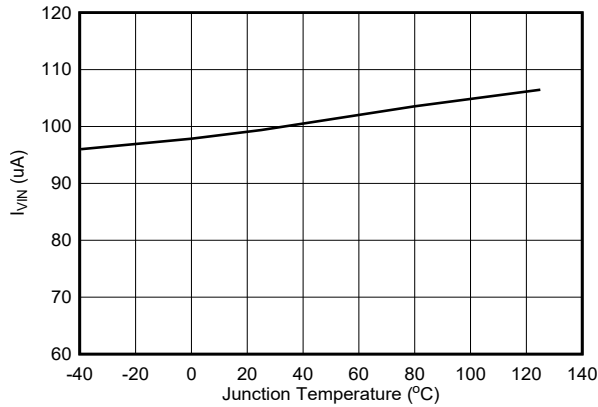


Figure 7-1. TPSM863252 Quiescent Current

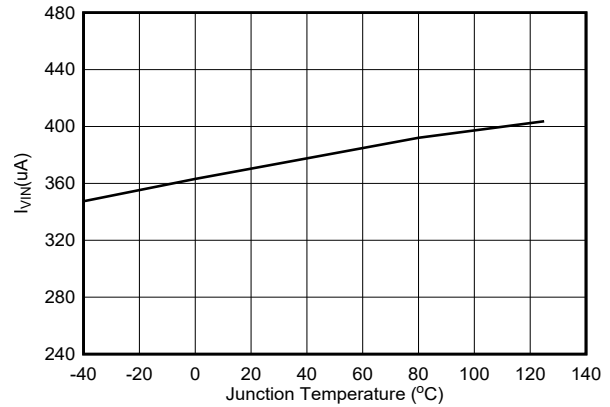


Figure 7-2. TPSM863257 Quiescent Current

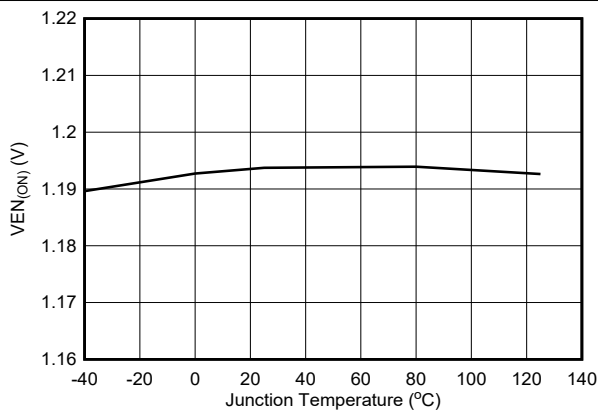


Figure 7-3. Enable On Threshold Voltage

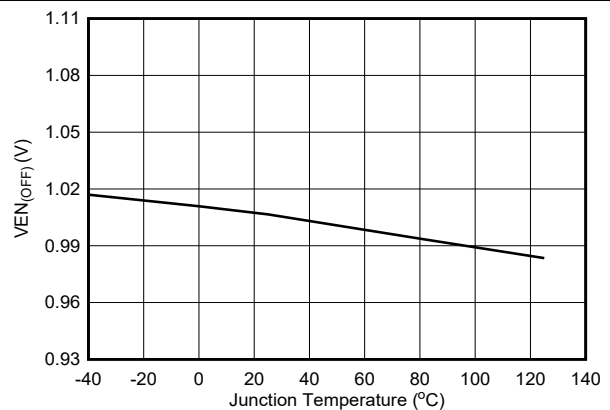


Figure 7-4. Enable Off Threshold Voltage

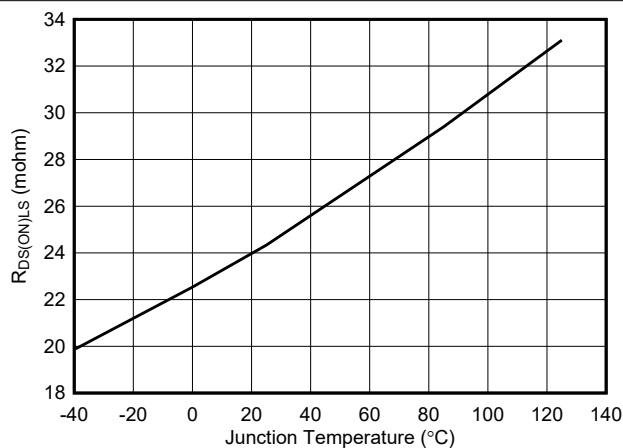


Figure 7-5. Low-Side $R_{DS(ON)}$

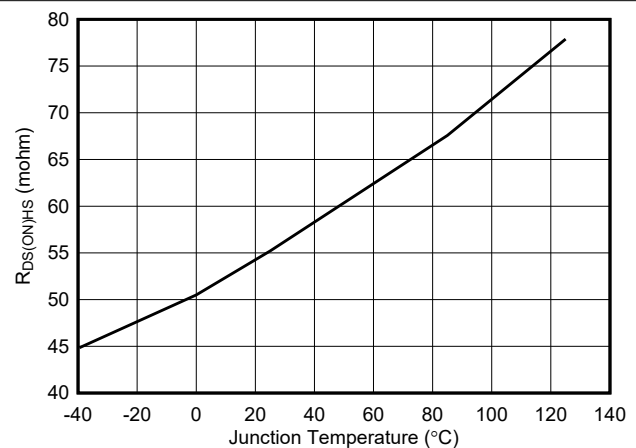


Figure 7-6. High-Side $R_{DS(ON)}$

7.6 Typical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

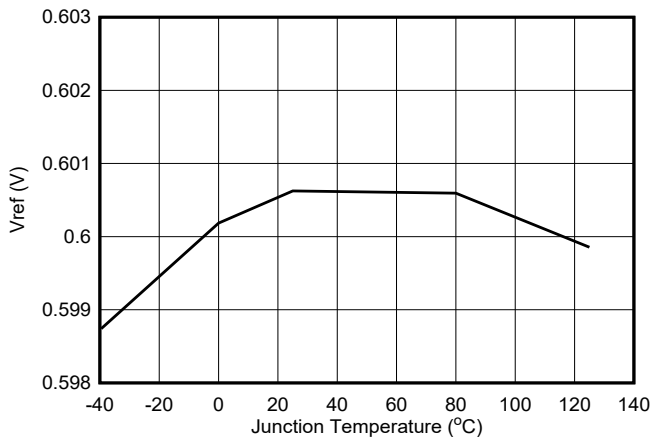


Figure 7-7. VREF Voltage

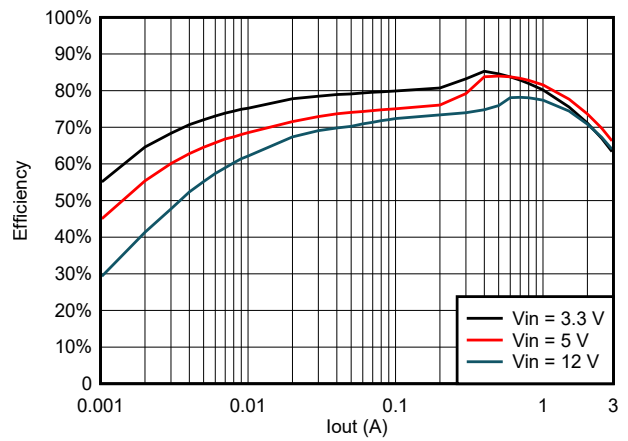


Figure 7-8. TPSM863252 Efficiency at 0.6 V_{OUT}

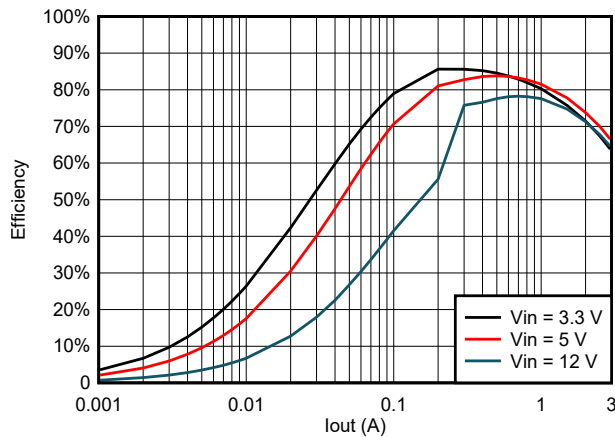


Figure 7-9. TPSM863257 Efficiency at 0.6 V_{OUT}

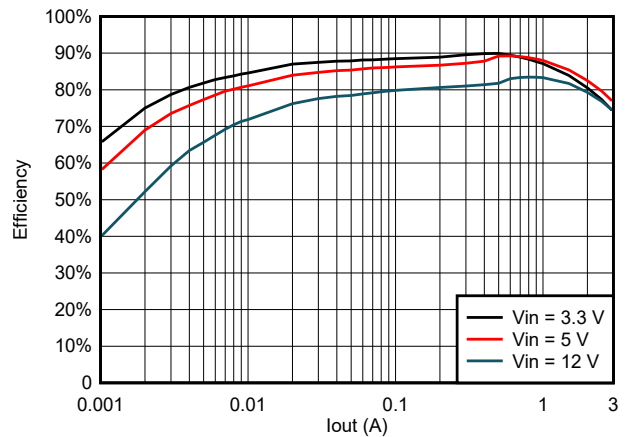


Figure 7-10. TPSM863252 Efficiency at 1.05 V_{OUT}

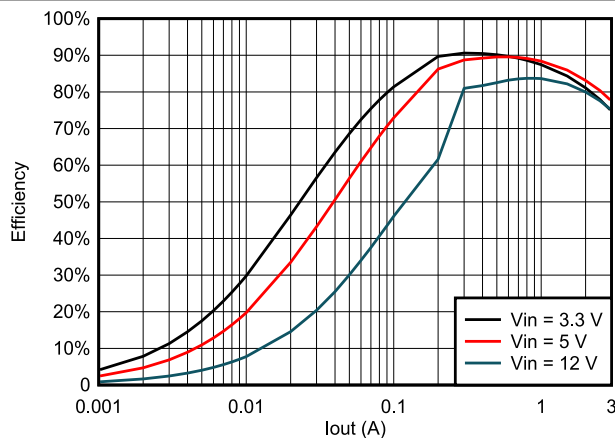


Figure 7-11. TPSM863257 Efficiency at 1.05 V_{OUT}

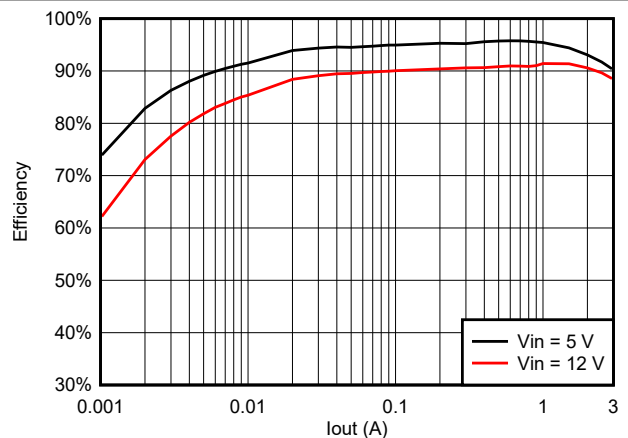


Figure 7-12. TPSM863252 Efficiency at 3.3 V_{OUT}

7.6 Typical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

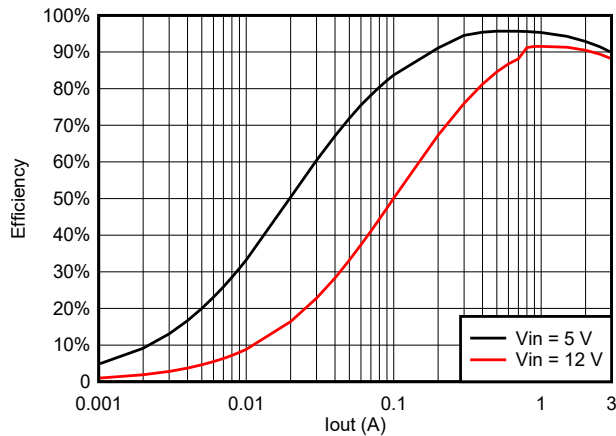


Figure 7-13. TPSM863257 Efficiency at 3.3 V_{OUT}

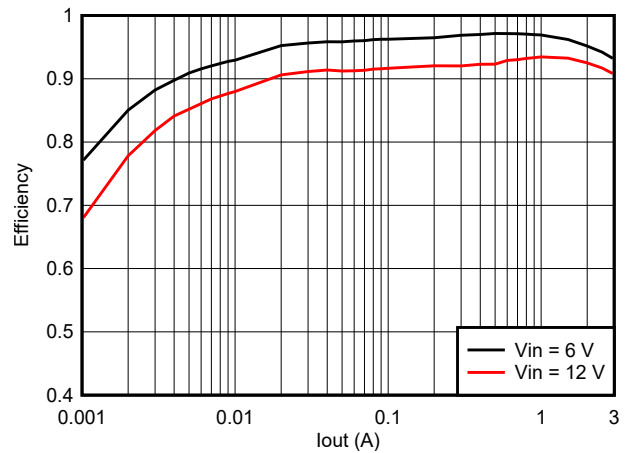


Figure 7-14. TPSM863252 Efficiency at 5 V_{OUT}

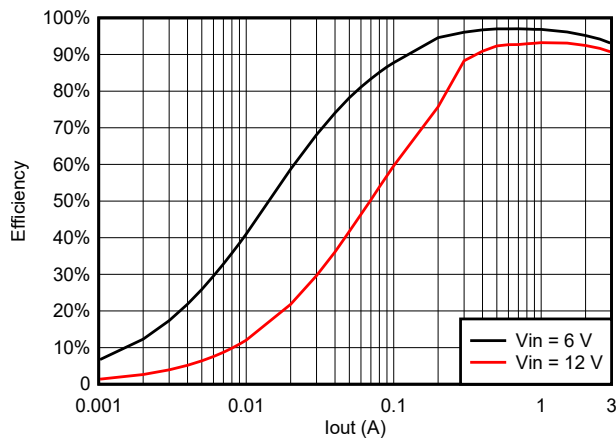


Figure 7-15. TPSM863257 Efficiency at 5 V_{OUT}

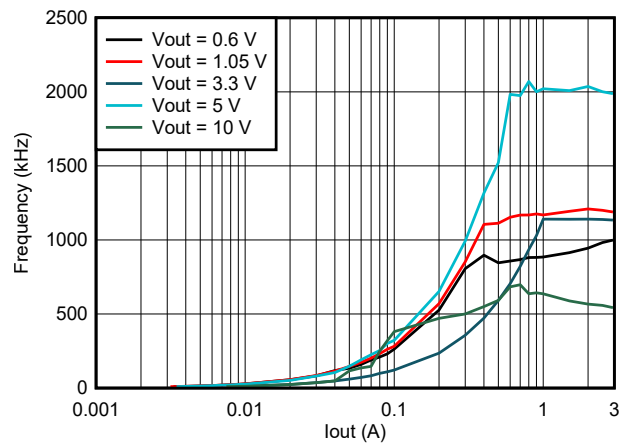


Figure 7-16. TPSM863252 Frequency vs Loading at 12-V Input Voltage

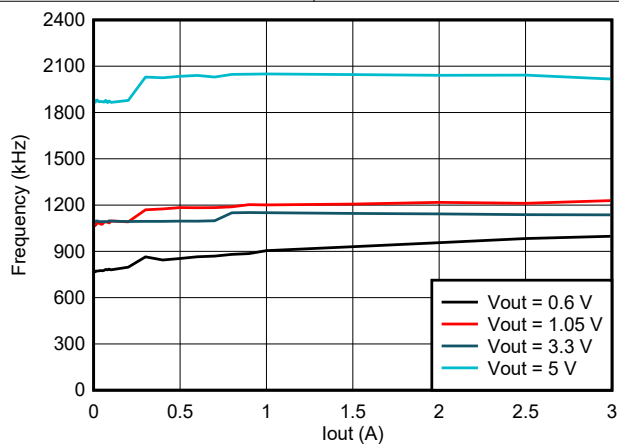


Figure 7-17. TPSM863257 Frequency vs Loading at 12-V Input Voltage

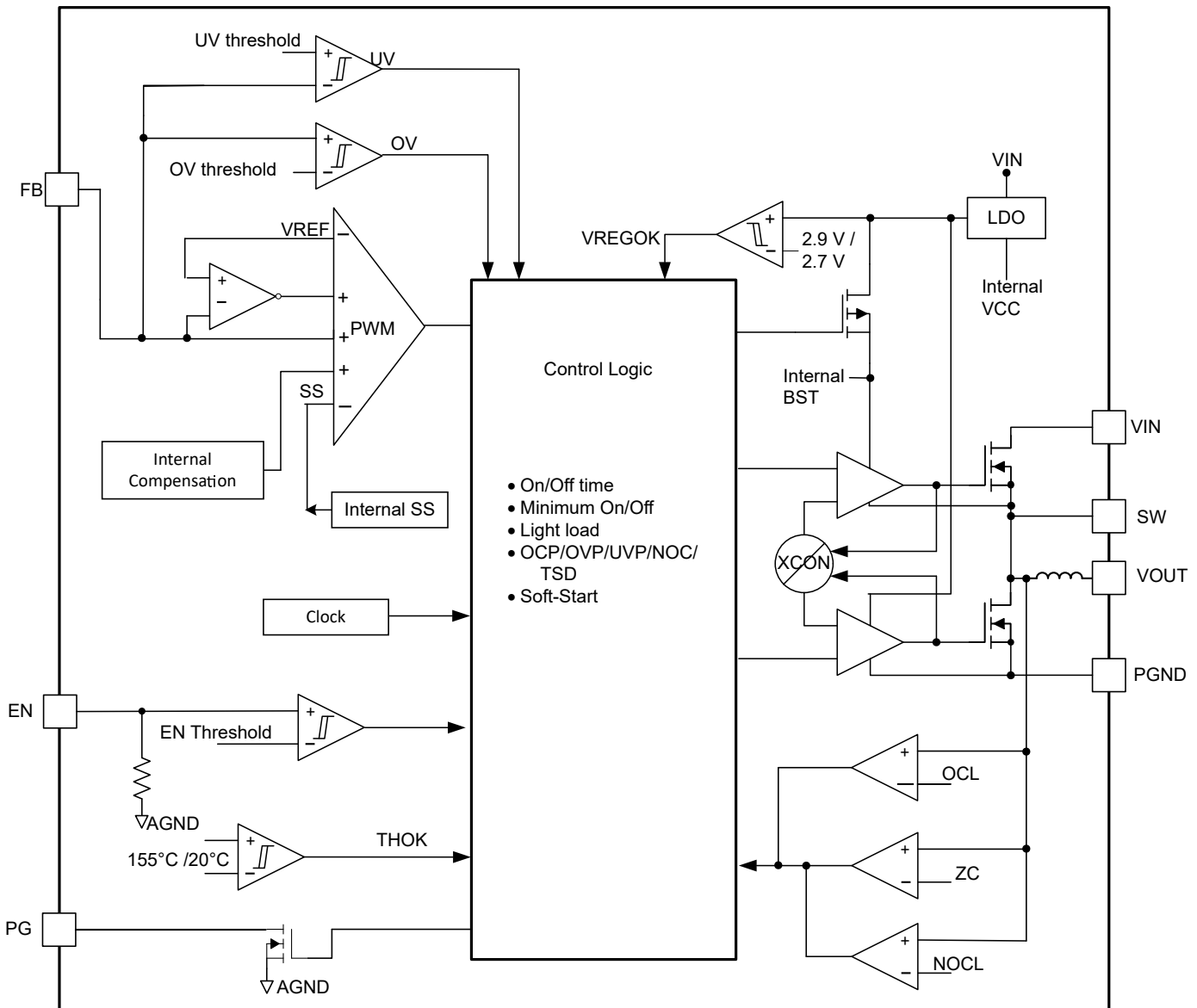
8 Detailed Description

8.1 Overview

The TPSM86325x is a 3-A, integrated, FET, synchronous buck module that operates from 3-V to 17-V input voltage and TPSM863252 output voltage range is 0.6 V to 10 V. TPSM863257 output voltage range is 0.6 V to 5.5 V. The device employs a D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The proprietary D-CAP3 control mode enables low external component count, ease of design, and optimization of the power design for cost, size, and efficiency. The topology provides a seamless transition between CCM operating mode at higher load condition and DCM operation mode at lighter load condition.

The Eco-mode version allows the TPSM863252 to maintain high efficiency at light load. The FCCM version allows the TPSM863257 to maintain a fixed switching frequency and lower voltage output ripple. The TPSM86325x is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PWM Operation and D-CAP3™ Control Mode

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The device is stable even with virtually no ripple at the output. The TPSM86325x also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT} , and is inversely proportional to the converter input voltage, V_{IN} , to maintain a pseudo-fixed frequency over the input voltage range, hence, it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage to emulate the output ripple, enabling the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode.

8.3.2 Eco-mode Control

The TPSM86325x is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This event makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Use the below equation to calculate the transition point to the light load operation $I_{OUT(LL)}$ current. The typical inductance is 1 μ H.

$$I_{out(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

8.3.3 Soft Start and Prebiased Soft Start

The TPSM86325x has an internal fixed 1.6-ms soft-start time. The EN default status is low. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes higher than the feedback voltage, V_{FB} . This scheme makes sure that the converter ramps up smoothly into the regulation point.

8.3.4 Overvoltage Protection

The TPSM86325x has the overvoltage protection feature. When the output voltage becomes higher than the OVP threshold, the OVP is triggered with a 24- μ s deglitch time. Both the high-side MOSFET and the low-side MOSFET drivers are turned off. When the overvoltage condition is removed, the device returns to switching.

8.3.5 Frequency

TPSM86325x default frequency is about 1.2 MHz. When output voltage is higher than 3.6 V and the ration of output voltage to input voltage < 0.62 (the hysteresis is 0.04), frequency changes to 2 MHz to decrease output voltage ripple. A summary is as below table.

Table 8-1. TPSM86325x Frequency at CCM

Conditions	Conditions	Frequency
Output voltage < 3.6 V		1.2 MHz
Output voltage ≥ 3.6 V	Duty ≥ 0.62	1.2 MHz
	Duty < 0.62	2 MHz

8.3.6 Large Duty Operation

The TPSM86325x can support large duty operations up to 95% by smoothly dropping down the switching frequency. When $V_{IN} / V_{OUT} < 1.6$ and V_{FB} is lower than internal V_{REF} , the switching frequency is allowed to smoothly drop to make t_{ON} extended to implement the large duty operation and keep output voltage. The minimum switching frequency is limited to approximately 600 kHz.

8.3.7 Current Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the off state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by the following:

- V_{IN}
- V_{OUT}
- On time
- Output inductor value

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, I_{OUT} . If the monitored valley current is above the OCL level, the converter maintains a low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter, which can cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects it and the device shuts down after the UVP delay time (typically 220 μ s) and restarts after the hiccup wait time (typically 14 ms).

When the overcurrent condition is removed, the output voltage returns to the regulated value.

The TPSM863257 is a FCCM mode part. In this mode, the device has negative inductor current at light loading. The device has NOC (negative overcurrent) protection to avoid too large negative current. NOC protection detects the valley of inductor current. When the valley value of inductor current exceeds the NOC threshold, the IC turns off the low side then turns on the high side. When the NOC condition is removed, the device returns to normal switching.

8.3.8 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is a non-latch protection.

8.3.9 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value, the device is shut off. This protection is a non-latch protection.

8.4 Device Functional Modes

8.4.1 Eco-mode Operation

The TPSM863252 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This event makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

8.4.2 FCCM Mode Operation

The TPSM863257 operates in forced CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency is maintained at an almost constant level over the entire load range, which is designed for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The device is a typical buck DC/DC converter that is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for TPSM86325x. Alternately, the WEBENCH® Power Designer software can be used to generate a complete design. The WEBENCH Power Designer software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

9.2 Typical Application

The application schematic in Figure 9-1 was developed to meet the requirements in Table 9-1. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

Figure 9-1 shows the 12-V input, 1.05-V output converter schematic.

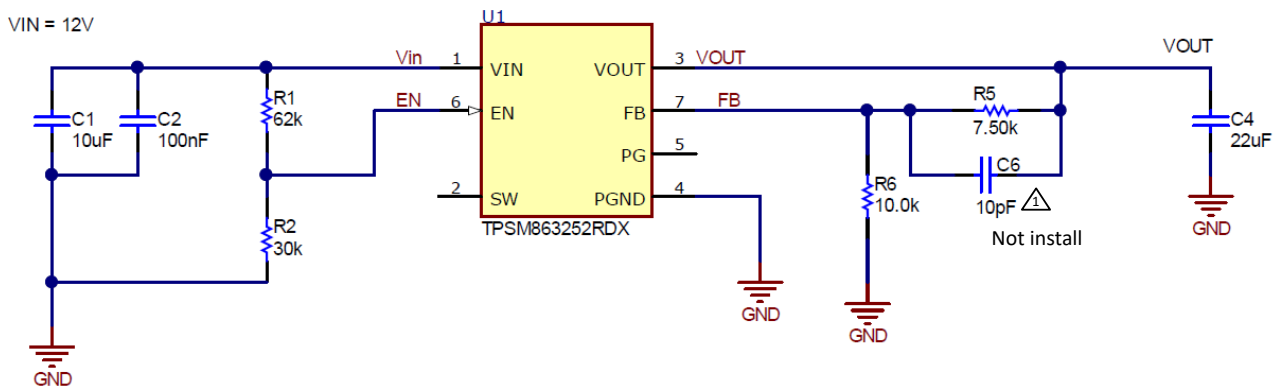


Figure 9-1. Schematic

9.2.1 Design Requirements

Table 9-1 shows the design parameters for this application.

Table 9-1. Design Parameters

Parameter	Conditions	MIN	TYP	MAX	Unit
V_{OUT}	Output voltage		1.05		V
I_{OUT}	Output current		3		A
ΔV_{OUT}	Transient response	0.3-A – 2.7-A load step, 1-A/ μ s slew rate		$\pm 3\% \times V_{OUT}$	V
V_{IN}	Input voltage	4.5	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple	CCM condition		20	mV
T_A	Ambient temperature		25		$^{\circ}$ C

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Start by using [Equation 2](#) to calculate V_{OUT} .

To improve efficiency at very light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. Use a 10-k Ω resistor for R_6 to start the design.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_5}{R_6}\right) \quad (2)$$

9.2.2.2 Output Filter Selection

TPSM86325x integrates a 1-uH inductor. TI suggests to use below output cap to make the loop stable. TI suggests CFF range to use 10 pF to 100 pF.

Table 9-2. Recommended Component Values

Output Voltage (V)	R5 (k Ω)	R6 (k Ω)	Minimum C_{OUT} (μ F)	Typical C_{OUT} (μ F)	Maximum C_{OUT} (μ F)	CFF (pF)
0.8	3.3	10.0	22	44	100	—
1.05	7.5	10.0	10	22	88	—
2.5	95.0	30.0	10	22	88	22
3.3	135.0	30.0	22	44	100	22
5	220.0	30.0	22	44	100	22
10	470.0	30.0	22	44	100	10

The capacitor value and ESR determines the amount of output voltage ripple. The TPSM86325x are intended for use with ceramic or other low-ESR capacitors. Use [Equation 3](#) to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times f_{SW}} \quad (3)$$

For this design, one MuRata GRM21BR61A226ME44L 22- μ F output capacitor are used. The typical ESR is 2 m Ω each.

9.2.2.3 Input Capacitor Selection

The TPSM86325x requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 μ F for the decoupling capacitor. TI recommends an additional 0.1- μ F capacitor from the VIN pin to ground to provide high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

9.2.2.4 Enable Circuit

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold, the device starts switching and when the EN pin voltage falls below the turn-off threshold IC stops switching. The default status is low. There is a 2-M Ω internal pulldown resistor in the EN pin.

EN can be controlled by a typical divider resistor circuit from Vin or by a voltage of lower than 5.5 V.

Because there is a 2-M Ω internal pulldown resistor in the EN pin, TPSM86325x also supports to only connect a top resistor from VIN pin to EN pin. EN voltage is got by the divide net of top resistor and 2 M Ω . EN voltage cannot be allowed to be over 6 V.

9.2.3 Application Curves

The following data is tested with $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

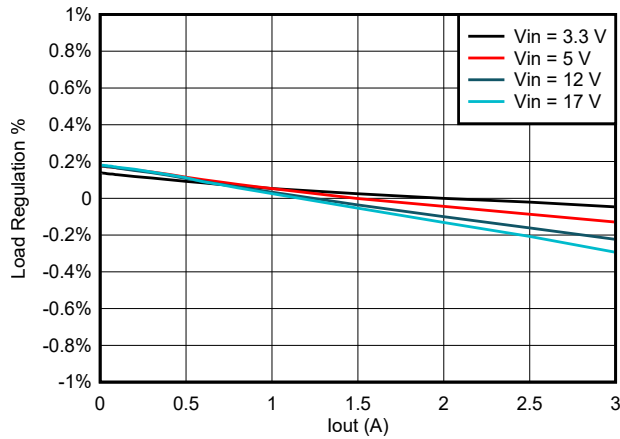


Figure 9-2. TPSM863252 Load Regulation vs Loading

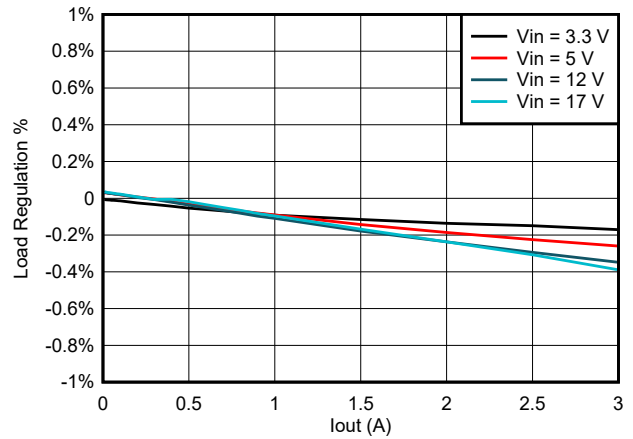


Figure 9-3. TPSM863257 Load Regulation vs Loading

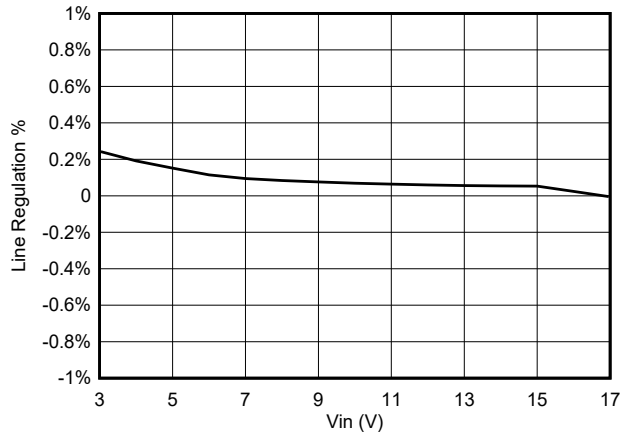


Figure 9-4. TPSM863252 Line Regulation vs V_{IN} at 3-A Loading

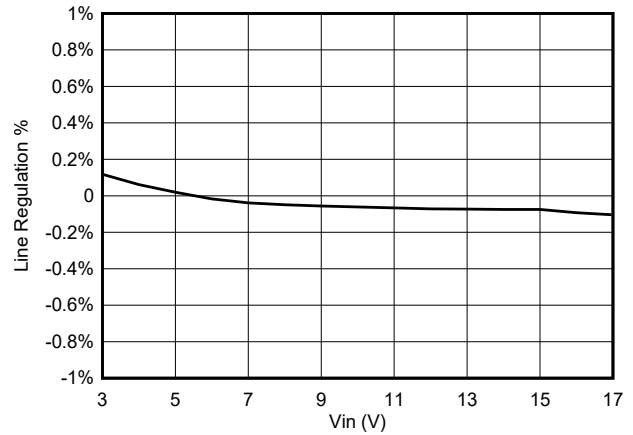


Figure 9-5. TPSM863257 Line Regulation vs V_{IN} at 3-A Loading

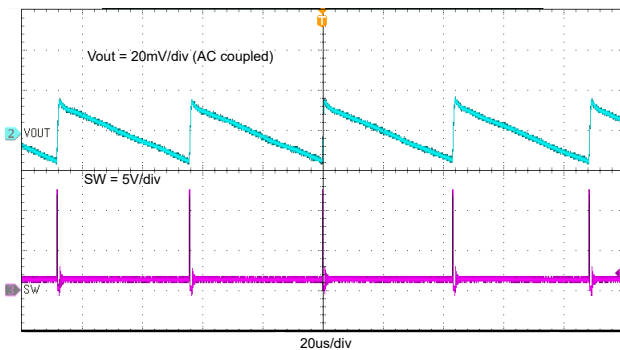


Figure 9-6. TPSM863252 Output Voltage Ripple With 0.01-A Loading

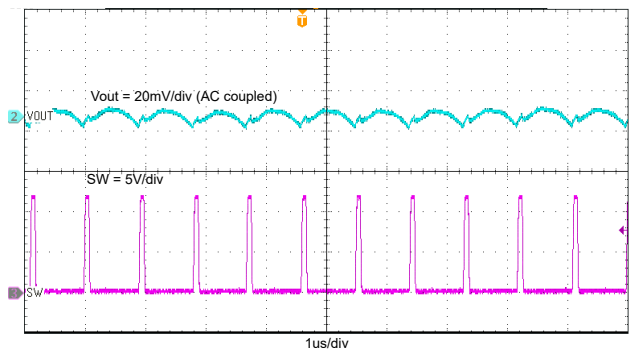


Figure 9-7. TPSM863257 Output Voltage Ripple With 0.01-A Loading

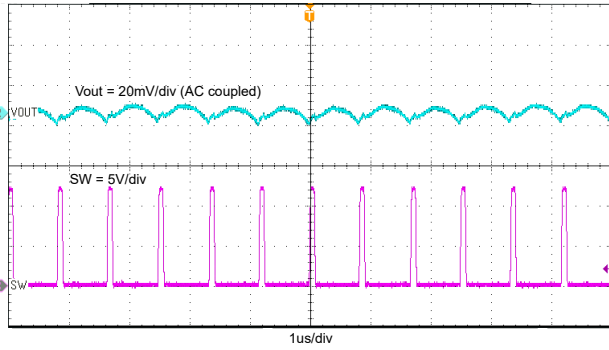


Figure 9-8. TPSM86325x Output Voltage Ripple With 3-A Loading

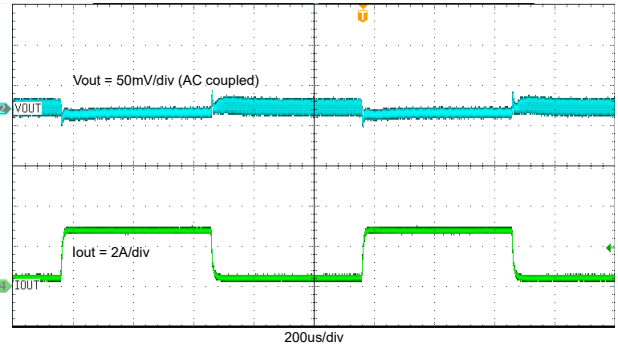


Figure 9-9. TPSM863252 Transient Response With 0.3 A to 2.7 A

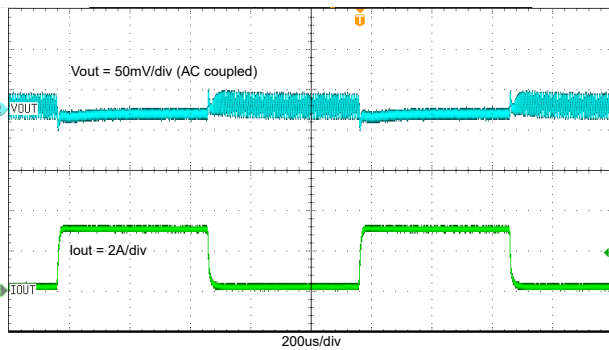


Figure 9-10. TPSM863252 Transient Response With 0.1 A to 3 A

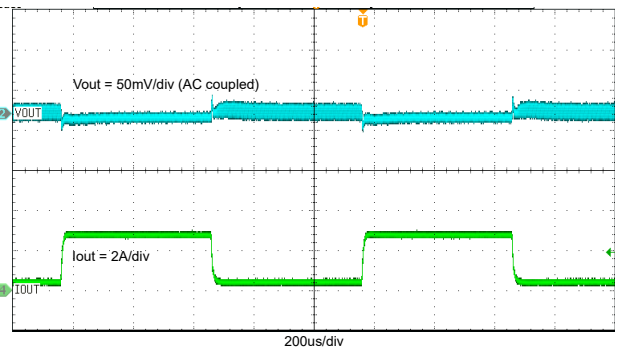


Figure 9-11. TPSM863257 Transient Response With 0.3 A to 2.7 A

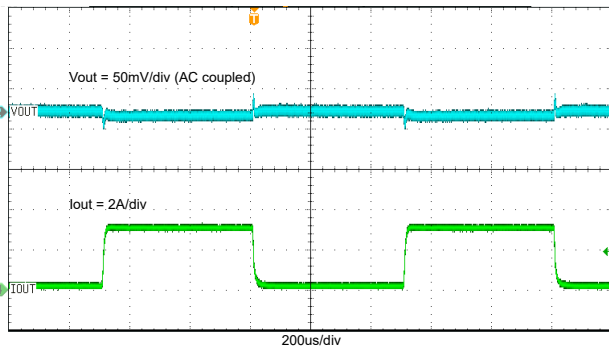


Figure 9-12. TPSM863257 Transient Response With 0.1 A to 3 A

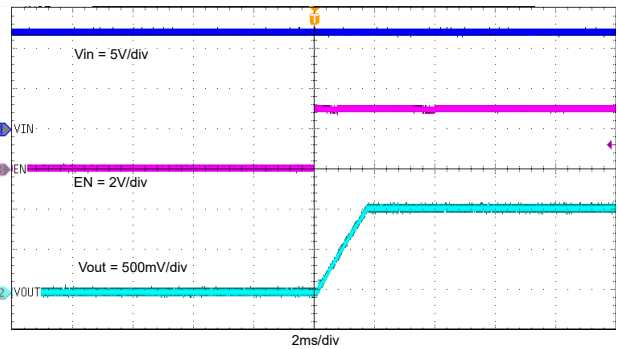


Figure 9-13. Start-Up Through EN, I_{OUT} = 3 A

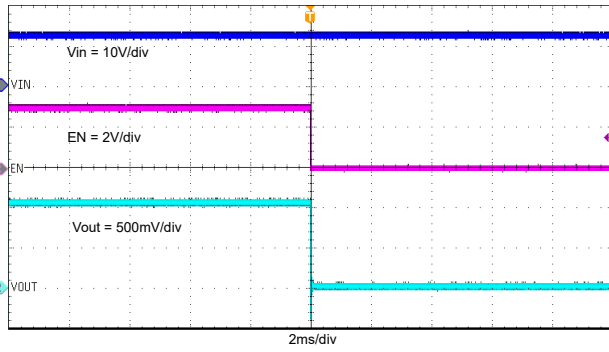


Figure 9-14. Shutdown Through EN, $I_{OUT} = 3\text{ A}$

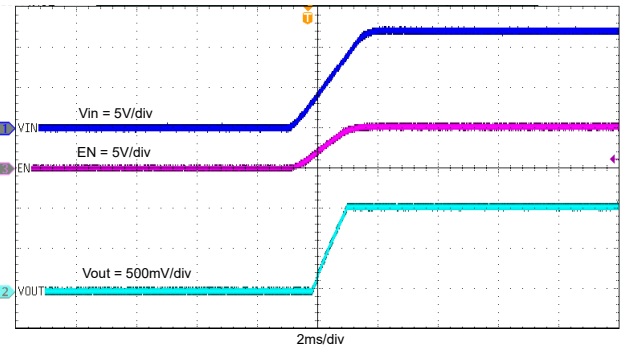


Figure 9-15. Start-Up with V_{IN} Rising, $I_{OUT} = 3\text{ A}$

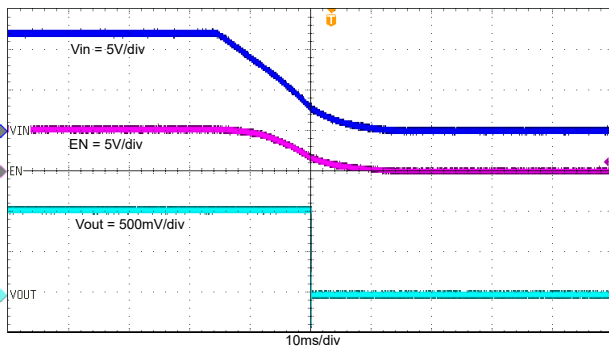


Figure 9-16. Shutdown with V_{IN} Falling, $I_{OUT} = 3\text{ A}$

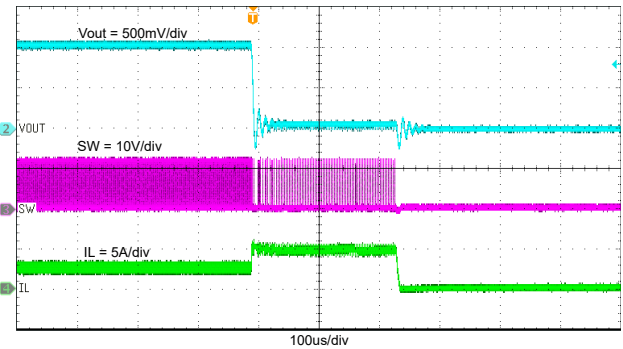


Figure 9-17. TPSM863252 Normal Operation to Output Hard Short

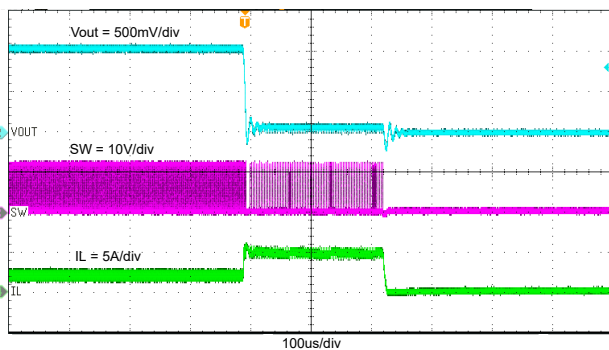


Figure 9-18. TPSM863257 Normal Operation to Output Hard Short

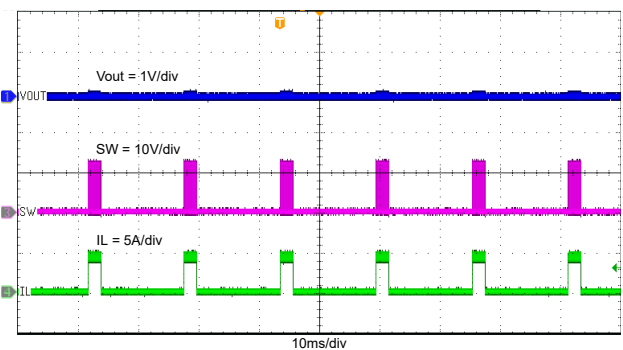


Figure 9-19. Output Hard Short Hiccup

9.3 Power Supply Recommendations

The TPSM86325x are designed to operate from input supply voltages in the range of 3 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation.

9.4 Layout

9.4.1 Layout Guidelines

- Make sure the VIN and GND traces are as wide as possible to reduce trace impedance. The wide areas are also an advantage from the view point of heat dissipation.
- Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Connect a separate VOUT path to the upper feedback resistor.
- Place a voltage feedback loop away from the high-voltage switching trace, and preferably has ground shield.
- Make sure the trace of the FB node is as small as possible to avoid noise coupling.
- Make sure the GND trace between the output capacitor and the GND pin are as wide as possible to minimize its trace impedance.

9.4.2 Layout Example

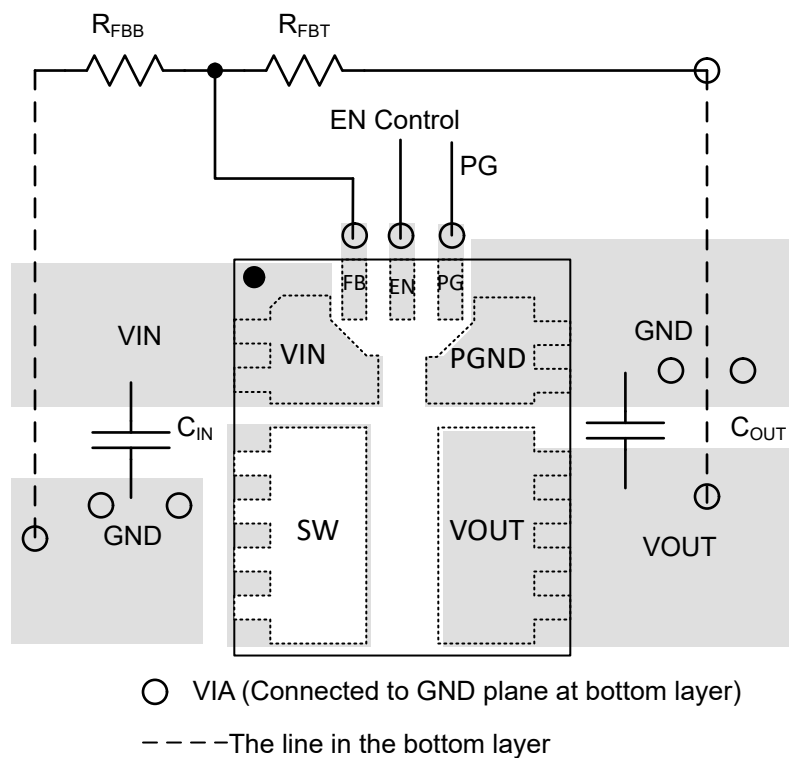


Figure 9-20. Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPSM863253RDXR	ACTIVE	QFN-FCMOD	RDX	7	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPSM863252RDXR	ACTIVE	QFN-FCMOD	RDX	7	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	863252	Samples
TPSM863257RDXR	ACTIVE	QFN-FCMOD	RDX	7	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	863257	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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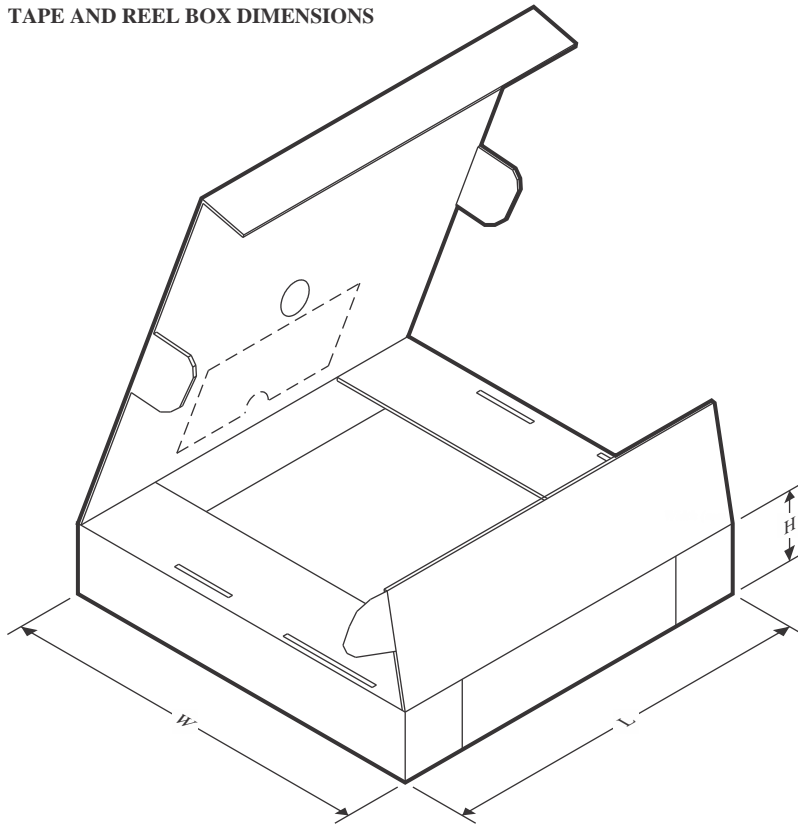
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

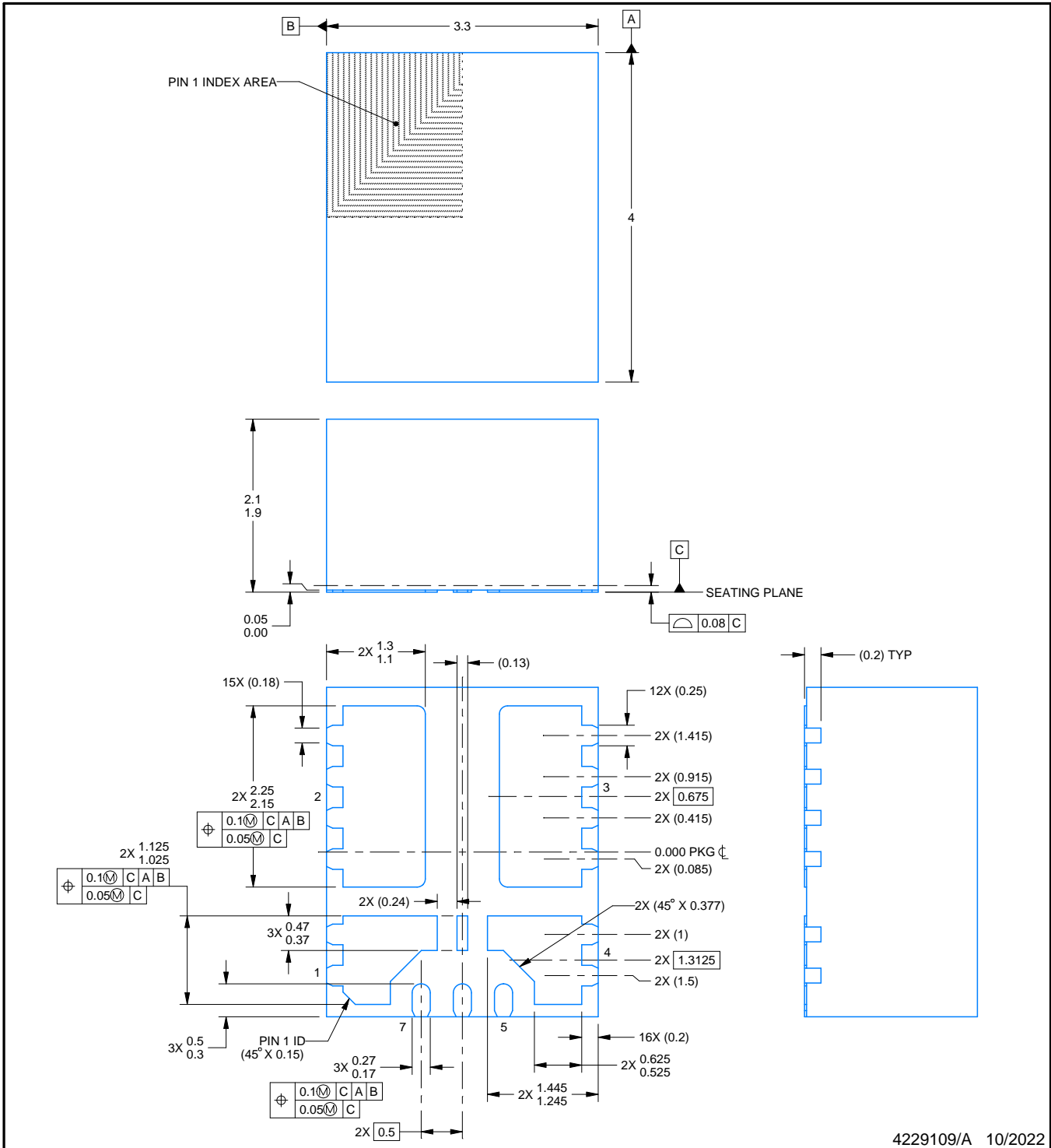

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM863252RDXR	QFN-FCMOD	RDX	7	3000	330.0	17.6	3.6	4.3	2.25	8.0	12.0	Q1
TPSM863257RDXR	QFN-FCMOD	RDX	7	3000	330.0	17.6	3.6	4.3	2.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM863252RDXR	QFN-FCMOD	RDX	7	3000	336.0	336.0	48.0
TPSM863257RDXR	QFN-FCMOD	RDX	7	3000	336.0	336.0	48.0



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NOTES:

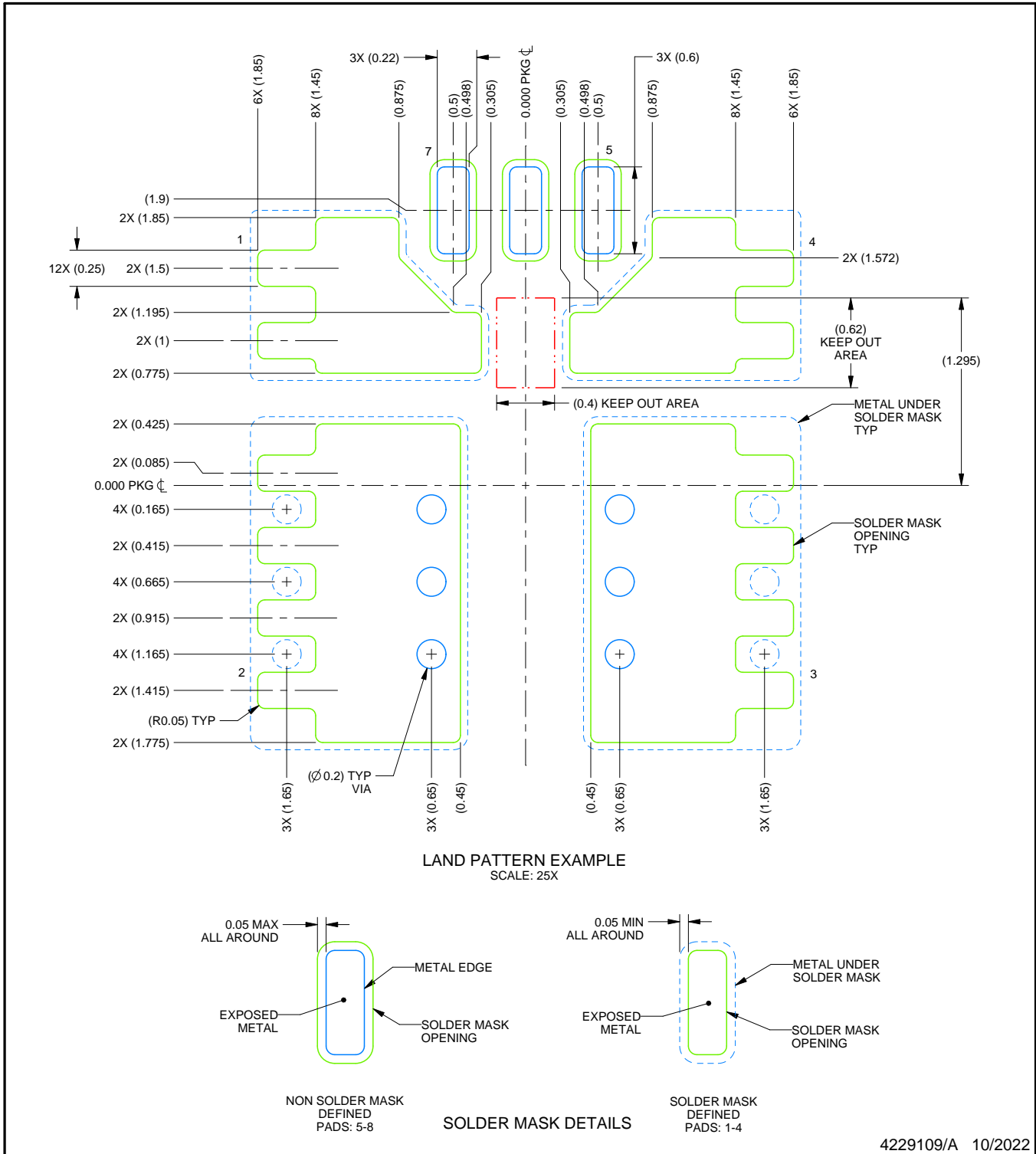
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

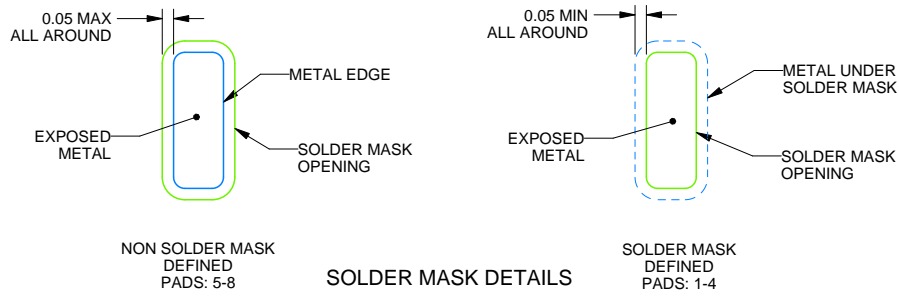
RDX0007A

QFN-FCMOD - 2.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 25X



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NOTES: (continued)

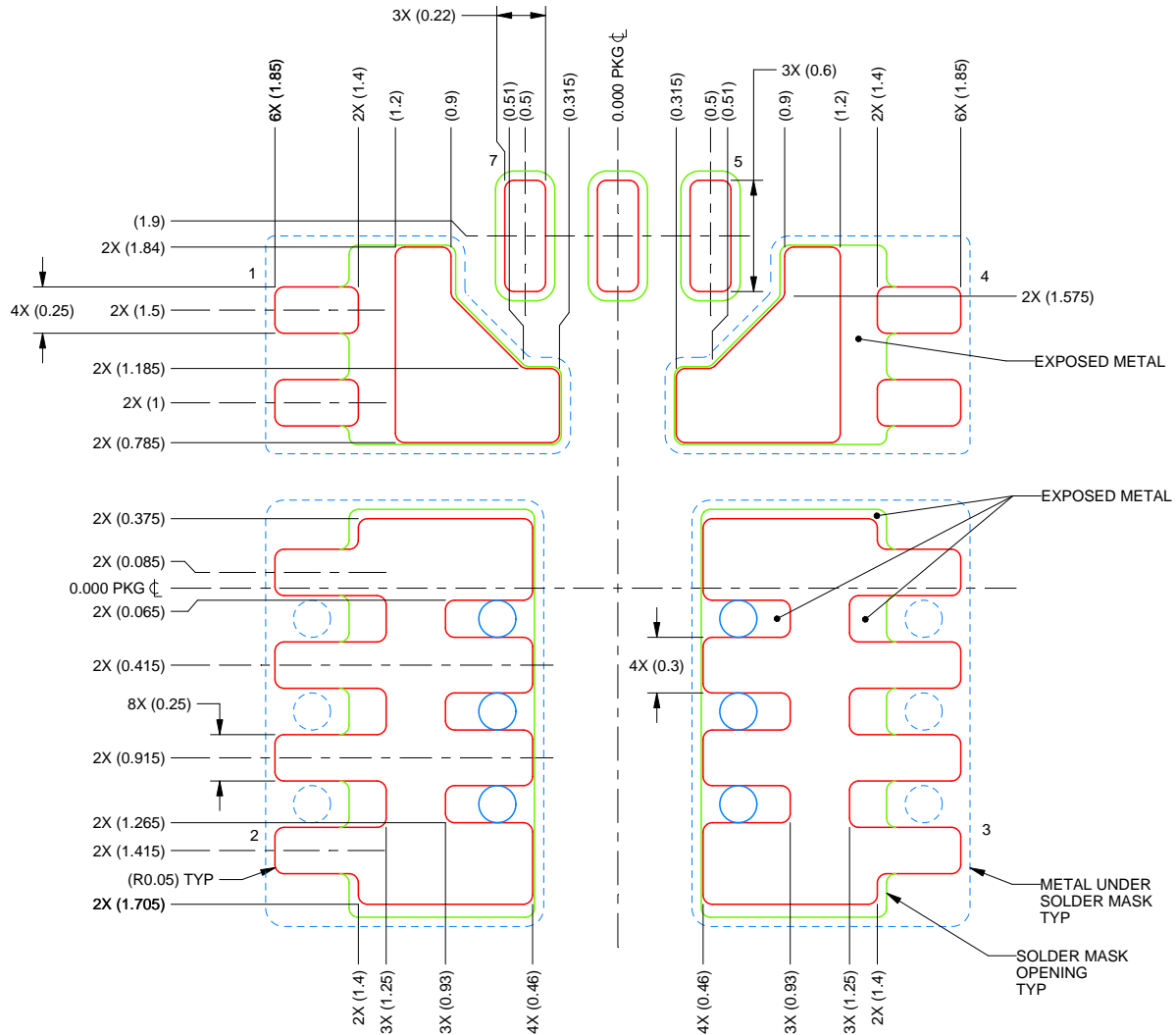
- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RDX0007A

QFN-FCMOD - 2.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE

BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS: 1, 2, 3 & 4: 75%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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[AST1S31PUR](#) [NCP81203PMNTXG](#) [NCP81208MNTXG](#) [PCA9412AUKZ](#) [NCP81109GMNTXG](#) [NCP3235MNTXG](#) [NCP81109JMNTXG](#)
[NCP81241MNTXG](#) [NTE7223](#) [NTE7222](#) [NTE7224](#) [L6986FTR](#) [MPQ4481GU-AEC1-P](#) [MP8756GD-P](#) [MPQ2171GJ-P](#) [MPQ2171GJ-AEC1-P](#)
[N JW4153U2-A-TE2](#) [MP2171GJ-P](#) [MP28160GC-Z](#) [MPM3509GQVE-AEC1-P](#) [XDPE132G5CG000XUMA1](#) [LM60440AQRPKRQ1](#)
[MP5461GC-P](#) [IW673-20](#) [MPQ4409GQBE-AEC1-P](#) [S-19903DA-A8T1U7](#) [S-19903CA-A6T8U7](#) [S-19903CA-S8T1U7](#) [S-19902BA-A6T8U7](#)
[S-19902CA-A6T8U7](#) [S-19902AA-A6T8U7](#) [S-19903AA-A6T8U7](#) [S-19902AA-S8T1U7](#) [S-19902BA-A8T1U7](#) [AU8310](#)
[LMR23615QDRRRQ1](#) [LMR33630APAQRNXRQ1](#) [LMR33630APCQRNXRQ1](#) [LMR36503R5RPER](#) [LMR36503RFRPER](#)
[LMR36503RS3QRPERQ1](#)