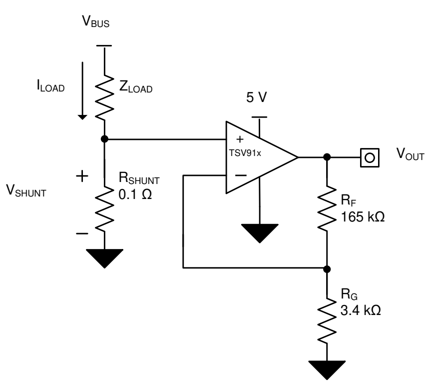
TSV91xA-Q1 汽车轨到轨输入/输出、8MHz 运算放大器

1 特性

- 轨至轨输入和输出
- 低噪声：1kHz 时为 18nV/√Hz
- 低功耗：550µA（典型值）
- 高增益带宽：8MHz
- 工作电源电压范围是 2.5V 至 5.5V
- 低输入偏置电流：1pA（典型值）
- 低输入失调电压：1.5mV（最大值）
- 低失调电压漂移：±0.5µV/°C（典型值）
- ESD 内部保护：±4kV 人体放电模型 (HBM)
- 工作温度范围：–40°C 至 125°C

2 应用

- 针对 AEC-Q100 1 级应用进行了优化
- 信息娱乐系统与仪表组
- 被动安全
- 车身电子装置和照明
- 混合动力汽车/电动汽车逆变器和电机控制
- 车载充电器 (OBC) 和无线充电器
- 动力总成电流传感器
- 高级驾驶辅助系统 (ADAS)
- 单电源、低侧、单向电流感应电路



低侧电机控制

3 说明

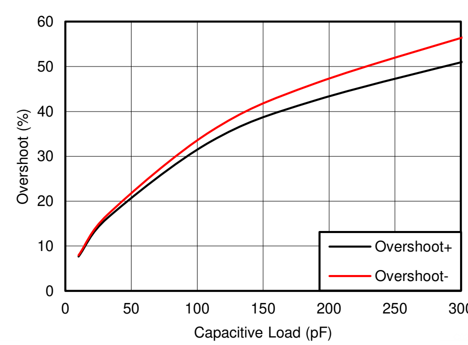
TSV91xA-Q1 系列单通道、双通道和四通道运算放大器专为通用汽车应用而设计。此系列器件具有轨至轨输入和输出 (RRIO) 摆幅、宽带宽 (8MHz) 和低失调电压（0.3mV 典型值）等特性，专为需要在速度与功耗之间实现良好平衡的各种应用而设计。该系列运算放大器的单位增益稳定，具有超低输入偏置电流，这些特性使其适用于具有高源阻抗的应用。该系列器件还具有低输入偏置电流，适用于传感器接口和有源滤波。

TSV91xA-Q1 采用稳健耐用的设计，方便电路设计人员使用。特性包括具有单位增益稳定的集成 RFI-EMI 抑制滤波器，在过驱条件下不会出现反相，以及具有高静电放电 (ESD) 保护（4kV HBM）。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
TSV911A-Q1	SOT-23 (5)(2)	1.60mm × 2.90mm
TSV912A-Q1	SOIC (8)	3.91mm × 4.90mm
	VSSOP (8)	3.00mm × 3.00mm
TSV914A-Q1	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	4.40mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 对于 TSV91xA-Q1，封装仅供预览。



小信号过冲与负载电容间的关系

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2020) to Revision B (February 2021)	Page
• 删除了器件信息 表中 VSSOP 封装的预览标签	1
• Updated thermal information for DGK (VSSOP) package in *Thermal Information: TSV912A-Q1* table	6

Changes from Revision * (June 2020) to Revision A (December 2020)	Page
• 更新了整个文档的表、图和交叉参考的编号格式	1
• 删除了器件信息 表中 TSSOP 封装的预览标签	1
• Deleted package preview note from TSV914-Q1 pinout drawing and *Pin Functions* table	4
• Added note 4 to differential input voltage in *Absolute Maximum Ratings* table	6
• Added thermal information for TSSOP (14) to *Thermal Information: TSV914A-Q1* table	7

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS			
		DBV	D	DGK	PW
TSV911A-Q1	1	5	—	—	—
TSV912A-Q1	2	—	8	8	—
TSV914A-Q1	4	—	14	—	14

6 Pin Configuration and Functions

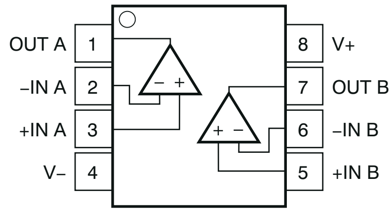


图 6-1. TSV912A-Q1 D and DGK Package 8-Pin SOIC and VSSOP Top View

表 6-1. Pin Functions: TSV912A-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
– IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
– IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V –	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

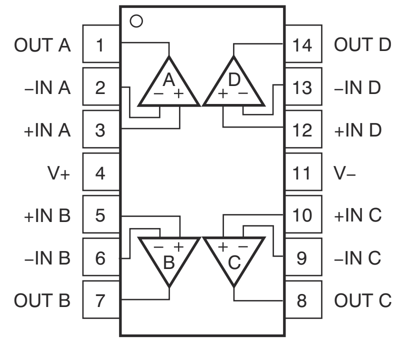


图 6-2. TSV914A-Q1 D and PW Package 14-Pin SOIC and TSSOP Top View

表 6-2. Pin Functions: TSV914A-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
Supply voltage				6	V
Signal input pins	Voltage[(2)]	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential[(4)]		(V+) – (V–) + 0.2	V
	Current[(2)]		–10	10	mA
Output short-circuit[(3)]			Continuous		mA
Specified, T_A			–40	125	°C
Junction, T_J				150	°C
Storage, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 Specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	2.5	5.5	V
	Specified temperature	–40	125	°C

7.4 Thermal Information: TSV912A-Q1

THERMAL METRIC[(1)]		TSV912A-Q1 D (SOIC) 8 PINS	TSV912A-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.6	198.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.6	87.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.7	120.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	55.6	23.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.2	118.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: TSV914A-Q1

THERMAL METRIC(1)		TSV914A-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.1	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	62.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67	76.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.4	13.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.6	76.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics

V_S (Total Supply Voltage) = (V+) – (V–) = 2.5 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.3	±1.5	mV
		V_S = 5 V T_A = –40°C to 125°C			±3	
dV_{OS}/dT	Drift	V_S = 5 V T_A = –40°C to 125°C		±0.5		μV/°C
PSRR	Power-supply rejection ratio	V_S = 2.5 V – 5.5 V, V_{CM} = (V–)		±7		μV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 2.5 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C	80	103		dB
		V_S = 5.5 V, V_{CM} = –0.1 V to 5.6 V T_A = –40°C to 125°C	57	75		
		V_S = 2.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V T_A = –40°C to 125°C		88		
		V_S = 2.5 V, V_{CM} = –0.1 V to 1.9 V T_A = –40°C to 125°C		70		
INPUT BIAS CURRENT						
I_B	Input bias current			±5		pA
I_{OS}	Input offset current			±5		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		4.77		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz		12		nV/√Hz
		V_S = 5 V, f = 1 kHz		18		
i_n	Input current noise density	f = 1 kHz		23		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 2.5 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V R_L = 10 kΩ		100		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V R_L = 10 kΩ	104	130		
		V_S = 2.5 V, (V–) + 0.06 V < V_O < (V+) – 0.06 V R_L = 2 kΩ		100		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = 1		8		MHz
ϕ_m	Phase margin	V_S = 5 V, G = 1		55		°
SR	Slew rate	V_S = 5 V, G = 1 R_L = 2 kΩ C_L = 100 pF		4.5		V/μs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = 1 C_L = 100 pF		0.5		μs
		To 0.01%, V_S = 5 V, 2-V step , G = 1 C_L = 100 pF		1		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.2		μs

7.6 Electrical Characteristics (continued)

V_S (Total Supply Voltage) = (V+) – (V–) = 2.5 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion + noise[1]	V_S = 5 V, V_O = 1 V_{RMS}, G = 1, f = 1 kHz		0.0008%		

7.6 Electrical Characteristics (continued)

V_S (Total Supply Voltage) = (V+) – (V–) = 2.5 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ			20	mV
		V_S = 5.5 V, R_L = 2 kΩ			60	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		100		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA		550	750	μA
		V_S = 5.5 V, I_O = 0 mA T_A = –40°C to 125°C			1100	

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

7.7 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

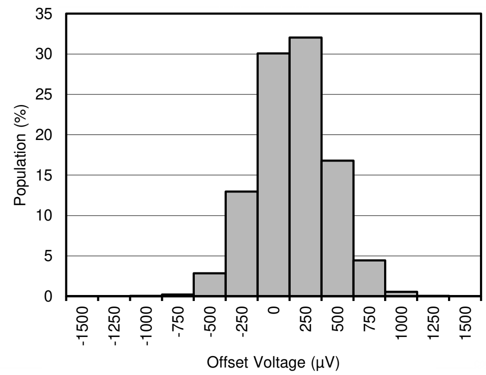
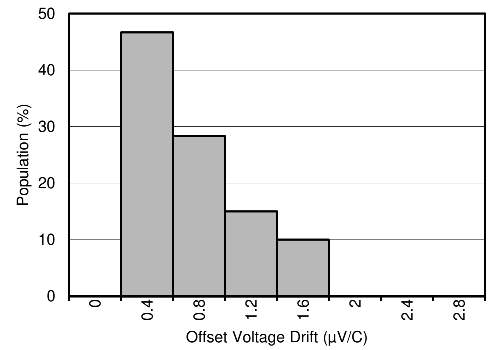


图 7-1. Offset Voltage Production Distribution



T_A = –40°C to 125°C

图 7-2. Offset Voltage Drift Distribution

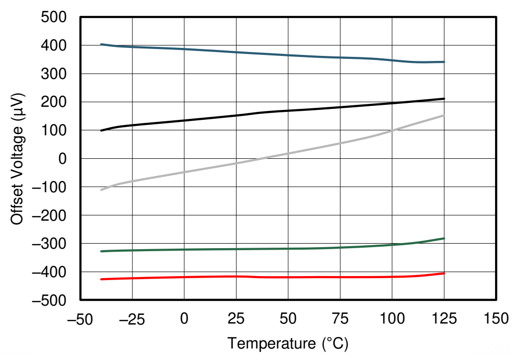
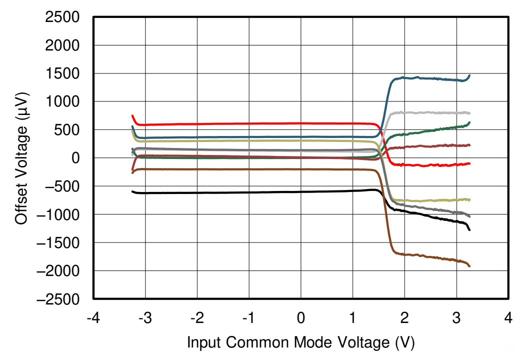
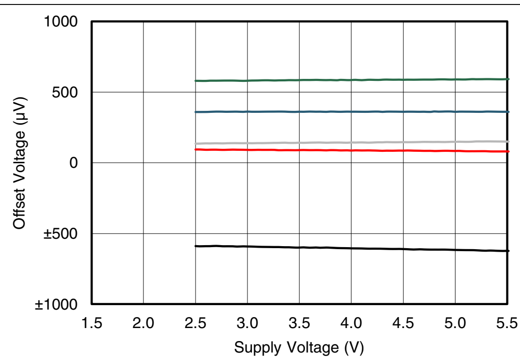


图 7-3. Offset Voltage vs Temperature



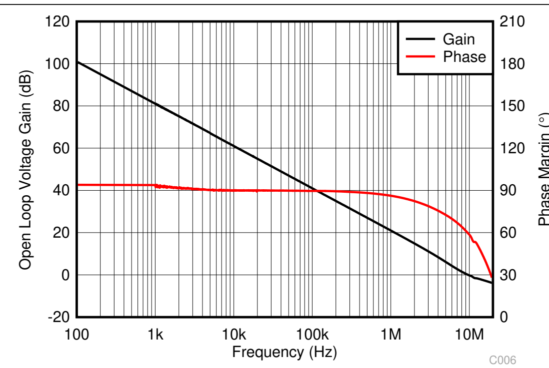
V+ = 2.75 V, V– = –2.75 V

图 7-4. Offset Voltage vs Common-Mode Voltage



V_S = 2.5 V to 5.5 V

图 7-5. Offset Voltage vs Power Supply



C_L = 10 pF

图 7-6. Open-Loop Gain and Phase vs Frequency

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

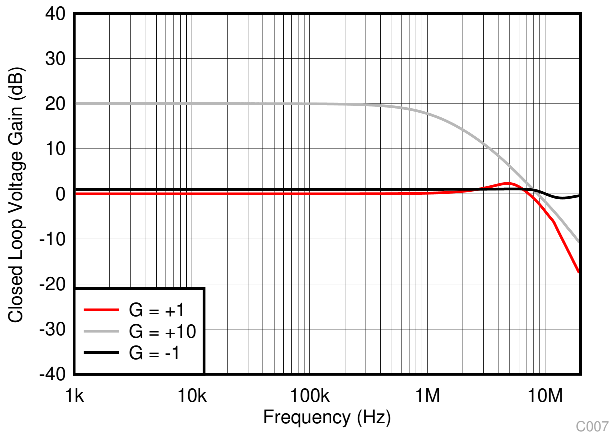


图 7-7. Closed-Loop Gain vs Frequency

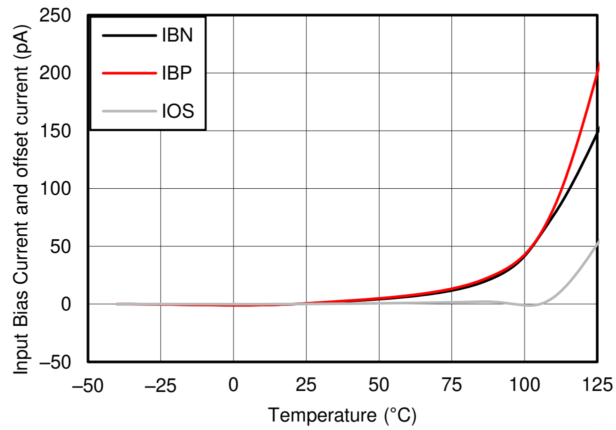
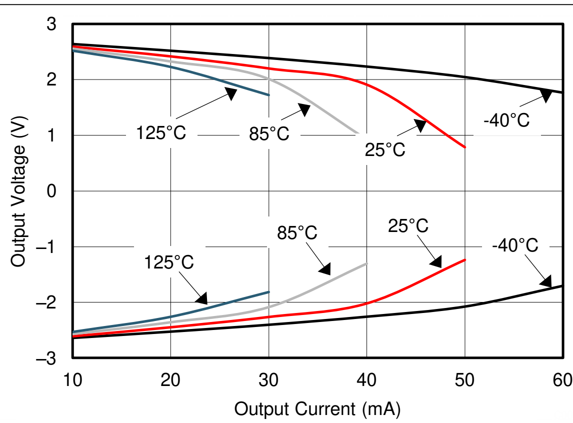


图 7-8. Input Bias Current vs Temperature



V+ = 2.75 V, V– = –2.75 V

图 7-9. Output Voltage Swing vs Output Current

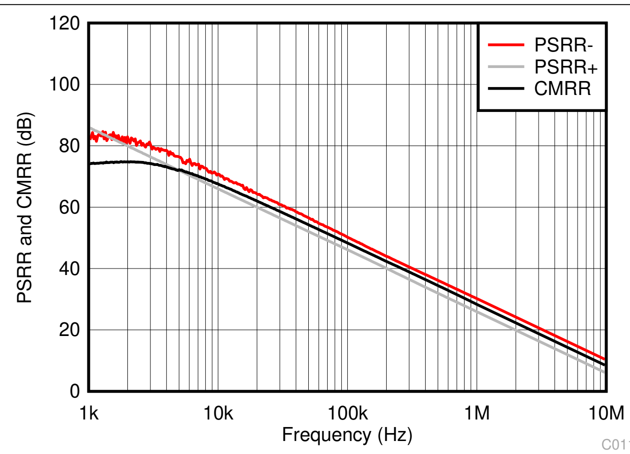
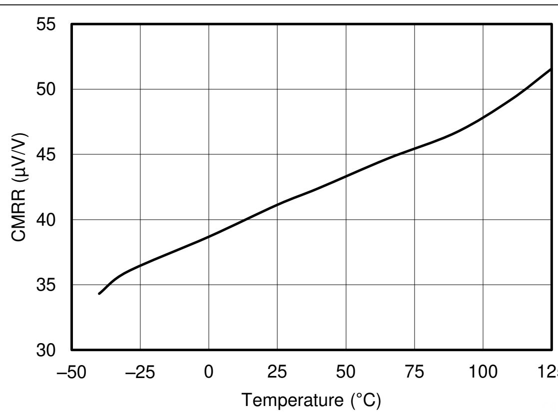


图 7-10. CMRR and PSRR vs Frequency (Referred to Input)



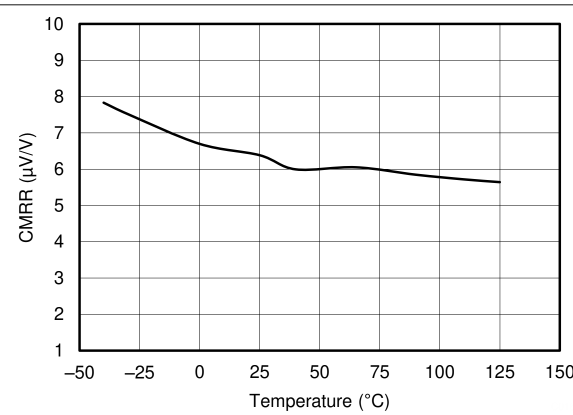
V_S = 5.5 V

V_{CM} = (V–) – 0.1 V to (V+) + 0.1 V

R_L= 10 kΩ

T_A= –40°C to 125°C

图 7-11. CMRR vs Temperature



V_S = 5.5 V

V_{CM} = (V–) – 0.1 V to (V+) – 1.4 V

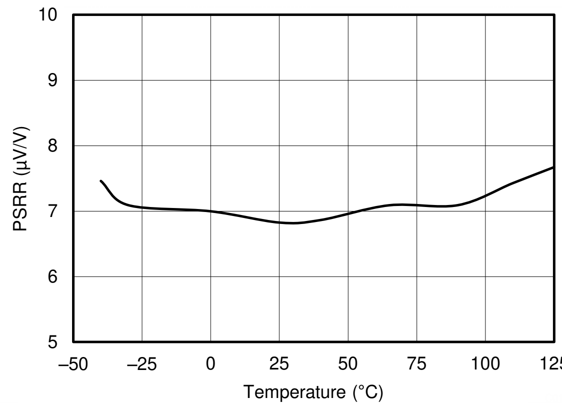
R_L= 10 kΩ

T_A= –40°C to 125°C

图 7-12. CMRR vs Temperature

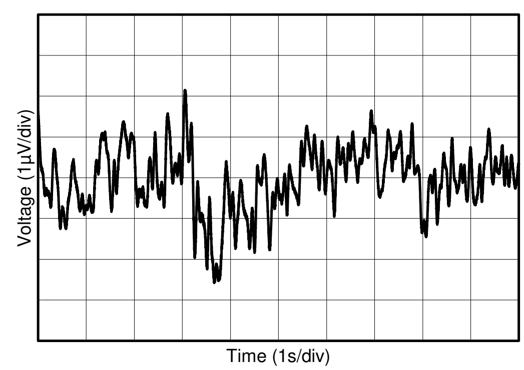
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 2.5 V to 5.5 V

图 7-13. PSRR vs Temperature



V_S = 2.5 V to 5.5 V

图 7-14. 0.1-Hz to 10-Hz Input Voltage Noise

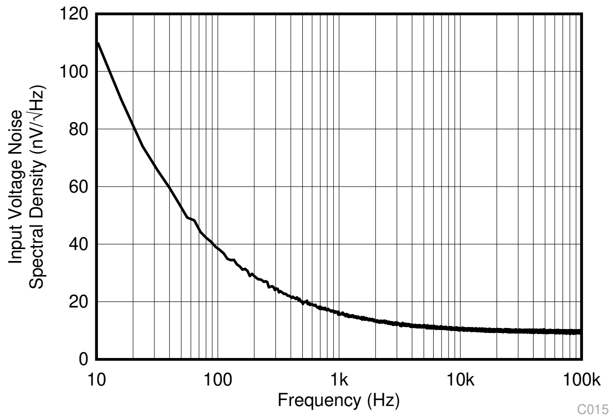
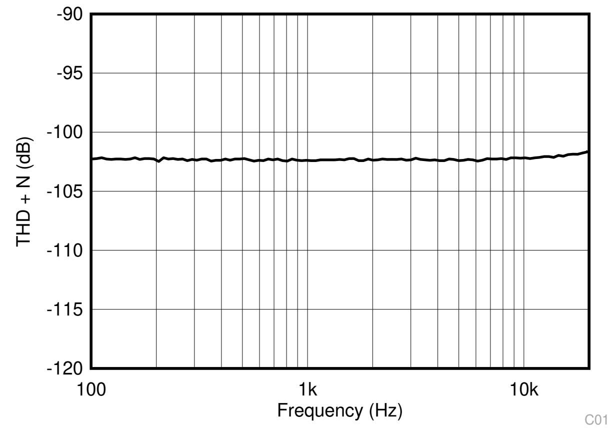
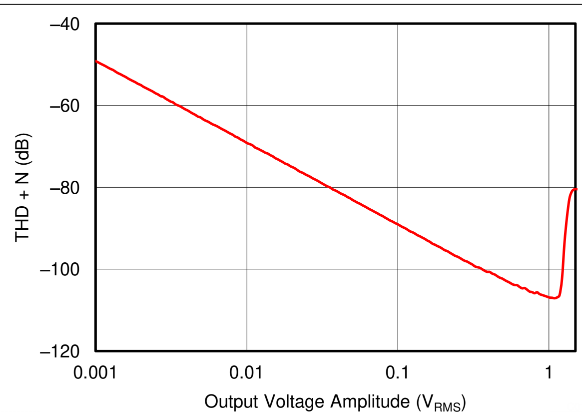


图 7-15. Input Voltage Noise Spectral Density vs Frequency



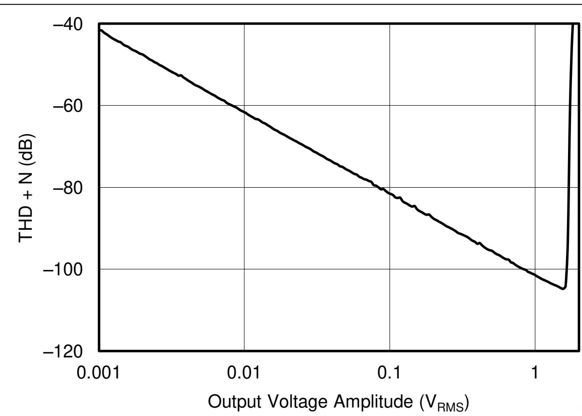
V_S = 5.5 V　V_{CM} = 2.5 V　R_L = 2 kΩ
G = 1　V_{OUT} = 0.5 V_{RMS}　BW = 80 kHz

图 7-16. THD + N vs Frequency



V_S = 5.5 V　V_{CM} = 2.5 V　R_L = 2 kΩ
G = 1　BW = 80 kHz　f = 1 kHz

图 7-17. THD + N vs Amplitude



V_S = 5.5 V　V_{CM} = 2.5 V　R_L = 2 kΩ
G = –1　BW = 80 kHz　f = 1 kHz

图 7-18. THD + N vs Amplitude

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

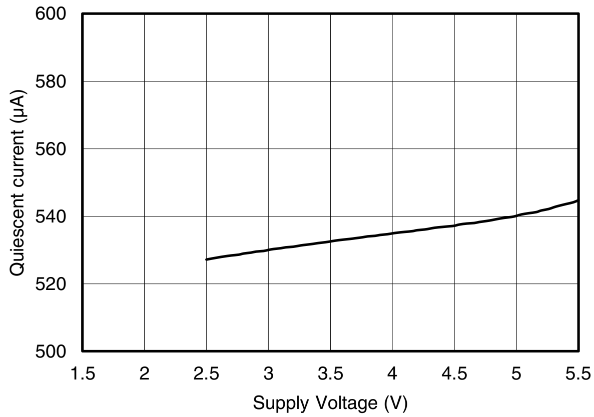


图 7-19. Quiescent Current vs Supply Voltage

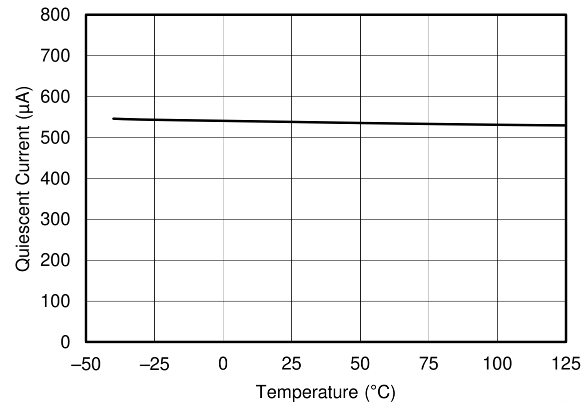


图 7-20. Quiescent Current vs Temperature

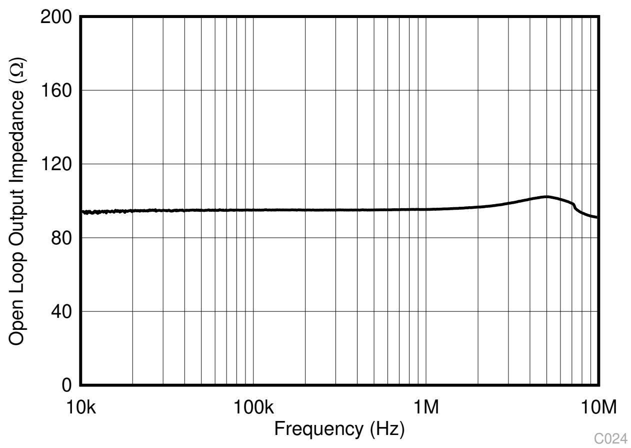
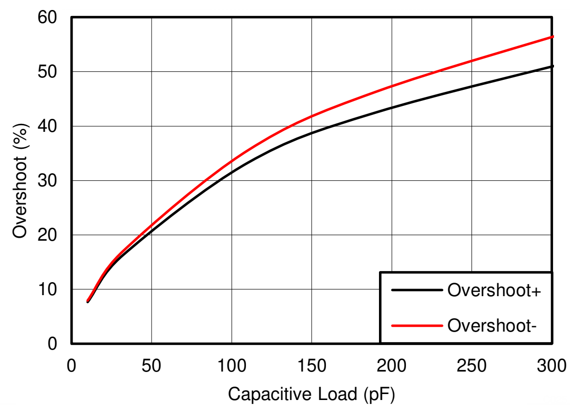
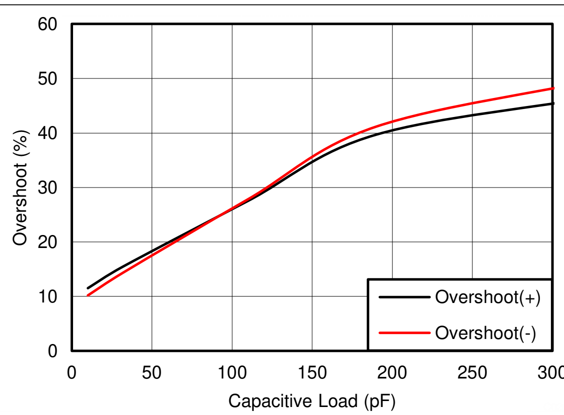


图 7-21. Open-Loop Output Impedance vs Frequency



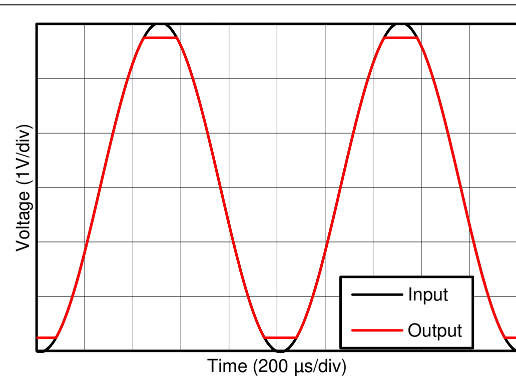
V+ = 2.75 V V– = –2.75 V G = 1 V/V
R_L = 10 kΩ V_{OUT} step = 100 mV_{p-p}

图 7-22. Small-Signal Overshoot vs Load Capacitance



V+ = 2.75 V V– = –2.75 V R_L = 10 kΩ
G = –1 V/V V_{OUT} step = 100 mV_{p-p}

图 7-23. Small-Signal Overshoot vs Load Capacitance

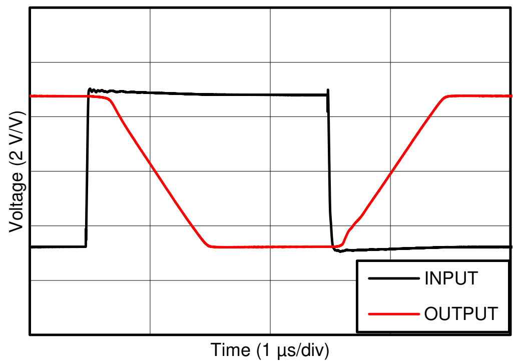


V+ = 2.75 V, V– = –2.75 V

图 7-24. No Phase Reversal

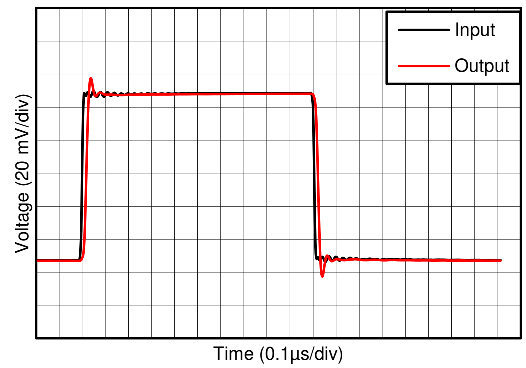
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



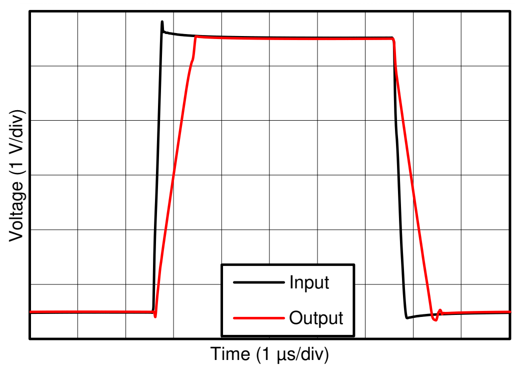
V+ = 2.75 V, V – = – 2.75 V, G = – 10 V/V

图 7-25. Overload Recovery



V+ = 2.75 V, V – = – 2.75 V, G = 1 V/V

图 7-26. Small-Signal Step Response



V+ = 2.75 V V – = – 2.75 V C_L = 100 pF
G = 1 V/V

图 7-27. Large-Signal Step Response

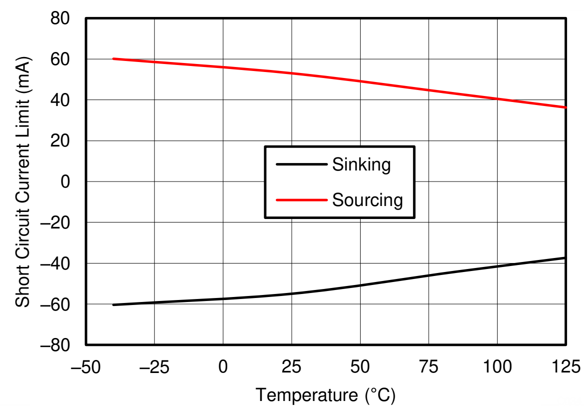
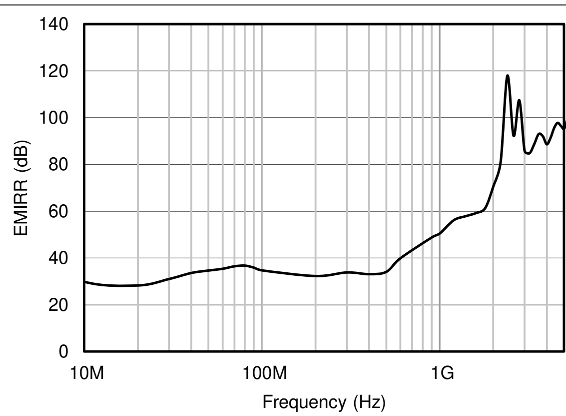
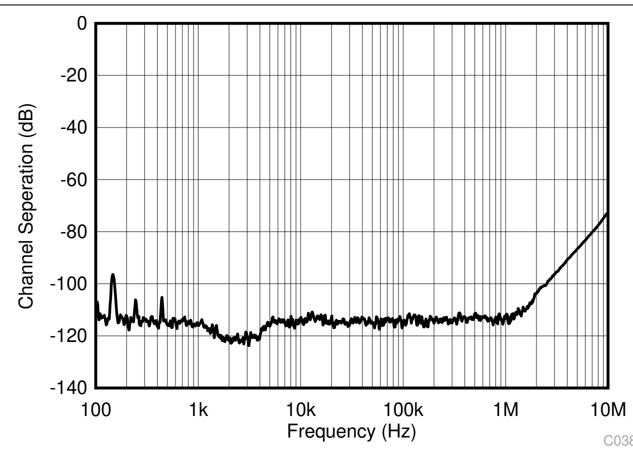


图 7-28. Short-Circuit Current vs Temperature



P_{RF} = – 10 dBm

图 7-29. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

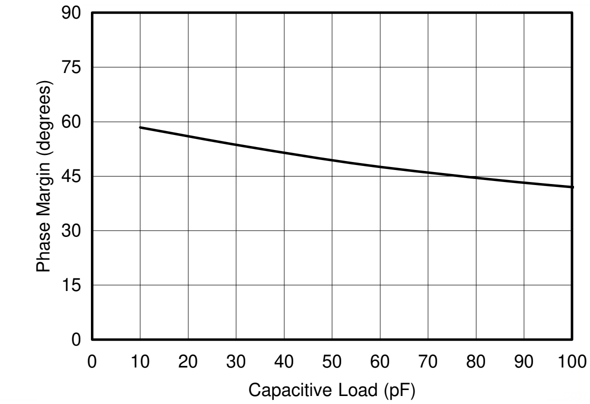


V+ = 2.75 V, V – = – 2.75 V

图 7-30. Channel Separation vs Frequency

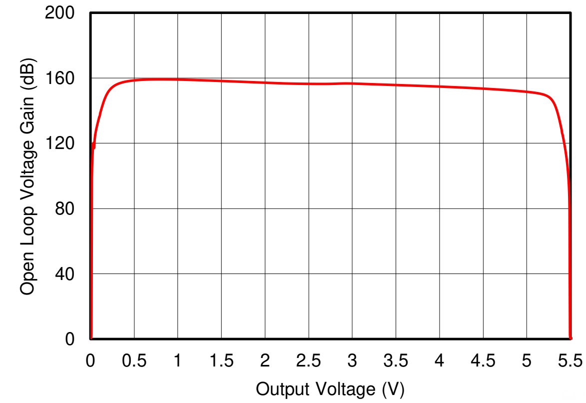
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V

图 7-31. Phase Margin vs Capacitive Load



A. V_S = 5.5 V

图 7-32. Open Loop Voltage Gain vs Output Voltage

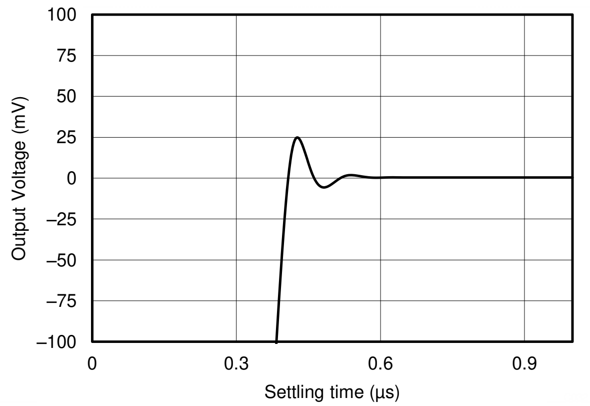


图 7-33. Large Signal Settling Time (Positive)

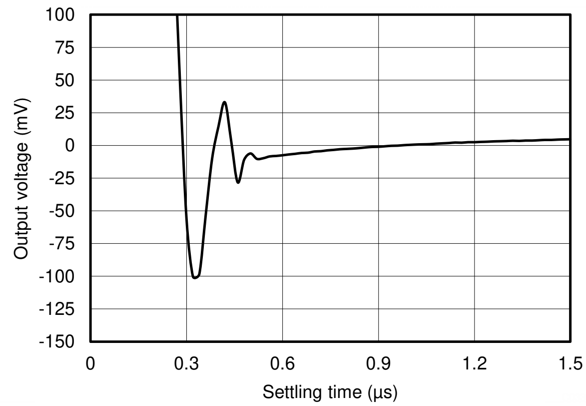


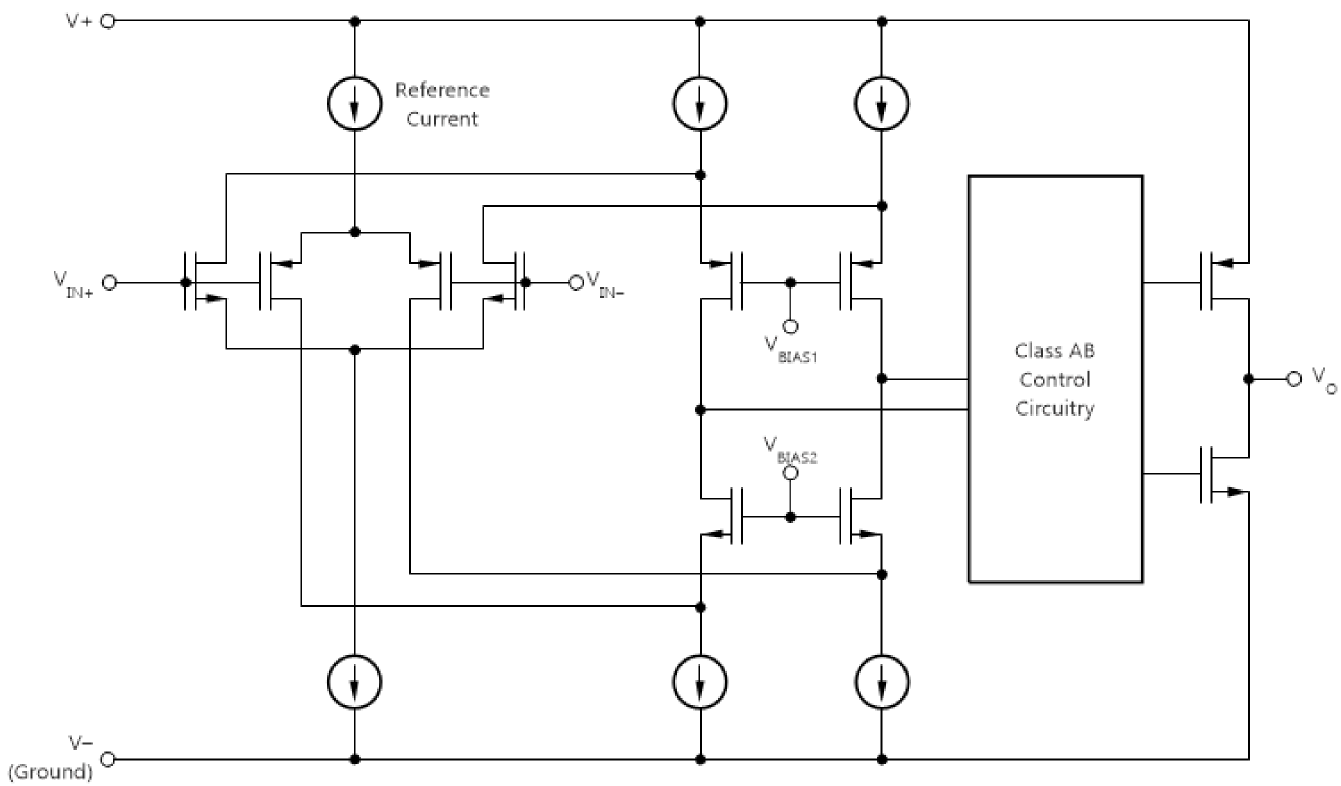
图 7-34. Large Signal Settling Time (Negative)

8 Detailed Description

8.1 Overview

The TSV91xA-Q1 series is a family of low-power, rail-to-rail input and output op amps. These devices operate from 2.5 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose automotive applications. The input common-mode voltage range includes both rails and allows the TSV91xA-Q1 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications and are designed for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TSV91xA-Q1 family extends 100 mV beyond the supply rails for the full supply voltage range of 2.5 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TSV91xA-Q1 series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.3 Packages With an Exposed Thermal Pad

The TSV91xA-Q1 family is available in packages such as the WSON-8 (DSG) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other then V– is not allowed, and the performance of the device is not assured when doing so.

8.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TSV91xA-Q1 series is approximately 200 ns.

8.4 Device Functional Modes

The TSV91xA-Q1 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 2.5 V (±1.25 V) and 5.5 V (±2.75 V).

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TSV91xA-Q1 series features 8-MHz bandwidth and 4.5-V/µs slew rate with only 550 µA of supply current per channel, providing good AC performance at low power consumption. DC applications are well served with a low input noise voltage of 18 nV / $\sqrt{Hz}$ at 1 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

9.2 Typical Application

图 9-1 shows the TSV91xA-Q1 configured in a low-side, motor-control application.

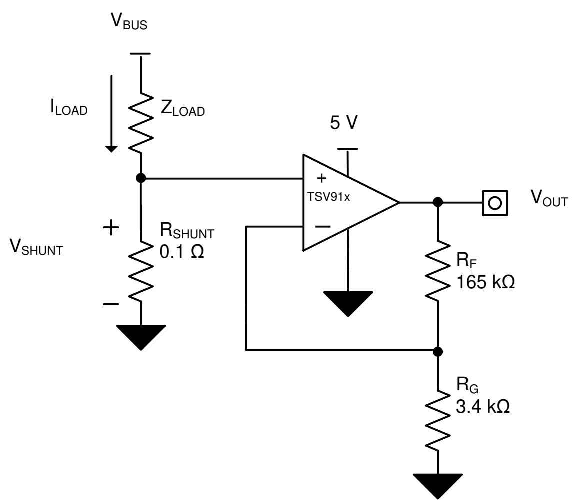


图 9-1. TSV91xA-Q1 in a Low-Side, Motor-Control Application

9.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

9.2.2 Detailed Design Procedure

The transfer function of the circuit in 图 9-1 is shown in 方程式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 方程式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using 方程式 2, R_{SHUNT} is 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TSV91xA-Q1 to produce an output voltage of approximately 0 V to 4.95 V. The gain required by the TSV91xA-Q1 to produce the necessary output voltage is calculated using 方程式 3:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using 方程式 3, the required gain is calculated to be 49.5 V/V, which is set with resistors R_F and R_G. 方程式 4 is used to size the resistors, R_F and R_G, to set the gain of the TSV91xA-Q1 to 49.5 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F as 165 kΩ and R_G as 3.4 kΩ provides a combination that equals roughly 49.5 V/V. 图 9-2 shows the measured transfer function of the circuit shown in 图 9-1.

9.2.3 Application Curve

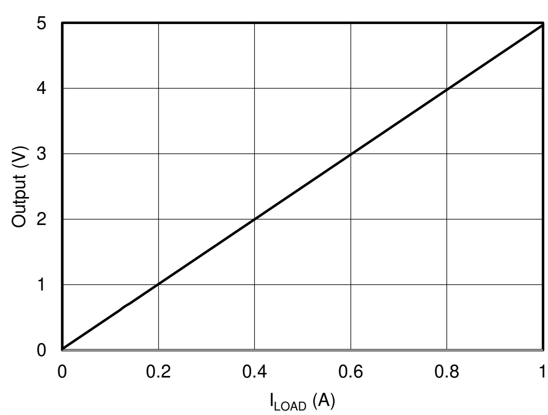


图 9-2. Low-Side, Current-Sense, Transfer Function

10 Power Supply Recommendations

The TSV91xA-Q1 series is specified for operation from 2.5 V to 5.5 V (±1.25 V to ±2.75 V); many specifications apply from –40°C to 125°C. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Example*.

10.1 Input and ESD Protection

The TSV91xA-Q1 series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the *Absolute Maximum Ratings* table. 图 10-1 shows how a series input resistor is added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

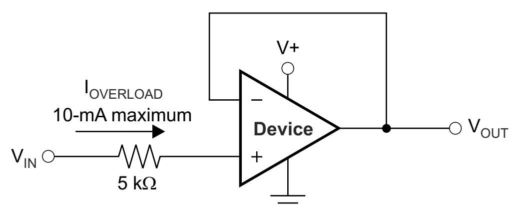


图 10-1. Input Current Protection

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 11-2, keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

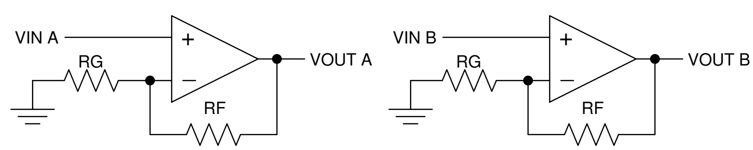


图 11-1. Schematic Representation of Layout Example

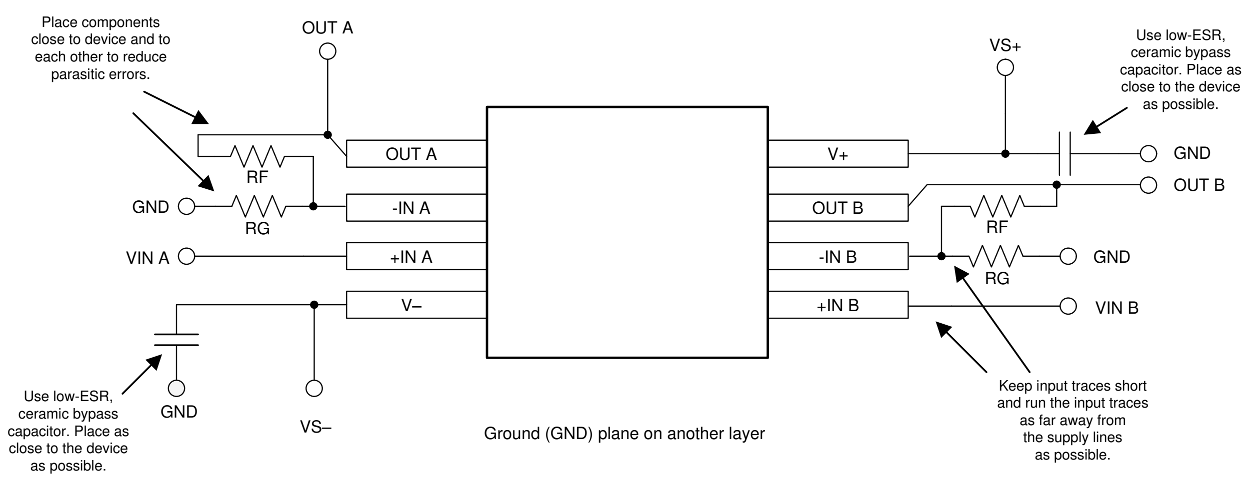


图 11-2. Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TSV912A-Q1	Click here	Click here	Click here	Click here	Click here
TSV914A-Q1	Click here	Click here	Click here	Click here	Click here

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSV912AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	29IT	Samples
TSV912AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TS912Q	Samples
TSV914AQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSV914AQD	Samples
TSV914AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T914AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

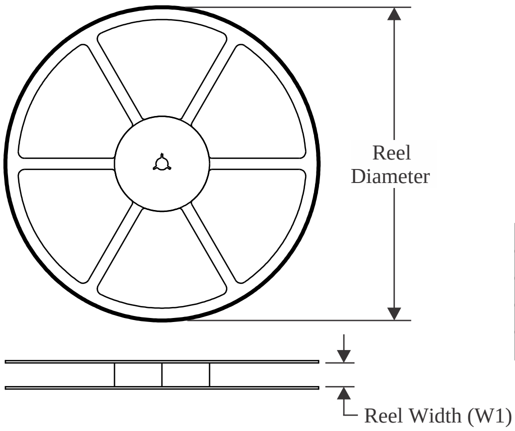
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

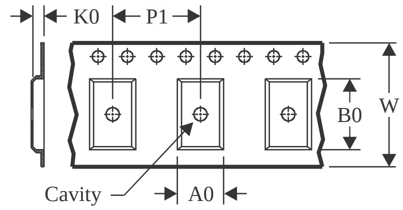
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

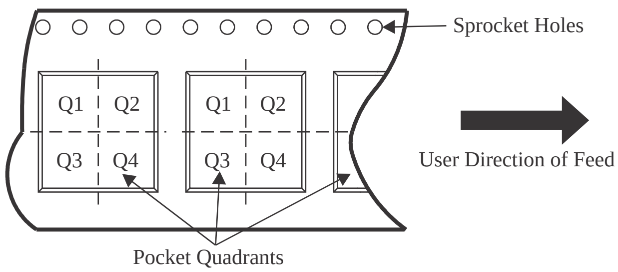


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

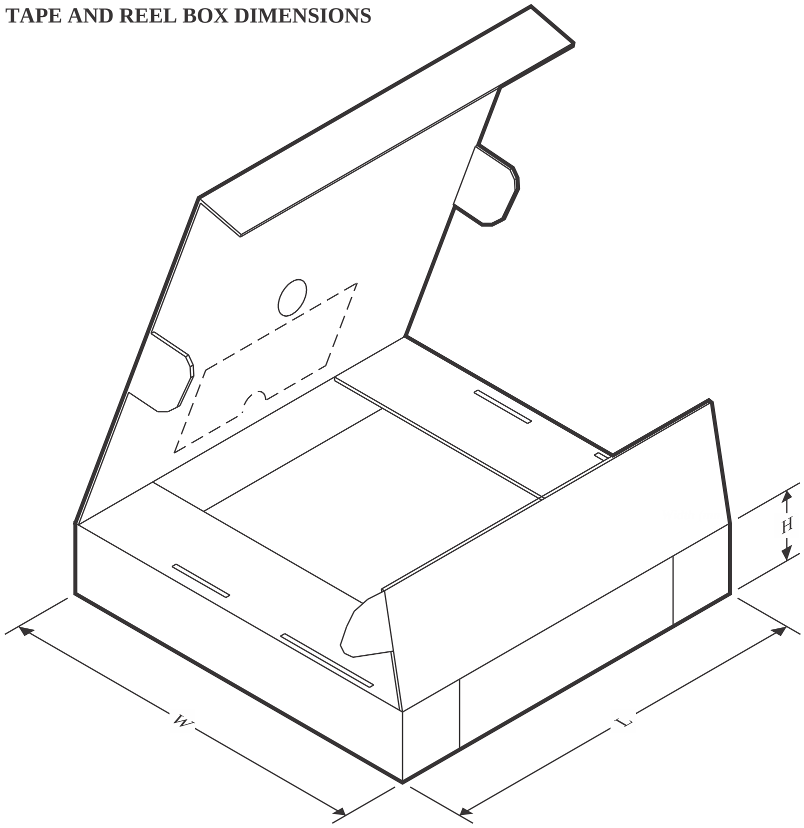
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSV912AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TSV912AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TSV914AQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TSV914AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

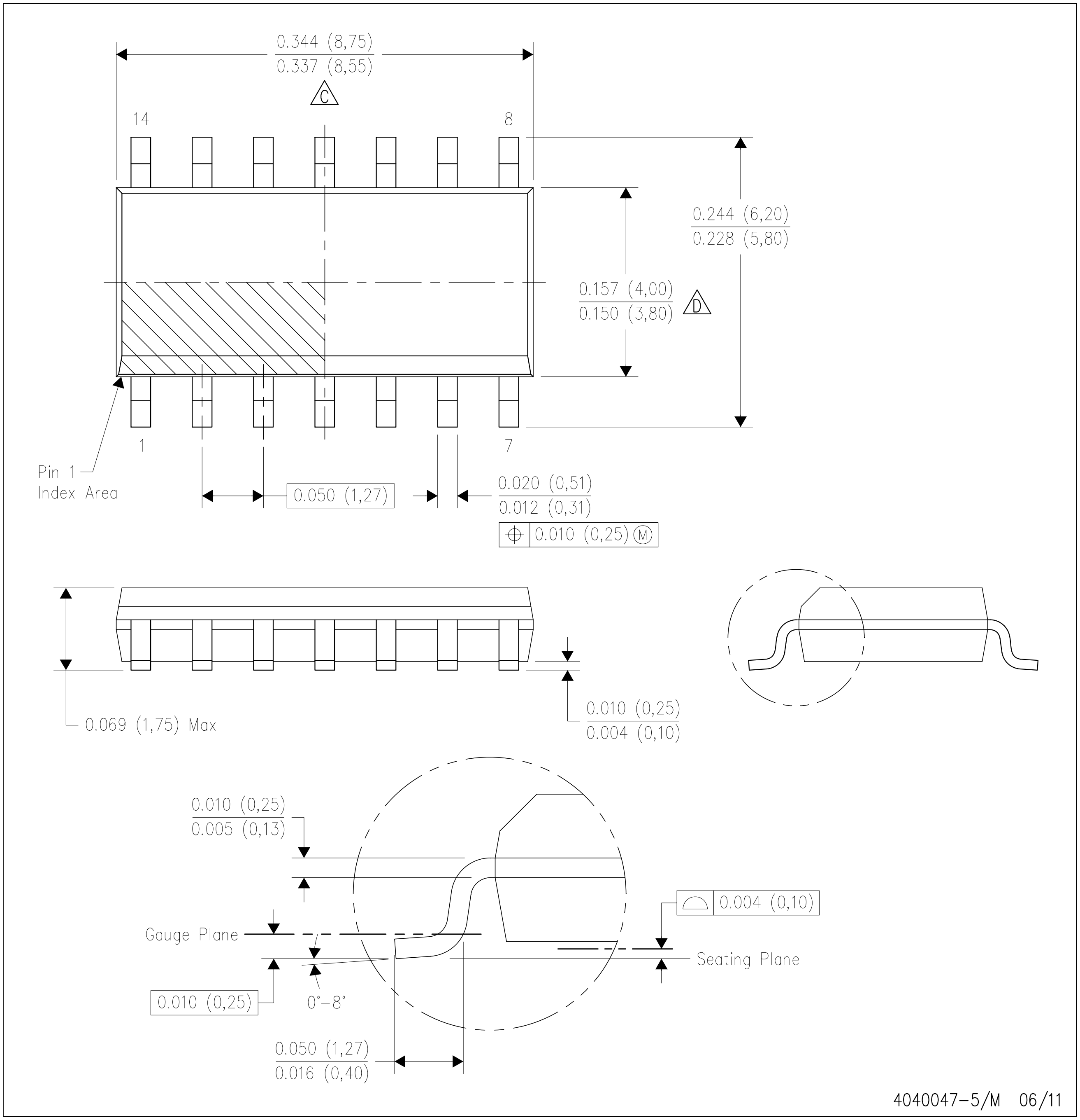
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

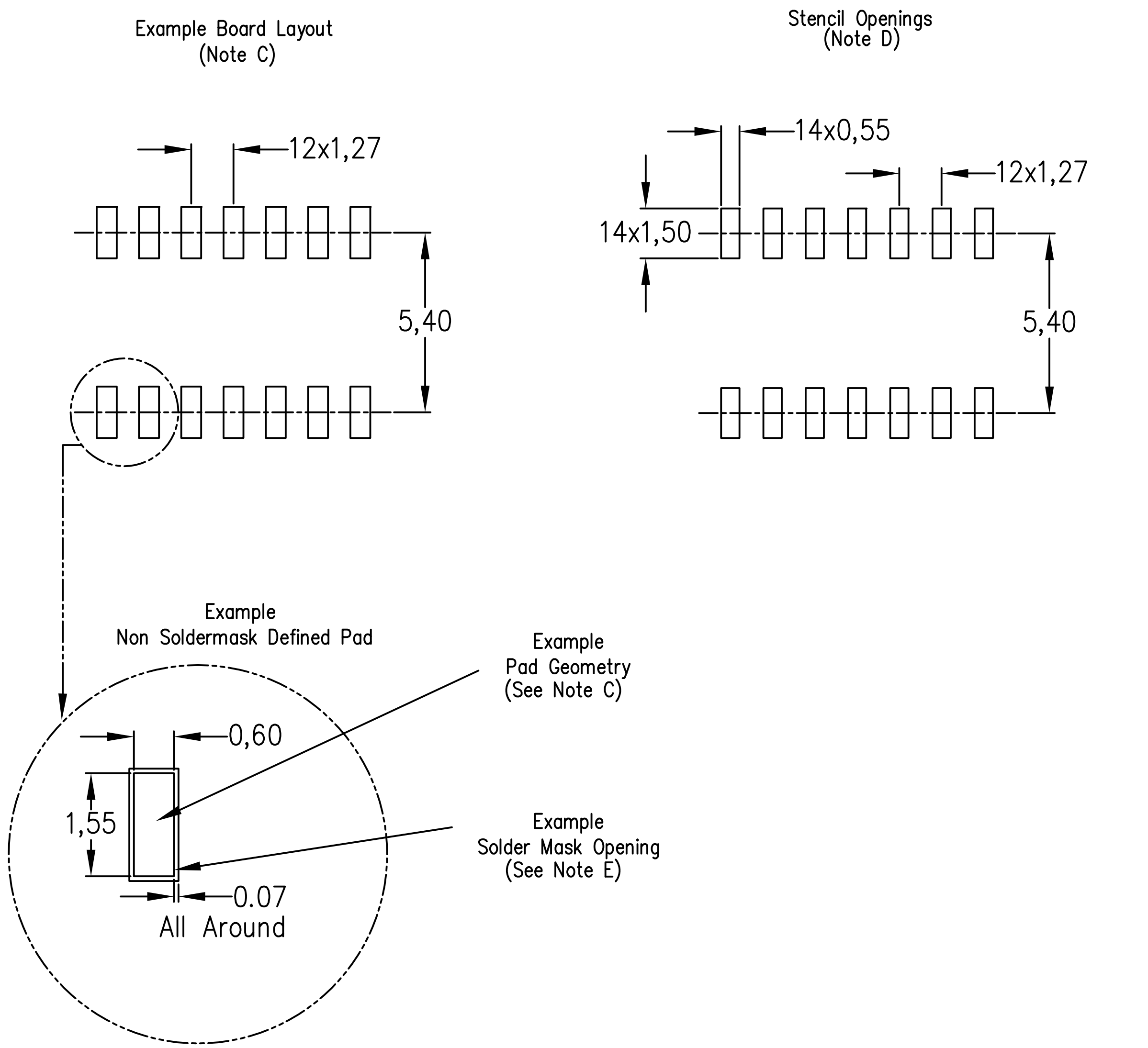
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSV912AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TSV912AQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TSV914AQDRQ1	SOIC	D	14	2500	356.0	356.0	35.0
TSV914AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

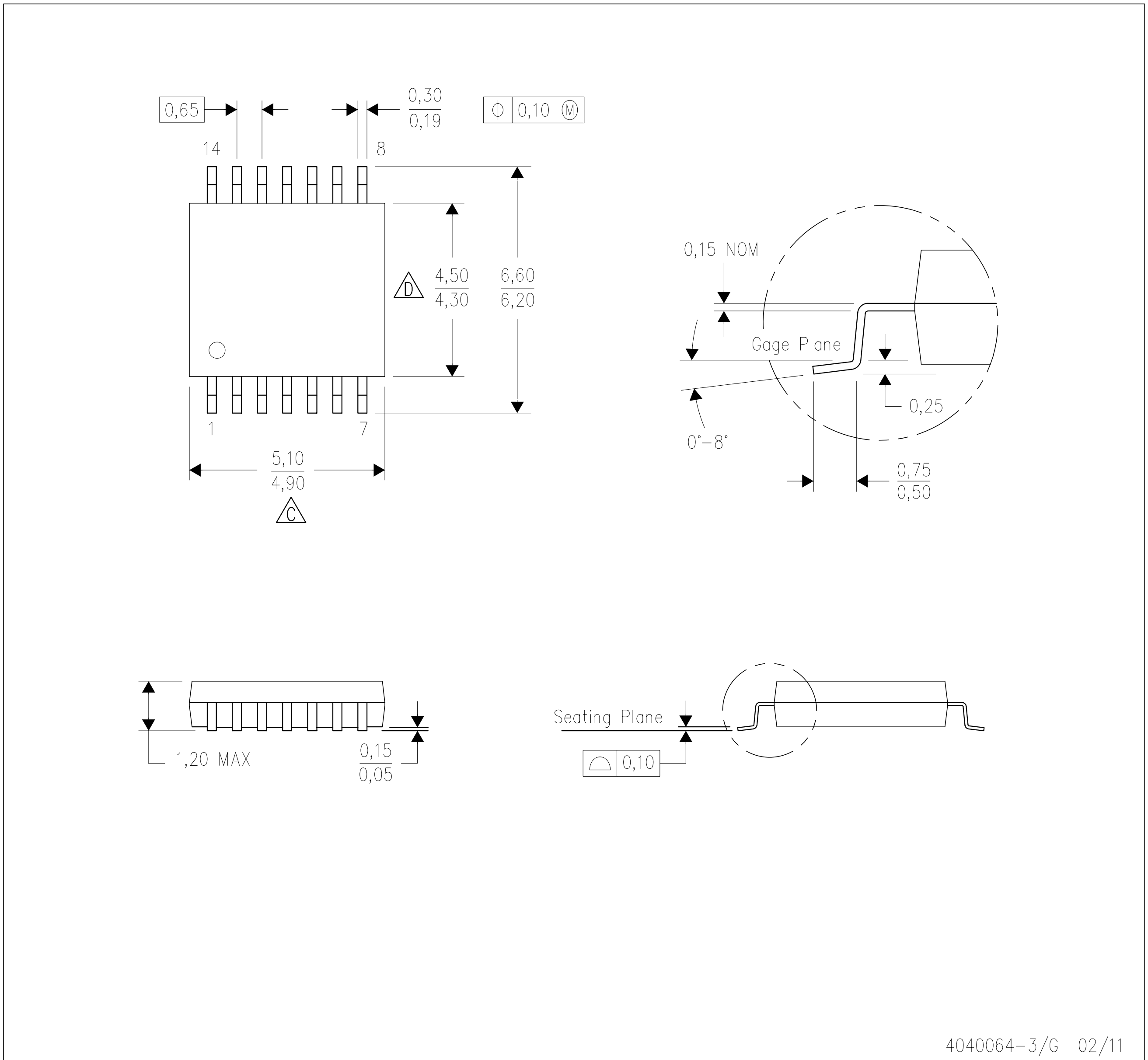
D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211283-3/E 08/12

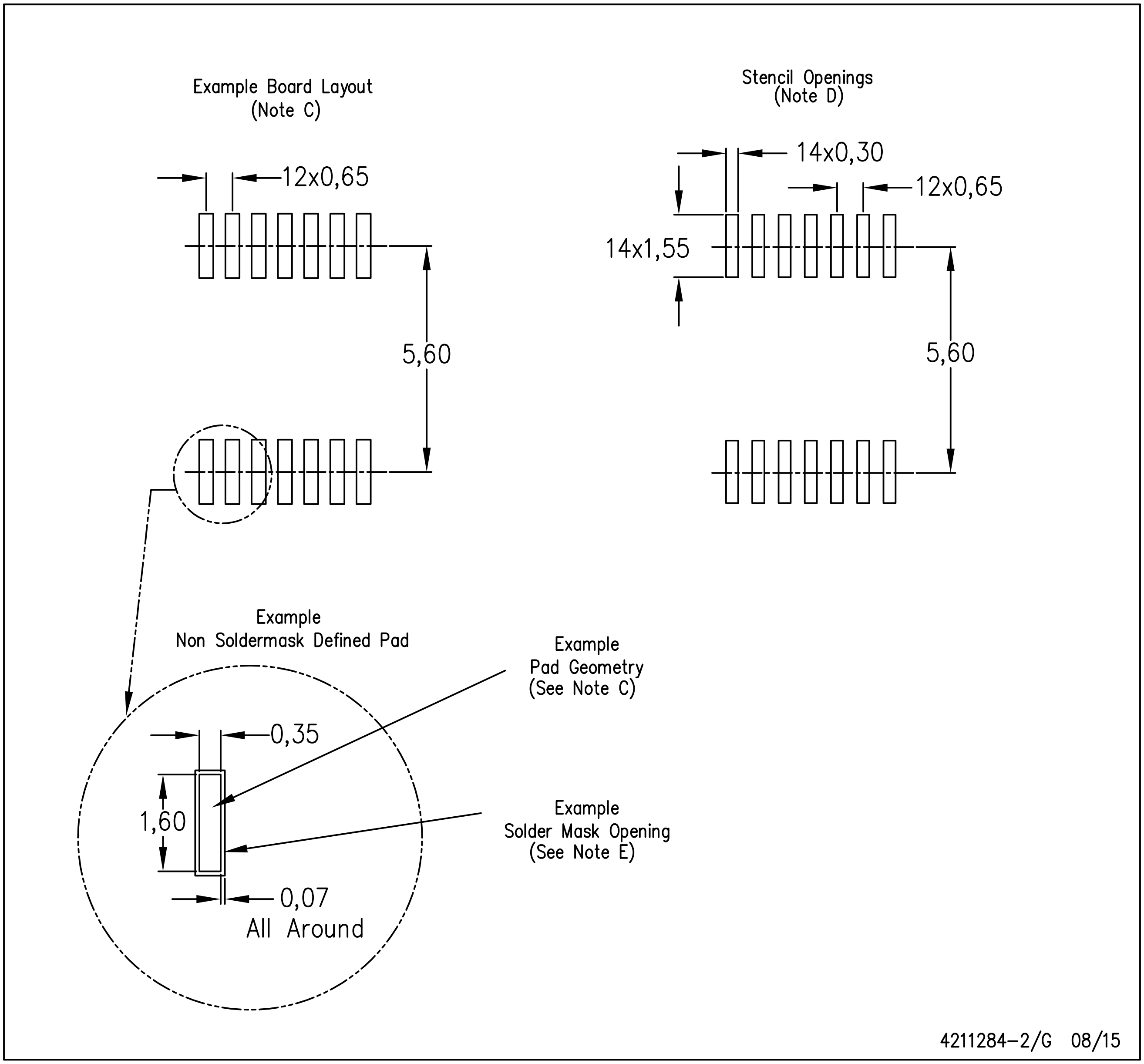
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

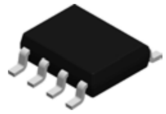


NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

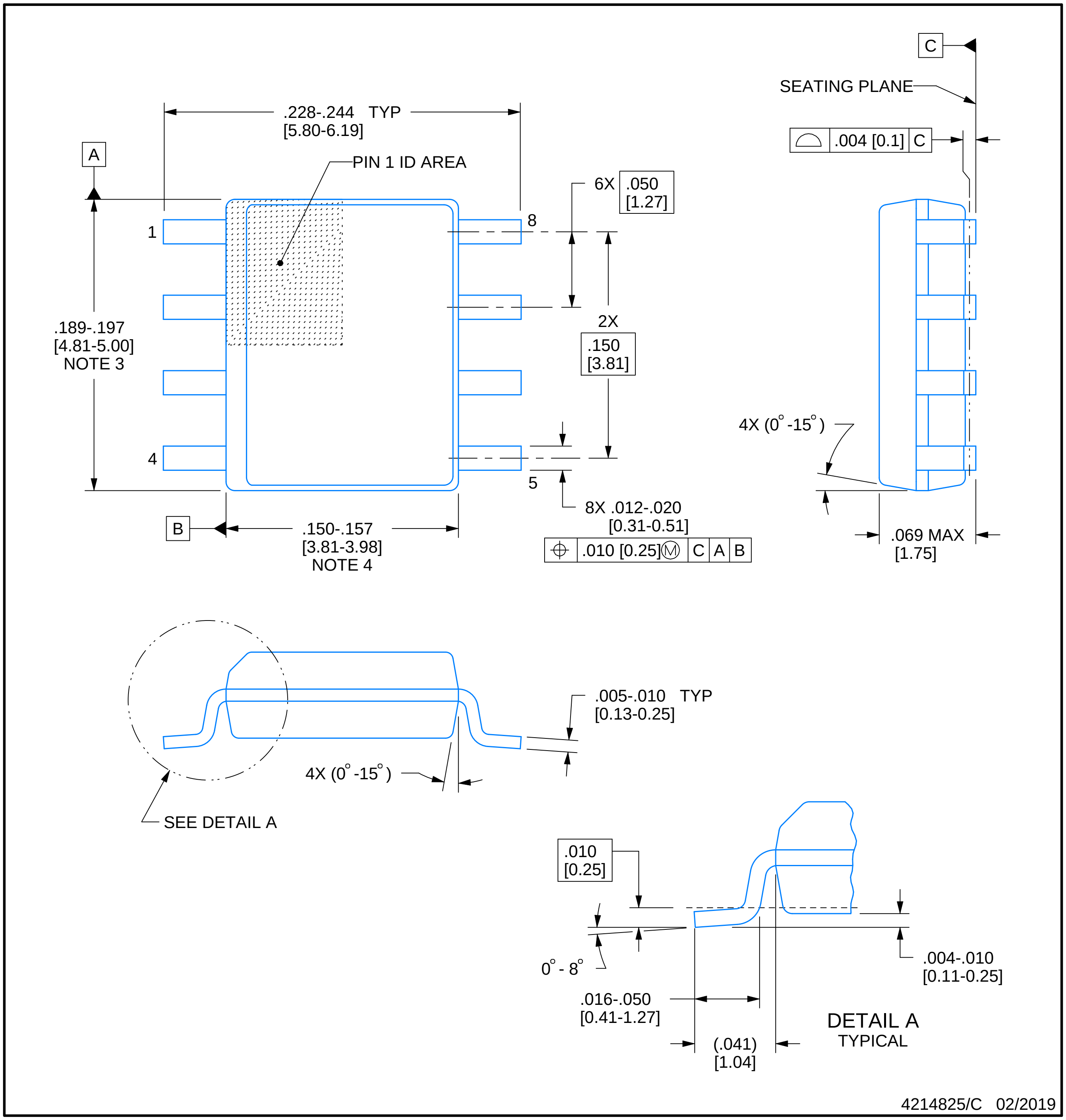


PACKAGE OUTLINE

D0008A

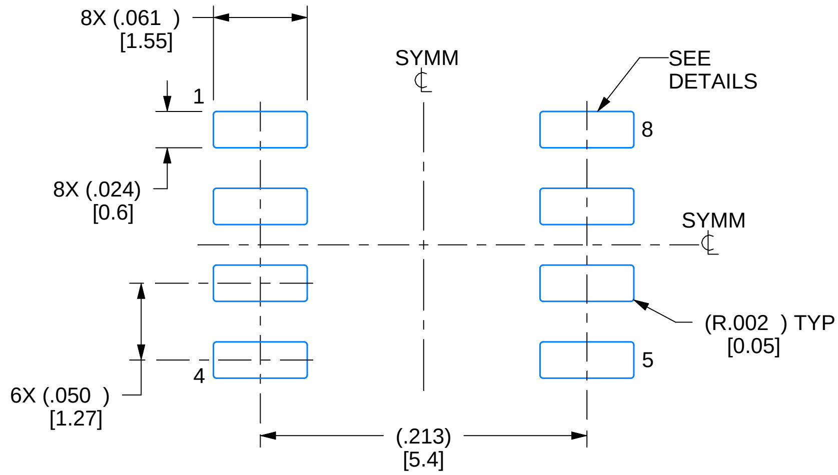
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

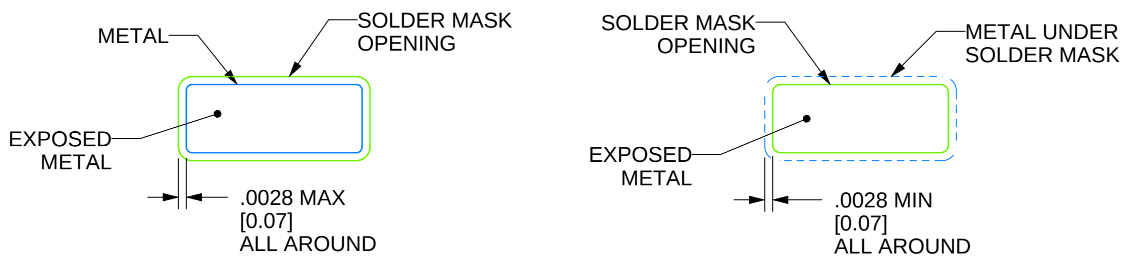


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

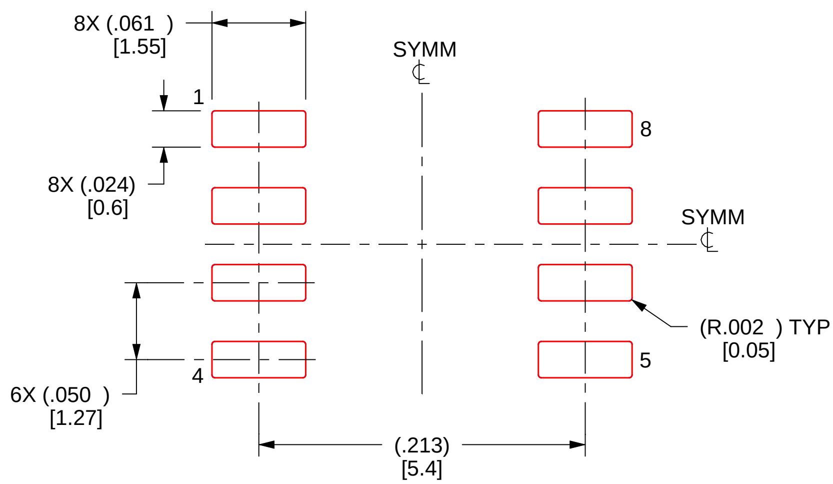
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



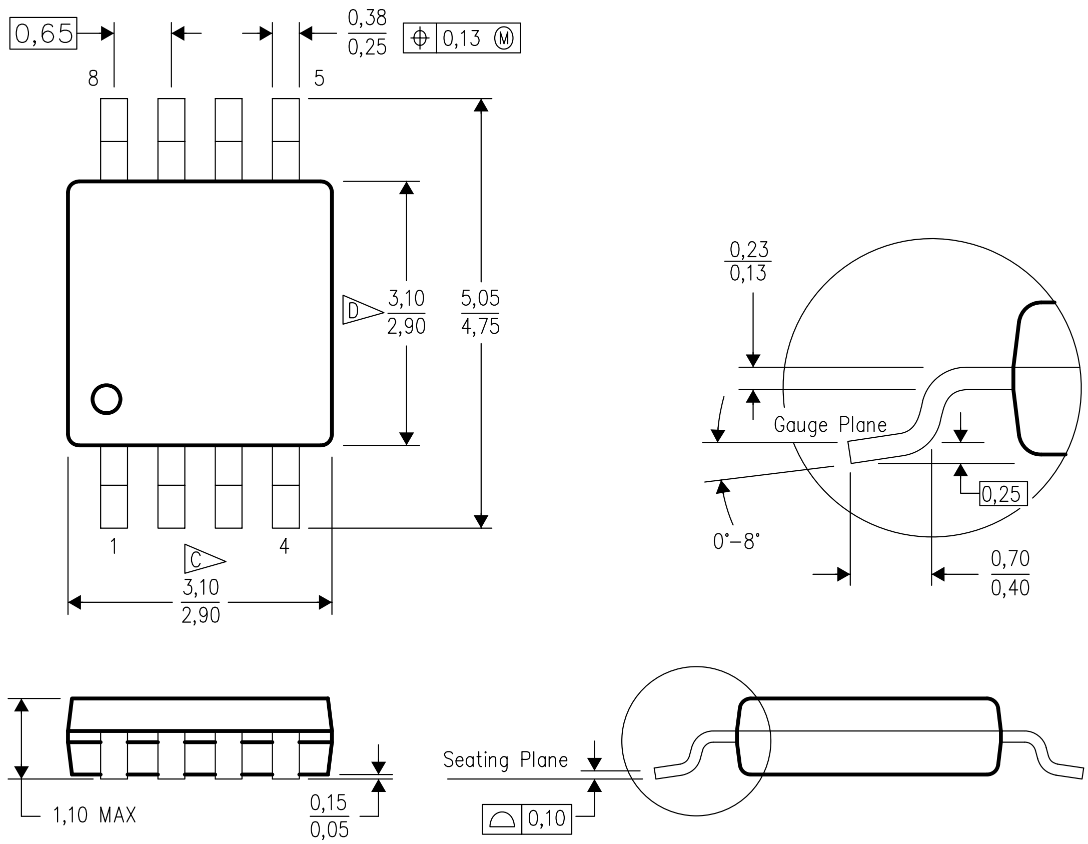
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

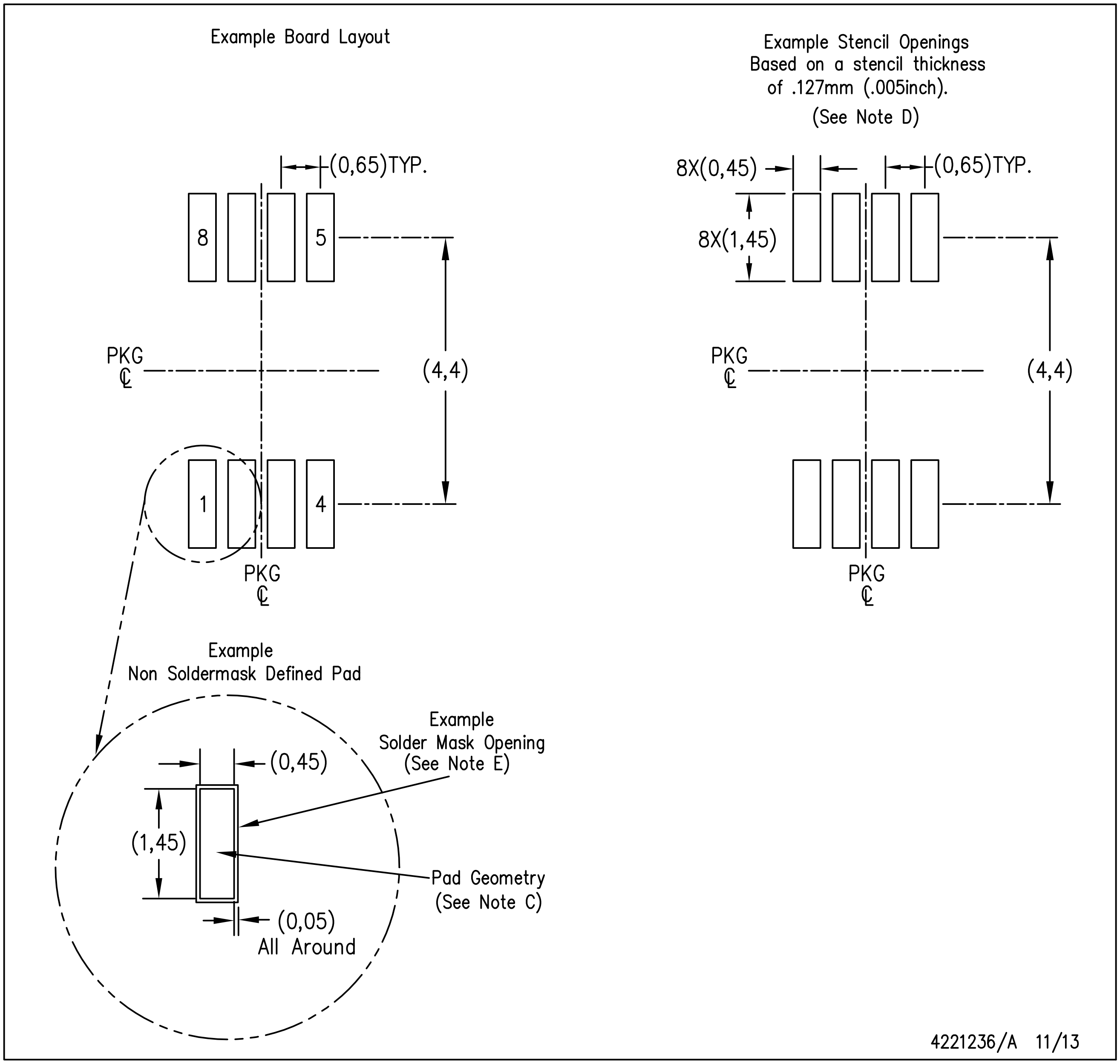
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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