TUSB544 USB TYPE-C™ 8.1 Gbps 多协议线性转接驱动器

1 特性

- 支持高达 8.1 Gbps 的协议无关正反两用式 4 通道线性转接驱动器。
  - 带有 USB 3.1 第 1 代和 DisplayPort 1.4 作为交替模式的 USB Type-C。
- 支持集成有 USB 3.1 和 DisplayPort 多路复用器，适用于 Type-C 应用的处理器
- 支持信号调节内部 Type-C 线缆
- 适用于 SBU 信号的交叉点多路复用器
- 频率为 4.05GHz 时，支持高达 11dB 的线性均衡功能
- 用于通道方向和均衡的 GPIO 和 I^2C 控制
- 通过监控 USB 功耗状态和嗅探 DP 链路训练可实现高级电源管理
- 可通过 GPIO 或 I^2C 进行配置
- 支持热插拔
- 3.3V 单电源
- 工业级温度范围：–40ºC 至 85ºC (TUSB544I)
- 商业级温度范围：0ºC 至 70ºC (TUSB544)
- 4mm × 6mm、0.4mm 间距、40 引脚 QFN 封装

2 应用

- 平板电脑
- 笔记本电脑
- 台式机
- 扩展坞

3 说明

TUSB544 是一种 USB Type-C 交替模式转接驱动器开关，可支持高达 8.1Gbps 的数据速率。此协议无关线性转接驱动器能够支持包括 VESA DisplayPort 在内的 USB Type-C 交替模式接口。

TUSB544 提供多个接收线性均衡级别，用于补偿因线缆或电路板线迹损耗产生的码间串扰 (ISI)。该器件由 3.3V 单电源供电运行，支持商业级温度范围和工业级温度范围。

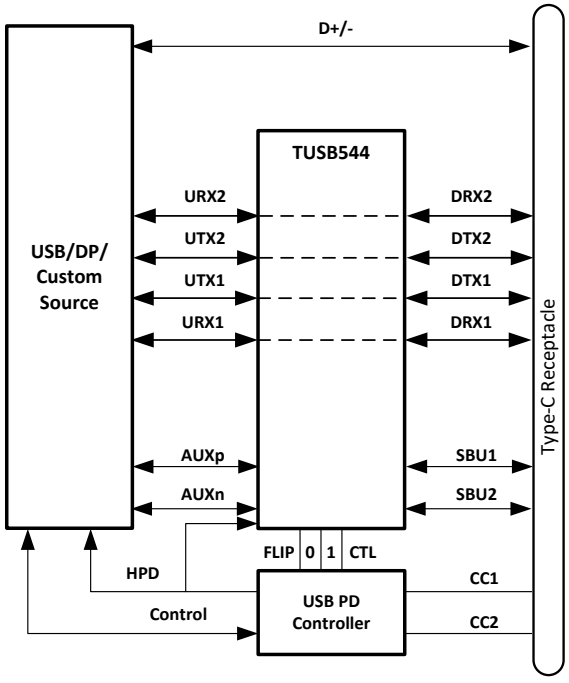
TUSB544 的全部四个通道均为正反两用式，这使其成为可用于诸多应用的多用途 信号调节器。

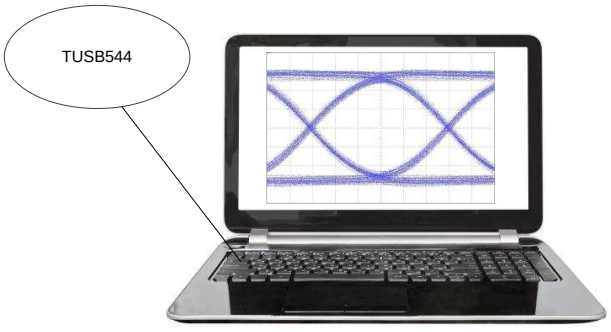
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TUSB544	WQFN (40)	4.00mm x 6.00mm
TUSB544I		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图





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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (November 2017) to Revision E — **Page**

- 更改了简化原理图 ... 1

Changes from Revision C (October 2017) to Revision D — **Page**

- 更改了*说明* 部分第二段中的文本，将“..因码间串扰 (ISI) 产生的线缆或电路板迹线损耗”更改成了“..因线缆或电路板线迹损耗产生的码间串扰 (ISI)。” ... 1
- Changed Pin 2 and Pin 35 text From: "When I2C_EN !=0,.." To: "In I2C mode,.." in the *Pin Functions* ... 4
- Changed Pin 14 text From: "..levels for the GPIO configuration.." To: "..levels for the 2-level GPIO configuration.." in the *Pin Functions* ... 5
- Changed Pin 17 in the text From: 0 = GPIO Mode (I^2C disabled) To: 0 = GPIO Mode AUX Snoop enabled (I^2C disabled) in the *Pin Functions* ... 5
- Changed Pins 21, 22, and 23 From: "When I2C_EN !=0,.." To: "In GPIO mode,.." in the *Pin Functions* ... 5
- Removed "When I2C_EN = 0" from pin 32. ... 5
- In pin 32, changed 2ms to $t_{CTL1\_DEBOUNCE}$ ... 5
- From: DEQ1 sets the high-frequency equalizer gain for downstream facing URX1, URX2, UTX1, UTX2 receivers. To: DEQ1 sets the high-frequency equalizer gain for downstream facing DRX1, DRX2, DTX1, DTX2 receivers ... 5
- Deleted the MAX value of 10 ms from $t_{CTL1\_DEBOUNCE}$ in the *Switching Characteristics* ... 10
- Added test Condition " DP lanes will be disabled if low for greater than min value" for $t_{CTL1\_DEBOUNCE}$ in the *Switching Characteristics* ... 10
- Changed text From: "There is an internal 30 kΩ pull-up and a 94kΩ pull-down." To: "There are internal pull-up and a pull-down resisters." in *4-Level Inputs* ... 18
- Changed text From: "..when I2C_EN = “0”." To: "..when I2C_EN = “0” or "F"." in the first paragraph of *Device Configuration in GPIO Mode* ... 19
- Changed 表 4 ... 21
- Changed text From: "..when I2C_EN is not equal to “0”." To: "..when I2C_EN is equal to “1”. " in *Device*

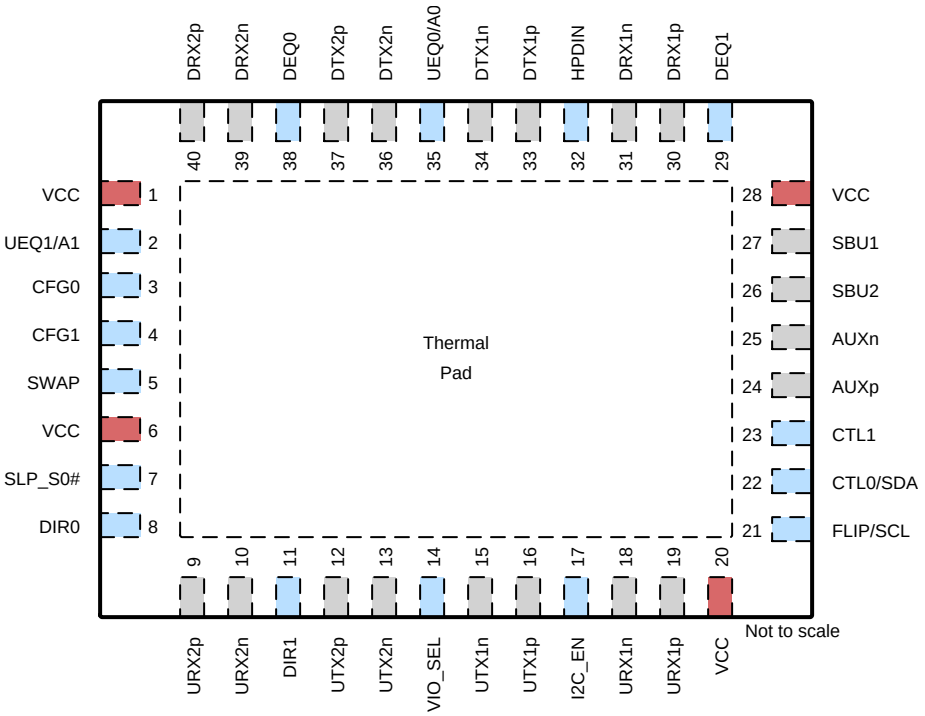
Changes from Revision B (Mayl 2017) to Revision C **Page**

Changes from Revision A (April 2017) to Revision B **Page**

Changes from Original (April 2017) to Revision A **Page**

5 Pin Configuration and Functions

RNQ Package
40-Pin (WQFN)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VCC	P	3.3 V Power Supply
2	UEQ1/A1	4 Level I	This pin along with UEQ0 sets the high-frequency equalizer gain for upstream facing URX1, URX2, UTX1, UTX2 receivers. Up to 9.4 dB of EQ available. In I^2C mode, this pin will also set TUSB544 I^2C address. Refer to 表 10.
3	CFG0	4 Level I	CFG0. This pin along with CFG1 will select VOD linearity range and DC gain for all the downstream and upstream channels. Refer to 表 8 for VOD linearity range and DC gain options.
4	CFG1	4 Level I	CFG1. This pin along with CFG0 will set VOD linearity range and DC gain for all the downstream and upstream channels. Refer to 表 8 for VOD linearity range and DC gain options.
5	SWAP	2 Level I	This pin swaps all the channel directions and EQ settings of downstream facing and upstream facing data path inputs. 0 – Do not swap channel directions and EQ settings (Default) 1. – Swap channel directions and EQ settings.
6	VCC	P	3.3V Power Supply
7	SLP_S0#	2 Level I	This pin when asserted low will disable Receiver Detect functionality. While this pin is low and TUSB544 is in U2/U3, TUSB544 will disable LOS and LFPS detection circuitry and RX termination for both channels will remain enabled. If this pin is low and TUSB544 is in Disconnect state, the RX detect functionality will be disabled and RX termination for both channels will be disabled. 0 – RX Detect disabled 1 – RX Detect enabled (Default)
8	DIR0	2 Level I	This pin along with DIR1 sets the data path signal direction format. Refer to 表 4 for signal direction formats.
9	URX2p	Diff I/O	Differential positive input/output for upstream facing RX2 port.
10	URX2n	Diff I/O	Differential negative input/output for upstream facing RX2 port.
11	DIR1	2 Level I/O	This pin along with DIR0 sets the data path signal direction format. Refer to 表 4 for signal direction formats.
12	UTX2p	Diff I/O	Differential positive input/output for upstream facing TX2 port.
13	UTX2n	Diff I/O	Differential negative input/output for upstream facing TX2 port.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
14	VIO_SEL	4 Level I/O	This pin selects I/O voltage levels for the 2-level GPIO configuration pins and the I^2C interface: 0 = 3.3-V configuration I/O voltage, 3.3-V I^2C interface (Default) R = 3.3-V configuration I/O voltage, 1.8-V I^2C interface F = 1.8-V configuration I/O voltage, 3.3-V I^2C interface 1 = 1.8-V configuration I/O voltage, 1.8-V I^2C interface.
15	UTX1n	Diff I/O	Differential negative input/output for upstream facing TX1 port.
16	UTX1p	Diff I/O	Differential positive input/output for upstream facing TX1 port.
17	I2C_EN	4 Level I	I^2C Programming or Pin Strap Programming Select. 0 = GPIO Mode AUX Snoop enabled (I^2C disabled) R = TI Test Mode (I^2C enabled) F = GPIO Mode, AUX Snoop Disabled (I^2C disabled) 1 = I^2C enabled.
18	URX1n	Diff I/O	Differential negative input/output for upstream facing RX1 port.
19	URX1p	Diff I/O	Differential positive input/output for upstream facing RX1 port.
20	VCC	P	3.3V Power Supply
21	FLIP/SCL	2 Level I (Failsafe)	In GPIO mode, this is Flip control pin, otherwise this pin is I^2C clock.
22	CTL0/SDA	2 Level I (Failsafe)	In GPIO mode, this is a USB3.1 Switch control pin, otherwise this pin is I^2C data.
23	CTL1	2 Level I (PD)	DP Alt mode Switch Control Pin. In GPIO mode, this pin will enable or disable DisplayPort functionality. Otherwise DisplayPort functionality is enabled and disabled through I^2C registers. L = DisplayPort Disabled. H = DisplayPort Enabled. In I^2C mode, this pin is not used by device.
24	AUXp	I/O, CMOS	AUXp. DisplayPort AUX positive I/O connected to the DisplayPort source or sink through an AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 100-kΩ resistor to GND between the AC coupling capacitor and the AUXp pin if the TUSB544 is used on the DisplayPort source side, or a 1-MΩ resistor to DP_PWR (3.3V) between the AC coupling capacitor and the AUXp pin if TUSB544 is used on the DisplayPort sink side. This pin along with AUXn is used by the TUSB544 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C plug.
25	AUXn	I/O, CMOS	AUXn. DisplayPort AUX I/O connected to the DisplayPort source or sink through an AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 100-kΩ resistor to DP_PWR (3.3V) between the AC coupling capacitor and the AUXn pin if the TUSB544 is used on the DisplayPort source side, or a 1-MΩ resistor to GND between the AC coupling capacitor and the AUXn pin if TUSB544 is used on the DisplayPort sink side. This pin along with AUXp is used by the TUSB544 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C plug.
26	SBU2	I/O, CMOS	SBU2. When the TUSB544 is used on the DisplayPort source side, this pin should be DC coupled to the SBU2 pin of the Type-C receptacle. When the TUSB544 is used on the DisplayPort sink side, this pin should be DC coupled to the SBU1 pin of the Type-C receptacle. A 2-MΩ resistor to GND is also recommended.
27	SBU1	I/O, CMOS	SBU1. When the TUSB544 is used on the DisplayPort source side, this pin should be DC coupled to the SBU1 pin of the Type-C receptacle. When the TUSB544 is used on the DisplayPort sink side, this pin should be DC coupled to the SBU2 pin of the Type-C receptacle. A 2-MΩ resistor to GND is also recommended.
28	VCC	P	3.3V Power Supply
29	DEQ1	4 Level I	This pin along with DEQ0 sets the high-frequency equalizer gain for downstream facing DRX1, DRX2, DTX1, DTX2 receivers. Up to 11 dB of EQ available.
30	DRX1p	Diff I/O	Differential positive input/output for downstream facing RX1 port.
31	DRX1n	Diff I/O	Differential negative input/output for downstream facing RX1 port.
32	HPDIN	2 Level I (PD)	This pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is low for greater than $t_{CTL1\_DEBOUNCE}$, all DisplayPort lanes are disabled and AUX to SBU switch will remain closed.
33	DTX1p	Diff I/O	Differential positive input/output for downstream facing TX1 port.
34	DTX1n	Diff I/O	Differential negative input/output for downstream facing TX1 port.
35	UEQ0/A0	4 Level I	This pin along with UEQ1 sets the high-frequency equalizer gain for upstream facing URX1, URX2, UTX1, UTX2 receivers. Up to 9.4 dB of EQ available. In I^2C mode, this pin will also set TUSB544 I^2C address. Refer to 表 10.
36	DTX2n	Diff I/O	Differential negative input/output for downstream facing TX2 port.
37	DTX2p	Diff I/O	Differential positive input/output for downstream facing TX2 port.
38	DEQ0	4 Level I	This pin along with DEQ1 sets the high-frequency equalizer gain for downstream facing DRX1, DRX2, DTX1, DTX2 receivers. Up to 11 dB of EQ available.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
39	DRX2n	Diff I/O	Differential negative input/output for downstream facing RX2 port.
40	DRX2p	Diff I/O	Differential positive input/output for downstream facing RX2 port.
Thermal Pad		GND	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage	V_{CC}	–0.3	4	V
Voltage Range at any input or output pin	Differential voltage between positive and negative inputs	–2.5	2.5	V
	Voltage at differential inputs	–0.5	V_{CC} + 0.5	V
	CMOS Inputs	–0.5	V_{CC} + 0.5	V
Maximum junction temperature, T_J			125	°C
Storage temperature ,T_{STG}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6	kV
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Main power supply		3	3.3	3.6	V
	Supply ramp requirement				100	ms
V_{I2C}	Supply that external resistors on SDA and SCL are pulled up to.		1.70		3.6	V
V_{PSN}	Supply Noise on V_{CC} terminals				100	mV
T_A	Operating free-air temperature	TUSB544	0		70	°C
		TUSB544I	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TUSB544 RNQ (QFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{CC\text{-}ACTIVE\text{-}USB}$	Average active power USB Only	Link in U0 with GEN1 data transmission. EQ control pins = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000 $mV_{p\text{-}p}$; VOD Linearity = 900 $mV_{p\text{-}p}$; CTL1 = L; CTL0 = H		297		mW
$P_{CC\text{-}ACTIVE\text{-}USB\text{-}DP1}$	Average active power USB + 2 Lane DP	Link in U0 with GEN1 data transmission. EQ control pins = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000 $mV_{p\text{-}p}$; VOD Linearity = 900 $mV_{p\text{-}p}$; CTL1 = H; CTL0 = H		578		mW
$P_{CC\text{-}ACTIVE\text{-}USB\text{-}CUSTOM}$	Average active power USB + 2 Channel Custom Alt Mode	Link in U0 with GEN1 data transmission. EQ control pins = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000 $mV_{p\text{-}p}$; VOD Linearity = 900 $mV_{p\text{-}p}$; CTL1 = H; CTL0 = H		578		mW
$P_{CC\text{-}Active\text{-}DP}$	Average active power 4 Lane DP Only	Four active DP lanes operating at 8.1 Gbps; EQ control pins = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000 $mV_{p\text{-}p}$; VOD Linearity = 900 $mV_{p\text{-}p}$; CTL1 = H; CTL0 = L;		564		mW
$P_{CC\text{-}NC\text{-}USB}$	Average power with no connection	No GEN1 device is connected to TXP/TXN; CTL1 = L; CTL0 = H;		2.5		mW
$P_{CC\text{-}U2U3}$	Average power in U2/U3	Link in U2 or U3 USB Mode Only; CTL1 = L; CTL0 = H;		2.0		mW
$P_{CC\text{-}SHUTDOWN}$	Device Shutdown	CTL1 = L; CTL0 = L; I2C_EN = 0;		0.65		mW

6.6 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4-State CMOS Inputs(UEQ[1:0];DEQ[1:0], CFG[1:0], A[1:0], I2C_EN, VIO_SEL)						
I_{IH}	High level input current	V_{CC} = 3.6 V_{IN} = 3.6 V	20		80	µA
I_{IL}	Low level input current	V_{CC} = 3.6 V; V_{IN} = 0 V	–160		–40	µA
4-Level V_{TH}	Threshold 0 / R	V_{CC} = 3.3 V		0.55		V
	Threshold R/ Float	V_{CC} = 3.3 V		1.65		V
	Threshold Float / 1	V_{CC} = 3.3 V		2.7		V
R_{PU}	Internal pull-up resistance			35		kΩ
R_{PD}	Internal pull-down resistance			95		kΩ
2-State CMOS Input (CTL0, CTL1, FLIP, HPDIN, SLP_S0#, SWAP, DIR[1:0]).						
V_{IH}	High-level input voltage		0.7×V_{IO}		3.6	V
V_{IL}	Low-level input voltage		0		0.3×V_{IO}	V
R_{PD}	Internal pull-down resistance for CTL1			500		kΩ
I_{IH}	High-level input current	V_{IN} = 3.6 V	–25		25	µA
I_{IL}	Low-level input current	V_{IN} = GND, V_{CC} = 3.6 V	–25		25	µA
I^2C Control Pins SCL, SDA						

DC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	I2C_EN = 0	0.7 x V_{I2C}		3.6	V
V_{IL}	Low-level input voltage	I2C_EN = 0	0		0.3 x V_{I2C}	V
V_{OL}	Low-level output voltage	I2C_EN = 0; I_{OL} = 3 mA	0		0.4	V
I_{OL}	Low-level output current	I2C_EN = 0; V_{OL} = 0.4 V	20			mA
I_{I_I2C}	Input current on SDA pin	0.1 x V_{I2C} < Input voltage < 3.3 V	–10		10	µA
C_{I_I2C}	Input capacitance		0.5		10	pF

6.7 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB Gen 1 Differential Receiver (UTX1P/N, UTX2P/N, DRX1P/N, DRX2P/N)						
$V_{RX-DIFF-PP}$	Input differential peak-peak voltage swing linear dynamic range	AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel		2000		mVpp
$V_{RX-DC-CM}$	Common-mode voltage bias in the receiver (DC)			0		V
$R_{RX-DIFF-DC}$	Differential input impedance (DC)	Present after a GEN1 device is detected on receiver pins	72		120	Ω
$R_{RX-CM-DC}$	Receiver DC common mode impedance	Present after a GEN1 device is detected on receiver pins	18		30	Ω
$Z_{RX-HIGH-IMP-DC-POS}$	Common-mode input impedance with termination disabled (DC)	Present when no GEN1 device is detected on receiver pins. Measured over the range of 0-500mV with respect to GND.	25			kΩ
$V_{SIGNAL-DET-DIFF-PP}$	Input differential peak-to-peak signal detect assert level	At 5 Gbps, no loss at the input, PRBS7 pattern		80		mV
$V_{RX-IDLE-DET-DIFF-PP}$	Input differential peak-to-peak signal detect de-assert Level	At 5 Gbps, no loss at the input, PRBS7 pattern		60		mV
$V_{RX-LFPS-DET-DIFF-PP}$	Low frequency periodic signaling (LFPS) detect threshold	Below the minimum is squelched.	100		300	mV
$V_{RX-CM-AC-P}$	Peak RX AC common-mode voltage	Measured at package pin			150	mV
C_{RX}	RX input capacitance to GND	At 2.5 GHz		0.5	1	pF
$RL_{RX-DIFF}$	Differential return Loss	50 MHz – 1.25 GHz at 90 Ω		–16		dB
		2.5 GHz at 90 Ω		–14		dB
RL_{RX-CM}	Common-mode return loss	50 MHz – 2.5 GHz at 90 Ω		–13		dB
EQ_{SS}	Receiver equalization at maximum setting	UEQ[1:0] and DEQ[1:0]. at 2.5 GHz			9	dB
USB Gen 1 Differential Transmitter (DTX1P/N, DTX2P/N, URX1P/N, URX2P/N)						
$V_{TX-DIFF-PP}$	Transmitter dynamic differential voltage swing range.			1600		mV_{PP}
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during receiver detection				600	mV
$V_{TX-CM-IDLE-DELTA}$	Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS		–600		600	mV
$V_{TX-DC-CM}$	Common-mode voltage bias in the transmitter (DC)			1.75		V
$V_{TX-CM-AC-PP-ACTIVE}$	Tx AC common-mode voltage active	Max mismatch from Txp + Txn for both time and amplitude			100	mV_{PP}
$V_{TX-IDLE-DIFF-AC-PP}$	AC electrical idle differential peak-to-peak output voltage	At package pins	0		10	mV
$V_{TX-IDLE-DIFF-DC}$	DC electrical idle differential output voltage	At package pins after low pass filter to remove AC component	0		14	mV
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC common-mode voltage between U1 and U0	At package pin			200	mV
$R_{TX-DIFF}$	Differential impedance of the driver		75		120	Ω
$C_{AC-COUPLING}$	AC coupling capacitor		75		265	nF
R_{TX-CM}	Common-mode impedance of the driver	Measured with respect to AC ground over 0–500 mV	18		30	Ω

AC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{TX-SHORT}$	TX short circuit current	TXP/N shorted to GND			67	mA
$RL_{TX-DIFF}$	Differential return loss	50 MHz – 1.25 GHz at 90 Ω		–16		dB
		2.5 GHz at 90 Ω		–13		dB
RL_{TX-CM}	Common-mode return loss	50 MHz – 2.5 GHz at 90 Ω		–11		dB
AC Characteristics						
Crosstalk	Differential crosstalk between any signal pairs	at 4.05 GHz		–30		dB
G_{LF}	Low frequency voltage gain	at 10 MHz, 200 mV_{PP} < V_{ID} < 2000 mV_{PP}; 0-dB low-frequency gain setting	–1	0	1	dB
CP_{1dB-LF}	Low frequency 1-dB compression point	at 10 MHz, 200 mV_{PP} < V_{ID} < 2000 mV_{PP}; VOD linearity setting = 1100mV_{PP}		1100		mV_{PP}
CP_{1dB-HF}	High frequency 1-dB compression point	at 4.05 GHz, 200 mV_{PP} < V_{ID} < 2000 mV_{PP}; VOD linearity setting = 1100mV_{PP}		1200		mV_{PP}
f_{LF}	Low frequency cutoff	200 mV_{PP}< V_{ID} < 2000 mV_{PP}		25	50	kHz
DJ	TX output deterministic jitter	200 mV_{PP} < V_{ID} < 2000 mV_{PP}, PRBS7, 5 Gbps		0.05		UIpp
		200 mV_{PP} < V_{ID} < 2000 mV_{PP}, PRBS7, 8.1 Gbps		0.08		UIpp
TJ	TX output total jitter	200 mV_{PP} < V_{ID} < 2000 mV_{PP}, PRBS7, 5 Gbps		0.08		UIpp
		200 mV_{PP} < V_{ID} < 2000 mV_{PP}, PRBS7, 8.1 Gbps		0.135		UIpp
DisplayPort Receiver UTX1P/N, UTX2P/N, URX1P/N, URX2P/N						
V_{ID_PP}	Peak-to-peak input differential dynamic voltage range			2000		mV_{pp}
V_{IC}	Input common mode voltage			0		V
C_{AC}	AC coupling capacitance		75		200	nF
EQ_{DP}	Receiver equalizer at maximum setting	DEQ[1:0],UEQ[1:0] at 4.05 GHz		9.5		dB
d_R	Data rate	HBR3			8.1	Gbps
R_{ti}	Input termination resistance		80	100	120	Ω
DisplayPort Transmitter DTX1P/N, DTX2P/N, DRX1P/N, DRX2P/N						
$V_{TX-DIFFPP}$	VOD dynamic range			1500		mV
$I_{TX-SHORT}$	TX short circuit current	TXP/N shorted to GND			67	mA
$V_{TX(DC-CM)}$	Common-mode voltage bias in the transmitter (DC)			1.75		V
AUXP/N and SBU1/2						
R_{ON}	Output ON resistance	V_{CC} = 3.3 V; V_I = 0 to 0.4 V for AUXP; V_I = 2.7 V to 3.6 V for AUXN		5	10	Ω
ΔR_{ON}	ON resistance mismatch within pair	V_{CC} = 3.3 V; V_I = 0 to 0.4V for AUXP; V_I = 2.7V to 3.6V for AUXN			1	Ω
R_{ON_FLAT}	ON resistance flatness (R_{ON} max – R_{ON} min) measured at identical V_{CC} and temperature	V_{CC} = 3.3 V; V_I = 0 to 0.4V for AUXP; V_I = 2.7V to 3.6 V for AUXN			2	Ω
$V_{AUXP\_DC\_CM}$	AUX Channel DC common mode voltage for AUXP and SBU1.	V_{CC} = 3.3 V	0		0.4	V
$V_{AUXN\_DC\_CM}$	AUX Channel DC common mode voltage for AUXN and SBU2	V_{CC} = 3.3 V	2.7		3.6	V
C_{AUX_ON}	ON-state capacitance	V_{CC} = 3.3V; CTL1 = 1; V_I = 0V or 3.3V		4	7	pF
C_{AUX_OFF}	OFF-state capacitance	V_{CC} = 3.3V; CTL1 = 0; V_I = 0V or 3.3V		3	6	pF

6.8 Timing Requirements

			MIN	NOM	MAX	UNIT
USB Gen 2						
$t_{IDLEEntry}$	Delay from U0 to electrical idle	See 图 4		10		ns
$t_{IDELExit\_U1}$	U1 exist time: break in electrical idle to the transmission of LFPS	See 图 4		6		ns
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS			10		µs
t_{RXDET_INTVL}	RX detect interval while in Disconnect				12	ms
$t_{IDLEExit\_DISC}$	Disconnect Exit Time			15		ms
t_{Exit_SHTDN}	Shutdown Exit Time			1		ms
t_{DIFF_DLY}	Differential Propagation Delay	See 图 3			300	ps
t_R, t_F	Output Rise/Fall time (see 图 5)	20%-80% of differential voltage measured 1 inch from the output pin		40		ps
t_{RF_MM}	Output Rise/Fall time mismatch	20%-80% of differential voltage measured 1 inch from the output pin			2.6	ps

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUXP/N and SBU1/2						
t_{AUX_PD}	Switch propagation delay				400	ps
$t_{AUX\_SW\_OFF}$	Switching time CTL1 to switch OFF	Not including $t_{CTL1\_DEBOUNCE}$			500	ns
$t_{AUX\_SW\_ON}$	Switching time CTL1 to switch ON				500	ns
t_{AUX_INTRA}	Intra-pair output skew				100	ps
USB3.1 and DisplayPort mode transition requirement GPIO mode						
$t_{GP\_USB\_4DP}$	Min overlap of CTL1 and CTL1 when transitioning from USB 3.1 only mode to 4-Lane DisplayPort mode or vice versa.		4			µs
CTL1 and HPDIN						
$t_{CTL1\_DEBOUNCE}$	CTL1 and HPDIN debounce time when transitioning from H to L.	DP Lanes will be disabled if low for greater than min value.	3			ms
I^2C (Refer to 图 1)						
f_{SCL}	I^2C clock frequency				1	MHz
t_{BUF}	Bus free time between START and STOP conditions		0.5			µs
t_{HDSTA}	Hold time after repeated START condition.	After this period, the first clock pulse is generated	0.26			µs
t_{LOW}	Low period of the I^2C clock		0.5			µs
t_{HIGH}	High period of the I^2C clock		0.26			µs
t_{SUSTA}	Setup time for a repeated START condition		0.26			µs
t_{HDDAT}	Data hold time		0			µs
t_{SUDAT}	Data setup time		50			ns
t_R	Rise time of both SDA and SCL signals				120	ns
t_F	Fall time of both SDA and SCL signals		20 × (V_{I2C}/5.5 V)		120	ns
t_{SUSTO}	Setup time for STOP condition		0.26			µs
C_b	Capacitive load for each bus line				100	pF

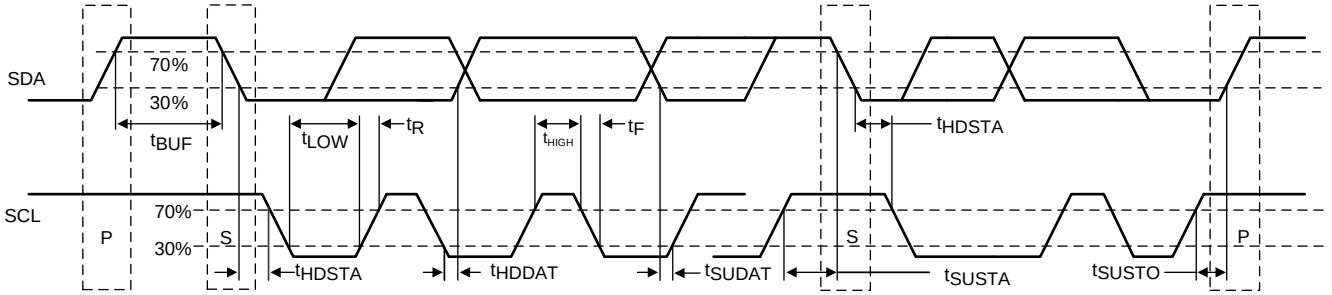


图 1. I²C Timing Diagram Definitions

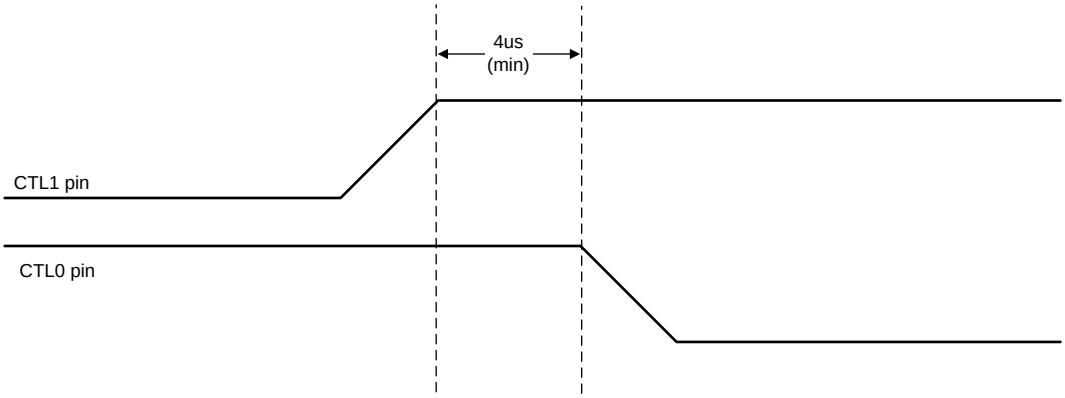


图 2. USB3.1 to 4-Lane DisplayPort in GPIO Mode

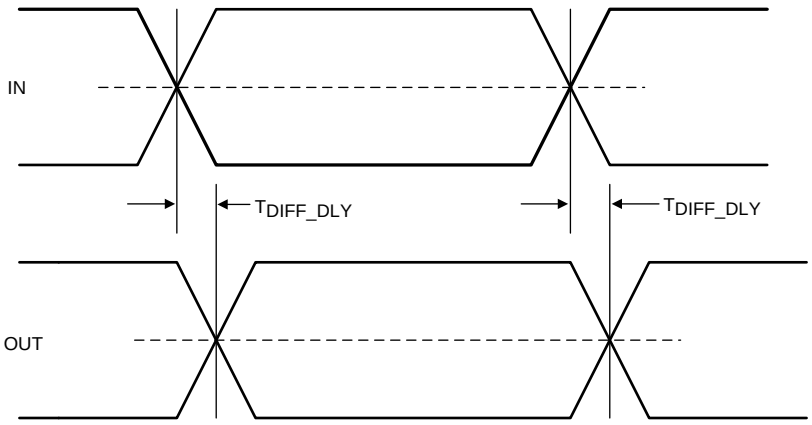


图 3. Propagation Delay

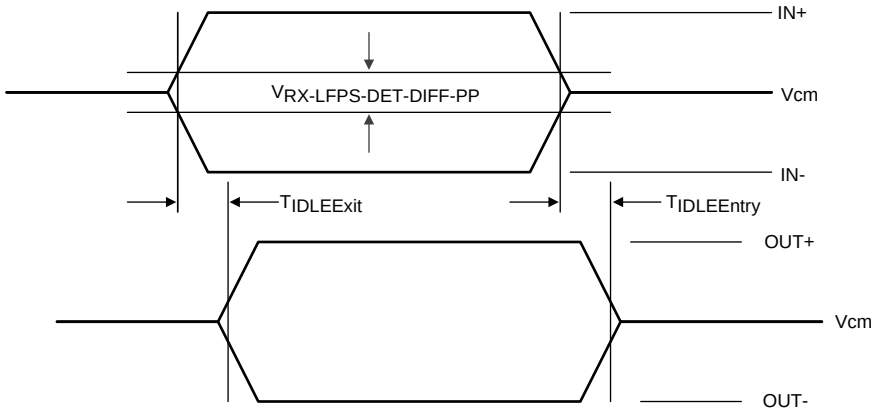


图 4. Electrical Idle Mode Exit and Entry Delay

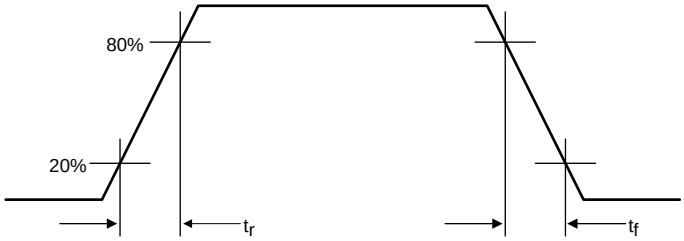


图 5. Output Rise and Fall Times

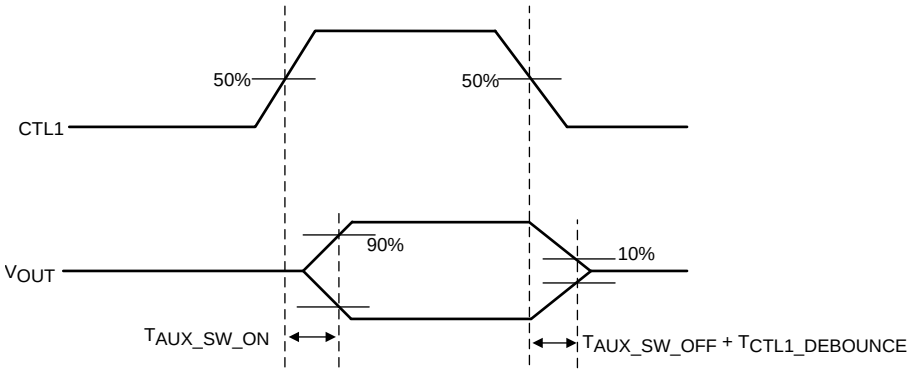


图 6. AUX and SBU Switch ON and OFF Timing Diagram

6.10 Typical Characteristics

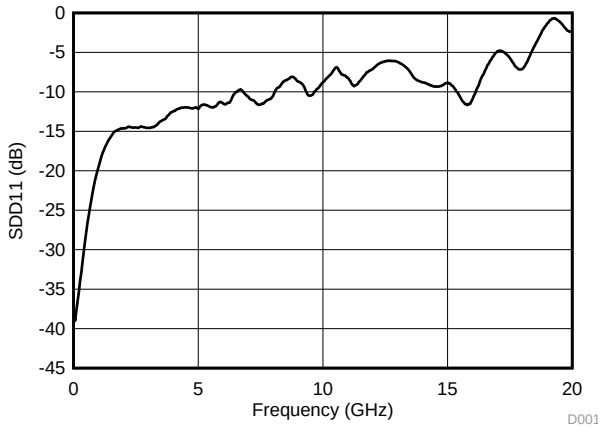


图 7. Input Return Loss Performance of the Downstream Ports

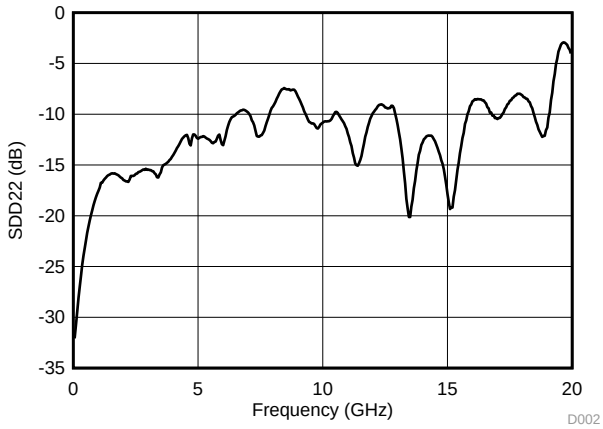


图 8. Output Return Loss Performance of the Downstream Ports

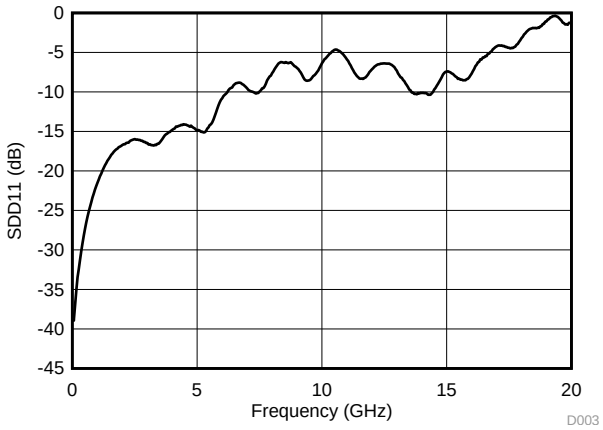


图 9. Input Return Loss Performance of the Upstream Ports

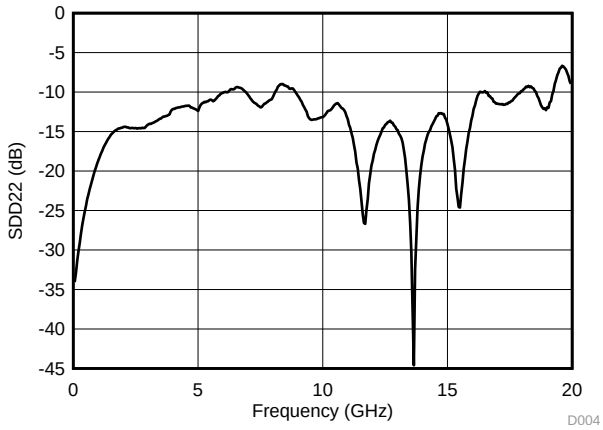


图 10. Output Return Loss Performance of the Upstream Ports

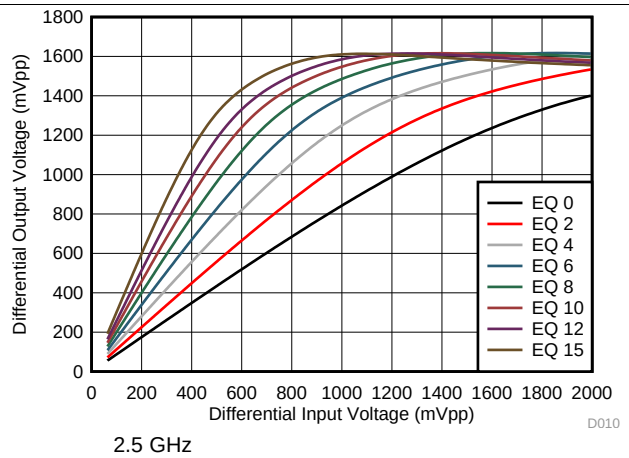


图 11. Downstream-to-Upstream Linearity Performance at 2.5 GHz

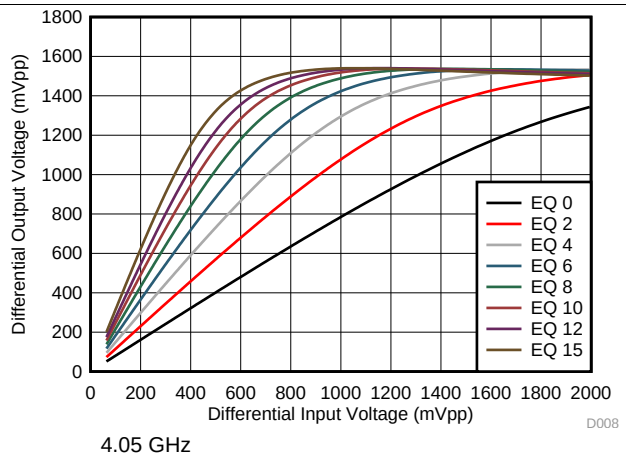
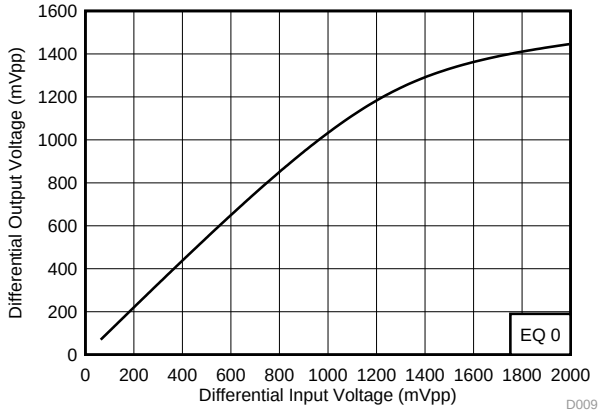


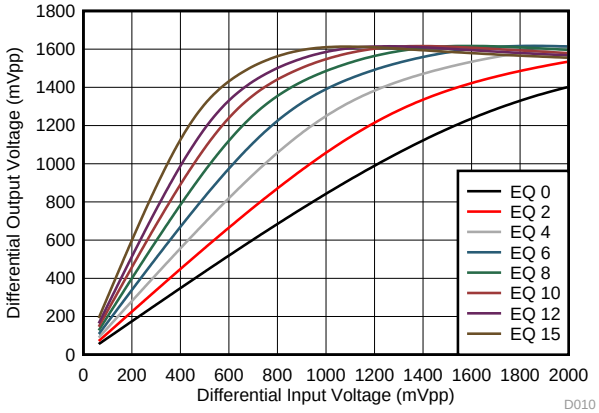
图 12. Downstream-to-Upstream Linearity Performance at 4.05 GHz

Typical Characteristics (接下页)



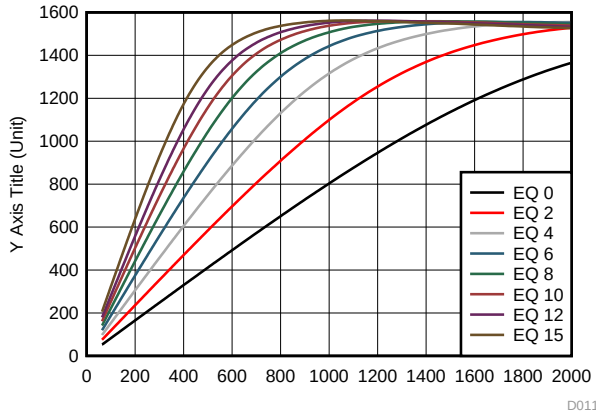
100 MHz

图 13. Downstream-to-Upstream Linearity Performance at 100 MHz



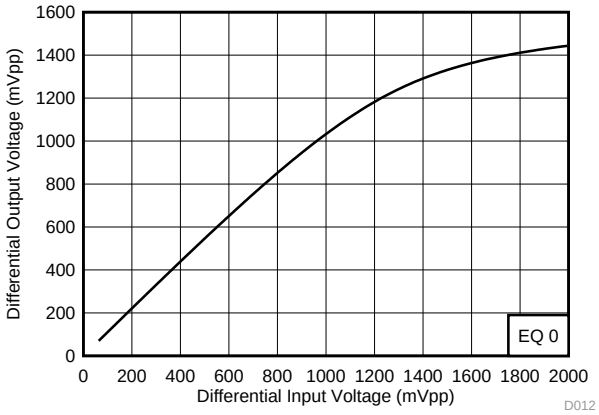
2.5 GHz

图 14. Upstream-to-Downstream Linearity Performance at 2.5 GHz



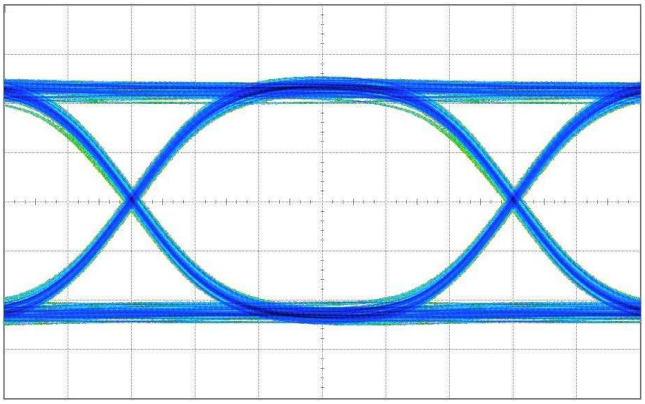
4.05 GHz

图 15. Upstream-to-Downstream Linearity Performance at 4.05 GHz



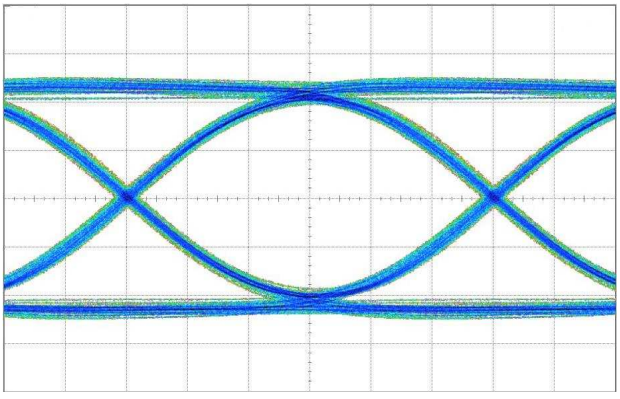
100 MHz

图 16. Upstream-to-Downstream Linearity Performance at 100 MHz



Source	Data Rate: 5 Gbps	Swing: 1 Vpp
	Data Pattern: PRBS7	
Channel	Upstream-to-Downstream, 12 in 6 mil Input PCB Channel	
Settings	EQ Setting: 7	DC Gain Setting: 0 dB
	Linear Range Setting: 1100 mVpp	

图 17. Output Eye-Pattern Performance at 5 Gbps



Source	Data Rate: 8.1 Gbps	Swing: 1 Vpp
	Data Pattern: PRBS7	
Channel	Upstream-to-Downstream, 12 in 6 mil Input PCB Channel	
Settings	EQ Setting: 7 DC Gain Setting: 0 dB	
	Linear Range Setting: 1100 mVpp	

图 18. Output Eye-Pattern Performance at 8.1 Gbps

Typical Characteristics (接下页)

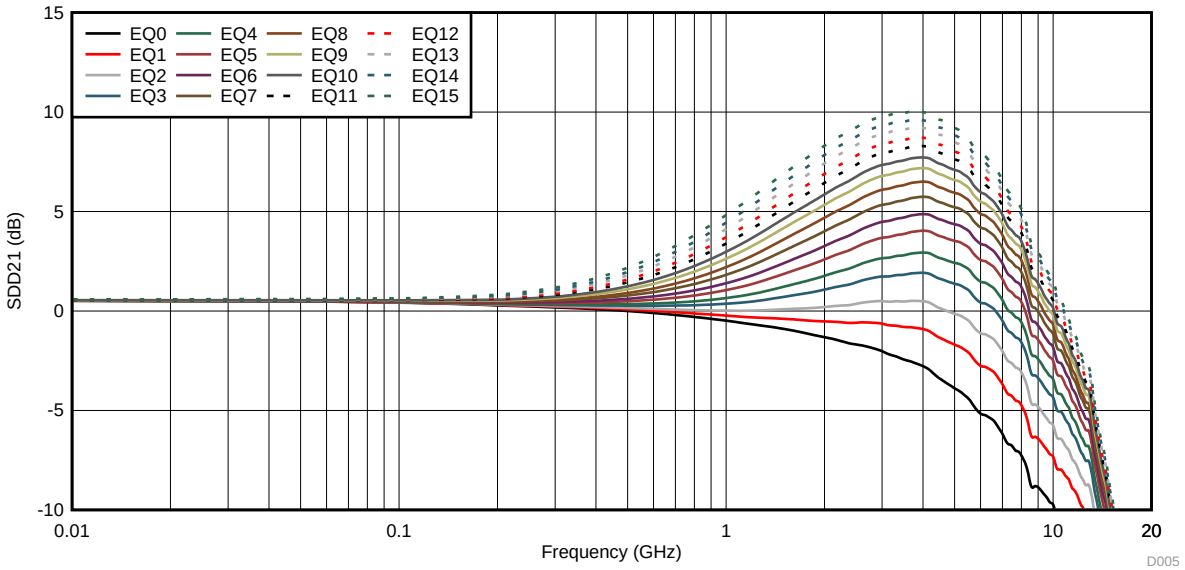


图 19. Upstream-to-Downstream EQ Settings Curves

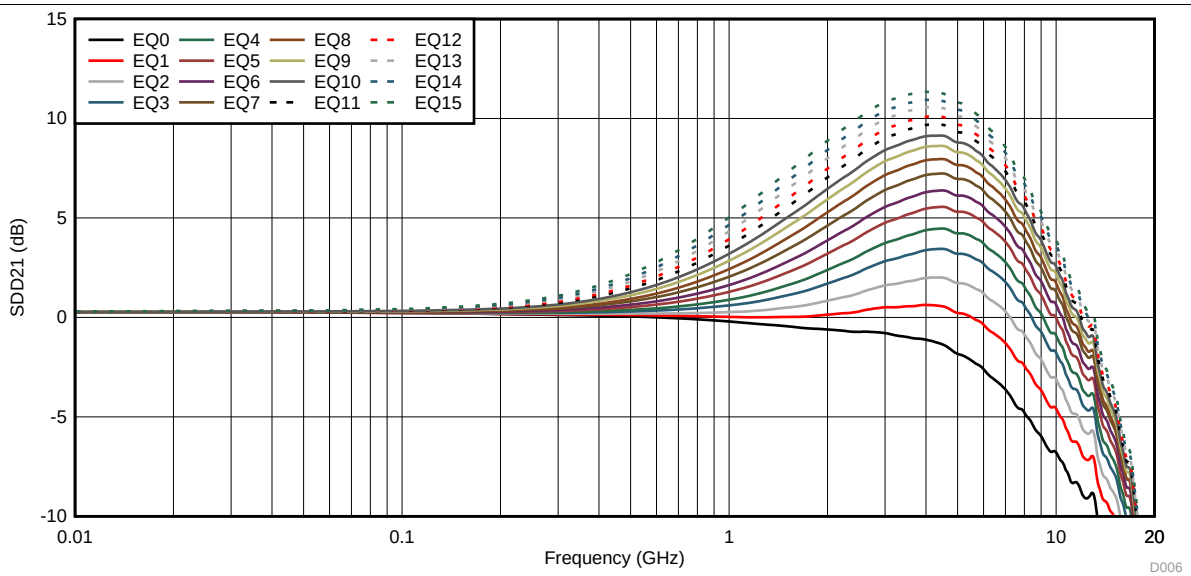


图 20. Downstream-to-Upstream EQ Settings Curves

7 Detailed Description

7.1 Overview

The TUSB544 is a USB Type-C Alt Mode redriver switch supporting data rates up to 8.1 Gbps. This device implements 5th generation USB redriver technology. The device is utilized for configurations C, D, E, and F from the VESA DisplayPort Alt Mode on USB Type-C Standard. It can also be configured to support custom USB Type-C alternate modes.

The TUSB544 provides several levels of receive equalization to compensate for cable and board trace loss due to inter-symbol interference (ISI) when USB 3.1 Gen 1 or DisplayPort (or other Alt modes) signals travel across a PCB or cable. This device requires a 3.3V power supply. It comes for both commercial temperature range and industrial temperature range operation.

For host (source) or device (sink) applications the TUSB544 enables the system to pass both transmitter compliance and receiver jitter tolerance tests for USB 3.1 Gen 1 and DisplayPort version 1.4 HBR3. The re-driver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. Equalization control for upstream and downstream facing ports can be set using UEQ[1:0], and DEQ[1:0] pins respectively or through the I^2C interface.

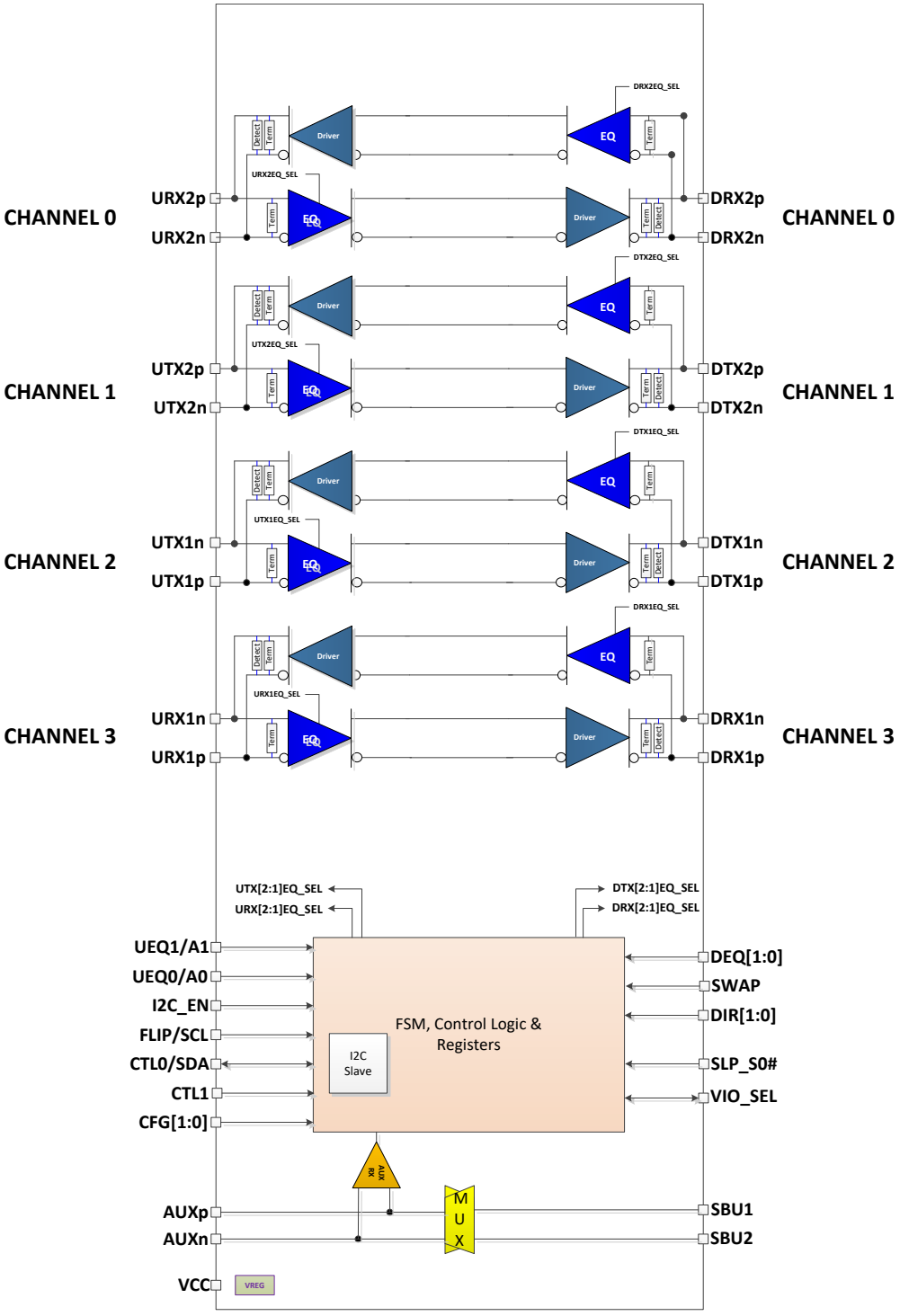
Moreover, the CFG[1:0] or the equivalent I^2C registers provide the ability to control the EQ DC gain and the voltage linearity range for all the channels (Refer to 表 8). This flexible control makes it easy to set up the device to pass various standard compliance requirements.

The TUSB544 advanced state machine makes it transparent to hosts and devices. After power up, the TUSB544. periodically performs receiver detection on the TX pairs. If it detects a USB 3.1 Gen 1 receiver, the RX termination is enabled, and the TUSB544 is ready to re-drive.

The TUSB544 provides extremely flexible data path signal direction control using the CTL[1:0], FLIP, DIR[1:0], and SWAP pins or through the I^2C interface. Refer to 表 4 for detailed information on the input to output signal pin mapping.

The device ultra-low-power architecture operates at a 3.3 V power supply and achieves enhanced performance. The automatic LFPS De-Emphasis control further enables the system to be USB 3.1 compliant.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 USB 3.1

The TUSB544 supports USB 3.1 data rates up to 5 Gbps. The TUSB544 supports all the USB defined power states (U0, U1, U2, and U3). Because the TUSB544 is a linear redriver, it can't decode USB3.1 physical layer traffic. The TUSB544 monitors the actual physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB3.1 interface.

The TUSB544 features an intelligent low frequency periodic signaling (LFPS) detector. The LFPS detector automatically senses the low frequency signals and disables receiver equalization functionality. When not receiving LFPS, the TUSB544 will enable receiver equalization based on the UEQ[1:0] and DEQ[1:0] pins or values programmed into UEQ[3:0]_SEL, and DEQ[3:0]_SEL registers.

7.3.2 DisplayPort

The TUSB544 supports up to 4 DisplayPort lanes at data rates up to 8.1Gbps (HBR3). The TUSB544, when configured in DisplayPort mode, monitors the native AUX traffic as it traverses between DisplayPort source and DisplayPort sink. For the purposes of reducing power, the TUSB544 will manage the number of active DisplayPort lanes based on the content of the AUX transactions. The TUSB544 snoops native AUX writes to DisplayPort sink's DPCD registers 00101h (LANE_COUNT_SET) and 00600h (SET_POWER_STATE). TUSB544 will disable/enable lanes based on value written to LANE_COUNT_SET. The TUSB544 will disable all lanes when SET_POWER_STATE is in the D3. Otherwise active lanes will be based on value of LANE_COUNT_SET.

DisplayPort AUX snooping is enabled by default but can be disabled by changing the AUX_SNOOP_DISABLE register. Once AUX snoop is disabled, management of TUSB544's DisplayPort lanes are controlled through various configuration registers.

7.3.3 4-Level Inputs

The TUSB544 has (I2C_EN, UEQ[1:0], DEQ[1:0], CFG[1:0], and A[1:0]) 4-level inputs pins that are used to control the equalization gain, voltage linearity range, and place TUSB544 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There are internal pull-up and a pull-down resisters. These resistors together with the external resistor connection combine to achieve the desired voltage level.

表 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5%to V_{CC}. Option 2: Tie directly to V_{CC}.

注

All four-level inputs are latched on rising edge of internal reset. After T_{cfg_hd}, the internal pull-up and pull-down resistors will be isolated in order to save power.

7.3.4 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss. Two 4-level input pins enable up to 16 possible equalization settings. The upstream path, and the downstream path each have their own two 4-level inputs for equalization settings; UEQ[1:0] and DEQ[1:0] respectively. The TUSB544 also provides the flexibility of adjusting equalization settings through I^2C registers URX[2:1]EQ_SEL, UTX[2:1]EQ_SEL, DRX[2:1]EQ_SEL, and DTX[2:1]EQ_SEL for each individual channel and for each direction (upstream or downstream) .

7.4 Device Functional Modes

7.4.1 Device Configuration in GPIO Mode

The TUSB544 is in GPIO configuration when I2C_EN = “0” or "F". The TUSB544 supports operational combinations with USB and two different Type-C Alternate Modes.. One combination includes USB and Alternate Mode DisplayPort, and the other combination includes USB and custom Alternate Mode. For each operational combination the data path directions can be further set using the DIR[1:0] pins or through I2C to enable the device to operate in the source or sink sides. Please refer to 表 2 for all the configuration of all the operational modes.

When the device is set to operate in a USB and Alternate Mode DisplayPort the following configurations can be further set: USB3.1 only, 2 DisplayPort lanes + USB3.1, or 4 DisplayPort lanes (no USB3.1). The CTL1 pin controls whether DisplayPort is enabled. The combination of CTL1 and CTL0 selects between USB3.1 only, 2 lanes of DisplayPort, or 4-lanes of DisplayPort as detailed in 表 2. The AUXP/N to SBU1/2 mapping is controlled based on 表 3..

When the device is set to operate in a USB and custom Alternate Mode the following configurations can be further set: USB3.1 only, 2 Channels of custom Alternate Mode + USB3.1, or 4 Channels of custom Alternate Mode (no USB3.1). The CTL1 pin controls whether custom Alternate Mode is enabled. The combination of CTL1 and CTL0 selects between USB3.1 only, 2 channels of custom Alternate Mode, or 4 channels of custom Alternate Mode as detailed in 表 2. The AUXP/N to SBU1/2 mapping is controlled based on 表 3.

Further data path direction control can be achieved using the SWAP pin. When set high, the SWAP pin reverses the data path direction on all the channels and swaps the equalization settings of the upstream and downstream facing input ports. This pin may be found useful in active cable application with TUSB544 installed on only one end. The SWAP pin can be set based on which cable end is plugged to the source or sink side receptacle

After power-up (VCC from 0 V to 3.3 V), the TUSB544 will default to USB3.1 mode. The USB PD controller, upon detecting no device attached to Type-C port or USB3.1 operation not required by attached device, must take TUSB544 out of USB3.1 mode by transitioning the CTL0 pin from L to H and back to L.

表 2. GPIO Configuration Control

DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB544 CONFIGURATION	VESA DisplayPort ALT MODE DFP_D Configuration
USB + DisplayPort Alternate Mode (Source Side)						
L	L	L	L	L	Power Down	—
L	L	L	L	H	Power Down	—
L	L	L	H	L	One Port USB 3.1 - No Flip	—
L	L	L	H	H	One Port USB 3.1 – With Flip	—
L	L	H	L	L	4 Lane DP - No Flip	C and E
L	L	H	L	H	4 Lane DP – with Flip	C and E
L	L	H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
L	L	H	H	H	One Port USB 3.1 + 2 Lane DP– with Flip	D and F
USB + DisplayPort Alternate Mode (Sink Side)						
L	H	L	L	L	Power Down	–
L	H	L	L	H	Power Down	–
L	H	L	H	L	One Port USB 3.1 - No Flip	–
L	H	L	H	H	One Port USB 3.1 – With Flip	–
L	H	H	L	L	4 Lane DP - No Flip	C and E
L	H	H	L	H	4 Lane DP – With Flip	C and E
L	H	H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
L	H	H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F

Device Functional Modes (接下页)

表 2. GPIO Configuration Control (接下页)

DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB544 CONFIGURATION	VESA DisplayPort ALT MODE DFP_D Configuration
USB + Custom Alternate Mode (Source Side)						
H	L	L	L	L	Power Down	–
H	L	L	L	H	Power Down	–
H	L	L	H	L	One Port USB 3.1 - No Flip	–
H	L	L	H	H	One Port USB 3.1 – With Flip	–
H	L	H	L	L	4 Channel Custom Alt Mode - No Flip	–
H	L	H	L	H	4 Channel Custom Alt Mode– With Flip	–
H	L	H	H	L	One Port USB 3.1 + 2 Channel Custom Alt Mode- No Flip	–
H	L	H	H	H	One Port USB 3.1 + 2 Channel Custom Alt Mode – With Flip	–
USB + Custom Alternate Mode (Sink Side)						
H	H	L	L	L	Power Down	-
H	H	L	L	H	Power Down	-
H	H	L	H	L	One Port USB 3.1 - No Flip	-
H	H	L	H	H	One Port USB 3.1 – With Flip	-
H	H	H	L	L	4 Channel Custom Alt Mode - No Flip	-
H	H	H	L	H	4 Channel Custom Alt Mode– With Flip	-
H	H	H	H	L	One Port USB 3.1 + 2 Channel Custom Alt Mode- No Flip	-
H	H	H	H	H	One Port USB 3.1 + 2 Channel Custom Alt Mode – With Flip	-

表 3. GPIO AUXP/N to SBU1/2 Mapping

CTL1 pin	FLIP pin	Mapping
H	L	AUXP -> SBU1 AUXN -> SBU2
H	H	AUXP -> SBU2 AUXN -> SBU1
L > 2ms	X	Open

details the TUSB544 mux routing. This table is valid for GPIO mode. This table is also valid for I^2C mode for the case where CH_SWAP_SEL = 4'b0000 or 4'b1111.

表 4. INPUT to OUTPUT Mapping

					SWAP = L			SWAP = H		
					From	From	To	From	From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Rx EQ Control PINS	Input PIN	Output PIN	Rx EQ Control PINS	Input PIN	Output PIN
USB + DisplayPort Alternate Mode (Source Side)										
L	L	L	L	L	NA	NA	NA	NA	NA	NA
L	L	L	L	H	NA	NA	NA	NA	NA	NA
L	L	L	H	L	DEQ[1:0]	DRX1P	URX1P (SSRXP)	DEQ[1:0]	URX1P (SSTXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (SSRXN)	DEQ[1:0]	URX1N (SSTXN)	DRX1N
					UEQ[1:0]	UTX1P (SSTXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (SSRXP)
					UEQ[1:0]	UTX1N (SSTXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (SSRXN)
L	L	L	H	H	DEQ[1:0]	DRX2P	URX2P (SSRXP)	DEQ[1:0]	URX2P (SSTXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (SSRXN)	DEQ[1:0]	URX2N (SSTXN)	DRX2N
					UEQ[1:0]	UTX2P (SSTXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (SSRXP)
					UEQ[1:0]	UTX2N (SSTXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (SSRXN)
L	L	H	L	L	UEQ[1:0]	URX2P (DP0P)	DRX2P	UEQ[1:0]	DRX2P	URX2P (DP0P)
					UEQ[1:0]	URX2N (DP0N)	DRX2N	UEQ[1:0]	DRX2N	URX2N (DP0N)
					UEQ[1:0]	UTX2P (DP1P)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (DP1P)
					UEQ[1:0]	UTX2N (DP1N)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (DP1N)
					UEQ[1:0]	UTX1P (DP2P)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (DP2P)
					UEQ[1:0]	UTX1N (DP2N)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (DP2N)
					UEQ[1:0]	URX1P (DP3P)	DRX1P	UEQ[1:0]	DRX1P	URX1P (DP3P)
					UEQ[1:0]	URX1N (DP3N)	DRX1N	UEQ[1:0]	DRX1N	URX1N (DP3N)

表 4. INPUT to OUTPUT Mapping (接下页)

					SWAP = L			SWAP = H		
					From	From	To	From	From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Rx EQ Control PINS	Input PIN	Output PIN	Rx EQ Control PINS	Input PIN	Output PIN
L	L	H	L	H	UEQ[1:0]	URX1P (DP0P)	DRX1P	UEQ[1:0]	DRX1P	URX1P (DP0P)
					UEQ[1:0]	URX1N (DP0N)	DRX1N	UEQ[1:0]	DRX1N	URX1N (DP0N)
					UEQ[1:0]	UTX1P (DP1P)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (DP1P)
					UEQ[1:0]	UTX1N (DP1N)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (DP1N)
					UEQ[1:0]	UTX2P (DP2P)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (DP2P)
					UEQ[1:0]	UTX2N (DP2N)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (DP2N)
					UEQ[1:0]	URX2P (DP3P)	DRX2P	UEQ[1:0]	DRX2P	URX2P (DP3P)
					UEQ[1:0]	URX2N (DP3N)	DRX2N	UEQ[1:0]	DRX2N	URX2N (DP3N)
L	L	H	H	L	DEQ[1:0]	DRX1P	URX1P (SSRXP)	DEQ[1:0]	URX1P (SSTXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (SSRXN)	DEQ[1:0]	URX1N (SSTXN)	DRX1N
					UEQ[1:0]	UTX1P (SSTXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (SSRXP)
					UEQ[1:0]	UTX1N (SSTXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (SSRXN)
					UEQ[1:0]	URX2P (DP0P)	DRX2P	UEQ[1:0]	DRX2P	URX2P (DP0P)
					UEQ[1:0]	URX2N (DP0N)	DRX2N	UEQ[1:0]	DRX2N	URX2N (DP0N)
					UEQ[1:0]	UTX2P (DP1P)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (DP1P)
					UEQ[1:0]	UTX2N (DP1N)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (DP1N)
L	L	H	H	H	DEQ[1:0]	DRX2P	URX2P (SSRXP)	DEQ[1:0]	URX2P (SSTXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (SSRXN)	DEQ[1:0]	URX2N (SSTXN)	DRX2N
					UEQ[1:0]	UTX2P (SSTXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (SSRXP)
					UEQ[1:0]	UTX2N (SSTXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (SSRXN)
					UEQ[1:0]	URX1P (DP0P)	DRX1P	UEQ[1:0]	DRX1P	URX1P (DP0P)
					UEQ[1:0]	URX1N (DP0N)	DRX1N	UEQ[1:0]	DRX1N	URX1N (DP0N)
					UEQ[1:0]	UTX1P (DP1P)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (DP1P)
					UEQ[1:0]	UTX1N (DP1N)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (DP1N)
USB + DisplayPort Alternate Mode (Sink Side)										
L	H	L	L	L	NA	NA	NA	NA	NA	NA
L	H	L	L	H	NA	NA	NA	NA	NA	NA

表 4. INPUT to OUTPUT Mapping (接下页)

					SWAP = L			SWAP = H		
					From	From	To	From	From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Rx EQ Control PINS	Input PIN	Output PIN	Rx EQ Control PINS	Input PIN	Output PIN
L	H	L	H	L	UEQ[1:0]	UTX2P	DTX2P (SSRXP)	UEQ[1:0]	DTX2P (SSTXP)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (SSRXN)	UEQ[1:0]	DTX2N (SSTXN)	UTX2N
					DEQ[1:0]	DRX2P (SSTXP)	URX2P	DEQ[1:0]	URX2P	DRX2P (SSRXP)
					DEQ[1:0]	DRX2N (SSTXN)	URX2N	DEQ[1:0]	URX2N	DRX2N (SSRXN)
L	H	L	H	H	UEQ[1:0]	UTX1P	DTX1P (SSRXP)	UEQ[1:0]	DTX1P (SSTXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (SSRXN)	UEQ[1:0]	DTX1N (SSTXN)	UTX1N
					DEQ[1:0]	DRX1P (SSTXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (SSRXP)
					DEQ[1:0]	DRX1N (SSTXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (SSRXN)
L	H	H	L	L	UEQ[1:0]	URX2P	DRX2P (DP3P)	UEQ[1:0]	DRX2P (DP3P)	URX2P
					UEQ[1:0]	URX2N	DRX2N (DP3N)	UEQ[1:0]	DRX2N (DP3N)	URX2N
					UEQ[1:0]	UTX2P	DTX2P (DP2P)	UEQ[1:0]	DTX2P (DP2P)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (DP2N)	UEQ[1:0]	DTX2N (DP2N)	UTX2N
					UEQ[1:0]	UTX1P	DTX1P (DP1P)	UEQ[1:0]	DTX1P (DP1P)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (DP1N)	UEQ[1:0]	DTX1N (DP1N)	UTX1N
					UEQ[1:0]	URX1P	DRX1P (DP0P)	UEQ[1:0]	DRX1P (DP0P)	URX1P
					UEQ[1:0]	URX1P	DRX1N (DP0P)	UEQ[1:0]	DRX1N (DP0N)	URX1N
L	H	H	L	H	UEQ[1:0]	URX1P	DRX1P (DP3P)	UEQ[1:0]	DRX1P (DP3P)	URX1P
					UEQ[1:0]	URX1N	DRX1N (DP3N)	UEQ[1:0]	DRX1N (DP3N)	URX1N
					UEQ[1:0]	UTX1P	DTX1P (DP2P)	UEQ[1:0]	DTX1P (DP2P)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (DP2N)	UEQ[1:0]	DTX1N (DP2N)	UTX1N
					UEQ[1:0]	UTX2P	DTX2P (DP1P)	UEQ[1:0]	DTX2P (DP1P)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (DP1N)	UEQ[1:0]	DTX2N (DP1N)	UTX2N
					UEQ[1:0]	URX2P	DRX2P (DP0P)	UEQ[1:0]	DRX2P (DP0P)	URX2P
					UEQ[1:0]	URX2N	DRX2N (DP0N)	UEQ[1:0]	DRX2N (DP0N)	URX2N

表 4. INPUT to OUTPUT Mapping (接下页)

					SWAP = L			SWAP = H		
					From	From	To	From	From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Rx EQ Control PINS	Input PIN	Output PIN	Rx EQ Control PINS	Input PIN	Output PIN
L	H	H	H	L	DEQ[1:0]	DRX2P (SSRXP)	URX2P	DEQ[1:0]	URX2P	DRX2P (SSRXP)
					DEQ[1:0]	DRX2N (SSRXN)	URX2N	DEQ[1:0]	URX2N	DRX2N (SSRXN)
					UEQ[1:0]	UTX2P	DTX2P (SSTXP)	UEQ[1:0]	DTX2P (SSTXP)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (SSTXN)	UEQ[1:0]	DTX2N (SSTXN)	UTX2N
					UEQ[1:0]	URX1P	DRX1P (DP0P)	UEQ[1:0]	DRX1P (DP0P)	URX1P
					UEQ[1:0]	URX1N	DRX1N (DP0N)	UEQ[1:0]	DRX1N (DP0N)	URX1N
					UEQ[1:0]	UTX1P	DTX1P (DP1P)	UEQ[1:0]	DTX1P (DP1P)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (DP1N)	UEQ[1:0]	DTX1N (DP1N)	UTX1N
L	H	H	H	H	DEQ[1:0]	DRX1P (SSRXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (SSRXP)
					DEQ[1:0]	DRX1N (SSRXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (SSRXN)
					UEQ[1:0]	UTX1P	DTX1P (SSTXP)	UEQ[1:0]	DTX1P (SSTXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (SSTXN)	UEQ[1:0]	DTX1N (SSTXN)	UTX1N
					UEQ[1:0]	URX2P	DRX2P (DP0P)	UEQ[1:0]	DRX2P (DP0P)	URX2P
					UEQ[1:0]	URX2N	DRX2N (DP0N)	UEQ[1:0]	DRX2N (DP0N)	URX2N
					UEQ[1:0]	UTX2P	DTX2P (DP1P)	UEQ[1:0]	DTX2P (DP1P)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (DP1N)	UEQ[1:0]	DTX2N (DP1N)	UTX2N
USB + Custom Alternate Mode (Source Side)										
H	L	L	L	L	NA	NA	NA	NA	NA	NA
H	L	L	L	H	NA	NA	NA	NA	NA	NA
H	L	L	H	L	DEQ[1:0]	DRX1P	URX1P (SSRXP)	DEQ[1:0]	URX1P (SSTXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (SSRXN)	DEQ[1:0]	URX1N (SSTXN)	DRX1N
					UEQ[1:0]	UTX1P (SSTXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (SSRXP)
					UEQ[1:0]	UTX1N (SSTXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (SSRXN)
H	L	L	H	H	DEQ[1:0]	DRX2P	URX2P (SSRXP)	DEQ[1:0]	URX2P (SSTXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (SSRXN)	DEQ[1:0]	URX2N (SSTXN)	DRX2N
					UEQ[1:0]	UTX2P (SSTXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (SSRXP)
					UEQ[1:0]	UTX2N (SSTXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (SSRXN)

表 4. INPUT to OUTPUT Mapping (接下页)

					SWAP = L			SWAP = H		
					From	From	To	From	From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Rx EQ Control PINS	Input PIN	Output PIN	Rx EQ Control PINS	Input PIN	Output PIN
H	L	H	L	L	DEQ[1:0]	DRX2P	URX2P (LN1RXP)	DEQ[1:0]	URX2P (LN1RXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN1RXN)	DEQ[1:0]	URX2N (LN1RXN)	DRX2N
					UEQ[1:0]	UTX2P (LN1TXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN1TXP)
					UEQ[1:0]	UTX2N (LN1TXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN1TXN)
					UEQ[1:0]	UTX1P (LN0TXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN0TXP)
					UEQ[1:0]	UTX1N (LN0TXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN0TXN)
					DEQ[1:0]	DRX1P	URX1P (LN0RXP)	DEQ[1:0]	URX1P (LN0RXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN0RXN)	DEQ[1:0]	URX1N (LN0RXN)	DRX1N
H	L	H	L	H	DEQ[1:0]	DRX1P	URX1P (LN1RXP)	DEQ[1:0]	URX1P (LN1RXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN1RXN)	DEQ[1:0]	URX1N (LN1RXN)	DRX1N
					UEQ[1:0]	UTX1P (LN1TXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN1TXP)
					UEQ[1:0]	UTX1N (LN1TXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN1TXN)
					UEQ[1:0]	UTX2P (LN0TXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN0TXP)
					UEQ[1:0]	UTX2N (LN0TXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN0TXN)
H	L	H	H	L	DEQ[1:0]	DRX2P	URX2P (LN0RXP)	DEQ[1:0]	URX2P (LN0RXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN0RXN)	DEQ[1:0]	URX2N (LN0RXN)	DRX2N
					DEQ[1:0]	DRX1P	URX1P (SSRXP)	DEQ[1:0]	URX1P (SSTXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (SSRXN)	DEQ[1:0]	URX1N (SSTXN)	DRX1N
					UEQ[1:0]	UTX1P (SSTXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (SSRXP)
					UEQ[1:0]	UTX1N (SSTXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (SSRXN)
					UEQ[1:0]	UTX2P (LN0TXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN0TXP)
					UEQ[1:0]	UTX2N (LN0TXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN0TXN)
					DEQ[1:0]	DRX2P	URX2P (LN0RXP)	DEQ[1:0]	URX2P (LN0RXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN0RXN)	DEQ[1:0]	URX2N (LN0RXN)	DRX2N

表 4. INPUT to OUTPUT Mapping (接下页)

					SWAP = L			SWAP = H		
					From	From	To	From	From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Rx EQ Control PINS	Input PIN	Output PIN	Rx EQ Control PINS	Input PIN	Output PIN
H	L	H	H	H	DEQ[1:0]	DRX2P	URX2P (SSRXP)	DEQ[1:0]	URX2P (SSTXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (SSRXN)	DEQ[1:0]	URX2N (SSTXN)	DRX2N
					UEQ[1:0]	UTX2P (SSTXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (SSRXP)
					UEQ[1:0]	UTX2N (SSTXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (SSRXN)
					UEQ[1:0]	UTX1P (LN0TXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN0TXP)
					UEQ[1:0]	UTX1N (LN0TXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN0TXN)
					DEQ[1:0]	DRX1P	URX1P (LN0RXP)	DEQ[1:0]	URX1P (LN0RXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN0RXN)	DEQ[1:0]	URX1N (LN0RXN)	DRX1N
USB + Custom Alternate Mode (Sink Side)										
H	H	L	L	L	NA	NA	NA	NA	NA	NA
H	H	L	L	H	NA	NA	NA	NA	NA	NA
H	H	L	H	L	UEQ[1:0]	UTX2P	DTX2P (SSRXP)	UEQ[1:0]	DTX2P (SSTXP)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (SSRXN)	UEQ[1:0]	DTX2N (SSTXN)	UTX2N
					DEQ[1:0]	DRX2P (SSTXP)	URX2P	DEQ[1:0]	URX2P	DRX2P (SSRXP)
					DEQ[1:0]	DRX2N (SSTXN)	URX2N	DEQ[1:0]	URX2N	DRX2N (SSRXN)
H	H	L	H	H	UEQ[1:0]	UTX1P	DTX1P (SSRXP)	UEQ[1:0]	DTX1P (SSTXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (SSRXN)	UEQ[1:0]	DTX1N (SSTXN)	UTX1N
					DEQ[1:0]	DRX1P (SSTXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (SSRXP)
					DEQ[1:0]	DRX1N (SSTXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (SSRXN)
H	H	H	L	L	DEQ[1:0]	DRX2P	URX2P (LN1TXP)	DEQ[1:0]	URX2P (LN1TXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN1TXN)	DEQ[1:0]	URX2N (LN1TXN)	DRX2N
					UEQ[1:0]	UTX2P (LN1RXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN1RXP)
					UEQ[1:0]	UTX2N (LN1RXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN1RXN)
					UEQ[1:0]	UTX1P (LN0RXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN0RXP)
					UEQ[1:0]	UTX1N (LN0RXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN0RXN)
					DEQ[1:0]	DRX1P	URX1P (LN0RXP)	DEQ[1:0]	URX1P (LN0RXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN0RXN)	DEQ[1:0]	URX1N (LN0RXN)	DRX1N

表 4. INPUT to OUTPUT Mapping (接下页)

					SWAP = L			SWAP = H		
					From	From	To	From	From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Rx EQ Control PINS	Input PIN	Output PIN	Rx EQ Control PINS	Input PIN	Output PIN
H	H	H	L	H	DEQ[1:0]	DRX2P	URX2P (LN0RXP)	DEQ[1:0]	URX2P (LN0RXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN0RXN)	DEQ[1:0]	URX2N (LN0RXN)	DRX2N
					UEQ[1:0]	UTX2P (LN0RXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN0RXP)
					UEQ[1:0]	UTX2N (LN0RXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN0RXN)
					UEQ[1:0]	UTX1P (LN0RXP)	DTX1P	UEQ[1:0]	DTX1P	UTX1P (LN0RXP)
					UEQ[1:0]	UTX1N (LN0RXN)	DTX1N	UEQ[1:0]	DTX1N	UTX1N (LN0RXN)
					DEQ[1:0]	DRX1P	URX1P (LN0TXP)	DEQ[1:0]	URX1P (LN0TXP)	DRX1P
					DEQ[1:0]	DRX1N	URX1N (LN0TXN)	DEQ[1:0]	URX1N (LN0TXN)	DRX1N
H	H	H	H	L	UEQ[1:0]	UTX2P	DTX2P (SSRXP)	UEQ[1:0]	DTX2P (SSTXP)	UTX2P
					UEQ[1:0]	UTX2N	DTX2N (SSRXN)	UEQ[1:0]	DTX2N (SSTXN)	UTX2N
					DEQ[1:0]	DRX2P (SSTXP)	URX2P	DEQ[1:0]	URX2P	DRX2P (SSRXP)
					DEQ[1:0]	DRX2N (SSTXN)	URX2N	DEQ[1:0]	URX2N	DRX2N (SSRXN)
					UEQ[1:0]	UTX1P	DTX1P (LN0RXP)	UEQ[1:0]	DTX1P (LN0RXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N(LN0RXN)	UEQ[1:0]	DTX1N(LN0RXN)	UTX1N
					DEQ[1:0]	DRX1P (LN0TXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (LN0TXP)
					DEQ[1:0]	DRX1N (LN0TXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (LN0TXN)
H	H	H	H	H	UEQ[1:0]	UTX1P	DTX1P (SSRXP)	UEQ[1:0]	DTX1P (SSSXP)	UTX1P
					UEQ[1:0]	UTX1N	DTX1N (SSRXN)	UEQ[1:0]	DTX1N (SSSXN)	UTX1N
					DEQ[1:0]	DRX1P (SSTXP)	URX1P	DEQ[1:0]	URX1P	DRX1P (SSRXP)
					DEQ[1:0]	DRX1N (SSTXN)	URX1N	DEQ[1:0]	URX1N	DRX1N (SSRXN)
					DEQ[1:0]	DRX2P	URX2P (LN0TXP)	DEQ[1:0]	URX2P (LN0TXP)	DRX2P
					DEQ[1:0]	DRX2N	URX2N (LN0TXN)	DEQ[1:0]	URX2N (LN0TXN)	DRX2N
					UEQ[1:0]	UTX2P (LN0RXP)	DTX2P	UEQ[1:0]	DTX2P	UTX2P (LN0RXP)
					UEQ[1:0]	UTX2N (LN0RXN)	DTX2N	UEQ[1:0]	DTX2N	UTX2N (LN0RXN)

7.4.2 Device Configuration in I²C Mode

The TUSB544 is in I²C mode when I2C_EN is equal to “1”. The same configurations defined in GPIO mode are also available in I²C mode. The TUSB544’s USB3.1, DisplayPort, and custom Alternate Mode configuration is controlled based on 表 5. The AUXP/N to SBU1/2 mapping control is based on 表 5.

表 5. I²C Configuration Control

Registers					TUSB544 Configuration	VESA DisplayPort Alt Mode DFP_D Configuration
DIRSEL1	DIRSEL0	CTLSEL1	CTLSEL0	FLIPSEL		
USB + DisplayPort Alternate Mode (Source Side)						
L	L	L	L	L	Power Down	–
L	L	L	L	H	Power Down	–
L	L	L	H	L	One Port USB 3.1 - No Flip	–
L	L	L	H	H	One Port USB 3.1 – With Flip	–
L	L	H	L	L	4 Lane DP - No Flip	C and E
L	L	H	L	H	4 Lane DP – With Flip	C and E
L	L	H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
L	L	H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F
USB + DisplayPort Alternate Mode (Sink Side)						
L	H	L	L	L	Power Down	–
L	H	L	L	H	Power Down	–
L	H	L	H	L	One Port USB 3.1 - No Flip	–
L	H	L	H	H	One Port USB 3.1 – With Flip	–
L	H	H	L	L	4 Lane DP - No Flip	C and E
L	H	H	L	H	4 Lane DP – With Flip	C and E
L	H	H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
L	H	H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F
USB + Custom Alternate Mode (Source Side)						
H	L	L	L	L	Power Down	–
H	L	L	L	H	Power Down	–
H	L	L	H	L	One Port USB 3.1 - No Flip	–
H	L	L	H	H	One Port USB 3.1 – With Flip	–
H	L	H	L	L	4 Channel Custom Alt Mode - No Flip	–
H	L	H	L	H	4 Channel Custom Alt Mode– With Flip	–
H	L	H	H	L	One Port USB 3.1 + 2 Channel Custom Alt Mode- No Flip	–
H	L	H	H	H	One Port USB 3.1 + 2 Channel Custom Alt Mode – With Flip	–
USB + Custom Alternate Mode (Sink Side)						
H	H	L	L	L	Power Down	–
H	H	L	L	H	Power Down	–
H	H	L	H	L	One Port USB 3.1 - No Flip	–
H	H	L	H	H	One Port USB 3.1 – With Flip	–
H	H	H	L	L	4 Channel Custom Alt Mode - No Flip	–

表 5. I²C Configuration Control (接下页)

Registers					TUSB544 Configuration	VESA DisplayPort Alt Mode DFP_D Configuration
DIRSEL1	DIRSEL0	CTLSEL1	CTLSEL0	FLIPSEL		
H	H	H	L	H	4 Channel Custom Alt Mode– With Flip	–
H	H	H	H	L	One Port USB 3.1 + 2 Channel Custom Alt Mode- No Flip	–
H	H	H	H	H	One Port USB 3.1 + 2 Channel Custom Alt Mode – With Flip	–

表 6. I²C Mode AUXP/N to SBU1/2 Mapping

Registers			
AUX_SBU_OVR	CTLSEL1	FLIPSEL	Mapping
00	H	L	AUXp -> SBU1 AUXn -> SBU2
00	H	H	AUXp -> SBU2 AUXn -> SBU1
00	L	X	Open
01	X	X	AUXp -> SBU1 AUXn -> SBU2
10	X	X	AUXp -> SBU2 AUXn -> SBU1
11	X	X	Open

7.4.3 DisplayPort Mode

The TUSB544 supports up to four DisplayPort lanes at datarates up to 8.1Gbps. TUSB544 can be enabled for DisplayPort through GPIO control or through I²C register control. In GPIO mode, DisplayPort is controlled based on 表 2. When not in GPIO mode, enable of DisplayPort functionality is controlled through I²C registers.

7.4.4 Custom Alternate Mode

The TUSB544 supports up to two lanes (or 4 channels) of custom Alternate Mode at datarates up to 8.1Gbps. TUSB544 can be enabled for custom Alternate Mode through GPIO control or through I²C register control. in GPIO mode, custom Alternate Mode is controlled based on 表 2. When not in GPIO mode, enable of custom Alternate Mode functionality is controlled through I²C registers. In I²C mode, the operation of this mode requires setting AUX_SNOOP_DISABLE register 13h bit 7 to 0.

7.4.5 Linear EQ Configuration

TUSB544 receiver lanes have controls for receiver equalization for upstream and downstream facing ports. The receiver equalization gain value can be controlled either through I²C registers or through GPIOs. 表 7 details the gain value for each available combination when TUSB544 is in GPIO mode. These same options are also available per channel and for upstream and downstream facing ports in I²C mode by updating registers URX[2:1]EQ_SEL, UTX[2:1]EQ_SEL, DRX[2:1]EQ_SEL, and DTX[2:1]EQ_SEL.

表 7. TUSB544 Receiver Equalization GPIO Control

Downstream Facing Ports				Upstream Facing Port			
DEQ1 pin Level	DEQ0 pin Level	EQ GAIN 2.5GHz (dB)	EQ GAIN 4.05GHz (dB)	UEQ1 pin Level	UEQ0 pin Level	EQ GAIN 2.5GHz (dB)	EQ GAIN 4.05GHz (dB)
0	0	-1.0	-1.4	0	0	-2.2	-3.3
0	R	0.1	0.4	0	R	-1.1	-1.5
0	F	1.0	1.7	0	F	-0.2	0.0
0	1	2.1	3.2	0	1	0.9	1.4

表 7. TUSB544 Receiver Equalization GPIO Control (接下页)

Downstream Facing Ports				Upstream Facing Port			
R	0	2.9	4.1	R	0	1.8	2.4
R	R	3.8	5.2	R	R	2.7	3.5
R	F	4.6	6.1	R	F	3.4	4.3
R	1	5.4	6.9	R	1	4.3	5.2
F	0	6.1	7.7	F	0	5.0	6.0
F	R	6.8	8.3	F	R	5.7	6.6
F	F	7.3	8.8	F	F	6.2	7.2
F	1	7.9	9.4	F	1	6.8	7.7
1	0	8.4	9.8	1	0	7.3	8.1
1	R	8.9	10.3	1	R	7.8	8.6
1	F	9.3	10.6	1	F	8.2	9.0
1	1	9.8	11.0	1	1	8.7	9.4

7.4.6 Adjustable VOD Linear Range and DC Gain

The CFG0 and CFG1 pins can be used to adjust the TUSB544 differential output voltage (VOD) swing linear range and receiver equalization DC gain for both downstream and upstream data path directions. 表 8 details the available options.

表 8. VOD Linear Range and DC Gain

Setting #	CFG1 pin Level	CFG0 pin Level	Downstream DC Gain (dB)	Upstream DC Gain (dB)	Downstream VOD Linear Range (mVpp)	Upstream VOD Linear Range (mVpp)
1	0	0	1	0	900	900
2	0	R	0	1	900	900
3	0	F	0	0	900	900
4	0	1	1	1	900	900
5	R	0	0	0	1100	1100
6	R	R	1	0	1100	1100
7	R	F	0	1	1100	1100
8	R	1	2	2	1100	1100
9	F	0	Reserved	Reserved	Reserved	Reserved
10	F	R	Reserved	Reserved	Reserved	Reserved
11	F	F	Reserved	Reserved	Reserved	Reserved
12	F	1	Reserved	Reserved	Reserved	Reserved
13	1	0	Reserved	Reserved	Reserved	Reserved
14	1	R	Reserved	Reserved	Reserved	Reserved
15	1	F	Reserved	Reserved	Reserved	Reserved
16	1	1	Reserved	Reserved	Reserved	Reserved

7.4.7 USB3.1 modes

The TUSB544 monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB3.1 interface. Depending on the state of the USB 3.1 interface, the TUSB544 can be in one of four primary modes of operation when USB 3.1 is enabled (CTL0 = H or CTLSEL0 = 1b1): Disconnect, U2/U3, U1, and U0.

The Disconnect mode is the state in which TUSB544 has not detected far-end termination on both upstream facing port (UFP) or downstream facing port (DFP). The disconnect mode is the lowest power mode of each of the four modes. The TUSB544 will remain in this mode until far-end receiver termination has been detected on both UFP and DFP. The TUSB544 will immediately exit this mode and enter U0 once far-end termination is detected.

Once in U0 mode, the TUSB544 will redrive all traffic received on UFP and DFP. U0 is the highest power mode of all USB3.1 modes. The TUSB544 will remain in U0 mode until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB544 will immediately transition to U1.

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB544's UFP and DFP receiver termination will remain enabled. The UFP and DFP transmitter DC common mode is maintained. The power consumption in U1 will be similar to power consumption of U0.

Next to the disconnect mode, the U2 and U3 mode is next lowest power state. While in this mode, the TUSB544 will periodically perform far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB544 will leave the U2 and U3 mode and transition to the Disconnect mode. It will also monitor for a valid LFPS. Upon detection of a valid LFPS, the TUSB544 will immediately transition to the U0 mode. In U2 and U3 mode, the TUSB544's receiver terminations will remain enabled but the TX DC common mode voltage will not be maintained.

When SLP_S0# is asserted low it will disable Receiver Detect functionality. While SLP_S0# is low and TUSB544 is in U2 and U3, TUSB544 will disable LOS and LFPS detection circuitry and RX termination for both channels will remain enabled. This allows even lower TUSB544 power consumption while in the U2 and U3 mode. Once SLP_S0# is asserted high, the TUSB544 will again start performing far-end receiver detection as well as monitor LFPS so it can know when to exit the U2 and U3 mode.

When SLP_S0# is asserted low and the TUSB544 is in Disconnect mode, the TUSB544 will remain in Disconnect mode and never perform far-end receiver detection. This allows even lower TUSB544 power consumption while in the Disconnect mode. Once SLP_S0# is asserted high, the TUSB544 will again start performing far-end receiver detection so it can know when to exit the Disconnect mode.

7.4.8 Operation Timing – Power Up

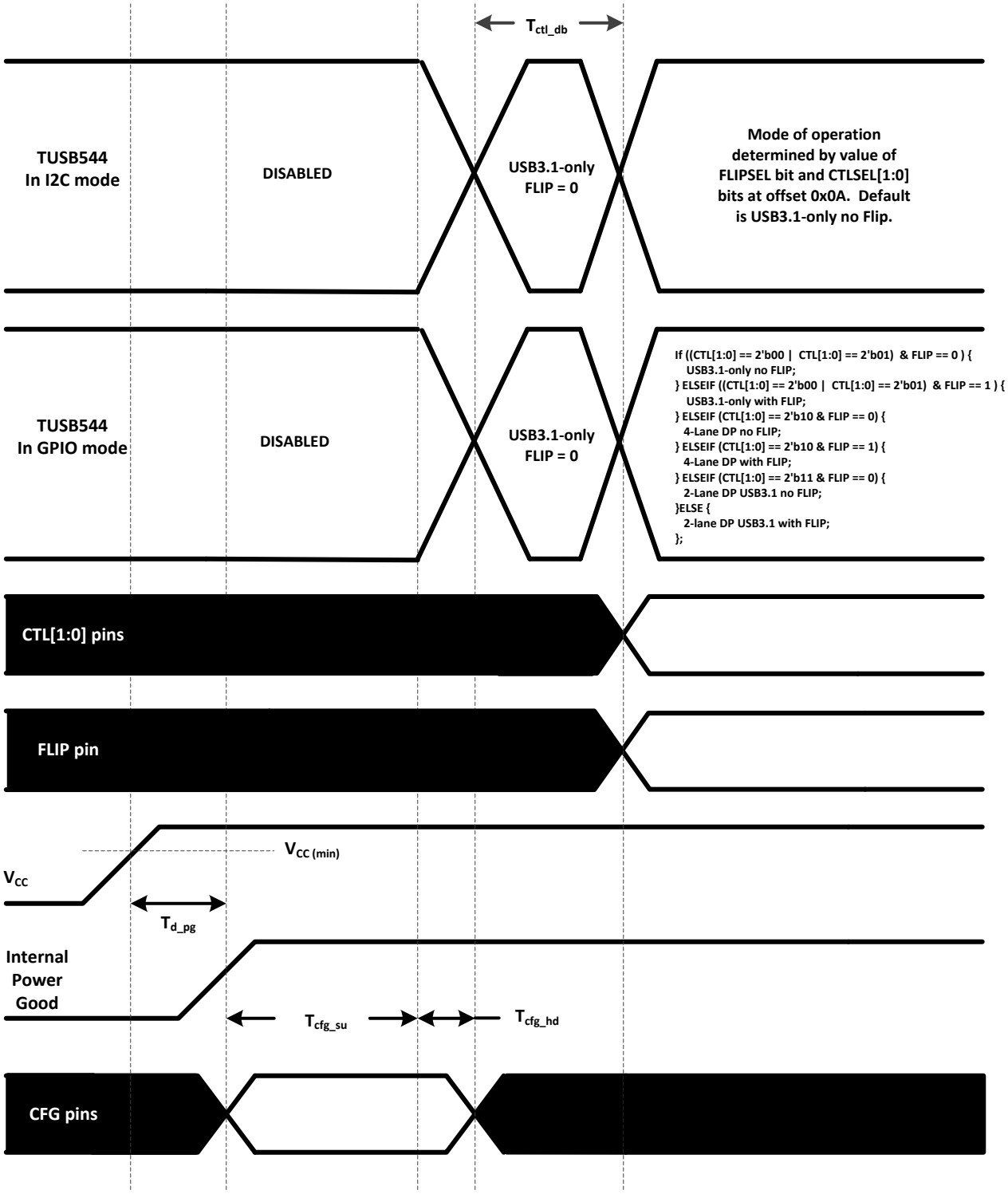


图 21. Power-Up Timing

表 9. Power-Up Timing

PARAMETER		MIN	MAX	UNIT
T_{d_pg}	V_{CC} (min) to Internal Power Good asserted high		500	µs
T_{cfg_su}	CFG(1) pins setup (2)	350		µs
T_{cfg_hd}	CFG(1) pins hold	10		µs
T_{CTL_DB}	CTL[1:0] and FLIP pin debounce		16	ms
T_{VCC_RAMP}	VCC supply ramp requirement		100	ms

(1) Following pins comprise CFG pins: I2C_EN, UEQ[1:0], DEQ[1:0], CFG[1:0], DIR[1:0],VIO_SEL, SLP_S0#, and SWAP.
(2) Recommend CFG pins are stable when VCC is at min.

7.5 Programming

For further programmability, the TUSB544 can be controlled using I^2C. The SCL and SDA terminals are used for I^2C clock and I^2C data respectively.

表 10. I^2C Slave Address

TUSB544 I^2C Slave Address									
UEQ1/A1 Pin Level	UEQ0/A0 Pin Level	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

7.5.1 The Following Procedure Should be Followed to Write to TUSB544 I^2C Registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB544 7-bit address and a zero-value “W/R” bit to indicate a write cycle .
2. The TUSB544 acknowledges the address cycle.
3. The master presents the sub-address (I^2C register within TUSB544) to be written, consisting of one byte of data, MSB-first.
4. The TUSB544 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^2C register.
6. The TUSB544 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB544.
8. The master terminates the write operation by generating a stop condition (P).

7.5.2 The Following Procedure Should be Followed to Read the TUSB544 I²C Registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TUSB544 7-bit address and a one-value “W/R” bit to indicate a read cycle
2. The TUSB544 acknowledges the address cycle.
3. The TUSB544 transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the TUSB544 I2C register occurred prior to the read, then the TUSB544 shall start at the sub-address specified in the write.
4. The TUSB544 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TUSB544 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

7.5.3 The Following Procedure Should be Followed for Setting a Starting Sub-Address for I²C Reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB544 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB544 acknowledges the address cycle.
3. The master presents the sub-address (I²C register within TUSB544) to be written, consisting of one byte of data, MSB-first.
4. The TUSB544 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

注

If no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I²C master terminates the read operation. If a I²C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

7.6 Register Maps

7.6.1 TUSB544 Registers

Table 11 lists the memory-mapped registers for the TUSB544. All register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified.

Table 11. TUSB544 Registers

Offset	Acronym	Register Name	Section
Ah	GENERAL_4	General Registers 4	Go
Bh	GENERAL_5	General Register 5	Go
Ch	GENERAL_6	General Register 6	Go
10h	DISPLAYPORT_1	DisplayPort Control/Status Registers 1	Go
11h	DISPLAYPORT_2	DisplayPort Control/Status Registers 2	Go
12h	DISPLAYPORT__3	DisplayPort Control/Status Registers 3	Go
13h	DISPLAYPORT_4	DisplayPort Control/Status Registers 4	Go
1Bh	DISPLAYPORT_5	DisplayPort Control/Status Registers 5	Go
20h	USB3.1_1	USB3.1 Control/Status Registers 1	Go
21h	USB3.1_2	USB3.1 Control/Status Registers 2	Go
22h	USB3.1_3	USB3.1 Control/Status Registers 3	Go
23h	USB3.1_4	USB3.1 Control/Status Registers 4	Go

Complex bit access types are encoded to fit into small table cells. Table 12 shows the codes that are used for access types in this section.

Table 12. TUSB544 Access Type Codes

Access Type	Code	Description
Read Type	R	The field can be read by software
	H	The field can be read by software but hardware may autonomously update the field.
Write Type	W	The field can be written by software.
	1S	The field can only be set by a write of one. Writes of zero to the field have no effect.
	1C	The field can only be cleared by a write of one. Writes of zero to the field have no effect.
	1SH	The field can only be set by a write of one but hardware will later autonomously clear the field. Writes of zero to the field have no effect.
Reset or default value	-n	Value after reset or the default value

7.6.1.1 GENERAL_4 Register (Offset = Ah) [reset = 1h]

GENERAL_4 is shown in Figure 22 and described in Table 13.

Return to Summary Table.

Figure 22. GENERAL_4 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	SWAP_SEL	EQ_OVERIDE	HPDIN_OVERRIDE	FLIPSEL	CTLSEL[1:0]	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	

Table 13. GENERAL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	SWAP_SEL	R/W	0h	Setting of this field performs global direction swap on all the channels 0 – Channel directions and EQ settings are in normal mode (Default) 1 – Reverse all channel directions and EQ settings for the input ports
4	EQ_OVERIDE	R/W	0h	Setting of this field will allow software to use EQ settings from registers instead of value sample from pins. 0 – EQ settings based on sampled state of the EQ pins. 1 – EQ settings based on programmed value of each of the EQ registers
3	HPDIN_OVERRIDE	R/W	0h	0 – HPD IN based on state of HPD_IN pin (Default) 1 – HPD_IN high.
2	FLIPSEL	R/W	0h	FLIPSEL. Refer to 表 5 and 表 6 for this field functionality.
1-0	CTLSEL[1:0]	R/W	1h	00 – Disabled. All RX and TX for USB3 and DisplayPort are disabled. 01 – USB3.1 only enabled. (Default) 10 – Four DisplayPort lanes enabled. 11 – Two DisplayPort lanes and one USB3.1

7.6.1.2 GENERAL_5 Register (Offset = Bh) [reset = 0h]

GENERAL_5 is shown in Figure 23 and described in Table 14.

Return to Summary Table.

Figure 23. GENERAL_5 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED		CH_SWAP_SEL			
R-0h		R-0h		R/W-0h			

Table 14. GENERAL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-0	CH_SWAP_SEL	R/W	0h	Setting of this field swaps direction (TX to RX and RX to TX) and EQ settings of individual channels. Channels are numbered 0 to 3 from top to bottom (see block diagram on Figure 8.1). 0 – Channel direction and EQ setting are in normal mode (Default) 1 – Reverse channel direction and EQ setting for the input port. For example, setting 0x0B[3:0] to 4b1100 swaps directions and EQ settings only on channels 2 and 3

7.6.1.3 GENERAL_6 Register (Offset = Ch) [reset = 0h]

GENERAL_6 is shown in Figure 24 and described in Table 15.

Return to Summary Table.

Figure 24. GENERAL_6 Register

7	6	5	4	3	2	1	0
RESERVED	VOD_DCGAIN_OVERRIDE	VOD_DCGAIN_SEL				DIR_SEL[1:0]	
R-0h	R/W-0h	R/W-0h				R/W-0h	

Table 15. GENERAL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	VOD_DCGAIN_OVERRIDE	R/W	0h	Setting of this field will allow software to use VOD linearity range and DC gain settings from registers instead of value sampled from pins. 0 – VOD linearity range and DC gain settings based on sampled state of CFG[2:1] pins. 1 – EQ settings based on programmed value of each of the VOD linearity range and DC gain registers
5-2	VOD_DCGAIN_SEL	R/W	0h	Field selects VOD linearity range and DC gain for all the channels and in all directions. When VOD_DCGAIN_OVERRIDE = 1'b0, this field reflects the sampled state of CFG[1:0] pins. When VOD_DCGAIN_OVERRIDE = 1'b1, software can change the VOD linearity range and DC gain for all the channels and in all directions based on value written to this field. Refer to Table 8 8. Each CFG is a 2-bit value. The register-to-CFG1/0 mapping is: [5:2] = {CFG1[1:0], CFG0[1:0]} where CFGx[1:0] mapping is: 00 = 0 01 = R 10 = F 11 = 1
1-0	DIR_SEL[1:0]	R/W	0h	DIR_SEL[1:0]. Sets operation mode 00 – USB + DP Alt Mode (source) (Default) 01 – USB + DP Alt Mode (sink) 10 – USB + Custom Alt Mode (source) 11 – USB + Custom Alt Mode (sink)

7.6.1.4 DISPLAYPORT_1 Register (Offset = 10h) [reset = 0h]

DISPLAYPORT is shown in Figure 25 and described in Table 16.

Return to Summary Table.

Figure 25. DISPLAYPORT Register

7	6	5	4	3	2	1	0
UTX2EQ_SEL				URX2EQ_SEL			
R/W-0h				R/W-0h			

Table 16. DISPLAYPORT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	UTX2EQ_SEL	RW	0h	Field selects between 0 to 9.4 dB of EQ for UTX2P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of UEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for UTX2P/N pins based on value written to this field.
3-0	URX2EQ_SEL	RW	0h	Field selects between 0 to 9.4 dB of EQ for URX2P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of UEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for URX2P/N pins based on value written to this field.

7.6.1.5 DISPLAYPORT_2 Register (Offset = 11h) [reset = 0h]

DISPLAYPORT_2 is shown in Figure 26 and described in Table 17.

Return to Summary Table.

Figure 26. DISPLAYPORT_2 Register

7	6	5	4	3	2	1	0
UTX1EQ_SEL				URX1EQ_SEL			
R/W-0h				R/W-0h			

Table 17. DISPLAYPORT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	UTX1EQ_SEL	R/W	0h	Field selects between 0 to 9.4 dB of EQ for UTX1P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of UEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for UTX1P/N pins based on value written to this field.
3-0	URX1EQ_SEL	R/W	0h	Field selects between 0 to 9.4 dB of EQ for URX1P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of UEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for URX1P/N pins based on value written to this field.

7.6.1.6 DISPLAYPORT_3 Register (Offset = 12h) [reset = 0h]

DISPLAYPORT__3 is shown in Figure 27 and described in Table 18.

Return to Summary Table.

Figure 27. DISPLAYPORT_3 Register

7	6	5	4	3	2	1	0
RESERVED	SET_POWER_STATE		LANE_COUNT_SET				
R-0h	RH-0h		RH-0h				

Table 18. DISPLAYPORT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-5	SET_POWER_STATE	RH	0h	This field represents the snooped value of the AUX write to DPCD address 0x00600. When AUX_SNOOP_DISABLE = 1'b0, the TUSB544 will enable/disable DP lanes based on the snooped value. When AUX_SNOOP_DISABLE = 1'b1, then DP lane enable/disable are determined by state of DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 2'b00 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0.
4-0	LANE_COUNT_SET	RH	0h	This field represents the snooped value of AUX write to DPCD address 0x00101 register. When AUX_SNOOP_DISABLE = 1'b0, TUSB544 will enable DP lanes specified by the snoop value. Unused DP lanes will be disabled to save power. When AUX_SNOOP_DISABLE = 1'b1, then DP lanes enable/disable are determined by DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0x0 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0.

7.6.1.7 DISPLAYPORT_4 Register (Offset = 13h) [reset = 0h]

DISPLAYPORT_4 is shown in Figure 28 and described in Table 19.

Return to Summary Table.

Figure 28. DISPLAYPORT_4 Register

7	6	5	4	3	2	1	0
AUX_SNOOP_DISABLE	RESERVED	AUX_SBU_OVR		DP3_DISABLE	DP2_DISABLE	DP1_DISABLE	DP0_DISABLE
R/W-0h	R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19. DISPLAYPORT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0h	0 – AUX snoop enabled. (Default) 1 – AUX snoop disabled.
6	RESERVED	R	0h	Reserved
5-4	AUX_SBU_OVR	R/W	0h	This field overrides the AUXP/N to SBU1/2 connect and disconnect based on CTL1 and FLIP. Changing this field to 1’b1 will allow traffic to pass through AUX to SBU regardless of the state of CTLSEL1 and FLIPSEL register. 00 – AUX to SBU connect/disconnect determined by CTLSEL1 and FLIPSEL (Default) 01 – AUXP -> SBU1 and AUXN -> SBU2 connection always enabled. 10 – AUXP -> SBU2 and AUXN -> SBU1 connection always enabled. 1 1 = AUX to SBU open.
3	DP3_DISABLE	R/W	0h	When AUX_SNOOP_DISABLE = 1b1, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 1b0, changes to this field will have no effect on lane 3 functionality. 0 – DP Lane 3 Enabled (default) 1 – DP Lane 3 Disabled.
2	DP2_DISABLE	R/W	0h	When AUX_SNOOP_DISABLE = 1 'b1, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 1b0, changes to this field will have no effect on lane 2 functionality. 0 – DP Lane 2 Enabled (default) 1 – DP Lane 2 Disabled.
1	DP1_DISABLE	R/W	0h	When AUX_SNOOP_DISABLE = 1’b1, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 1’b0, changes to this field will have no effect on lane 1 functionality. 0 – DP Lane 1 Enabled (default) 1 – DP Lane 1 Disabled.
0	DP0_DISABLE	R/W	0h	When AUX_SNOOP_DISABLE = 1’b1, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 1’b0, changes to this field will have no effect on lane 0 functionality. 0 – DP Lane 0 Enabled (default) 1 – DP Lane 0 Disabled.

7.6.1.8 DISPLAYPORT_5 Register (Offset = 1Bh) [reset = 0h]

DISPLAYPORT_5 is shown in Figure 29 and described in Table 20.

Return to Summary Table.

Figure 29. DISPLAYPORT_5 Register

7	6	5	4	3	2	1	0
I2C_RST	DPCD_RST	RESERVED					
R/WSH-0h	R/WSH-0h	R-00h					

Table 20. DISPLAYPORT_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C_RST	R/WSH	0h	Resets I2C registers to default values. This field is self- clearing.
6	DPCD_RST	R/WSH	0h	Resets DPCD registers to default values. This field is self- clearing.
5:0	Reserved	R	00h	Reserved

7.6.1.9 USB3.1_1 Register (Offset = 20h) [reset = 0h]

USB3.1 is shown in Figure 30 and described in Table 21.

Return to Summary Table.

Figure 30. USB3.1 Register

7	6	5	4	3	2	1	0
DTX2EQ_SEL				DRX2EQ_SEL			
R/W-0h				R/W-0h			

Table 21. USB3.1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DTX2EQ_SEL	R/W	0h	Field selects between 0 to 11 dB of EQ for DTX2P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DTX2P/N pins based on value written to this field.
3-0	DRX2EQ_SEL	R/W	0h	Field selects between 0 to 11 dB of EQ for DRX2P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DRX2P/N pins based on value written to this field.

7.6.1.10 USB3.1_2 Register (Offset = 21h) [reset = 0h]

USB3.1_2 is shown in Figure 31 and described in Table 22.

Return to Summary Table.

Figure 31. USB3.1_2 Register

7	6	5	4	3	2	1	0
DTX1EQ_SEL				DRX1EQ_SEL			
R/W-0h				R/W-0h			

Table 22. USB3.1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DTX1EQ_SEL	R/W	0h	Field selects between 0 to 11 dB of EQ for DTX1P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DTX1P/N pins based on value written to this field.
3-0	DRX1EQ_SEL	R/W	0h	Field selects between 0 to 11 dB of EQ for DRX1P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DRX1P/N pins based on value written to this field.

7.6.1.11 USB3.1_3 Register (Offset = 22h) [reset = 0h]

USB3.1_3 is shown in Figure 32 and described in Table 23.

Return to Summary Table.

Figure 32. USB3.1_3 Register

7	6	5	4	3	2	1	0
CM_ACTIVE	LFPS_EQ	U2U3_LFPS_DEBOUNCE	DISABLE_U2U3_RXDET	DFP_RXDET_INTERVAL		USB3_COMPLIANCE_CTRL	
RH-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h		R/W-0h	

Table 23. USB3.1_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CM_ACTIVE	RH	0h	0 - device not in USB 3.1 compliance mode. (Default) 1 - device in USB 3.1 compliance mode
6	LFPS_EQ	R/W	0h	Controls whether settings of EQ based on URX[2:1]EQ_SEL, UTX[2:1]EQ_SEL, DRX[2:1]EQ_SEL, and DTX[2:1]EQ_SEL applies to received LFPS signal. 0 - EQ set to zero when receiving LFPS (default) 1 - EQ set by the related registers when receiving LFPS.
5	U2U3_LFPS_DEBOUNCE	R/W	0h	0 - No debounce of LFPS before U2/U3 exit. (Default) 1 - 200us debounce of LFPS before U2/U3 exit.
4	DISABLE_U2U3_RXDET	R/W	0h	0 - Rx.Detect in U2/U3 enabled. (Default) 1 - Rx.Detect in U2/U3 disabled.
3-2	DFP_RXDET_INTERVAL	R/W	1h	This field controls the Rx.Detect interval for the Downstream facing port (TX1P/N and TX2P/N). 00 - 8 ms 01 - 12 ms (default) 10 - Reserved 11 - Reserved
1-0	USB3_COMPLIANCE_CTRL	R/W	0h	00 - FSM determined compliance mode. (Default) 01 - Compliance Mode enabled in DFP direction (UTX1/UTX2 DTX1/DTX2) 10 - Compliance Mode enabled in UFP direction (DRX1/DRX2 URX1/URX2) 11 - Compliance Mode Disabled.

7.6.1.12 USB3.1_4 Register (Offset = 23h) [reset = 23h]

USB3.1_4 is shown in Figure 33 and described in Table 24.

Return to Summary Table.

Figure 33. USB3.1_4 Register

7	6	5	4	3	2	1	0
RESERVED		CFG_LOS_HYST			CFG_LOS_VTH		
R-0h		R/W-4h			R/W-3h		

Table 24. USB3.1_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	CFG_LOS_HYST	R/W	4h	Controls LOS hysteresis defined as 20 log (LOS de-assert threshold/LOS assert threshold). 000 - 0.15 dB 001 - 0.85 dB 010 - 1.45 dB 011 - 2.00 dB 100 - 2.70 dB (default) 101 - 3.00 dB 110 - 3.40 dB 111 - 3.80 dB
2-0	CFG_LOS_VTH	R/W	3h	Controls LOS assert threshold voltage 000 - 67 mV 001 - 72 mV 010 - 79 mV 011 - 85 mV (default) 100 - 91 mV 101 - 97 mV 110 - 105 mV 111 - 112 mV

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TUSB544 is a linear redriver designed specifically to compensate for intersymbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cables. Because the TUSB544 has four independent inputs, it can be optimized to correct ISI on all those seven inputs through 16 different equalization choices. Placing the TUSB544 between a USB3.1 Host/DisplayPort 1.4 GPU and a USB3.1 Type-C receptacle can correct signal integrity issues resulting in a more robust system.

8.2 Typical Application

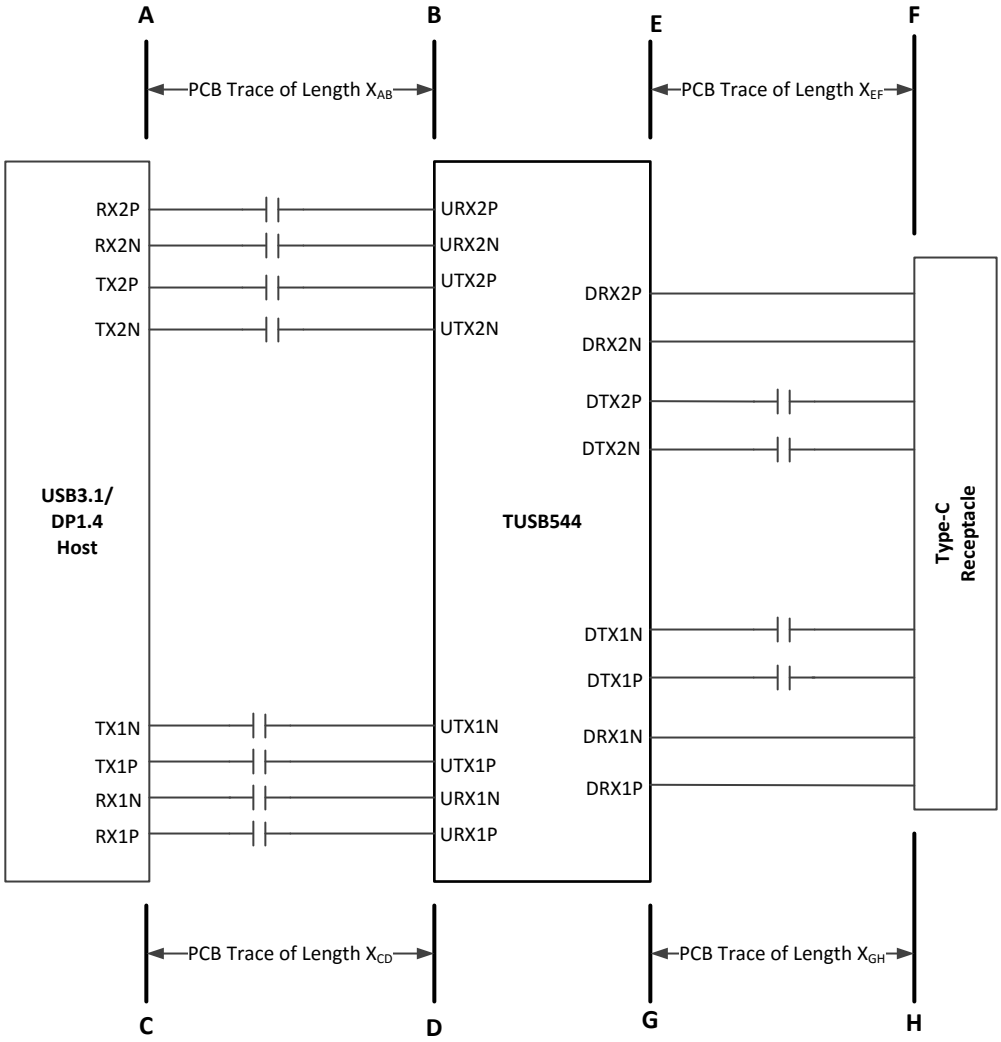


图 34. TUSB544 in a Host Application

Typical Application (接下页)

8.2.1 Design Requirements

For this design example, use the parameters shown in 表 25.

表 25. Design Parameters

PARAMETER	VALUE
A to B PCB trace length, X_{AB}	12 inches
C to D PCB trace length, X_{CD}	12 inches
E to F PCB trace length, X_{EF}	2 inches
G to H PCB trace length, X_{GH}	2 inches
PCB trace width	4 mils
AC-coupling capacitor (75 nF to 265 nF)	100 nF
VCC supply (3 V to 3.6 V)	3.3 V
I^2C Mode or GPIO Mode	I^2C Mode. (I2C_EN pin != "0")
1.8V or 3.3V I^2C Interface	3.3V I^2C. Pull-up the I2C_EN pin to 3.3V with a 1K ohm resistor.

8.2.2 Detailed Design Procedure

A typical usage of the TUSB544 device is shown in 图 35. The device can be controlled either through its GPIO pins or through its I^2C interface. In the example shown below, a Type-C PD controller is used to configure the device through the I^2C interface. In I^2C mode, the equalization settings for each receiver can be independently controlled through I^2C registers. For this reason, all of the equalization pins (UEQ[1:0] and DEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB544 7-bit I^2C slave address will be 12h because both UEQ1/A1 and UEQ0/A0 will be at pin level "F". If a different I^2C slave address is desired, UEQ1/A1 and UEQ0/A0 pins should be set to a level which produces the desired I^2C slave address.

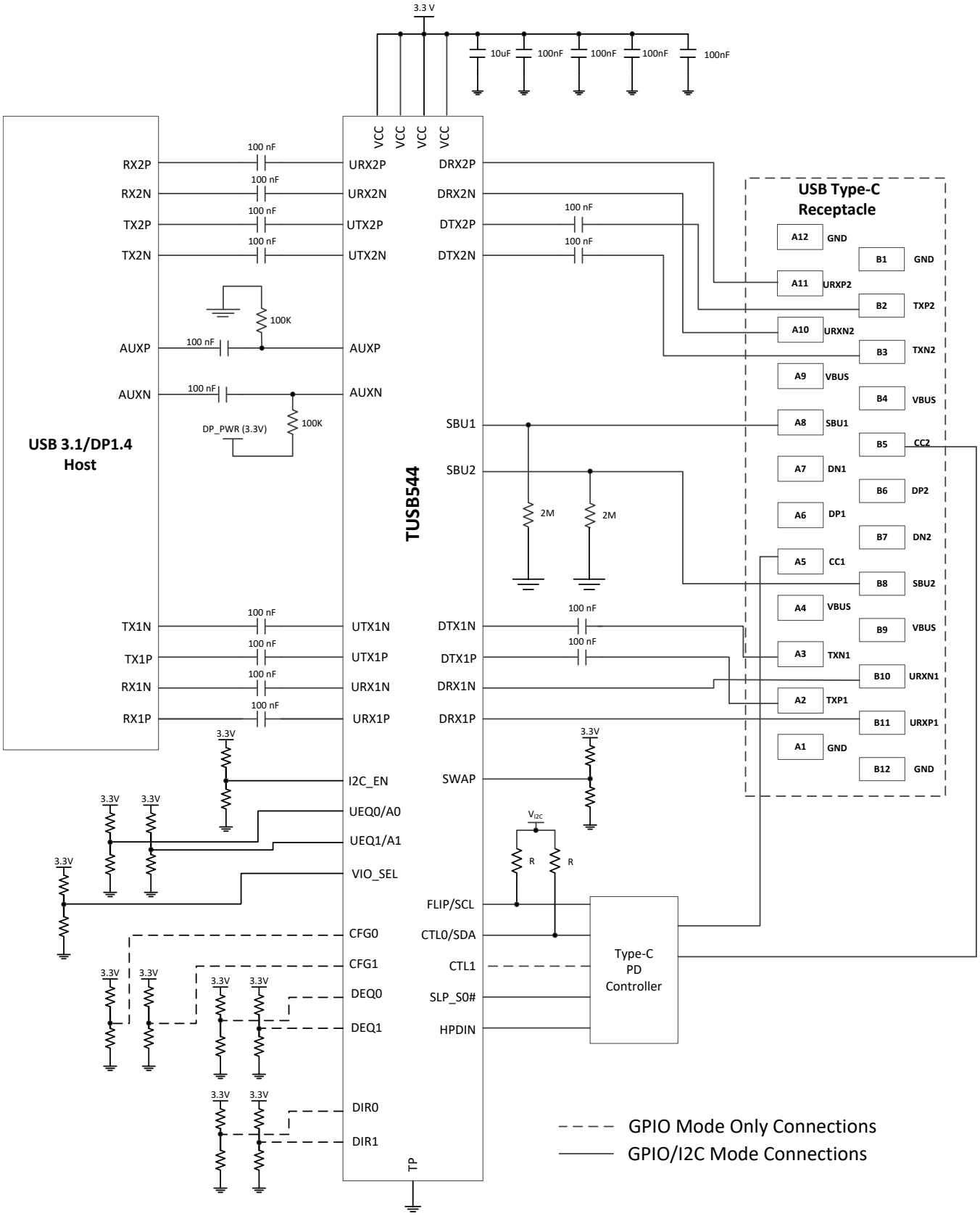


图 35. Typical Application Circuit

8.2.3 Application Curve

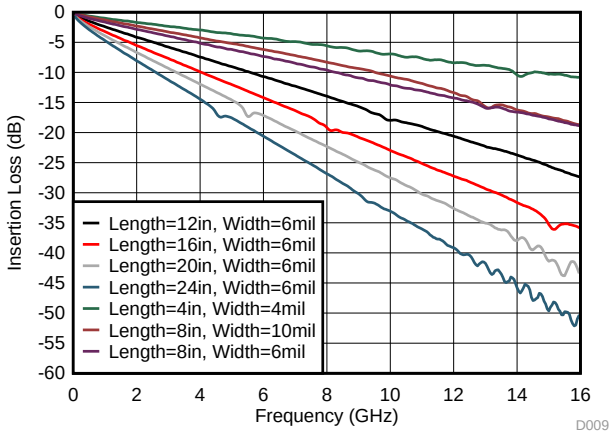


图 36. Insertion Loss of FR4 PCB Traces

8.3 System Examples

8.3.1 USB 3.1 only (USB/DP Alternate Mode)

The TUSB544 will be in USB3.1 only when the CTL1 pin is low and CTL0 pin is high.

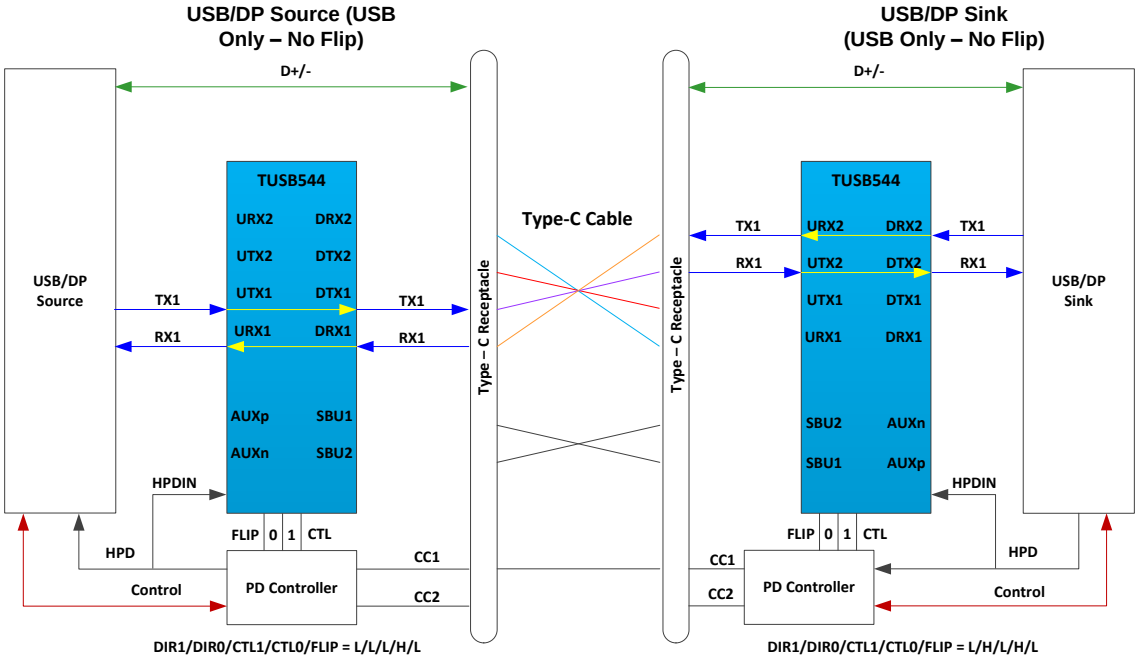


图 37. USB3.1 Only – No Flip

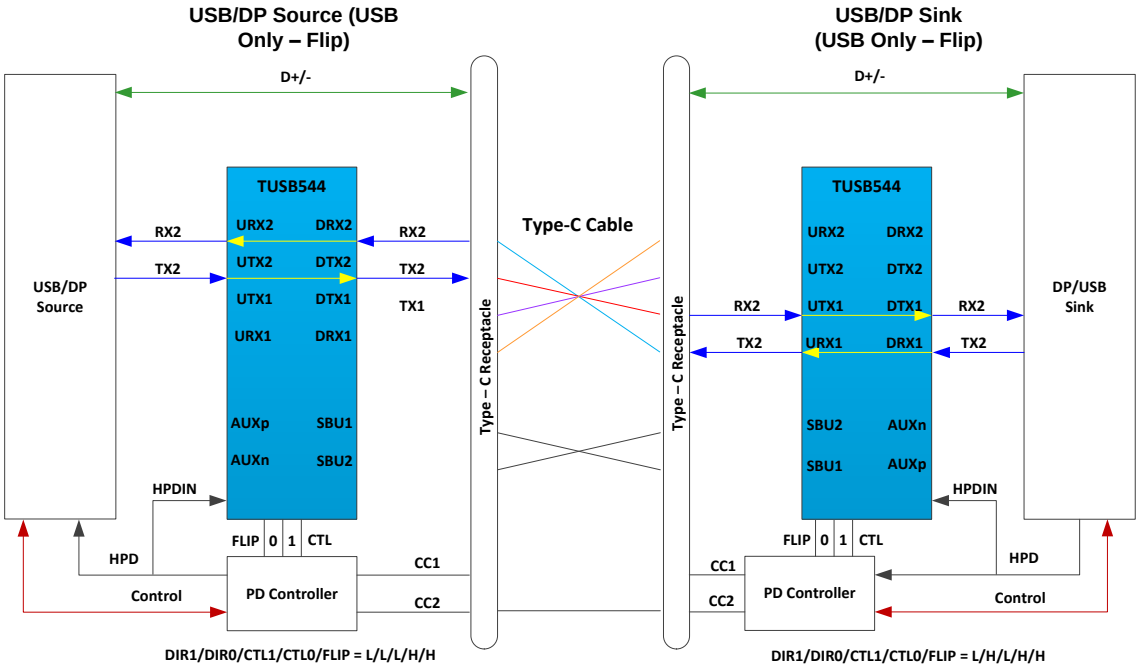


图 38. USB3.1 Only – With Flip

System Examples（接下页）

8.3.2 USB3.1 and 2 lanes of DisplayPort

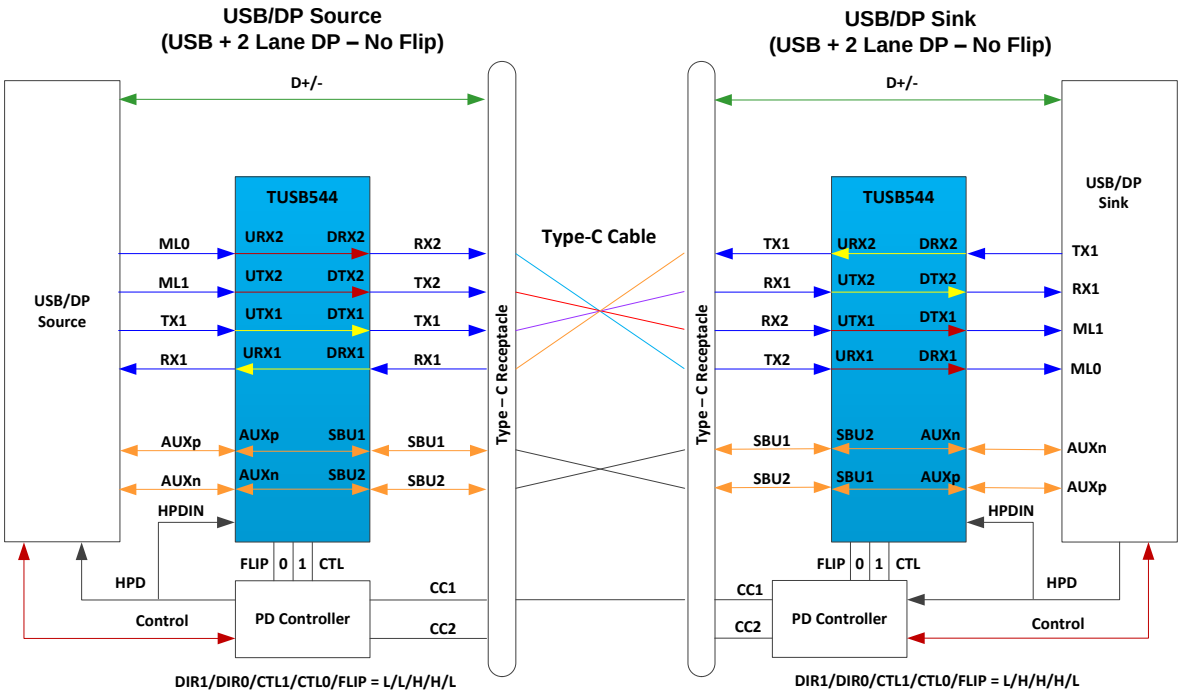


图 39. USB3.1 + 2 Lane DP – No Flip

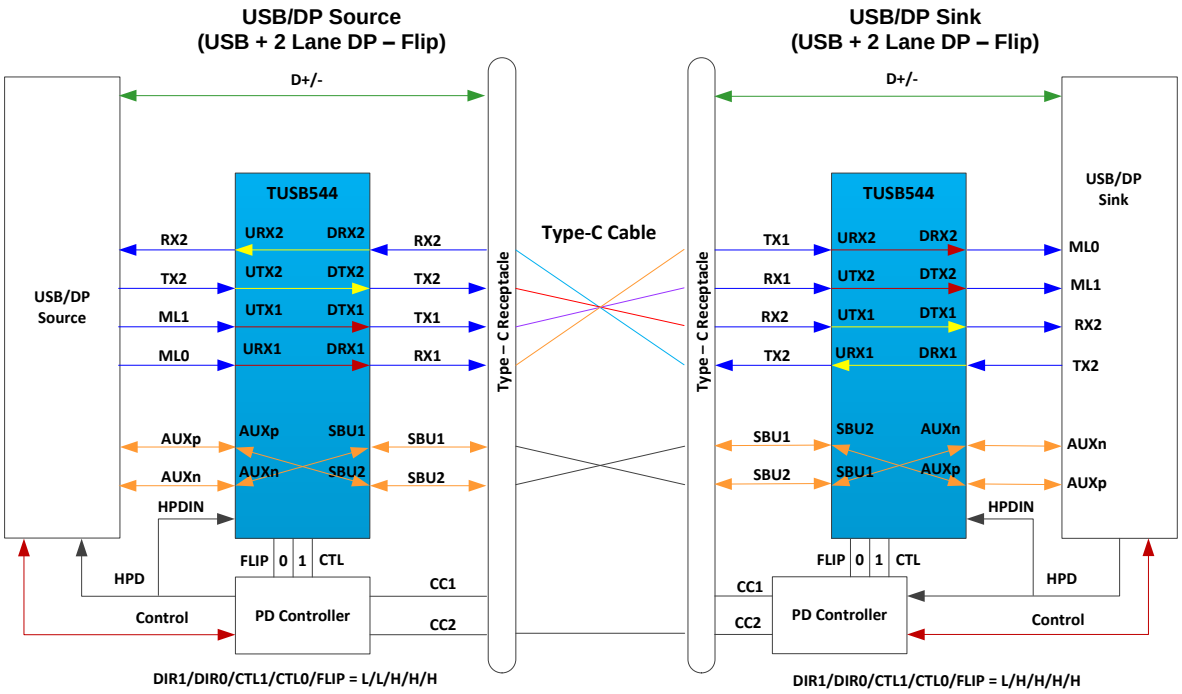


图 40. USB 3.1 + 2 Lane DP – Flip

System Examples（接下页）

8.3.3 DisplayPort Only

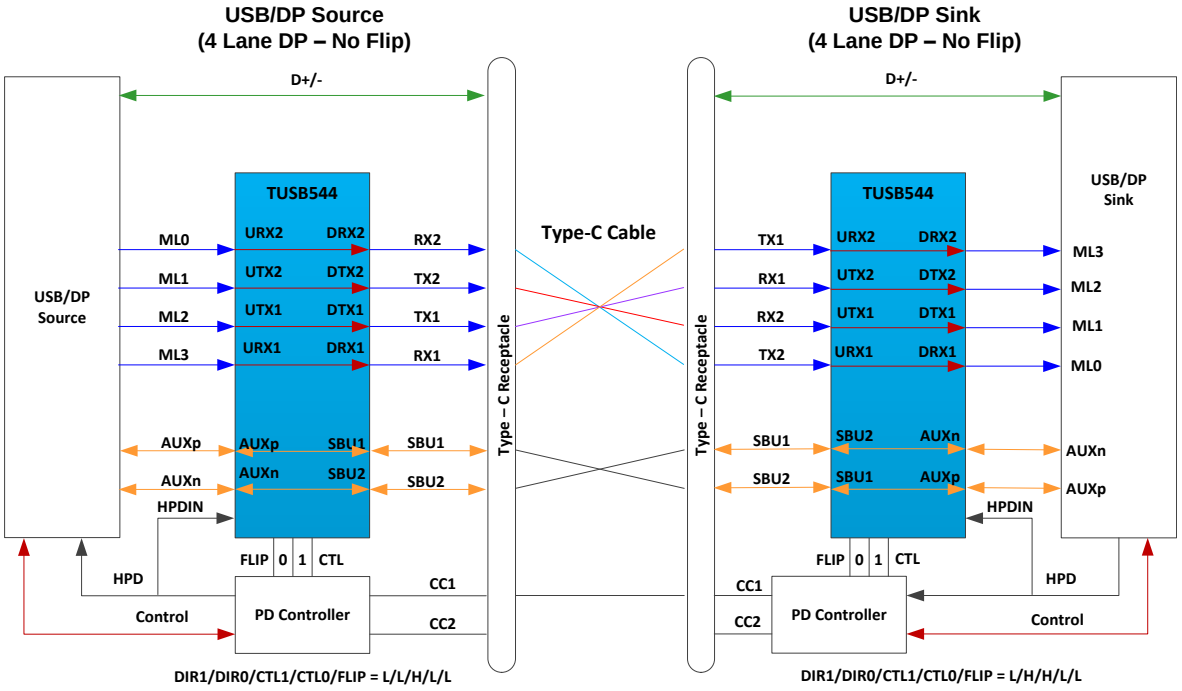


图 41. Four Lane DP – No Flip

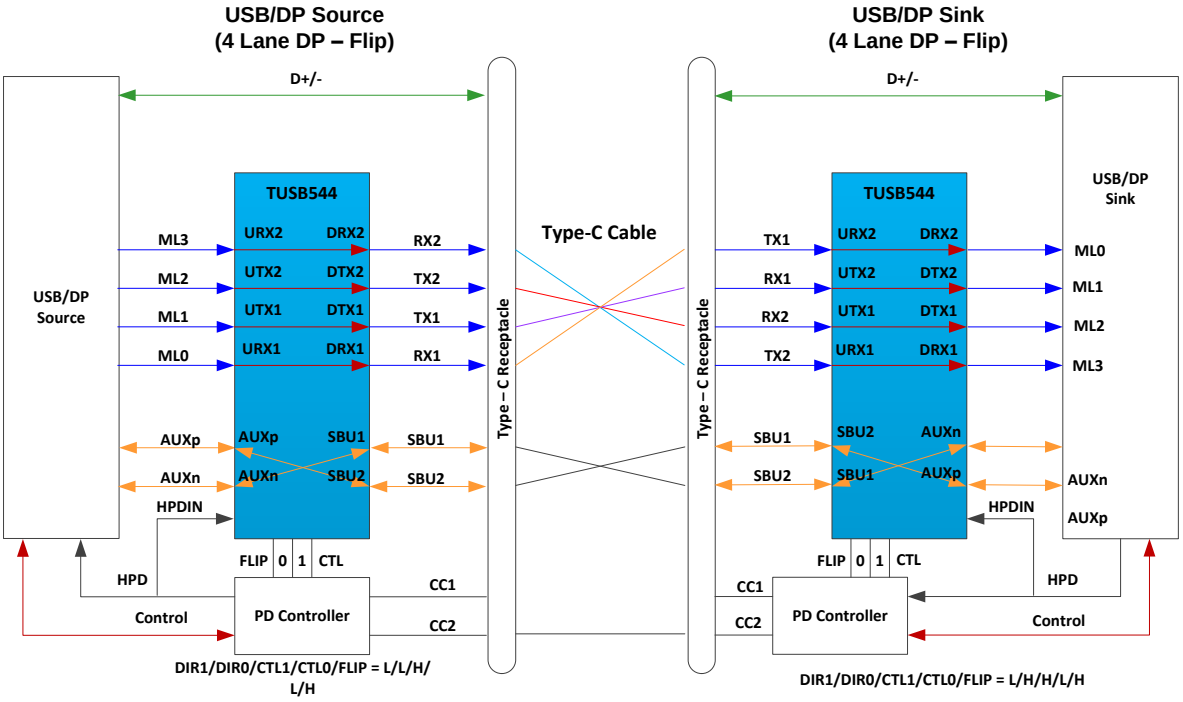


图 42. Four Lane DP – With Flip

System Examples（接下页）

8.3.4 USB 3.1 only (USB/Custom Alternate Mode)

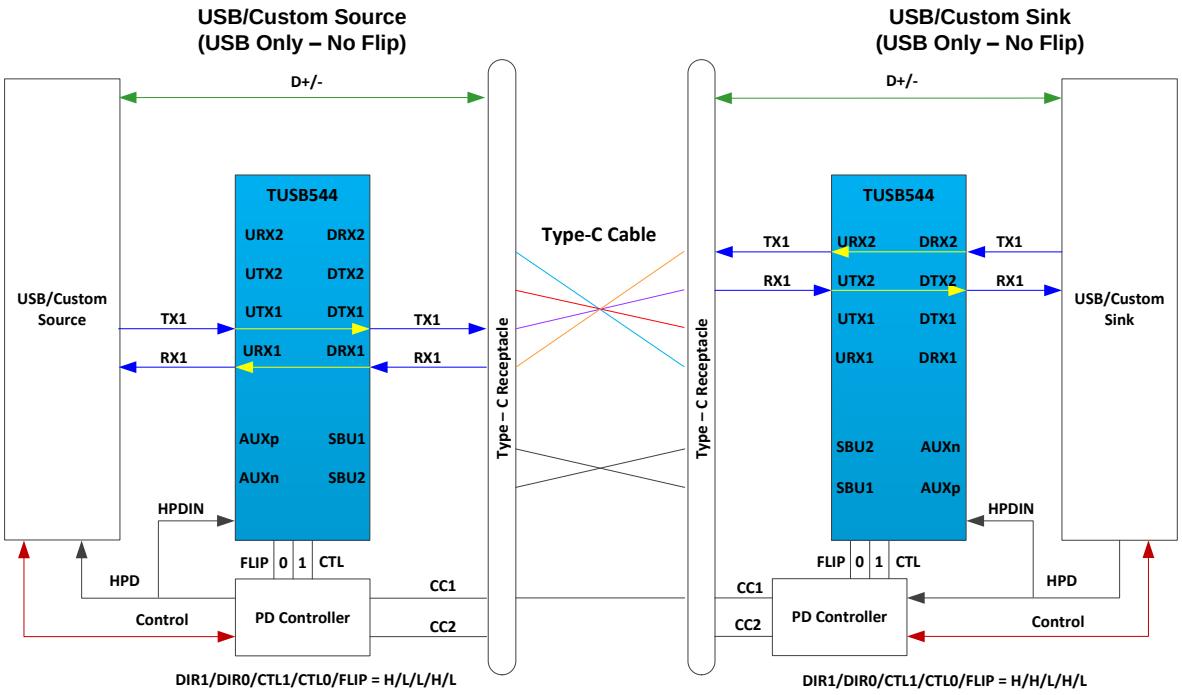


图 43. USB3.1 Only – No Flip

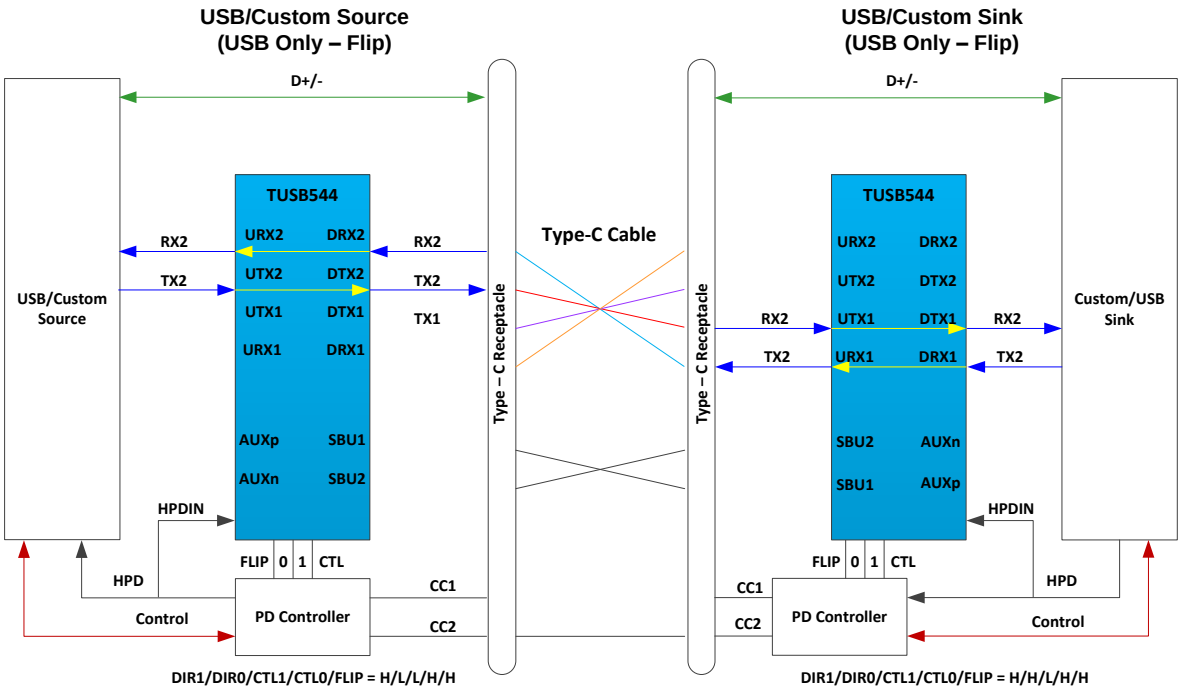


图 44. USB3.1 Only – With Flip

System Examples（接下页）

8.3.5 USB3.1 and 1 Lane of Custom Alt Mode

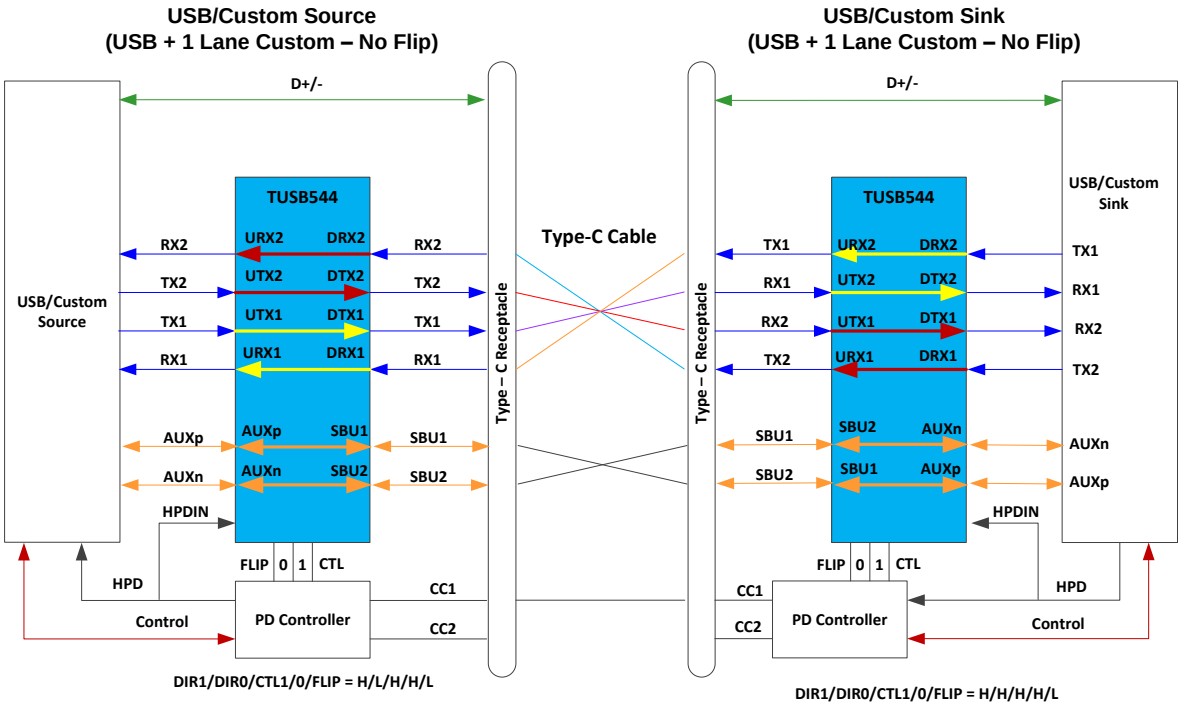


图 45. USB3.1 + 1 Lane Custom Alt Mode – No Flip

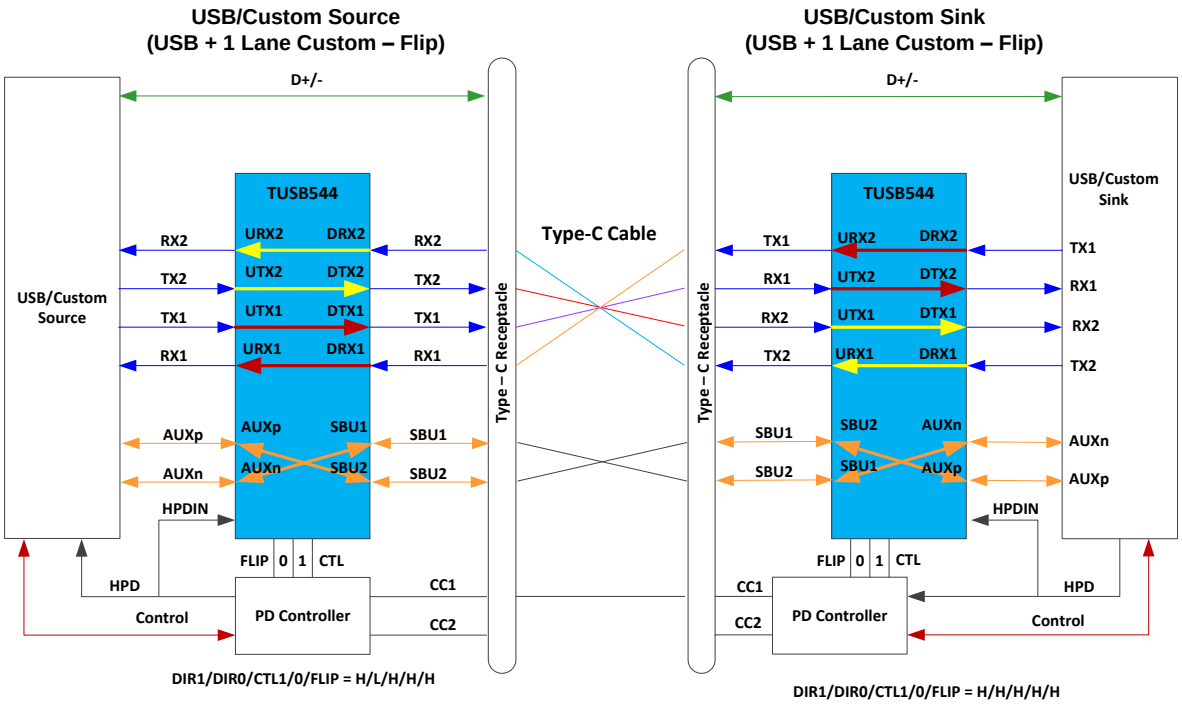


图 46. USB 3.1 + 1 Lane Custom Alt. Mode – Flip

System Examples（接下页）

8.3.6 USB3.1 and 2 Lane of Custom Alt Mode

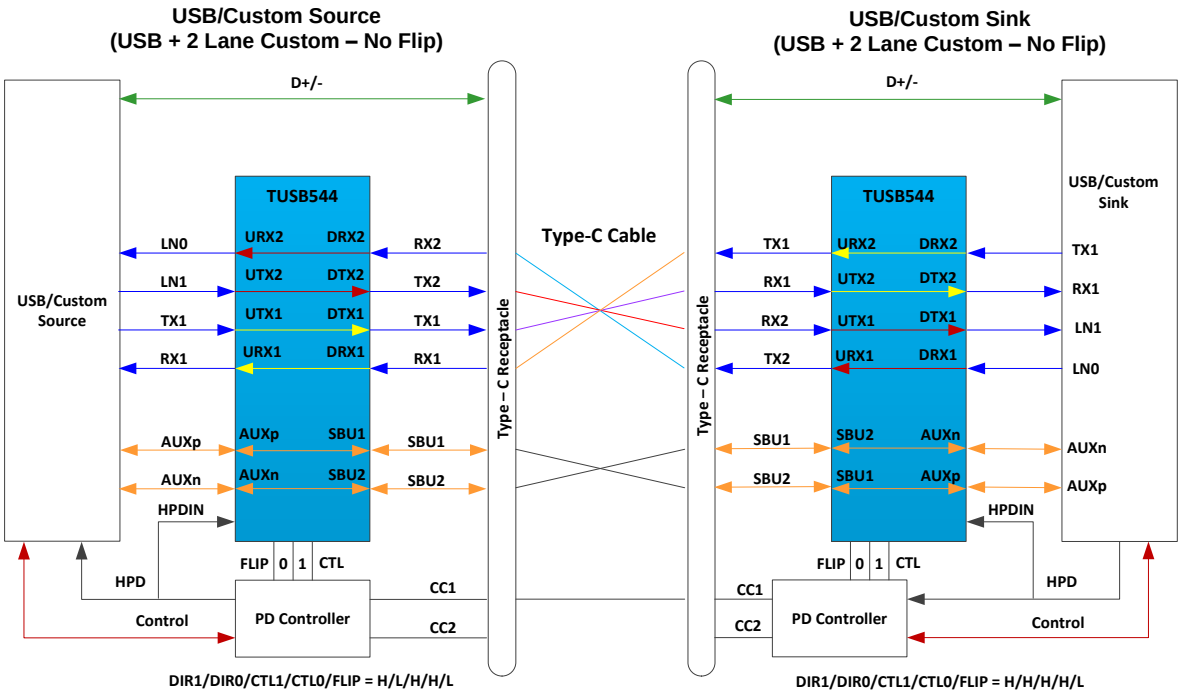


图 47. Two Lane Custom Alternate Mode – No Flip

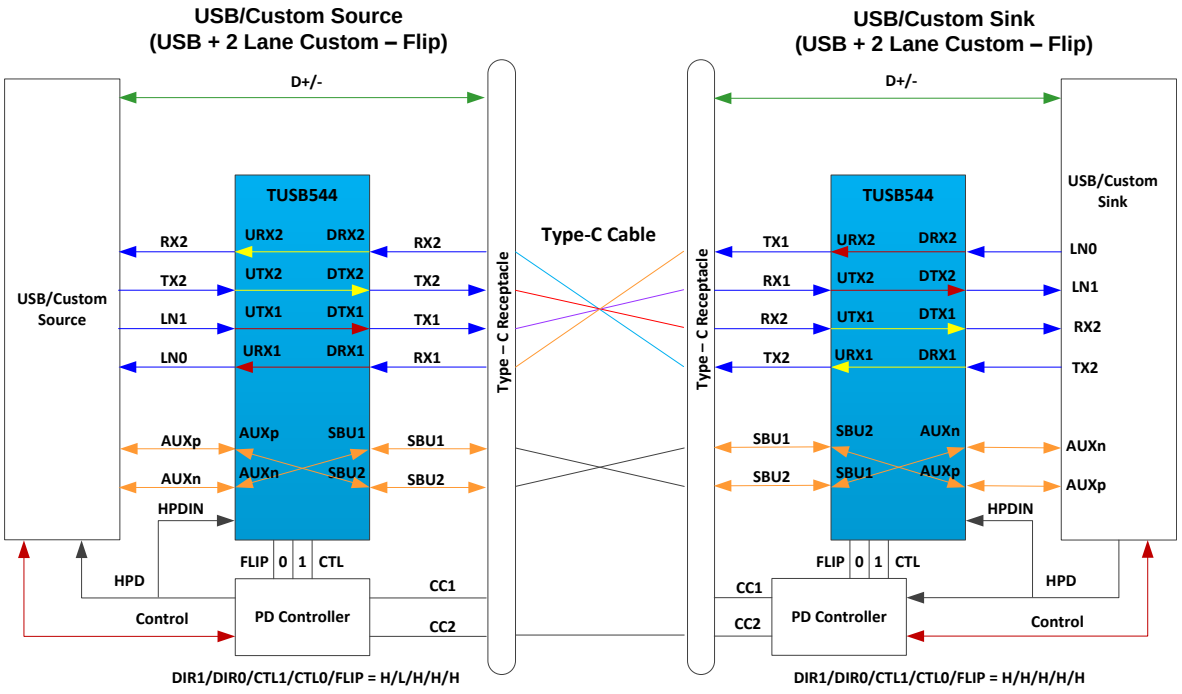


图 48. Two Lane Custom Alternate Mode – With Flip

System Examples（接下页）

8.3.7 USB3.1 and 4 Lane of Custom Alt Mode

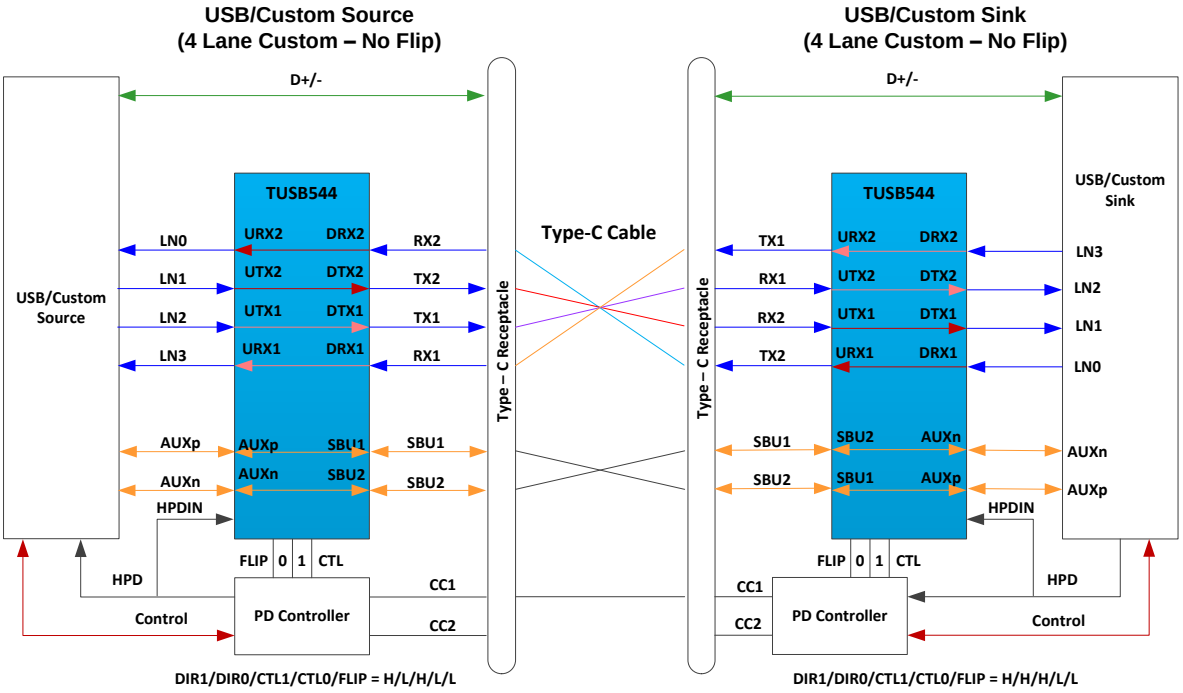


图 49. Four Lane Custom Alternate Mode – No Flip

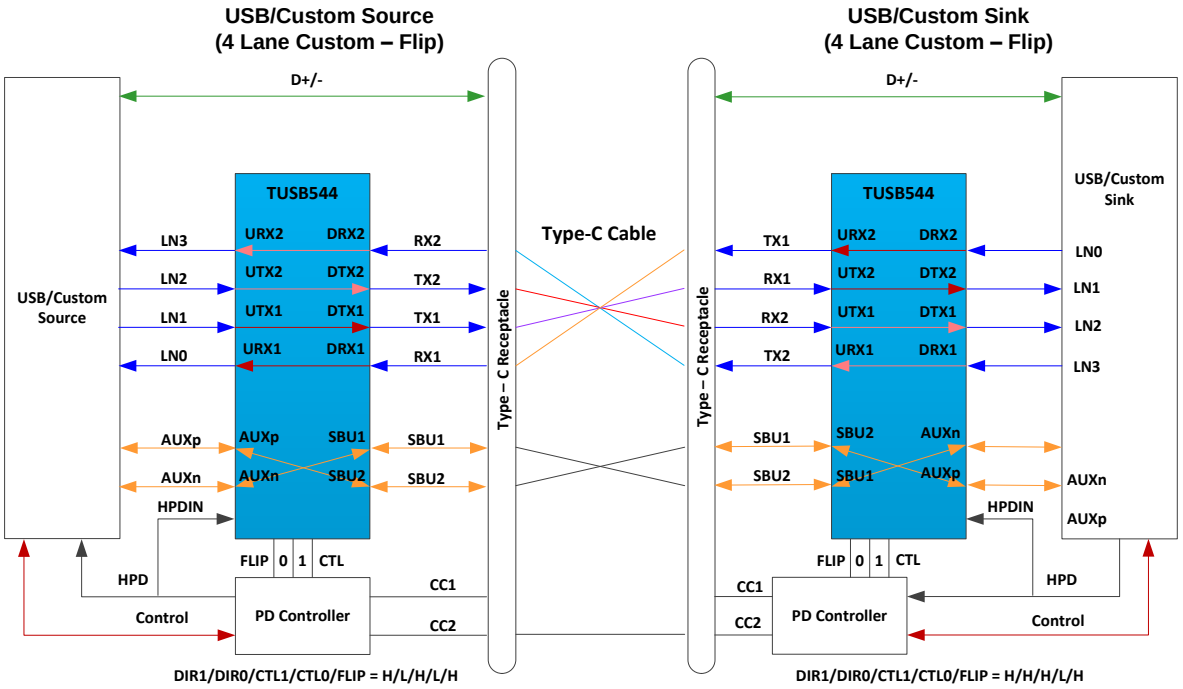


图 50. Four Lane Custom Alternate Mode – With Flip

9 Power Supply Recommendations

The TUSB544 is designed to operate with a 3.3 V power supply. Levels above those listed in the *Absolute Maximum Ratings* table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors should be used to reduce noise and improve power supply integrity. A 0.1-µF capacitor should be used on each power pin.

10 Layout

10.1 Layout Guidelines

1. RXP/N and TXP/N pairs should be routed with controlled 90-Ohm differential impedance (+/- 15%).
2. Keep away from other high speed signals.
3. Intra-pair routing should be kept to within 2 mils.
4. Length matching should be near the location of mismatch.
5. Each pair should be separated at least by 3 times the signal trace width.
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
7. Route all differential pairs on the same of layer.
8. The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Adding Test points will cause impedance discontinuity; and therefore, negatively impacts signal performance. If test points are used, the test points should be placed in series and symmetrically. The test points must not be placed in a manner that causes a stub on the differential pair.

10.2 Layout Example

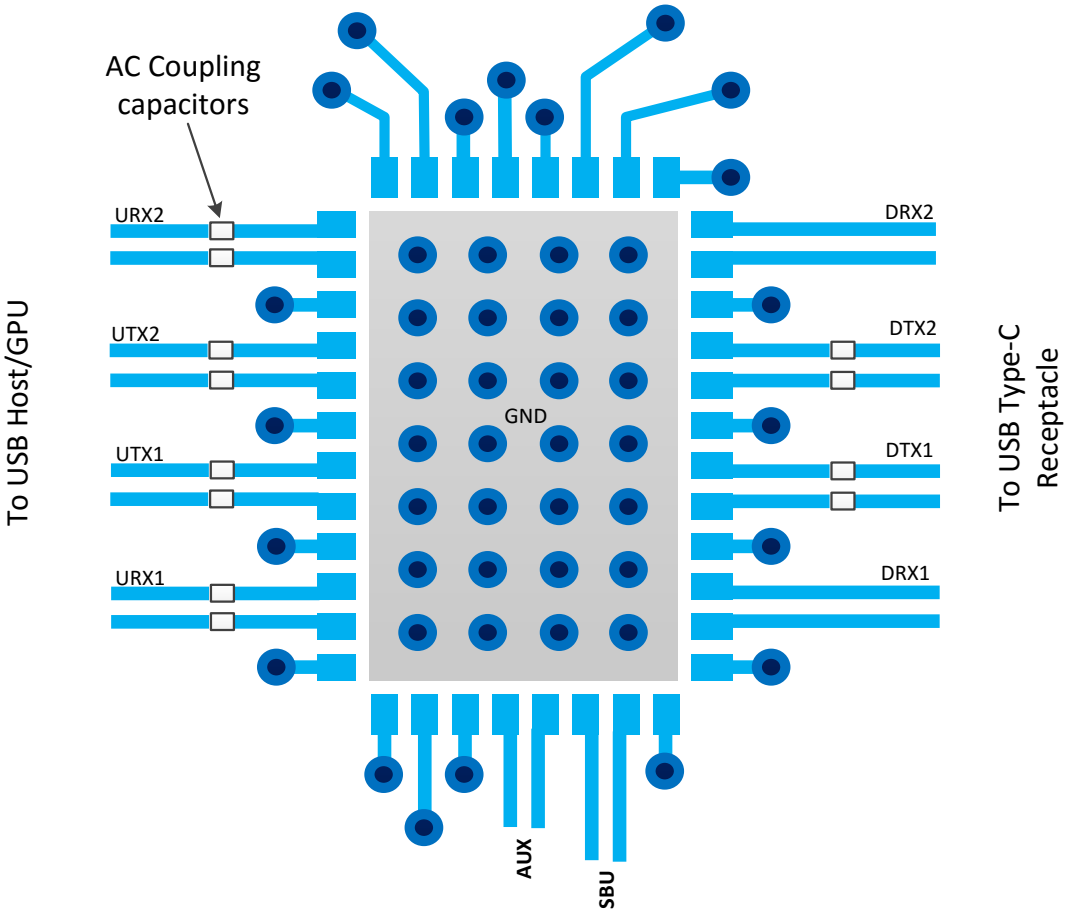


图 51.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

本节标识的文档均在本规范中引用。为简化文本，文中的大多数参考文献均用文档标签 [文档标签] 标识，而不使用完整的文档标题。

相关文档如下：

- [USB31] 通用串行总线 3.1 规范。
- [TYPEC] 通用串行总线 Type C 线缆和连接器规范

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB544IRNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TUSB544	Samples
TUSB544IRNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TUSB544	Samples
TUSB544RNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TUSB544	Samples
TUSB544RNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TUSB544	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

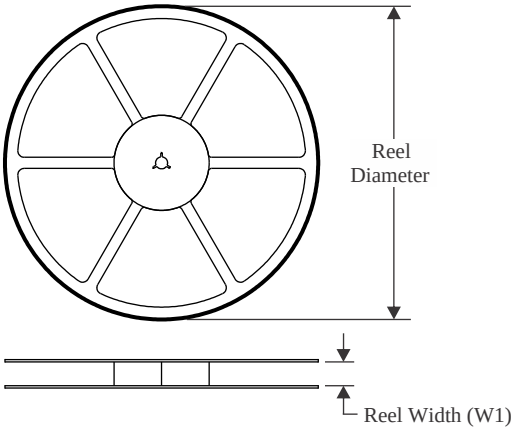
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

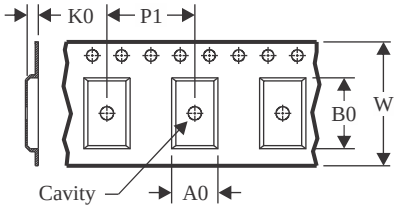
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

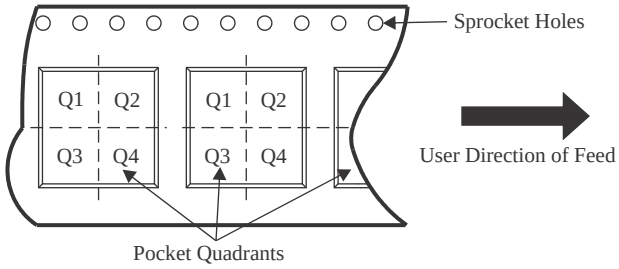


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

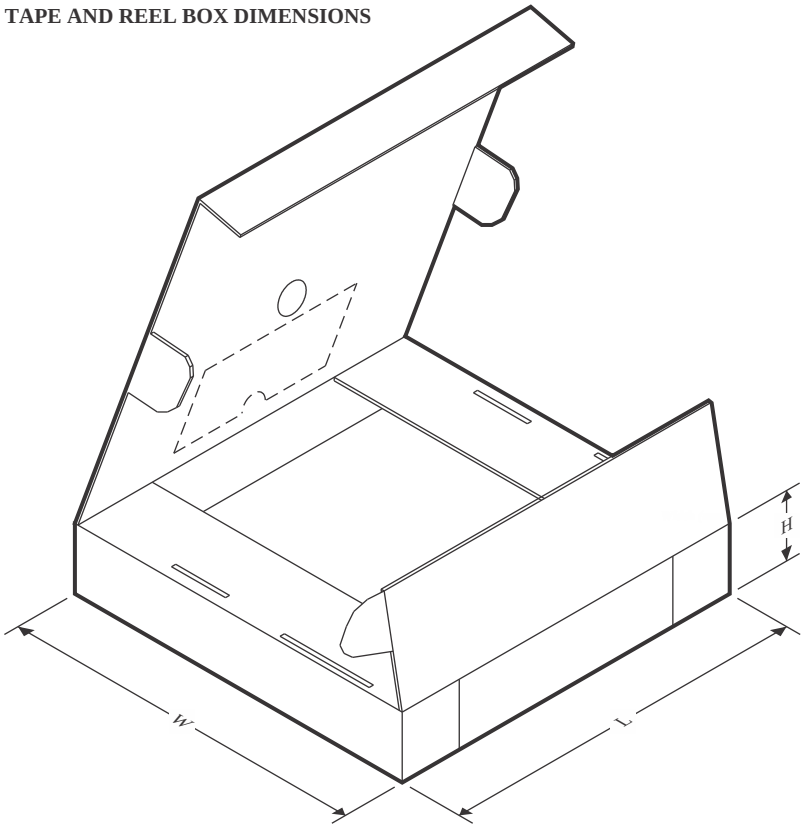
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB544IRNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB544IRNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB544RNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB544RNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

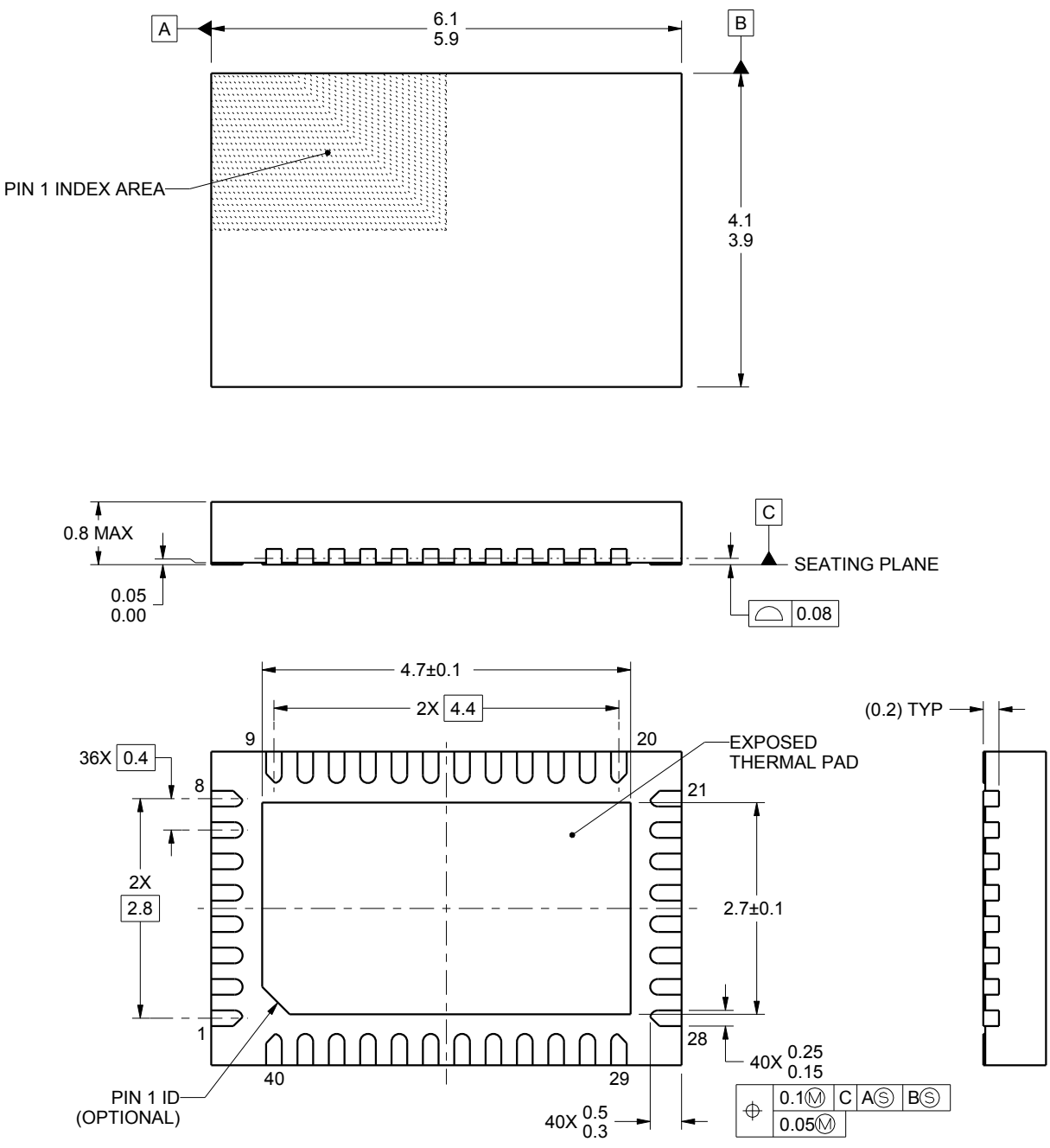
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB544IRNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
TUSB544IRNQT	WQFN	RNQ	40	250	210.0	185.0	35.0
TUSB544RNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
TUSB544RNQT	WQFN	RNQ	40	250	210.0	185.0	35.0

PACKAGE OUTLINE

RNQ0040A

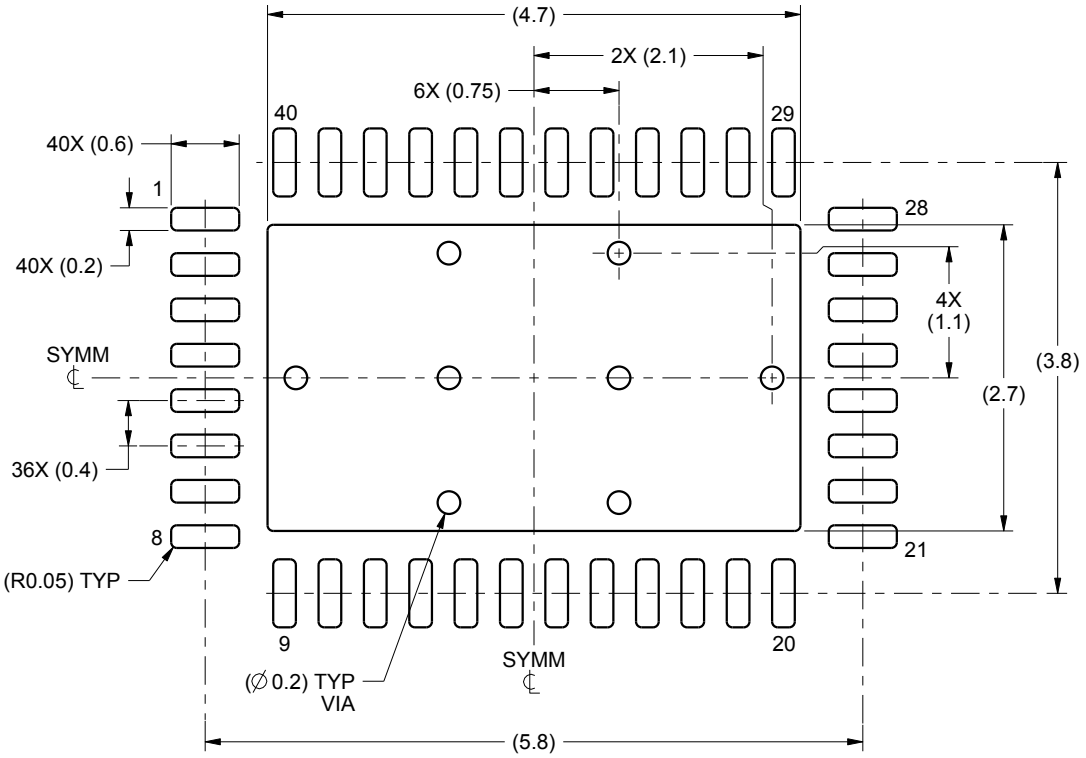
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

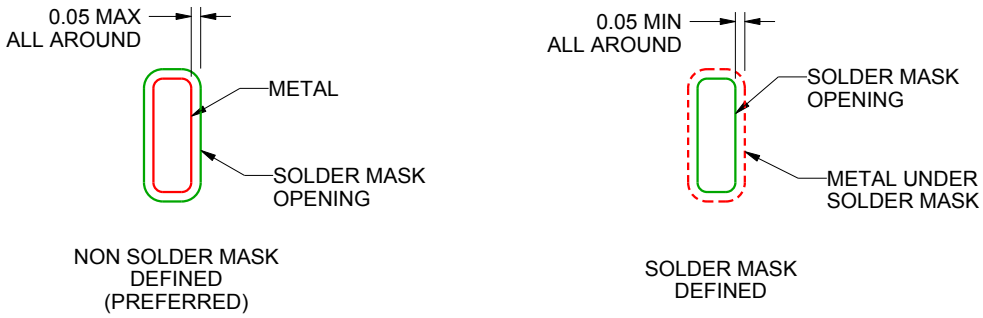


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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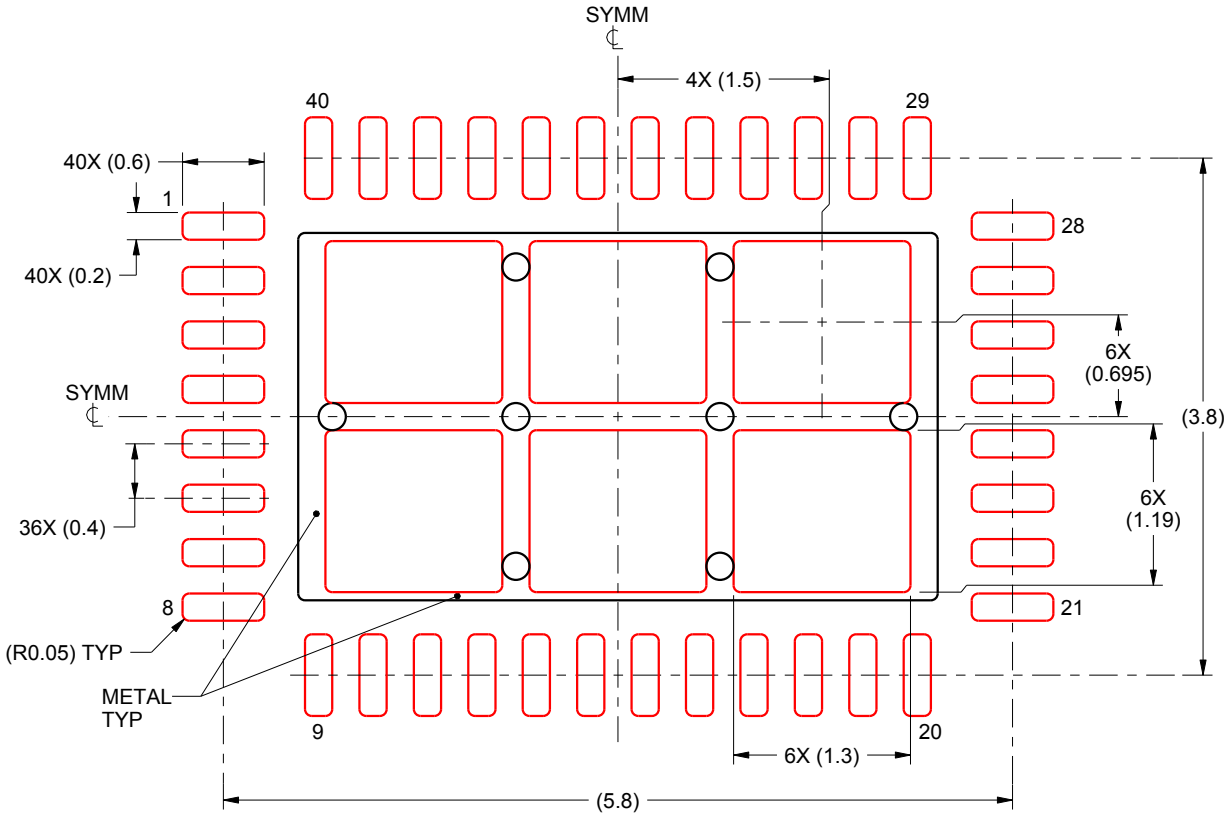
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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