TF Semiconductor Solutions

TF2106M

High-Side and Low-SideGate Driver

Features

- **Floating high-side driver in bootstrap operation to 600V**
- **Drives two N-channel MOSFETs or IGBTs in high-side/ low-side configuration**
- **Outputs tolerant to negative transients**
- **Wide low-side gate driver and logic supply: 10V to 20V**
- **Logic inputs CMOS and TTL compatible (down to 3.3V)**
- **Schmitt triggered logic inputs with internal pull down**
- **Undervoltage lockout for V_{CC}**
- **Space-saving SOIC-8 package available**
- **Extended temperature range:-40°C to +125°C**

Description

The TF2106M is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a high-side/low-side configuration . TF Semiconductor 's high voltage process enables the TF2106's high-side to switch to 600V in a bootstrap operation . The 50 ns (max) propagation delay matching between the high and the low side drivers allows high frequency switching.

The TF2106M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) for easy interfacing with controlling devices . The driver outputs feature high pulse current buffers designed for minimum driver cross conduction . The low -side gate driver and logic share a common ground

The TF2106M is available in a space-saving 8-pin SOIC package and a 8-pin PDIP; the operating temperature extends from -40 °C to +125°C .

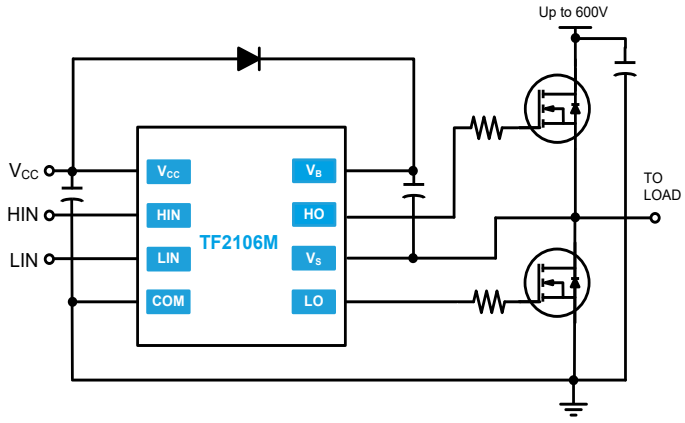
SOIC-8(N)

PDIP-8

Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

Typical Application

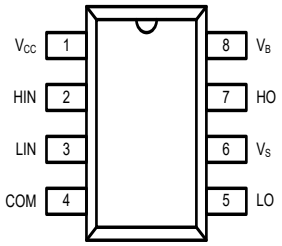


Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2106M-TAU	SOIC-8(N)	Tube / 100	YYWW TF2106 Lot ID
TF2106M-TAH	SOIC-8(N)	T & R/ 2500	YYWW TF2106 Lot ID
TF2106M-3AS	PDIP-8	Tube / 50	YYWW TF2106 Lot ID

Pin Diagrams



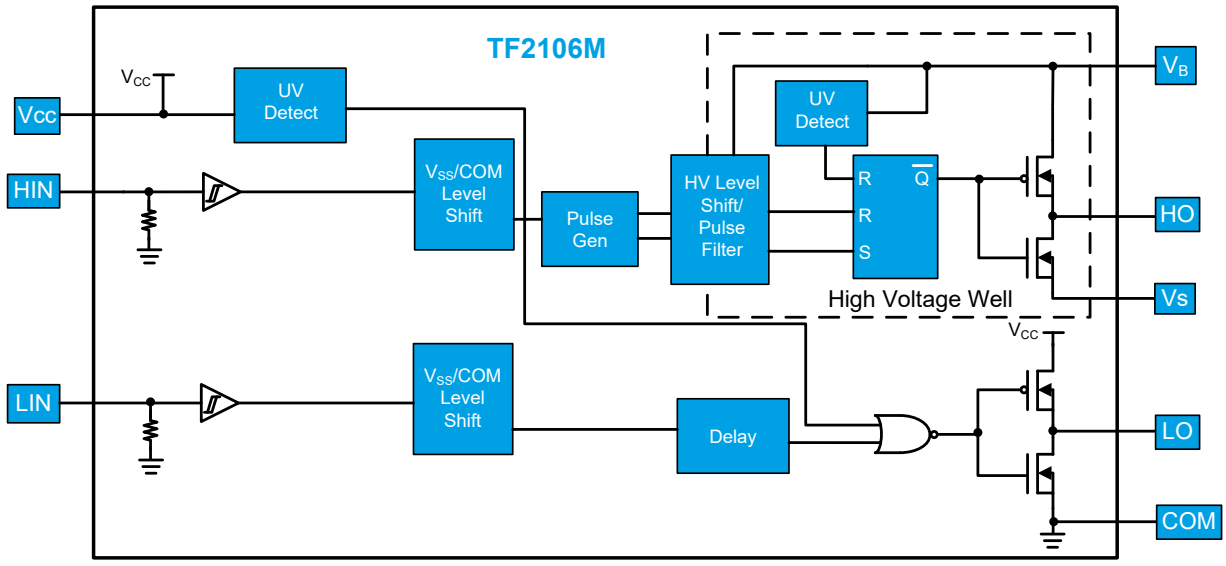
Top View: PDIP-8, SOIC-8

TF2106M

Pin Descriptions

PIN NAME	PIN DESCRIPTION
HIN	Logic input for high-side gate driver output (HO), in phase
LIN	Logic input for low-side gate driver output (LO), in phase
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return
NC	"No connect" pin

Functional Block Diagram



Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +624V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S / dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Low side and logic fixed supply voltage.....-0.3V to +24V
V_{LO} - Low side output voltage.....-0.3V to V_{CC}+0.3V
V_{IN} - Logic input voltage (HIN and LIN)... -0.3V to V_{CC}+0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-8.....0.625W
PDIP-8.....1.0W

SOIC-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....45 °C/W
θ_{JA}.....200 °C/W

PDIP-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....35 °C/W
θ_{JA}.....125 °C/W

T_J - Junction operating temperature .....+150 °C
T_L - Lead temperature (soldering, 10s) ..... +300 °C
T_{stg} - Storage temperature range .....-55 °C to +150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10		V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***		600	V
V_{HO}	High side floating output voltage	V_S		V_B	V
V_{CC}	Low side and logic fixed supply voltage	10		20	V
V_{LO}	Low side output voltage	0		V_{CC}	V
V_{IN}	Logic input voltage (HIN and LIN)	0		5	V
T_A	Ambient temperature	-40		125	°C

NOTE3 *Logic operational for V_S = -5 to +600V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10V to 20V *NOTE5*.	2.5			V
V_{IL}	Logic "0" input voltage				0.6	V
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2mA		0.05	0.2	V
V_{OL}	Low level output voltage, V_O	I_O = 2mA		0.02	0.1	V
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V	20	75	130	µA
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V	60	120	180	µA
I_{IN+}	Logic "1" input bias current	V_{IN} = 5V		5	20	µA
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V			2	µA
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		8	8.9	9.8	V
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9	V
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		8	8.9	9.8	V
V_{BSUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9	V
V_{UVLOH}	Undervoltage lockout hysteresis		0.3	0.7		V
I_{O+}	Output high short circuit pulsed current	V_O = 0V, V_{IN} = Logic "1", PW ≤ 10 µs	130	290		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15V, V_{IN} = Logic "0", PW ≤ 10 µs	270	600		mA

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C, and C_L = 1000pF, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ON}	Turn-on propagation delay	V_S = 0V		220	300	ns
t_{OFF}	Turn-off propagation delay	V_S = 0V or 600V		200	280	ns
t_r	Turn-on rise time			100	220	ns
t_f	Turn-off fall time	V_S = 0V		35	80	ns
t_{DM}	Delay matching				30	ns

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO.*

NOTE5 *For optimal operation, it is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum with a pulse width of 440ns minimum.*

Timing Waveforms

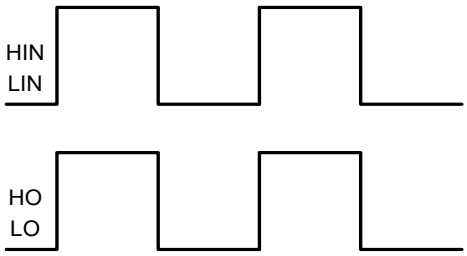


Figure 1. Input / Output Timing Diagram

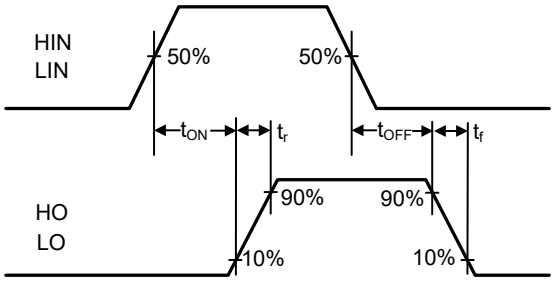


Figure 2. Switching Time Waveform Definitions

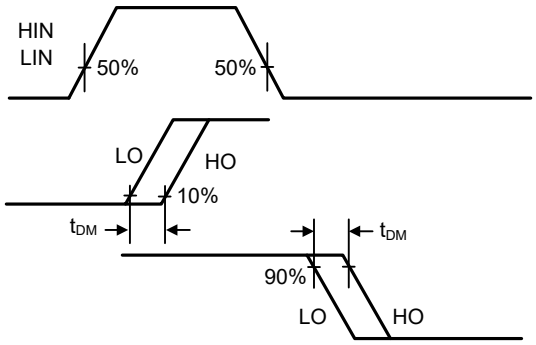


Figure 3. Delay Matching Waveform Definitions

Typical Characteristics

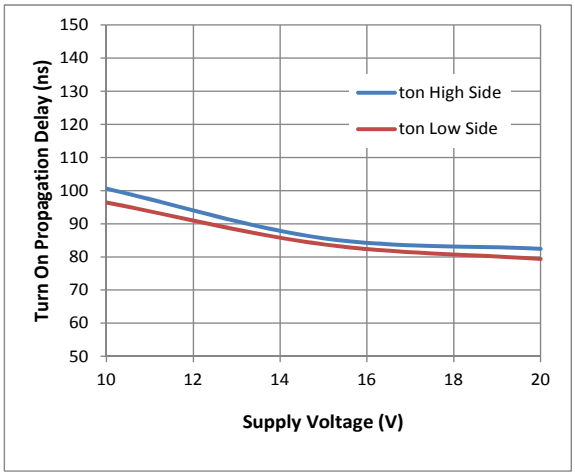


Figure 4. Turn-on Propagation Delay vs. Supply Voltage

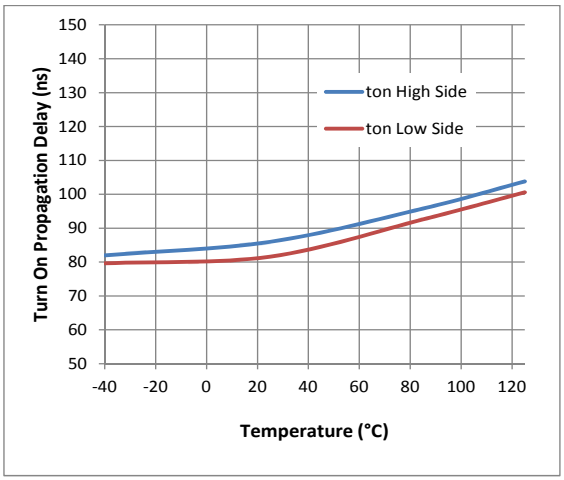


Figure 5. Turn-on Propagation Delay vs. Temperature

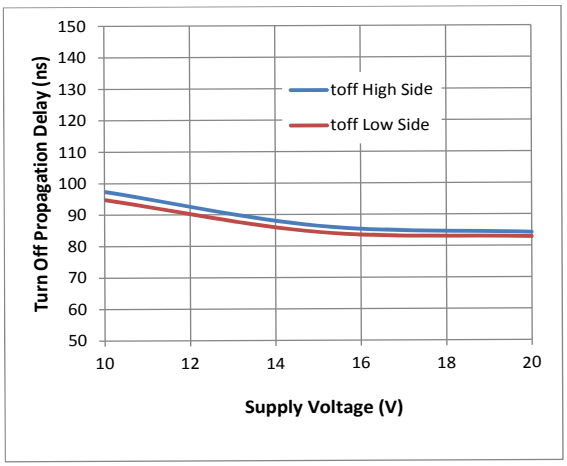


Figure 6. Turn-off Propagation Delay vs. Supply Voltage

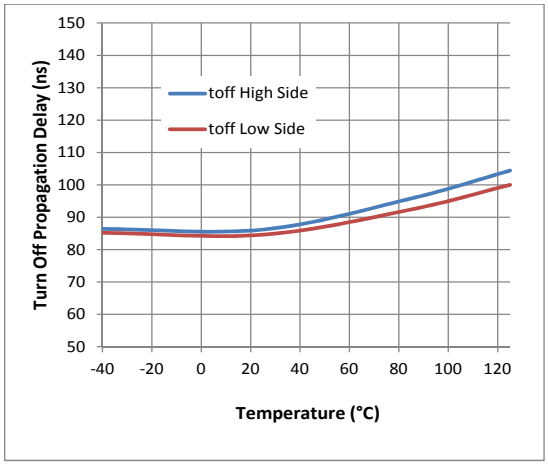


Figure 7. Turn-off Propagation Delay vs. Temperature

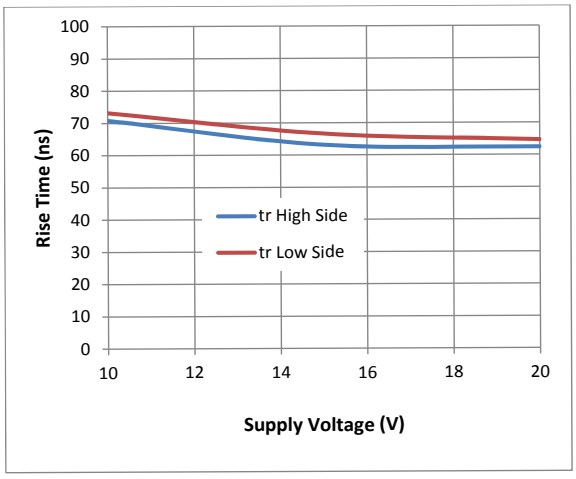


Figure 8. Rise Time vs. Supply Voltage

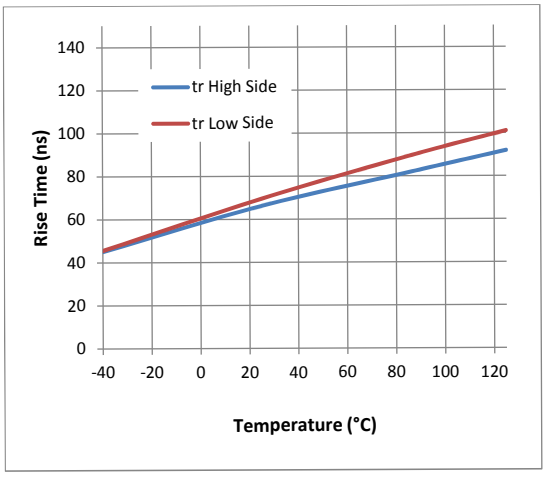


Figure 9. Rise Time vs. Temperature

Typical Characteristics, cont'd

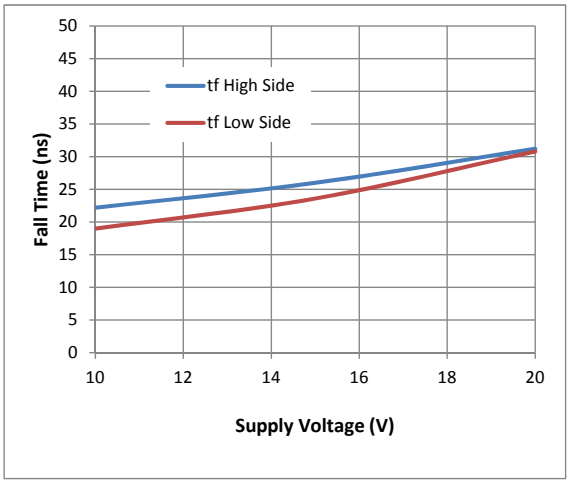


Figure 10. Fall Time vs. Supply Voltage

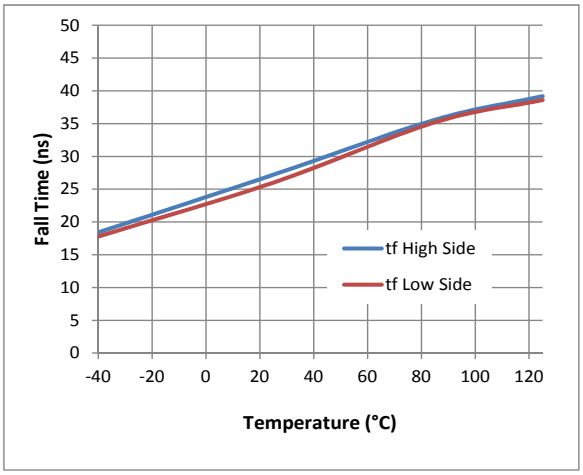


Figure 11. Fall Time vs. Temperature

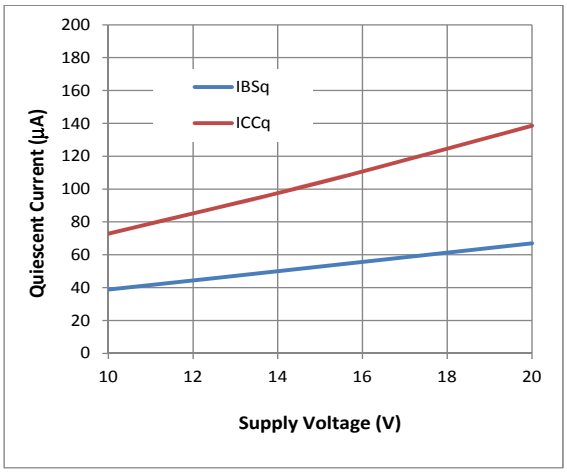


Figure 12. Quiescent Current vs. Supply Voltage

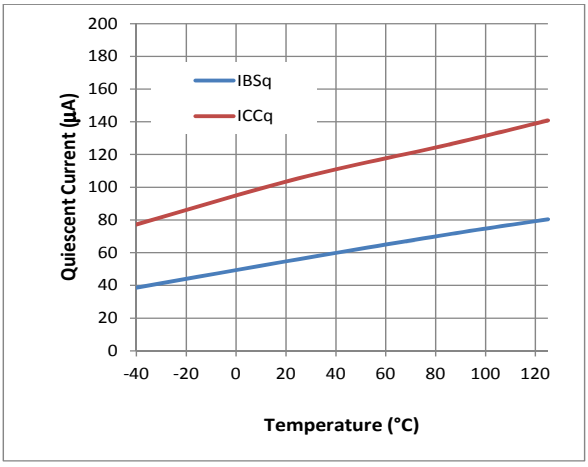


Figure 13. Quiescent Current vs. Temperature

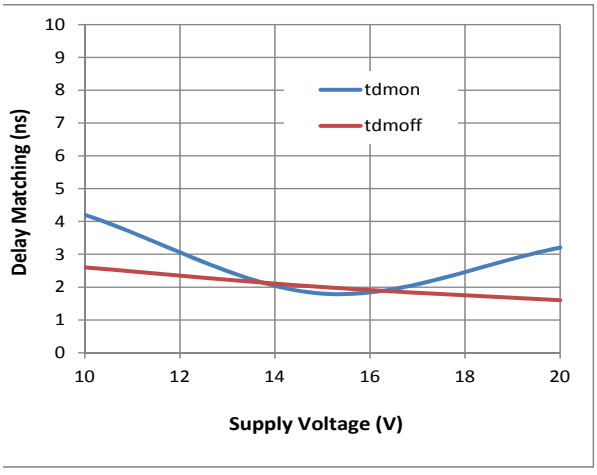


Figure 14. Delay Matching vs. Supply Voltage

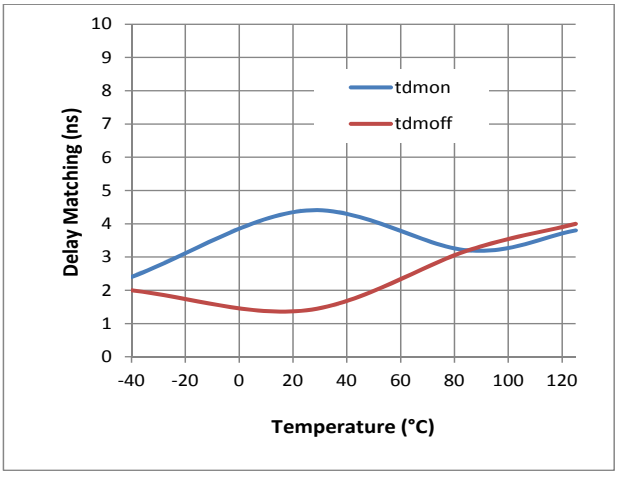


Figure 15. Delay Matching vs. Temperature

Typical Characteristics, cont'd

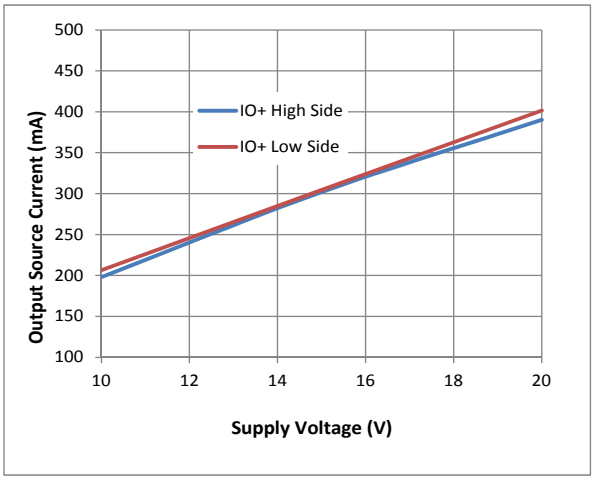


Figure 16. Output Source Current vs. Supply Voltage

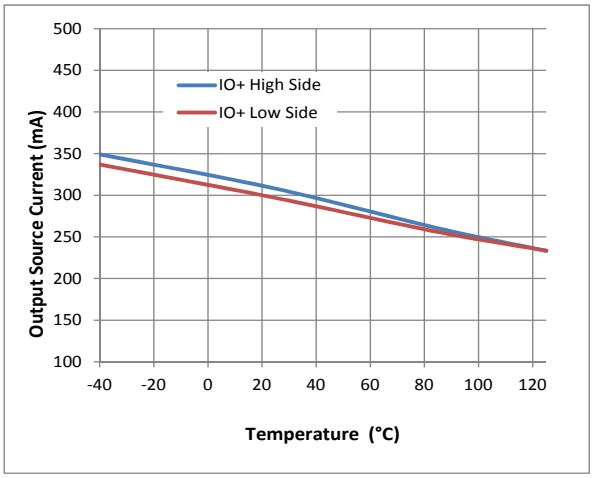


Figure 17. Output Source Current vs. Temperature

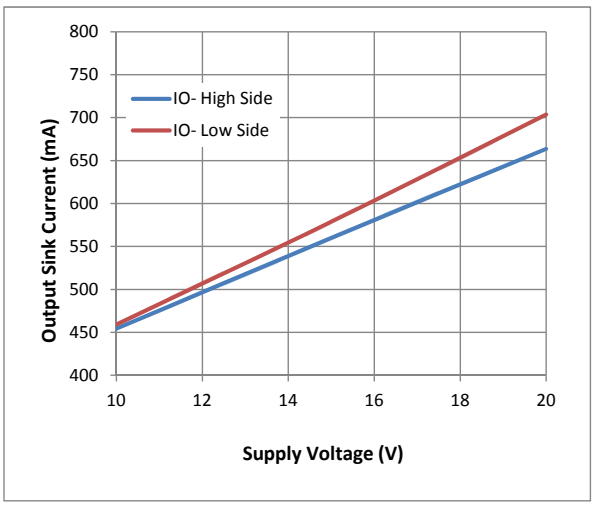


Figure 18. Output Sink Current vs. Supply Voltage

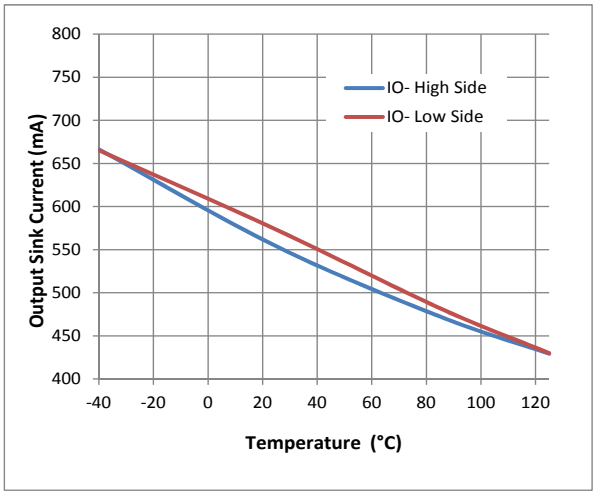


Figure 19. Output Sink Current vs. Temperature

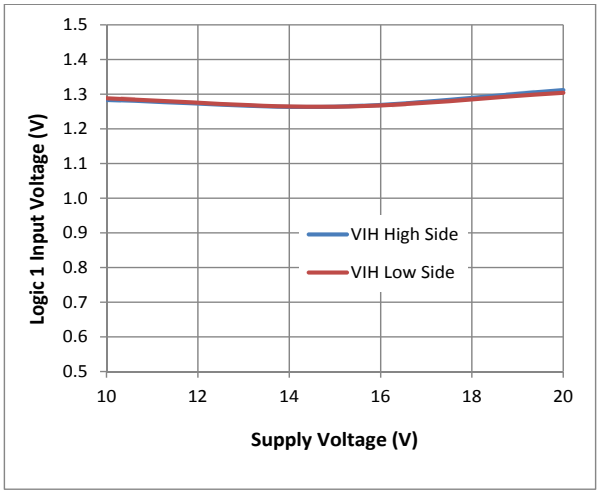


Figure 20. Logic 1 Input Voltage vs. Supply Voltage

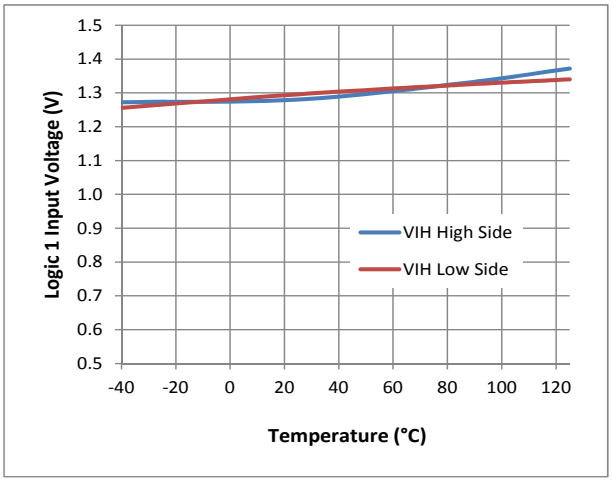


Figure 21. Logic 1 Input Voltage vs. Temperature

Typical Characteristics, cont'd

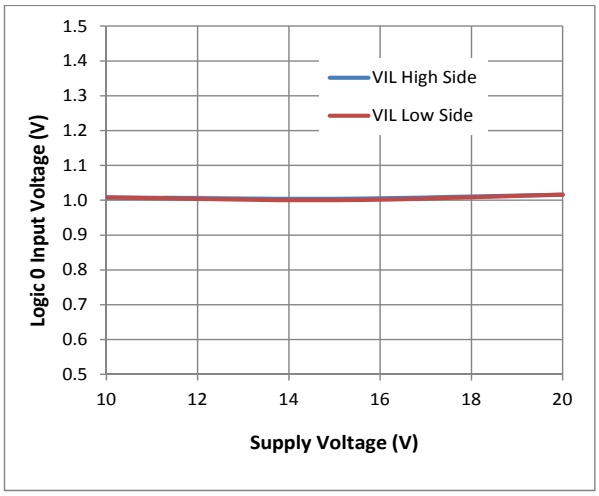


Figure 22. Logic 0 Input Voltage vs. Supply Voltage

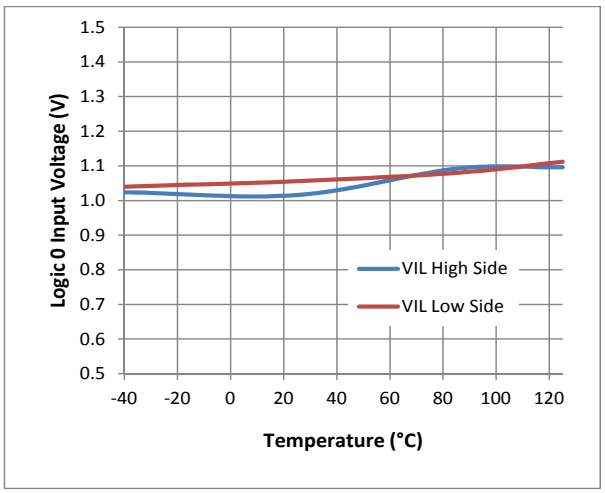


Figure 23. Logic 0 Input Voltage vs. Temperature

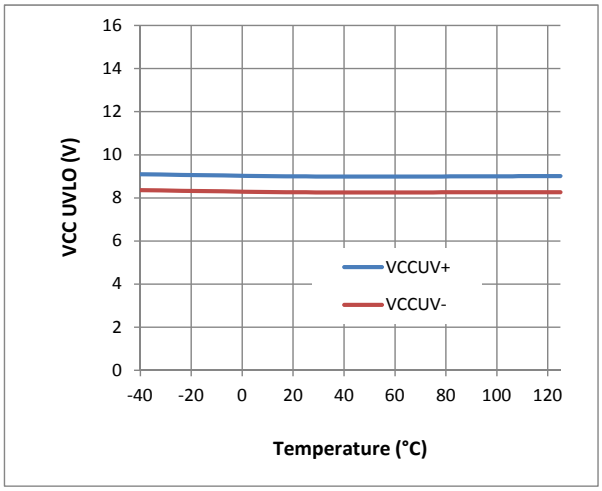


Figure 24. V_{CC} UVLO vs. Temperature

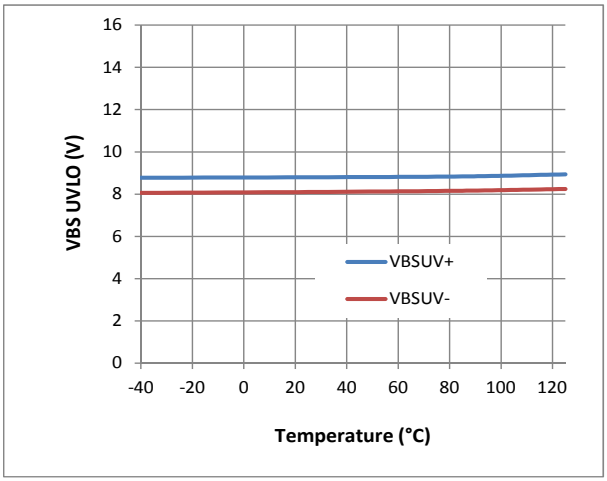


Figure 25. V_{BS} UVLO vs. Temperature

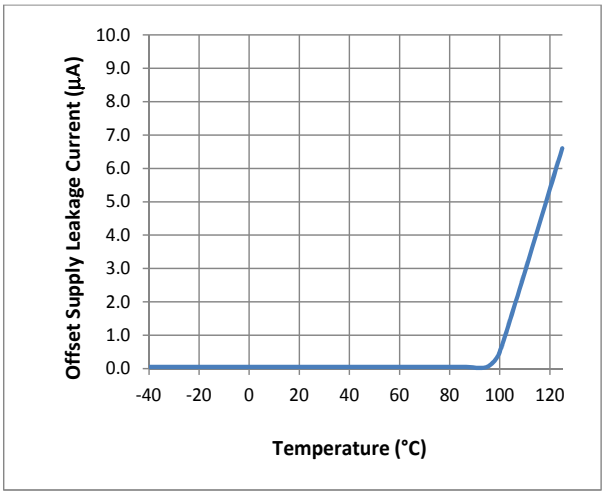


Figure 26. Offset Supply Leakage Current Temperature

Operation

Halfbridge Configuration

A common configuration used for the TF2106M is a half - bridge (see fig. 28). In a half -bridge configuration the source of the high-side MOSFET (Q_H) and the drain of the low-side MOSFET (Q_L) are connected. That line (V_S) is both the return for the high side in the gate driver IC as well as the output of the half-bridge. When Q_H is on and Q_L is off, V_S swings to high voltage, and when Q_H is off and Q_L is on, V_S swings to GND. Hence the output switches from GND to high voltage at the frequency of HIN and LIN, this line drives a transformer for a power supply, or a coil on a motor.

In this half-bridge configuration, high voltage DC is input to the MOSFETs, and converted to a high voltage switching signal to output to load (fig 28). The MOSFETs operate in saturation mode and an important function of the gate driver is to turn on the MOSFET quickly to minimize switching losses from the linear region of the MOSFET (turn on and turn off); the TF2106 has a typical rise/fall time of 100ns/35ns into a 1nF load.

Another important function of the gate driver IC in the half-bridge configuration is to convert the logic signals of control (TF2106 operates at logic 3.3V), to a voltage level and current capacity to drive the gate of the MOSFET and IGBT; this requires driving large currents initially to turn on/ turn off the MOSFET quickly. Also the floating well of the high-side allows high voltage operation in the bootstrap operation.

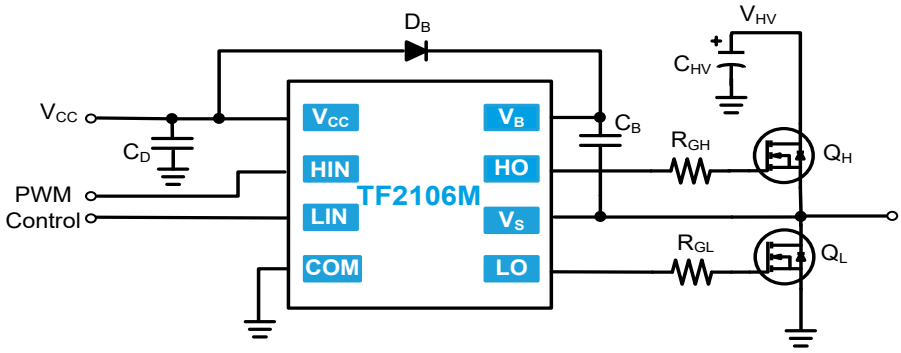


Figure 28. TF2106M in a half-bridge configuration

Bootstrap Operation

The supply for the TF 2106M High Side is provided by the bootstrap capacitor CB (see fig 29). In the half -bridge configuration, VS swings from 0V to VHV depending on the PWM input ot the IC. When VS is 0 V, VBS will go below VCC and V CC will charge CB. When HO goes high, VS swings to VHV, and VBS remains at VCC minus a diode drop (DB) due to the voltage on CB. This is the supply for the high side gate driver and allows the gate driver to function with the floating well (VS) at the high voltage.

When considering the *value of the bootstrap capacitor CB*, it is important that it is sized to provide enough energy to quickly drive the gate of QH. Values of 1 mF to 10mF are recommended, exact value depending on gate capacitance, and the noise in application. It is key to use a low ESR capacitor that is close to the device. This will best quickly supply charge to the gate of the MOSFET.

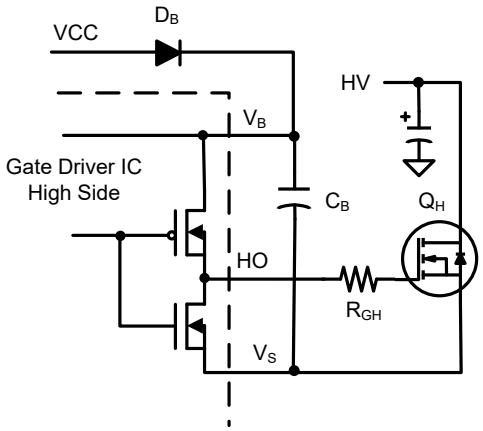


Figure 29. TF2106M high side in bootstrap operation

For a more detailed description on Gate Resistor Selection and Bootstrap Capacitor Selectrion, see the TF Semiconductor's Gate Driver Application Note (AN1347).

Gate Drive Control

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing, and too slow a rise/fall time will increase switching losses in the MOSFET.

An example of just the high side gate driver is shown in figure 30 (any selection of gate driver components should be the same for high side and low side drive); two extra components are seen, R_{DH} and D_H. With the careful selection of R_{GH} and R_{DH}, it is possible to selectively control the rise time and fall time of the gate drive. For turn on, all current will go from the IC through R_{GH} and charge the MOSFET gate capacitor, hence increasing or decreasing R_{GH} will increase or decrease rise time in the application. With the addition of D_H, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitor, through D_H and R_{DH} to the driver in the IC to VS. So increasing or decreasing R_{DH} will increase or decrease the fall time.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. For **gate resistor value selection** the exact value depends on the type of application and desired level of noise and ringing expected. Generally, power supplies switch at a fast speed, and want to squeeze out efficiency of the MOSFETs, so lower values are recommended, for example RGH = 5Ω - 20Ω. For motors, the switching speed is generally slower, and the application has more inherent noise, so higher values are recommended, for example RGH = 20Ω - 100Ω.

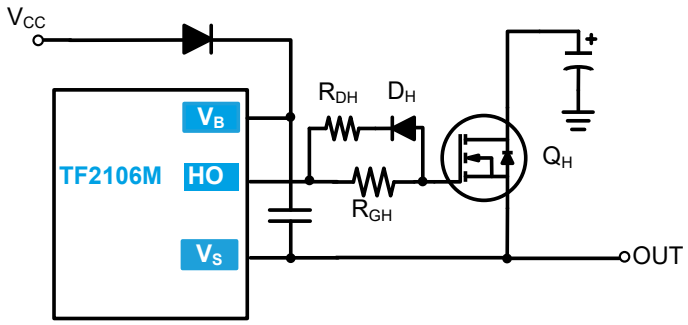


Figure 30. Gate Drive Control

Application Information

Layout Considerations

Layout plays a considerable role in noise and ringing in a circuit; unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 31 shows a halfbridge schematic with parasitic inductances in the high current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which would be caused by inductance in the metal of the trace. Considering fig. 31, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible. Low ESR ceramic capacitors should be used to minimize inductance. And finally the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

A layout example is seen in figure 32. Here there are two bootstrap capacitors (CB1 and CB2) and two decoupling capacitors (C1 and C2), and the caps are placed as close as possible to the HVIC. But even if only using one boostrap cap and one decoupling capacitor, it needs to be as close as possible to minimize inductance between the cap and the driver.

Generally, for the **decoupling capacitor** on VCC, at least one low ESR capacitor is recommended with it close to the device as shown in figure 32. Recommended values are 1µF to 10µF. A second smaller decoupling capacitor is sometimes added to provide better high frequency response (for example 0.1µF).

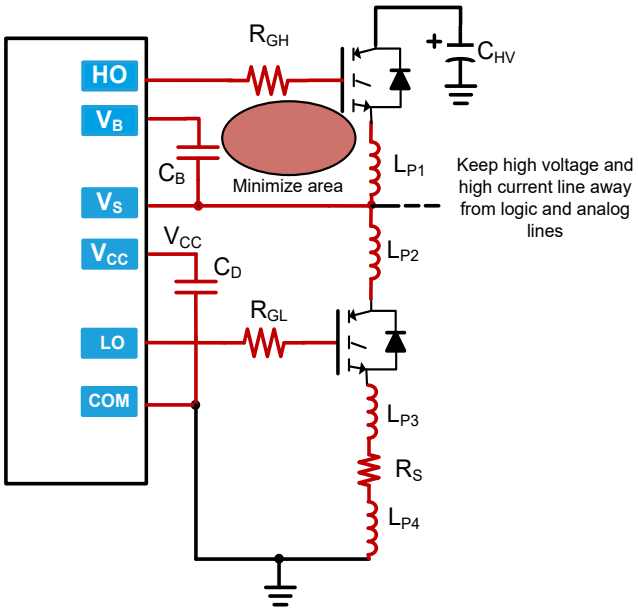


Figure 31. Layout Suggestions for TF2106M in a halfbridge

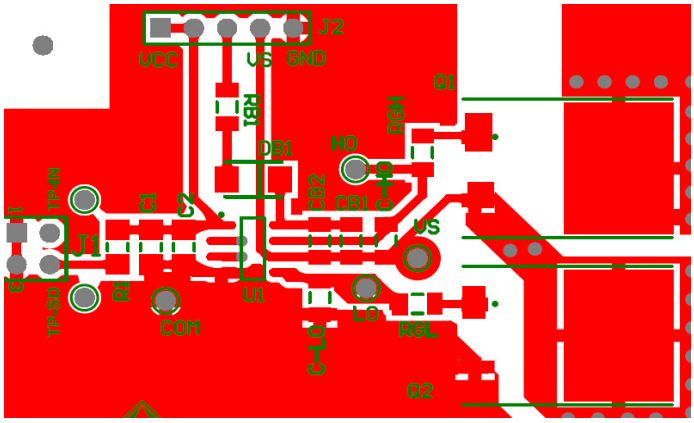
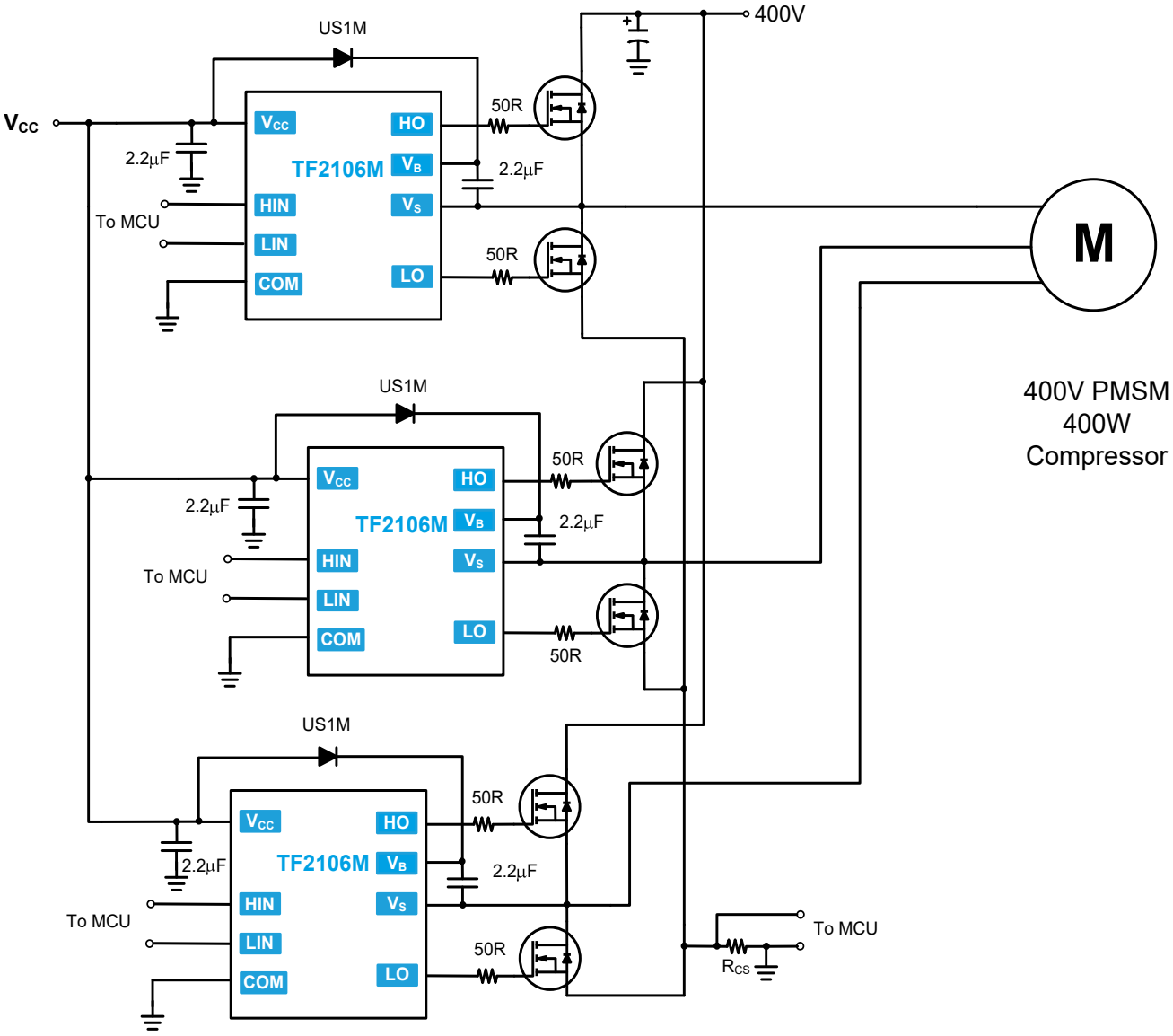


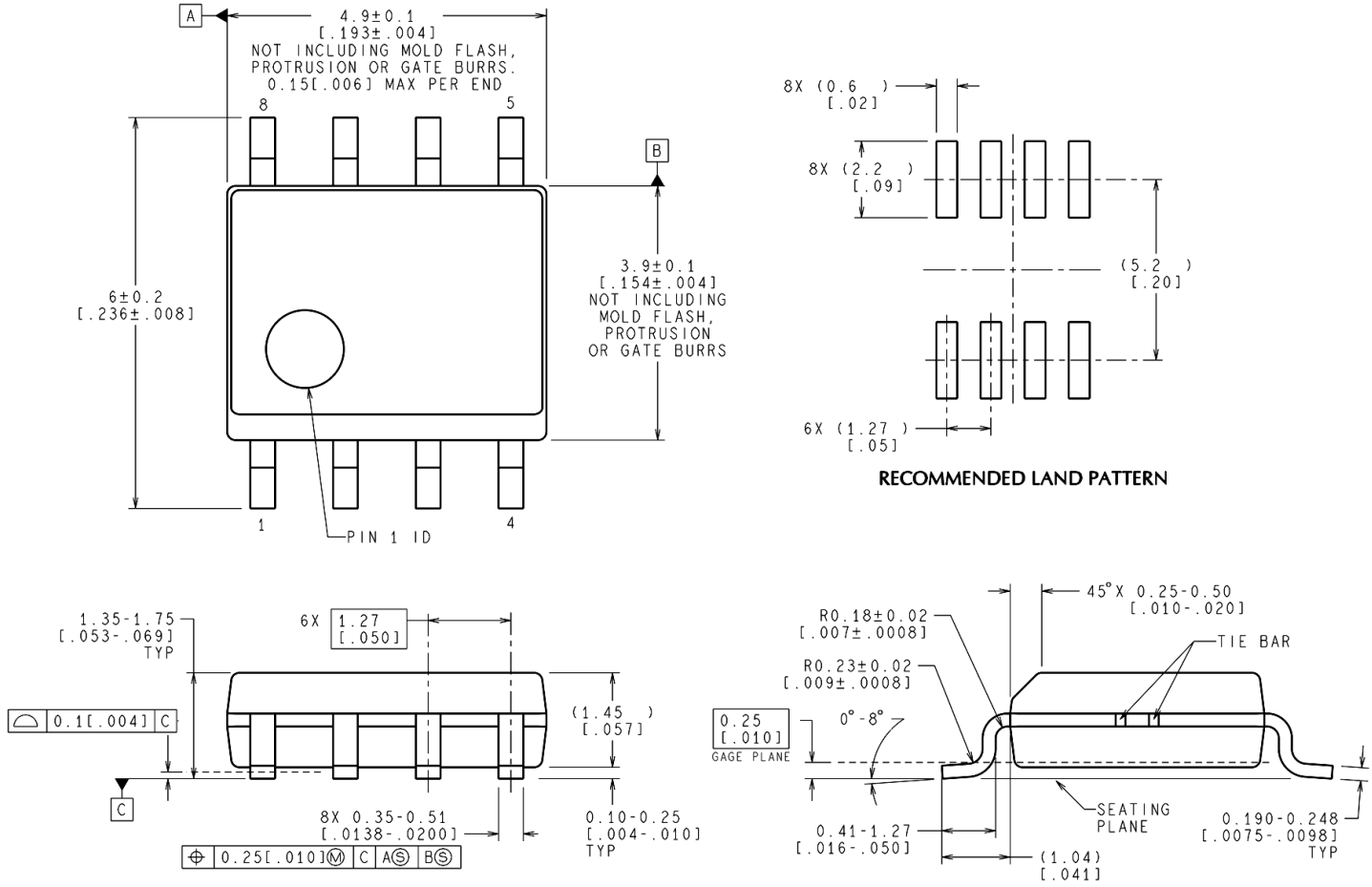
Figure 32 . Layout example for TF 2106 M (U 1) in a halfbridge, notice the bootstrap caps (CB1, CB2), VCC caps (C1 and C2), and bootstrap diode (DB1) adjacent to the IC.

Application Example



Package Dimensions (SOIC-8 N)

Please contact support@tfsemi.com for package availability.

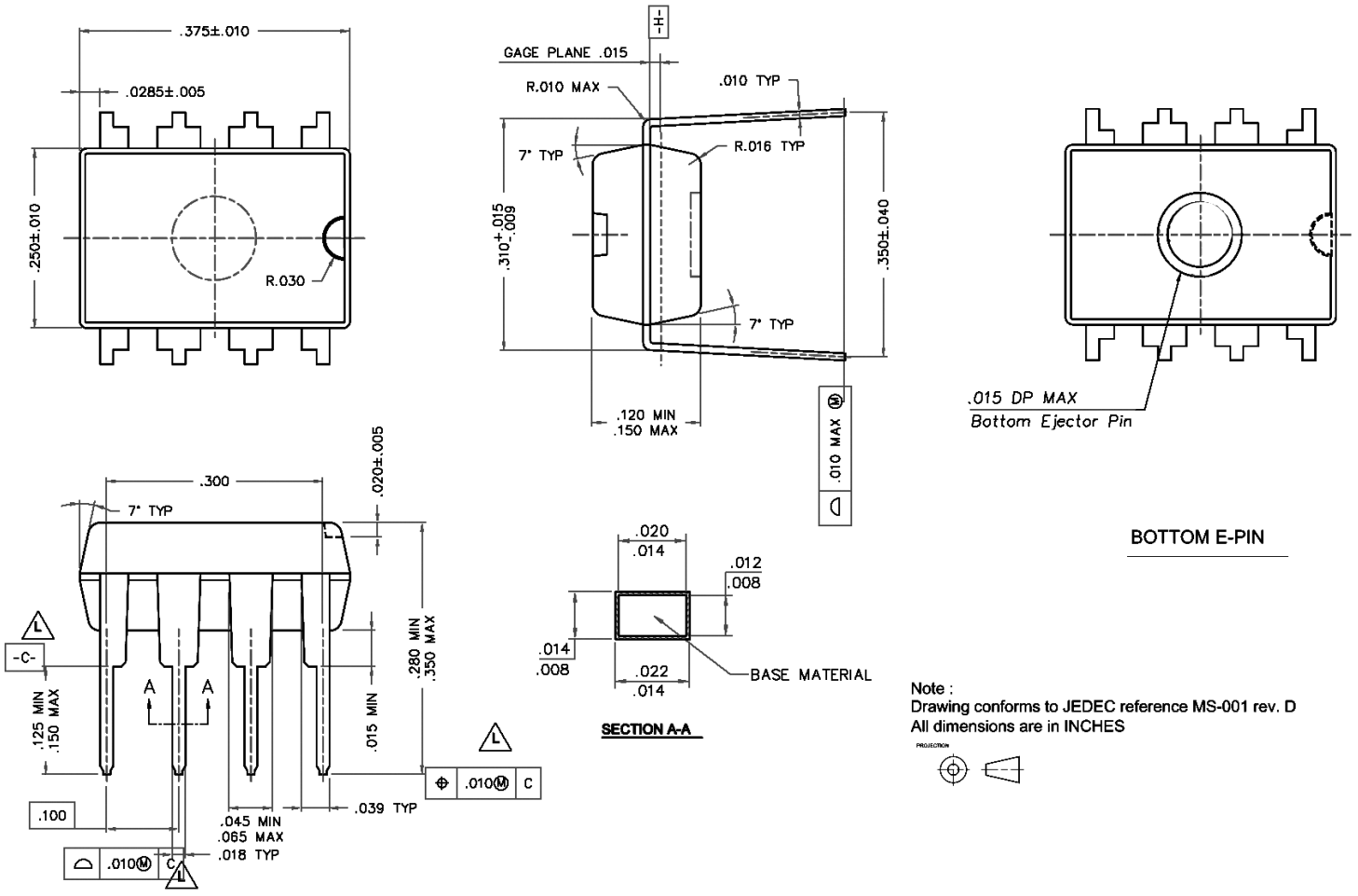


NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

Package Dimensions (PDIP-8)



Note :
Drawing conforms to JEDEC reference MS-001 rev. D
All dimensions are in INCHES

Revision History

Rev.	Change	Owner	Date
1.0	First release, final datasheet	Keith Spaulding	3/22/16
1.1	Text edit	Keith Spaulding	9/10/17
1.2	Add Note 5	Duke Walton	7/28/19

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