Advance Info

TF Semiconductor Solutions

TF2011M

High-Side and Low-Side Gate Driver

Features

- **Floating high-side driver in bootstrap operation to 200V**
- **Drives two N-channel MOSFETs or IGBTs in a half bridge configuration**
- **1.0A source / 1.0A sink output current capability**
- **Outputs tolerant to negative transients**
- **Wide low side gate driver supply voltage: 10V to 20V**
- **Logic input (HIN and LIN) 3.3V capability**
- **Schmitt triggered logic inputs with internal pull down**
- **Undervoltage lockout for high and low side drivers**
- **Extended temperature range: -40°C to +125°C**

Description

The TF2011M is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. TF Semiconductor's high voltage process enables the TF2011's high side to switch to 200V in a bootstrap operation.

The TF2011M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

The TF2011M is offered in a SOIC-8(N) package and operates over an extended -40 °C to +125 °C temperature range.

Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

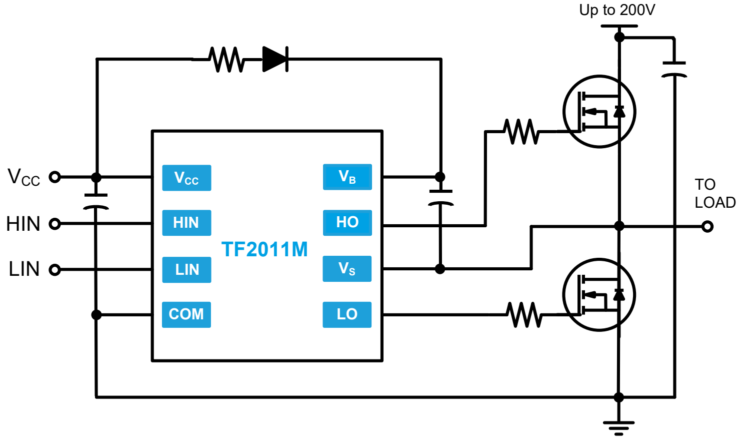
SOIC-8(N)

Ordering Information

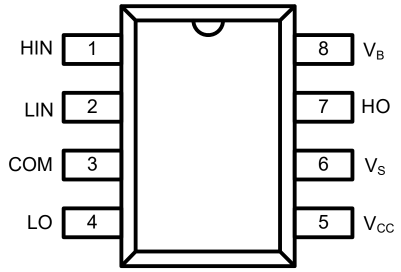
Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2011M-TAU	SOIC-8(N)	Tube / 100	TF YYWW TF2011M Lot ID
TF2011M-TAH	SOIC-8(N)	T&R / 2500	

Typical Application



Pin Diagrams

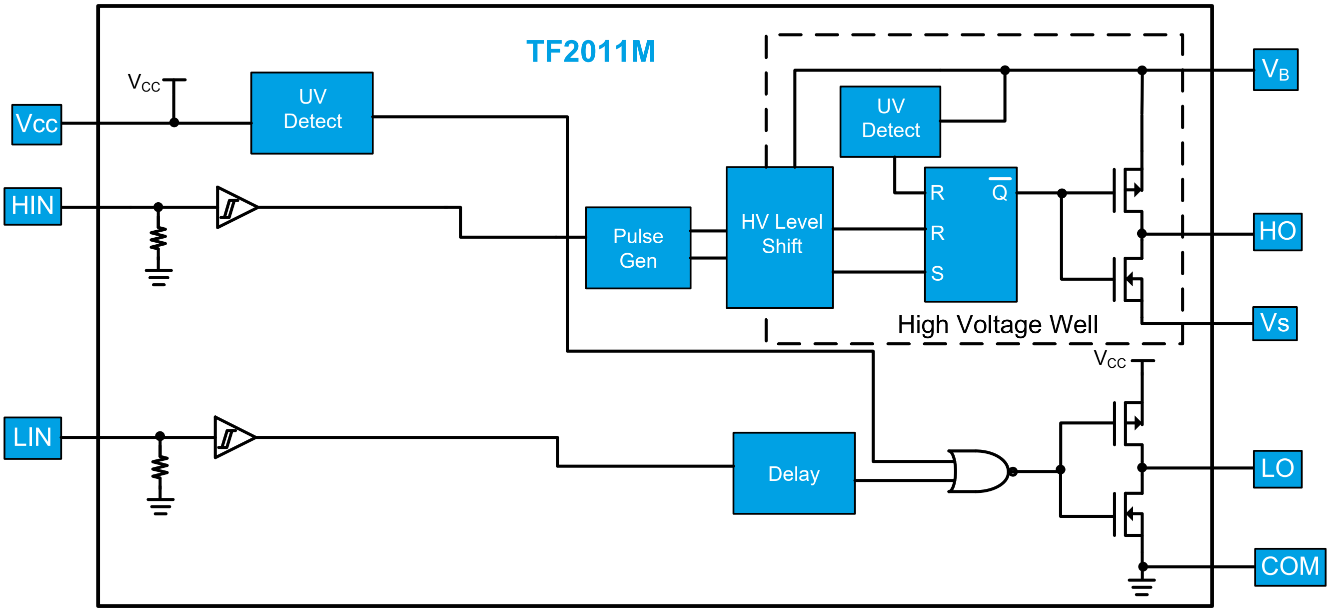


Top View: SOIC-8

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
HIN	1	Logic input for high-side gate driver output, in phase with HO.
LIN	2	Logic input for low-side gate driver output, in phase with LO.
COM	3	Low-side and logic return
LO	4	Low-side gate drive output
V_{CC}	5	Low-side and logic fixed supply
V_S	6	High-side floating supply return
HO	7	High-side gate drive output
V_B	8	High-side floating supply

Functional Block Diagram



Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage......................-0.3V to +224V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage...................V_S-0.3V to V_B+0.3V
dV_S/dt - Offset supply voltage transient..................................50 V/ns

V_{CC} - Low-side fixed supply voltage..............................-0.3V to +24V
V_{LO} - Low-side output voltage...................................-0.3V to V_{CC}+0.3V
V_{IN} - Logic input voltage (HIN and LIN)..................-0.3V to V_{CC} +0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-8...0.625W

SOIC-8(N) Thermal Resistance ***(NOTE2)***
θ_{JA}...200 °C/W

T_J - Junction operating temperature.......................................+150 °C
T_L - Lead Temperature (soldering, 10 seconds)......................+300 °C
T_{stg} - Storage temerature ....-55 to 150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	**Parameter**	**MIN**	**MAX**	**Unit**
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***	200	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (HIN and LIN)	0	5	V
T_A	Ambient temperature	-40	125	°C

NOTE3 *Logic operational for VS of -5V to +200V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10V to 20V ***NOTE5***	2.5			V
V_{IL}	Logic "0" input voltage				0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 0A			1.4	
V_{OL}	Low level output voltage, V_O	I_O = 20mA			0.2	
I_{LK}	Offset supply leakage current	VB = VS = 200V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V		60	150	
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V		120	240	µA
I_{IN+}	Logic "1" input bias current	V_{IN} = 5V		25	60	µA
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V			5.0	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		8.0	8.9	9.8	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		7.4	8.2	9.0	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		8.0	8.9	9.8	
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9.0	
I_{O+}	Output high short circuit pulsed current	V_O = 0V, PW ≤ 10 µs		1.0		A
I_{O-}	Output low short circuit pulsed current	V_O = 15V, PW ≤ 10 µs		1.0		

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are applicable to the two logic input pins: LIN and HIN. The V_O and I_O parameters are applicable to the respective output pins: HO and LO.*

NOTE5 *For optimal operation, it is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum with a pulse width of 240ns minimum.*

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, and T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propogation delay	V_S = 0V		120		ns
t_{off}	Turn-off propogation delay	V_S = 0V or 200V		120		
t_{DM}	Delay matching, HS & LS turn-on/off				20	
t_r	Turn-on rise time	V_S = 0V		30		
t_f	Turn-off fall time			30		

Timing Waveforms

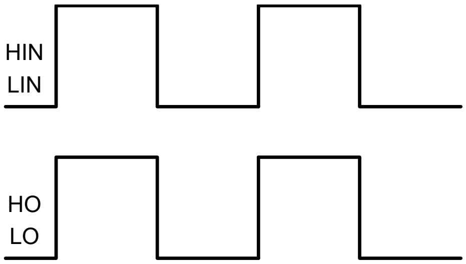


Figure 1. Input / Output Timing Diagram

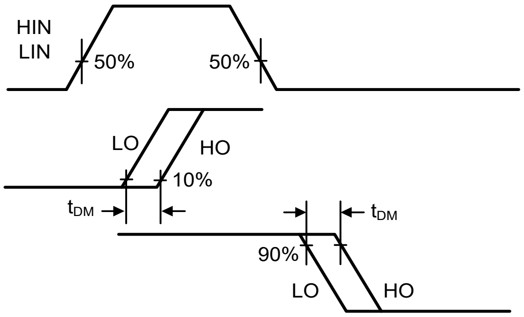


Figure 2. Delay Matching Waveform Definitions

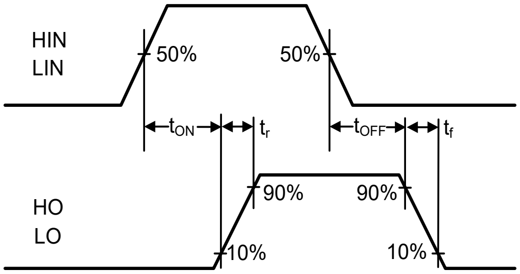


Figure 3. Switching Time Waveform Definitions

Application Information

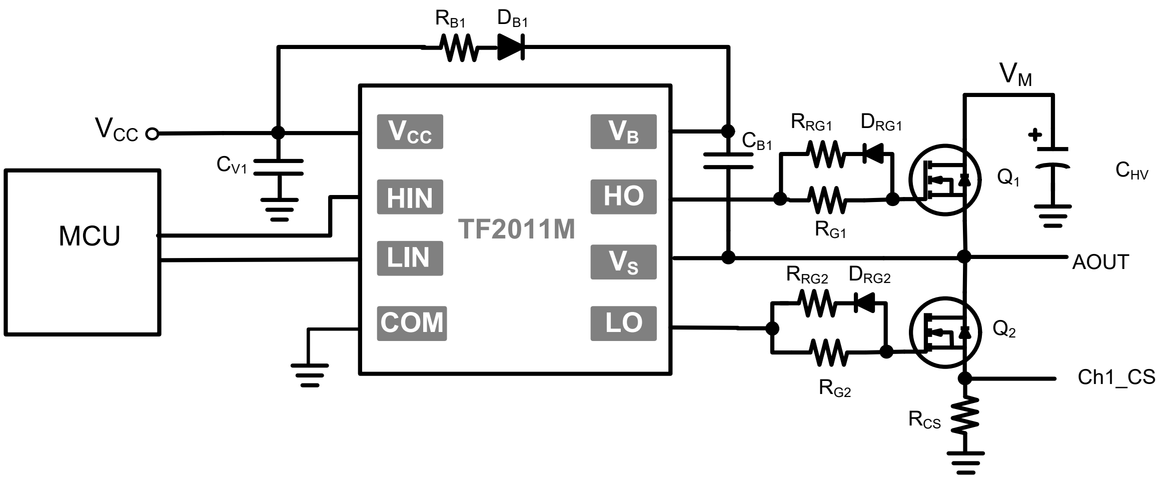


Figure 4. Single phase (of four) for Stepper motor driver application using the TF2011M

- RRG1 and RRG2 values are typically between 0Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

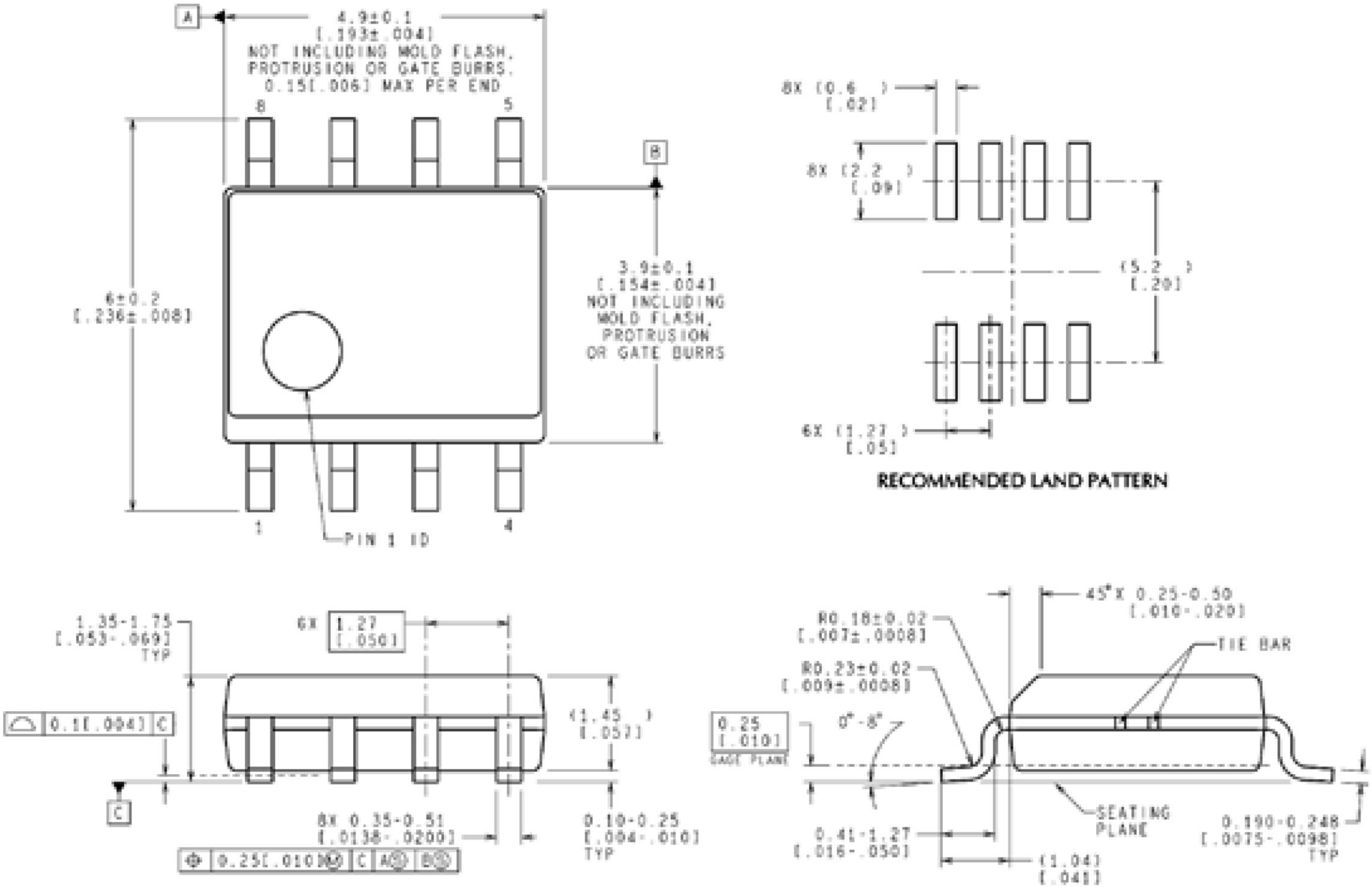
- RG1 and RG2 values are typically between 10Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.

- RB1 value is typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DB should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

- It is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum (for VDD=15V) with a minimum pulse width of 240ns.

Package Dimensions (SOIC-8 N)

Please contact support@tfsemi.com for package availability.



NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN [ ] FOR REFERENCE ONLY

Revision History

Rev.	Change	Owner	Date
1.0	Initial release Advance Info document	Duke Walton	3/13/2021
1.1	Add Applications Information page.	Keith Spaulding	9/1/2022

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