

# TF2183(4)M

## Half-Bridge Gate Driver

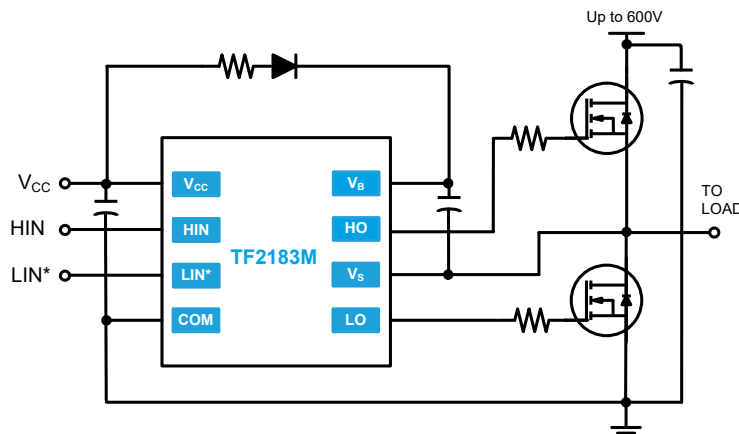
### Features

- Floating high-side driver in bootstrap operation to 600V
- Drives two N-channel MOSFETs or IGBTs in a half bridge configuration
- 1.9A source / 2.3A sink output current capability
- Outputs tolerant to negative transients
- Internal dead time of 400ns to protect MOSFETs
- Wide low side gate driver supply voltage: 10V to 20V
- Logic input (HIN and LIN\*) 3.3V capability
- Schmitt triggered logic inputs with internal pull down
- Undervoltage lockout for high and low side drivers
- Extended temperature range: -40°C to +125°C

### Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

### Typical Application



### Description

The TF2183(4)M is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. TF Semiconductor's high voltage process enables the TF2183(4)M's high side to switch to 600V in a bootstrap operation.

The TF2183(4)M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. TF2183(4)M has a fixed internal deadtime of 400ns (typical).

The TF2183M is offered in an SOIC-8(N) package and the TF21834M is offered in an SOIC-14(N) package and operates over an extended -40 °C to +125 °C temperature range.



SOIC-8(N)

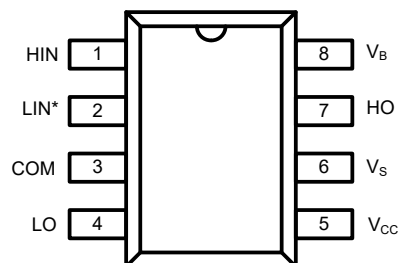


SOIC-14(N)

### Ordering Information

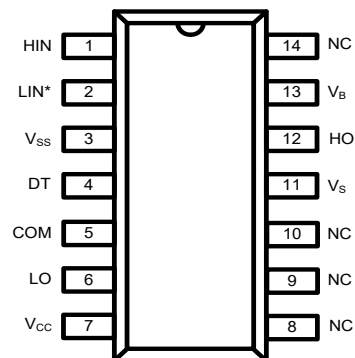
| PART NUMBER  | PACKAGE | PACK / Qty | MARK |                            |
|--------------|---------|------------|------|----------------------------|
|              |         |            | Year | Week                       |
| TF2183M-TAU  | SOIC-8  | Tube / 100 | TF   | YYWW<br>TF2183M<br>Lot ID  |
| TF2183M-TAH  | SOIC-8  | T&R / 2500 |      |                            |
| TF21834M-TUU | SOIC-14 | Tube / 100 | TF   | YYWW<br>TF21834M<br>Lot ID |
| TF21834M-TUH | SOIC-14 | T&R / 2500 |      |                            |

## Pin Diagrams



**Top View: SOIC-8**

**TF2183M**



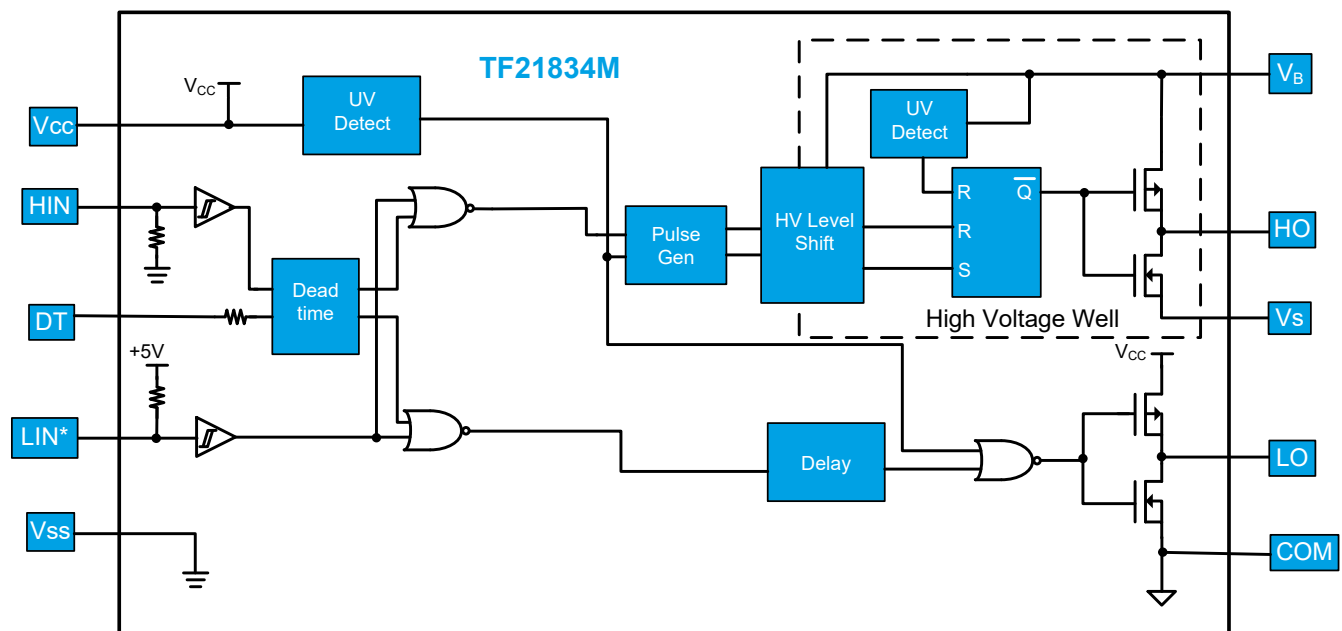
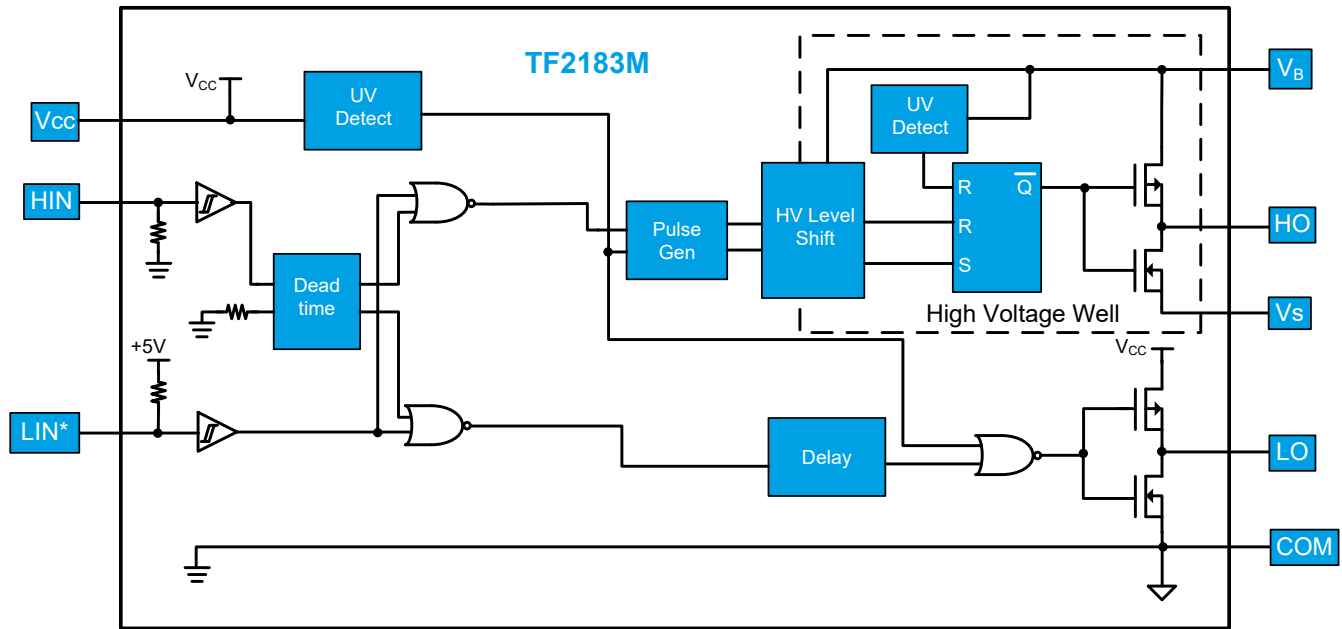
**Top View: SOIC-14**

**TF21834M**

## Pin Descriptions

| PIN NAME        | TF2183M Pin | TF21834M Pin | PIN DESCRIPTION  |
|-----------------|-------------|--------------|--|
| HIN             | 1           | 1            | Logic input for high-side gate driver, in phase with HO.     |
| LIN*            | 2           | 2            | Logic input for low-side gate driver, out of phase with LO.  |
| COM             | 3           | 5            | Low-side and logic return (TF2183M).                         |
| LO              | 4           | 6            | Low-side gate drive output.                                  |
| V <sub>CC</sub> | 5           | 7            | Low-side and logic fixed supply.                             |
| V <sub>S</sub>  | 6           | 11           | High-side floating supply return.                            |
| HO              | 7           | 12           | High-side gate drive output.                                 |
| V <sub>B</sub>  | 8           | 13           | High-side floating supply.                                   |
| V <sub>SS</sub> |             | 3            | Logic return.  |
| DT              |             | 4            | Programmable deadtime lead, set by external resistor to VSS. |

## Functional Block Diagrams



## Absolute Maximum Ratings (NOTE1)

$V_B$  - High side floating supply voltage.....-0.3V to +624V  
 $V_S$  - High side floating supply offset voltage... $V_B$ -24V to  $V_B$ +0.3V  
 $V_{HO}$ -Highside floating output voltage..... $V_S$ -0.3Vto $V_B$ +0.3V  
 $dV_S/dt$  - Offset supply voltage transient.....50V/ns

$V_{CC}$  - Low-side fixed supply voltage.....-0.3V to +24V  
 $V_{LO}$  - Low-side output voltage.....-0.3Vto $V_{CC}$ +0.3V  
 $V_{IN}$  - Logic input voltage (HIN and LIN\*).....-0.3V to  $V_{CC}$ +0.3V

**NOTE1** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$P_D$ - Package power dissipation at  $T_A \leq 25^\circ\text{C}$   
 SOIC-8.....0.625W  
 SOIC-14.....1.0W

SOIC-8(N) Thermal Resistance **(NOTE2)**  
 $\theta_{JA}$ .....200  $^\circ\text{C/W}$   
 SOIC-14(N) Thermal Resistance **(NOTE2)**  
 $\theta_{JA}$ .....120  $^\circ\text{C/W}$

$T_J$  - Junction operating temperature.....+150  $^\circ\text{C}$   
 $T_L$  - Lead Temperature (soldering, 10 seconds).....+300  $^\circ\text{C}$   
 $T_{stg}$  - Storage temperature .....-55 to 150  $^\circ\text{C}$

**NOTE2** When mounted on a standard JEDEC 2-layer FR-4 board.

## Recommended Operating Conditions

| Symbol   | Parameter                                  | MIN          | MAX        | Unit             |
|----------|--|--------------|------------|------------------|
| $V_B$    | High side floating supply absolute voltage | $V_S + 10$   | $V_S + 20$ | V                |
| $V_S$    | High side floating supply offset voltage   | <b>NOTE3</b> | 600        |                  |
| $V_{HO}$ | High side floating output voltage          | $V_S$        | $V_B$      |                  |
| $V_{CC}$ | Low side fixed supply voltage              | 10           | 20         |                  |
| $V_{LO}$ | Low side output voltage                    | 0            | $V_{CC}$   |                  |
| $V_{IN}$ | Logic input voltage (HIN and LIN*)         | 0            | 5          |                  |
| $V_{DT}$ | Programmable deadtime pin voltage          | $V_{SS}$     | $V_{CC}$   |                  |
| $V_{SS}$ | Logic ground (referenced to COM)           | -5           | 5          | $^\circ\text{C}$ |
| $T_A$    | Ambient temperature                        | -40          | 125        |                  |

**NOTE3** Logic operational for  $V_S$  of -5V to +600V.

**DC Electrical Characteristics** (NOTE4)

 $V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

| Symbol      | Parameter  | Conditions                              | MIN | TYP | MAX | Unit    |
|-------------|--|---|-----|-----|-----|---------|
| $V_{IH}$    | Logic "1" (HIN) and logic "0" (LIN*) input voltage     | $V_{CC} = 10V$ to $20V$<br><b>NOTES</b> | 2.5 |     |     | V       |
| $V_{IL}$    | Logic "0" (HIN) and logic "1" (LIN*) input voltage     |   |     |     | 0.8 |         |
| $V_{OH}$    | High level output voltage, $V_{BIAS} - V_O$            | $I_O = 0A$                              |     |     | 1.2 |         |
| $V_{OL}$    | Low level output voltage, $V_O$                        | $I_O = 20mA$                            |     |     | 0.1 |         |
| $I_{LK}$    | Offset supply leakage current                          | $V_B = V_S = 600V$                      |     |     | 50  | $\mu A$ |
| $I_{BSQ}$   | Quiescent $V_{BS}$ supply current                      | $V_{IN} = 0V$ or $5V$                   | 20  | 60  | 150 |         |
| $I_{CCQ}$   | Quiescent $V_{CC}$ supply current                      | $V_{IN} = 0V$ or $5V$                   | 0.4 | 1.6 | 2.0 | mA      |
| $I_{IN+}$   | Logic "1" input bias current                           | $HIN = 5V, LIN^* = 0V$                  |     | 25  | 60  | $\mu A$ |
| $I_{IN-}$   | Logic "0" input bias current                           | $HIN = 0V, LIN^* = 5V$                  |     |     | 1.0 |         |
| $V_{BSUV+}$ | $V_{BS}$ supply under-voltage positive going threshold |   | 8.0 | 8.9 | 9.8 | V       |
| $V_{BSUV-}$ | $V_{BS}$ supply under-voltage negative going threshold |   | 7.4 | 8.2 | 9.0 |         |
| $V_{CCUV+}$ | $V_{CC}$ supply under-voltage positive going threshold |   | 8.0 | 8.9 | 9.8 |         |
| $V_{CCUV-}$ | $V_{CC}$ supply under-voltage negative going threshold |   | 7.4 | 8.2 | 9.0 |         |
| $I_{O+}$    | Output high short circuit pulsed current               | $V_O = 0V, PW \leq 10\ \mu s$           | 1.4 | 1.9 |     | A       |
| $I_{O-}$    | Output low short circuit pulsed current                | $V_O = 15V, PW \leq 10\ \mu s$          | 1.7 | 2.3 |     |         |

**NOTE4** The  $V_{IH}$ ,  $V_{IL}$ , and  $I_{IN}$  parameters are applicable to the two logic input pins: HIN and LIN\*. The  $V_O$  and  $I_O$  parameters are applicable to the respective output pins: HO and LO

**NOTES** For optimal operation, it is recommended that the input pulse (to HIN and LIN\*) should have an amplitude of 2.5V minimum with a pulse width of 800ns minimum.

## AC Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000pF, and  $T_A$  = 25 °C, unless otherwise specified.

| Symbol    | Parameter  | Conditions                      | MIN | TYP | MAX | Unit    |
|-----------|--|---------------------------------|-----|-----|-----|---------|
| $t_{on}$  | Turn-on propagation delay                        | $V_S = 0V$                      |     | 180 | 270 | ns      |
| $t_{off}$ | Turn-off propagation delay                       | $V_S = 0V$ or 600V              |     | 220 | 330 |         |
| $t_{DM}$  | Delay matching                                   |                                 |     |     | 50  |         |
| $t_r$     | Turn-on rise time                                |                                 |     | 40  | 60  |         |
| $t_f$     | Turn-off fall time                               |                                 |     | 20  | 35  |         |
| $t_{DT}$  | Deadtime: $t_{DT LO-HO}$ & $t_{DT HO-LO}$        | $R_{DT} = 0\Omega$              | 280 | 400 | 520 | $\mu s$ |
|           |  | $R_{DT} = 200k\Omega$ (TF21834) | 4   | 5   | 6   |         |
| $t_{DTM}$ | Deadtime matching: $t_{DT LO-HO} - t_{DT HO-LO}$ | $R_{DT} = 0\Omega$              |     | 0   | 50  | ns      |
|           |  | $R_{DT} = 200k\Omega$ (TF21834) |     | 0   | 600 |         |

# Timing Waveforms

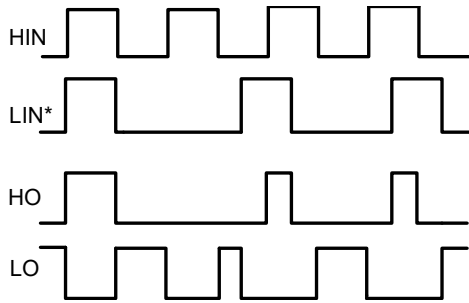


Figure 1. Input / Output Timing Diagram

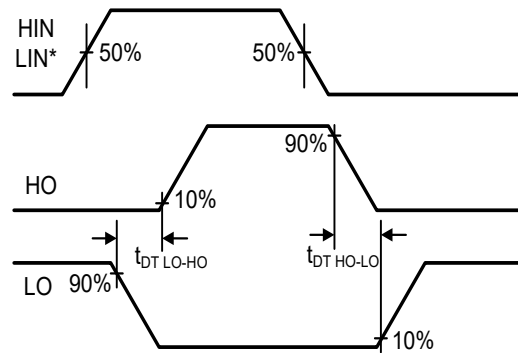


Figure 2. Deadtime Waveform Definitions

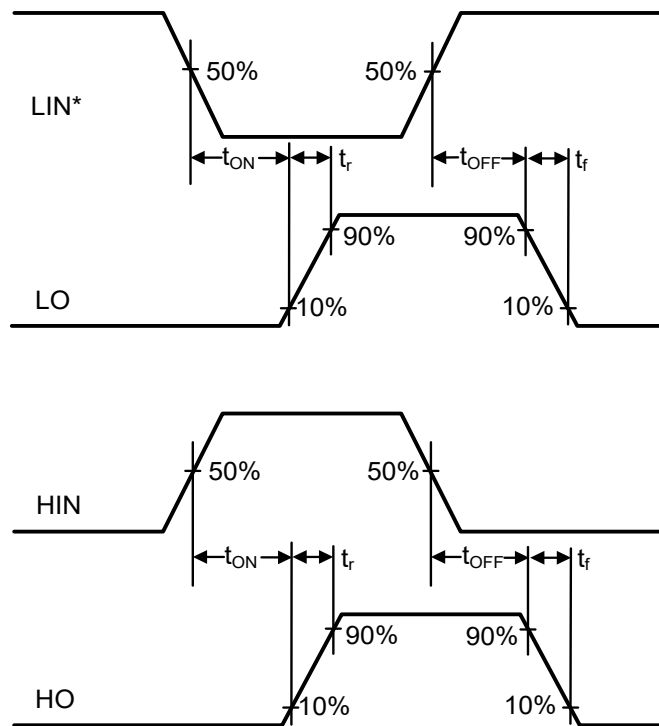
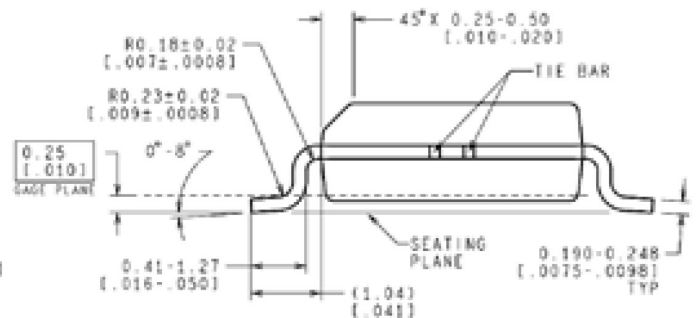
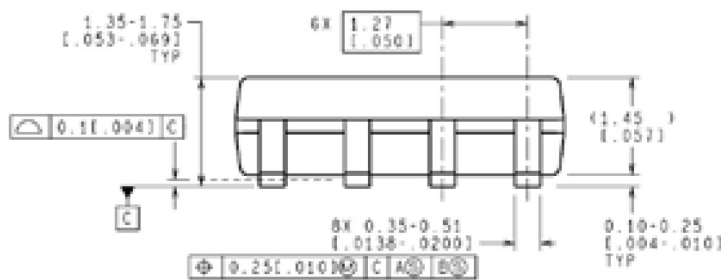
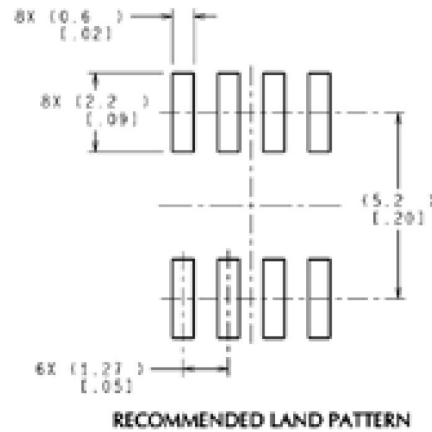
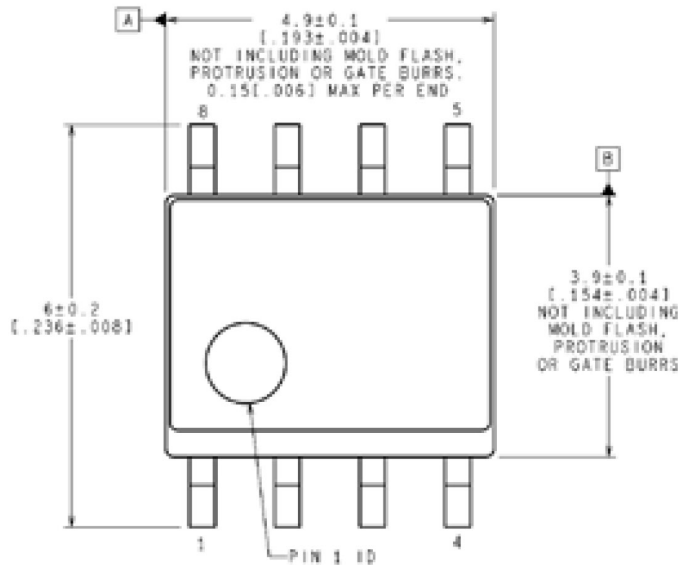


Figure 3. Switching Time Waveform Definitions

# Package Dimensions (SOIC-8 N)

Please contact support@tfsemi.com for package availability.



NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER  
VALUES IN [ ] ARE INCHES  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



## Revision History

| Rev. | Change                      | Owner           | Date      |
|------|-----------------------------|-----------------|-----------|
| 1.0  | First release, AI datasheet | Keith Spaulding | 7/15/2022 |

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