Advance Info

TF21844



Half-Bridge Gate Driver

Description

Features

- Floating high-side driver in bootstrap operation to 600V
- Drives two N-channel MOSFETs or IGBTs in a half-bridge configuration
- 1.4A source / 1.8A sink output current capability
- Outputs tolerant to negative transients
- Programmable dead time to protect MOSFETs
- Wide low-side gate driver supply voltage: 10V to 20V
- Wide logic supply voltage offset voltage: -5V to 5V
- Logic input (IN and SD*) 3.3V capability
- Schmitt triggered logic inouts with internal pull down
- Undervoltage lockout for high and low side drivers
- Extended temperature range:-40°C to +125°C

The TF21844 is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. TF Semiconductors's high voltage process enables the TF21844's high side to switch to 600V in a bootstrap operation.

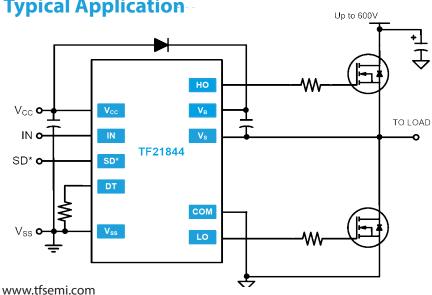
The TF21844 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. Programmable dead time, by an external resistor, provides more system level flexibility.

The TF21844 is offered in PDIP-14 and SOIC-14(N) packages. It operates over an extended -40 °C to +125 °C temperature range.



Ordering Information

		Y	ear Year VVeek VVeek
PART NUMBER	PACKAGE	PACK / Qty	MARK
TF21844-TUU		Tube / 50	TF21844
TF21844-TUH	SOIC-14(N)	T&R / 2500	Lot ID
TF21844-3BS	PDIP-14	Tube / 25	TF21844 Lot ID



Typical Application

Applications

DC-DC Converters

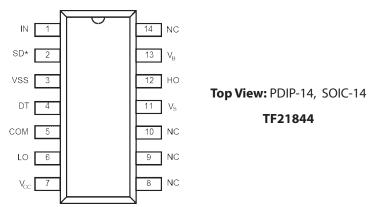
Class D Power Amplifiers

AC-DC Inverters Motor Controls

Rev. 1.2



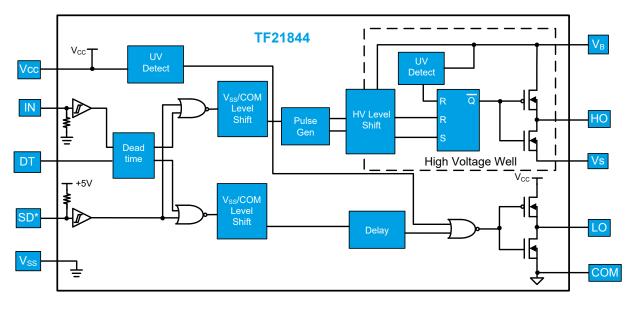




Pin Descriptions

PIN NAME	PIN DESCRIPTION
IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO (referenced to VSS).
SD*	Logic input for shutdown (referenced to VSS), enabled low.
V _{ss}	Logic ground
DT	Programmable deadtime lead, referenced to VSS.
СОМ	Low-side return
LO	Low-side gate drive output
V _{cc}	Low-side and logic fixed supply
V _B	High-side floating supply
НО	High-side gate drive output
V _s	High-side floating supply return

Functional Block Diagram





Absolute Maximum Ratings (NOTE1)

V _B - High side floating supply voltage	0.3V to +624V
V _s - High side floating supply offset voltage	V_{B} -24V to V_{B} +0.3V
V _{HO} - High side floating output voltage	V_{s} -0.3V to V_{B} +0.3V
dV _s /dt - Offset supply voltage transient	
V_{DT} - Programmable dead time pin voltageV	$V_{\rm ss}$ -0.3V to $V_{\rm cc}$ +0.3V

V _{cc} - Logic and Low side fixed supply voltage	e0.3V to +24V
V _{LO} - Low side output voltage	0.3V to V _{cc} +0.3V
V _{ss} - Logic supply offset voltage	V_{cc} -24V to V_{cc} +0.3V
V _{IN} - Logic input voltage (IN and SD*)V	$_{\rm cc}$ -0.3V to V _{cc} +0.3V

NOTE1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$P_{D}\text{-}$ Package power dissipation at $T_{A} \leq 25\ ^\circC$ SOIC-14
SOIC-14 Thermal Resistance (N0TE2)
θ _{JA} 120 °C/W
PDIP-14 Thermal Resistance (N0TE2)
θ_{JA}
T_{J} - Junction operating temperature+150 °C
T _L - Lead temperature (soldering, 10s) +300 °C
T_{stg} - Storage temperature range55 °C to +150 °C
NOTED When mounted on a standard IEDEC 2 Javar EP 4 heard

NOTE2 When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Symbol	Parameter	MIN	МАХ	Unit
V _B	High side floating supply absolute voltage	V _s + 10	V _s + 20	V
V _s	High side floating supply offset voltage	NOTE3	600	V
V _{HO}	High side floating output voltage	Vs	V _B	V
V _{cc}	Logic and Low side fixed supply voltage	10	20	V
V _{LO}	Low side output voltage	0	V _{cc}	V
V _{IN}	Logic input voltage (IN & SD*)	V _{ss}	5	V
V _{DT}	Programmable deadtime pin voltage	V _{ss}	V _{cc}	V
V _{ss}	Logic ground	-5	+5	V
T _A	Ambient temperature	-40	125	°C

NOTE3 Logic operational for VS of -5V to 600V. Logic state held for VS of -5V to VBS.



TF21844

DC Electrical Characteristics (NOTE4)

 $V_{\text{BIAS}}(V_{\text{CC}},V_{\text{BS}})$ = 15V, V_{SS} = COM, and T_{A} = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	ТҮР	MAX	Unit
V _{IH}	Logic "1" input voltage for HO & logic "0" for LO		2.5			
V _{IL}	Logic "0" input voltage for HO & logic "1" for LO	V _{cc} = 10 V to 20 V <i>Note5</i>			0.8	V
$V_{\text{SD, TH+}}$	SD* input poitive going threshold		2.5			
V _{SD, TH-}	SD* input negative going threshold				0.8	
V _{OH}	High level output voltage, V _{BIAS} - V _o	$I_{o} = 0A$			1.4	
V _{OL}	Low level output voltage, V _o	I _o =20mA			0.2	
I _{LK}	Offset supply leakage current	VB = VS = 600V			50	_
I _{BSO}	Quiescent V _{BS} supply current	$V_{IN} = 0V \text{ or } 5V$	20	60	150	μA
I _{ccq}	Quiescent V _{cc} supply current	$V_{IN} = 0V \text{ or } 5V$	0.4	1.0	1.8	mA
I _{IN+}	Logic "1" input bias current	IN= 5V, SD* = 0V		25	60	
I _{IN-}	Logic "0" input bias current	IN= 0V, SD* = 5V			1.0	μΑ
$V_{\rm BSUV+}$	V _{BS} supply under-voltage positive going threshold		8	8.9	9.8	
V _{BSUV-}	V _{BS} supply under-voltage negative going threshold		7.4	8.2	9	v
V_{CCUV+}	V _{cc} supply under-voltage positive going threshold		8	8.9	9.8	
V _{ccuv-}	V _{cc} supply under-voltage negative going threshold		7.4	8.2	9.0]
I _{O+}	Output high short circuit pulsed current	$V_{o} = 0V, PW \le 10 \ \mu s$	1.4	1.9		
I _{O-}	Output low short circuit pulsed current	$V_0 = 15V$, PW $\leq 10 \ \mu s$	1.7	2.3		A

Note4 The $V_{_{M}}V_{_{TH}}I_{_{N}}$ parameters are referenced to $V_{_{SS}}$ and are applicable to the two logic input pins: IN and SD*. The $V_{_{0}}$ and $I_{_{0}}$ parameters are referenced to COM and are applicable to the respective output pins: HO and LO.

Note5 For optimal operation, it is recommended that the input pulse (to IN and SD*) should have an amplitude of 2.5V minimum with a pulse width of 800ns minimum





AC Electrical Characteristics

$V_{BIAS}(V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_{L} = 1000 \text{ pF}, \text{ and } T_{A} = 25 ^{\circ}C \text{ unless othe}$	erwise specified.
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Symbol	Parameter	Conditions	MIN	ТҮР	MAX	Unit
t _{on}	Turn-on propagation delay	$V_s = 0V$		680	900	
t _{off}	Turn-off propagation delay	$V_{s} = 0 V \text{ or } 600 V$		270	400	
t _{sD}	Shut-down propagation delay			180	270	
t _{dm on}	Delay matching, HS & LS turn-on				90	ns
t _{dm off}	Delay matching, HS & LS turn-off				40	
t _r	Turn-on rise time	$V_s = 0V$		40	60	
t _f	Turn-off fall time			20	35	
		$R_{DT} = 0\Omega$	280	400	520	ns
t _{DT}	Deadtime: t _{DT LO-HO} & t _{DT HO-LO}	$R_{DT} = 200 k\Omega$	4	5	6	μs
		$R_{DT} = 0\Omega$		0	50	
t _{MDT}	Deadtime matching = $t_{DT LO-HO} - t_{DT HO-LO}$	$R_{DT} = 200 k\Omega$		0	600	ns





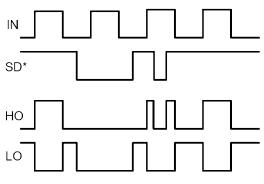


Figure 1. Input / Output Timing Diagram

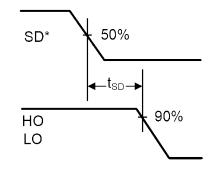
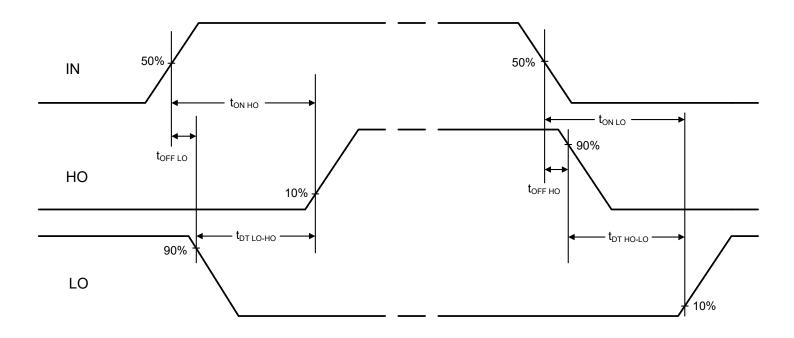
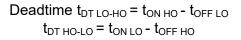


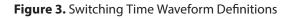
Figure 2. Shutdown Waveform Definitions





Deadtime matching $t_{\text{MDT}} = t_{\text{DT LO-HO}} - t_{\text{DT HO-LO}}$

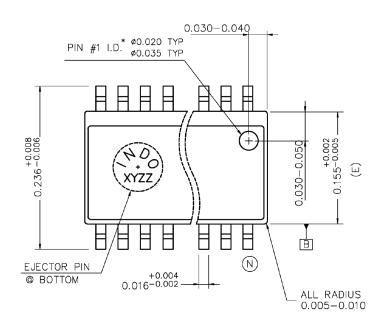
 $\begin{array}{l} \text{Delay matching} \\ t_{\text{DM OFF}} = t_{\text{OFF LO}} - t_{\text{OFF HO}} \\ t_{\text{DM ON}} = t_{\text{ON LO}} - t_{\text{ON HO}} \end{array}$

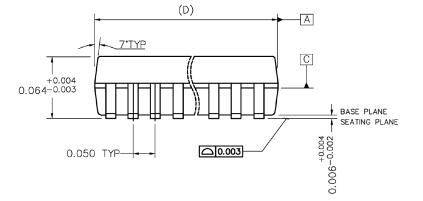




Package Dimensions (SOIC-14)

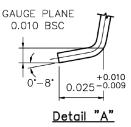
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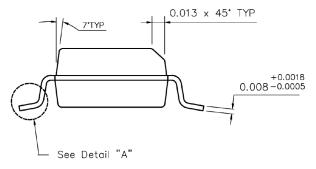


ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED NOTES:

- 1. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 6 MILS PER SIDE.
- 2. "N" IS THE NUMBER OF TERMINAL POSITIONS.
- 3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 3 MIL! (© SEATING PLANE) OUTGOING ASSEMBLY & 4 MILS AFTER TEST.
- 4. THE BOTTOM PACKAGE LEAD SIDE MAY BE BIGGER THAN THE TOP PACKAGE LEAD SIDE BY 4 MILS (2 MILS PER SIDE). BOTTOM PACKAGE DIMENSION SHALL FOLLOW DIMENSION STATED IN THIS DRAWING.
- 5. THE BOTTOM EJECTOR PIN CONTAINS COUNTRY OF ORIGIN "INDO" AND MOLD ID. (REFER TO TABLE FOR OPTION).
- 6. THIS DRAWING CONFORMS TO JEDEC REF. MS-012 REV. E



				-		MGP	MOLD	
	N		D VARIATION		STAN	IDARD	MATRIX	
	R	MIN	NOM	мах	PIN 1 I.D.	EJECT PIN	PIN 1 I.D.	EJECT PIN
	08	0.189	0.193	0.196	N/A		YES	YES
	14	0.337	0.339	0.344	YES	NO	YES	YES
⋒	16	0.386	0.390	0.393	N	/A	YES	YES

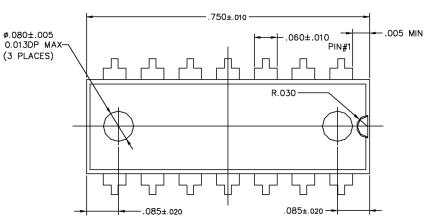


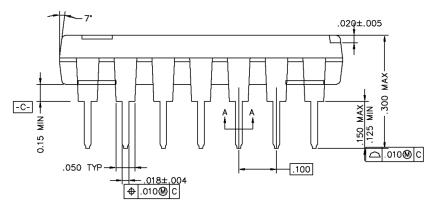


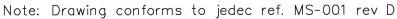


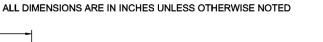
Package Dimensions (PDIP-14)

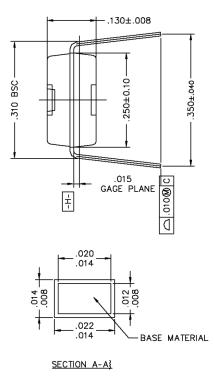
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Rev.	Change	Owner	Date
1.0	First release, Advance Info ds	Keith Spaulding	7/8/2014
1.1	Text edit	Keith Spaulding	7/17/2017
1.2	Add Note 5	Duke Walton	7/22/2019

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