

# THC63LVD1027

Dual Link LVDS Repeater

#### **General Description**

The THC63LVD1027 LVDS(Low Voltage Differential Signaling) repeater is designed to support pixel data transmission between Host and Flat Panel Display up to WUXGA resolution.

THC63LVD1027 receives the dual link LVDS data streams and transmits the LVDS data through various line rate conversion modes, Dual Link Input / Dual Link Output, Single Link Input / Dual Link Output, and Dual Link Input / Single Link Output.

#### **Features**

- 30bits/pixel dual link LVDS Receiver
- 30bits/pixel dual Link LVDS Transmitter
- Operating Temperature Range : -40°C~85°C
- Wide LVDS input skew margin: ± 480ps at 75MHz
- Accurate LVDS output timing: ± 250ps at 75MHz
- Reduced swing LVDS output mode supported to suppress the system EMI

• Various line rate conversion modes supported Dual link input / Dual link output [clkout=1x clkin] Single link input / Dual link output [clkout=1/2x clkin] Dual link input / Single link output [clkout=2x clkin]

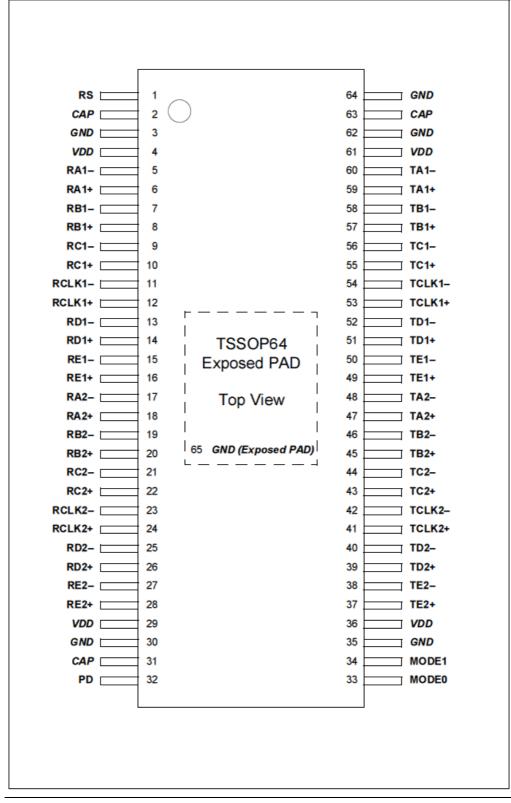
- Distribution (signal duplication) mode supported
- Power down mode supported
- 3.3V single voltage power supply
- No external components required for PLLs
- 64pin TSSOP with Exposed PAD (0.5mm lead pitch)

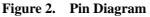
#### **Block Diagram** Dual In / Dual Out Mode THC63LVD1027 THine® THC63LVD1027 85MHz 85MH LVDS-Rx LVDS-Tx 30bit Date 30bit Data Distribution Mode Serialize e-Seriali THC63LVD1027 LVDS LVDS 85MH7 85MHz 1st Link 1st Link Inter-Link Multiplex 85MH: 8 PLL Clock De-Multi plex PLL Single In / Dual Out Mode THC63LVD1027 PLL Cloc Clock 67 5MHz 135MHz LVDS LVDS 67.5MHz 2nd Link 2nd Link LVDS-Rx LVDS-Tx 30bit Data 30bit Data Dual In / Single Out Mode Serialize Seriali LDO THC63LVD1027 Regulato 85MHz 42.5MHz 42.5MHz 3.3v Power Supp D ng Capacito

Figure 1. Block Diagram



#### Pin Diagram







### Pin Description

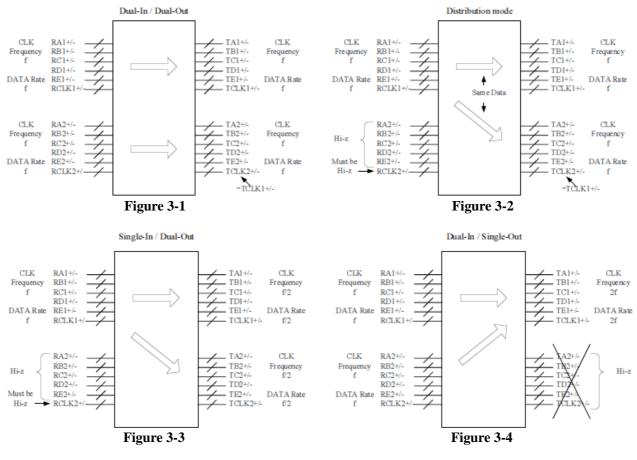
Pin Name	Direction	Туре	Description				
RA1+/-	2	-310	LVDS data input for channel A of 1st Link				
RB1+/-	-		LVDS data input for channel B of 1st Link				
RC1+/-			LVDS data input for channel C of 1st Link				
RD1+/-	-		LVDS data input for channel D of 1st Link				
RE1+/-	-		LVDS data input for channel E of 1st Link				
RCLK1+/-	Input LVDS Output		LVDS data input for channel E of 1st Link				
RA2+/-		LVDS data input for channel A of 2nd Link					
RB2+/-	Input		LVDS data input for channel B of 2nd Link				
RC2+/-	-		LVDS data input for channel C of 2nd Link				
RC2+/- RD2+/-	-		LVDS data input for channel D of 2nd Link				
RE2+/-	-		LVDS data input for channel E of 2nd Link				
RCLK2+/-							
KULK2+/-			<b>LVDS clock input for 2nd Link</b> In Distribution and Single-in/Dual-out mode,RCLK2+/- must be Hi-Z.				
		LVDS	(See "Mode selection" below in this page.)				
TA1+/-			LVDS data output for channel A of 1st Link				
TB1+/-			LVDS data output for channel B of 1st Link				
TC1+/-			LVDS data output for channel C of 1st Link				
TD1+/-			LVDS data output for channel D of 1st Link				
TE1+/-	Output		LVDS data output for channel E of 1st Link				
TCLK1+/-			LVDS clock output for 1st Link				
TA2+/-			LVDS data output for channel A of 2nd Link				
TB2+/-			LVDS data output for channel B of 2nd Link				
TC2+/-			LVDS data output for channel C of 2nd Link				
TD2+/-			LVDS data output for channel D of 2nd Link				
TE2+/-			LVDS data output for channel E of 2nd Link				
TCLK2+/-			LVDS clock output for 2nd Link				
PD			Power Down				
			H: Normal operation				
	-		L: Power down state, all LVDS output signals turn to Hi-Z				
RS			LVDS output swing level selection H: Normal swing				
			L: Reduced swing				
MODE1			Mode selection				
MODE0	Input	LV-TTL	MODE1 MODE0 RCLK2+/- Description				
-			L L Clkin Dual-in/Dual-out mode				
			L L Hi-Z Distribution mode				
			H         L         Hi-Z         Single-in/Dual-out mode           L         H         Clkin         Dual-in/Single-out mode				
			H H - Reserved				
			In Distribution and Single-in/Dual-out mode, RCLK2+/- must be Hi-Z.				
VDD			3.3V power supply pins				
GND	Power	-	Ground pins (Exposed PAD is also Ground)				
САР			Decoupling capacitor pins				
			These pins should be connected to external decoupling capacitors(Ccap).				
			Recommended Ccap is $0.1\mu$ F + $0.01\mu$ F.				



#### Mode Setting

Table 2. Mode Setting						
Input/Output	RCLK2+/-	MODE1	MODE0			
		(Input mode)	(Output mode)			
		H: Single	H: Single			
		L: Dual	L: Dual			
Dual-In/Dual-Out	CLK in	L	L			
(Fig.3-1,14-1)						
Distribution	Hi-Z	L	L			
(Fig.3-2,14-2)						
Single-In/Dual-Out	Hi-Z	Н	L			
(Fig.3-3,14-3)						
Dual-In/Single-Out	CLK in	L	Н			
(Fig.3-4,14-4)						
Reserved	-	Н	Н			

#### Signal Flow for Each Setting





#### Output Control / Fail Safe

THC63LVD1027 has a function to control output depending on LVDS input condition.

PD	RCLK1+/-	RCLK2+/-	Output
L	*	*	All Hi-Z
Н	Hi-Z	*	All Hi-Z
Н	CLK in	CLK in	Refer to p.4 Mode Setting #
Н	CLK in	Hi-Z	Refer to p.4 Mode Setting #

#### Table 3. Output Control

\*: Don't care

#: If a particular input data pair is Hi-Z, the corresponding output data become L according to LVDS DC spec.

For fail-safe purpose, all LVDS input pins are connected to VDD via resistance for detecting Hi-Z state.

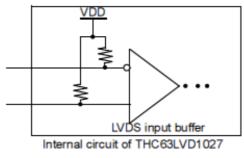


Figure 4. Fail Safe Circuit



### Absolute Maximum Ratings

Table 4	Absolute	Maximum	Rating
	Absolute	ViaAmum	Naung

		-	
Parameter	Min	Max	Unit
Power Supply Voltage	-0.3	+4.0	V
LVDS Input Voltage	-0.3	V <sub>DD</sub> +0.3	V
Junction Temperature	-	125	°C
Storage Temperature	-55	125	°C
Reflow Peak Temperature / Time	-	260 / 10sec	°C
Maximum Power Dissipation @+25°C	-	2.5	W

### **Operating Conditions**

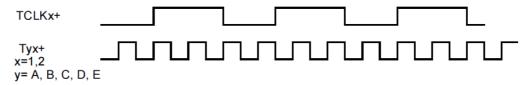
Table 5. Operating Condition

Symbol	Paramete	Min	Тур	Max	Unit		
Та	Operating Ambient 7	-40	25	+85	°C		
V <sub>DD</sub>	Power Supply Voltage		3.0	3.3	3.6	V	
	Dual-In/Dual-Out	Input	20	-	85	MHz	
	Dual-III/Dual-Out	Output	20	-	85	MITZ	
	Distribution	Input	20	-	85	MHz	
Б	Distribution	Output	20	-	85	MITZ	
<b>F</b> <sub>clk</sub>	Single In/Duel Out	Input	40	-	135	MHz	
	Single-In/Dual-Out	Output	20	-	67.5	MITZ	
	Dual In/Single Out	Input	20	-	42.5	MHz	
	Dual-In/Single-Out	Output	40	-	+85 3.6 85 85 85 85 135 67.5	IVITIZ	

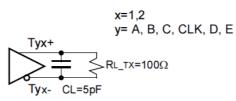


### Power Consumption

		Tab	le 6. Power Cons	sumption				
Symbol	Parameter		Conditions		Min	Тур.	Max	Unit
			CLKIN=40MHz		-	-	265	
		Dual-In/Dual-Out	CLKIN=65MHz		-	-	305	
		Duai-In/Duai-Out	CLKIN=75MHz		-	-	325	mA
			CLKIN=85MHz		-	-	340	
			CLKIN=40MHz		-	-	215	
		Distribution	CLKIN=65MHz		-	-	235	
		Distribution	CLKIN=75MHz	$R_{L Tx} = 100\Omega$	-	-	245	mA
	Operating Current		CLKIN=85MHz	L_IX -	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			
Ŧ	(Worst Case Pattern)		CLKIN=40MHz	CL=5pF RS=VDD	-	-	175	-
ICCW	(Worst Case Pattern)		CLKIN=65MHz		-	-	190	
	Fig 5.		CLKIN=75MHz		$\Omega = \frac{-}{-} \frac{265}{305}$ $- \frac{-}{305}$ $- \frac{-}{325}$ $- \frac{-}{340}$ $- \frac{-}{215}$ $- \frac{-}{235}$ $- \frac{-}{245}$ $- \frac{-}{260}$ $- \frac{-}{175}$ $- \frac{-}{190}$ $- \frac{-}{200}$ $- \frac{-}{210}$ $- \frac{-}{230}$ $- \frac{-}{250}$ $- \frac{-}{215}$ $- \frac{-}{245}$ $- \frac{-}{245}$ $- \frac{-}{260}$	mA		
		Single-In/Dual-Out	CLKIN=85MHz	Fig 6.	-	-	210	
			CLKIN=112MHz	_	-	-	230	1
			CLKIN=135MHz		-	-	250	
			CLKIN=20MHz		-	-	215	
		Dual In Sinala Out	CLKIN=32.5MHz		-	-	235	mA
		Dual-In/Single-Out	CLKIN=37.5MHz		-	-	245	
			CLKIN=42.5MHz		-	-	260	
I <sub>CCS</sub>	Power Down Current	-	-	-	-	-	8	mA







LVDS Output Load

Figure 6. LVDS Output Load



### **Electrical Characteristics**

#### **DC Specifications**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CAP</sub>	Capacitor pin appearance voltage	C <sub>CAP</sub> =0.1µF	-	1.8	-	V
V <sub>IL</sub>	LV-TTL Input Low Voltage	-	GND	-	0.8	V
V <sub>IH</sub>	LV-TTL Input High Voltage	-	2.0	-	VDD	V
I <sub>IN_TTL</sub>	LV-TTL Input Leakage Current	-	-4	-	+4	μΑ

#### Table 7. DC Specifications

### **LVDS Receiver DC Specifications**

#### Table 8. LVDS Receiver DC Specifications

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>IN_RX</sub>	LVDS-Rx Input Voltage Range	-	0.3	-	2.1	17
V <sub>IC_RX</sub>	LVDS-Rx Common Voltage	-	0.6	1.2	1.8	V
V <sub>TH_RX</sub>	LVDS-Rx Differential High Threshold	N 1 OV	-	-	+100	
V <sub>TL_RX</sub>	LVDS-Rx Differential Low Threshold	$V_{IC_{RX}} = 1.2V$	-100	-	-	mV
V <sub>ID_RX</sub>	LVDS-Rx Differential Input Voltage	-	100	-	600	
		PD=VDD	-0.3	-	+0.3	mA
I <sub>IN_RX</sub>	LVDS-Rx Input Leakage Current	PD=GND Vin=GND or VDD	-10	-	+10	μΑ

### LVDS Transmitter DC Specifications

#### **Table 9. LVDS Transmitter DC Specifications**

Symbol	Parameter	(	Min	Тур	Max	Unit		
V <sub>OC_TX</sub>	LVDS-Tx Common Voltage		-	1.125	1.25	1.375	v	
$\Delta V_{OC_TX}$	Change in VOC between complementary output states	л	-	-	-	35	mV	
157	LVDS-Tx Differential	$R_{L_{TX}} =$	Normal Swing	250	350	450	- mV	
V <sub>OD_TX</sub>	Output Threshold	100Ω	Reduced Swing	100	200	300		
$\Delta V_{OD_TX}$	Change in VOD between complementary output states		-	-	-	35	mV	
I <sub>OS_TX</sub>	LVDS-Tx Output Short Current	V <sub>DD</sub> =3.3V	V <sub>out</sub> =GND	-24	-	-	mA	
I <sub>OZ_TX</sub>	LVDS-Tx Output Tri-state Current	PD=GND	V <sub>out</sub> =GND to VDD	-10	-	+10	μΑ	



### **AC Specifications**

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
t <sub>LT</sub>	Phase Lock Loop Set Time (Fig 7.)	-	-	-	-	10	ms
		Dual-In/Dual-Out	CLKIN=75MHz	9t <sub>RCP</sub> +3	9t <sub>RCP</sub> +5	9t <sub>RCP</sub> +7	
	Data Latency (Fig 8.)	Distribution	CLKIN=75MHz	9t <sub>RCP</sub> +3	9t <sub>RCP</sub> +5	9t <sub>RCP</sub> +7	
t <sub>DL</sub>		Single-In/Dual-Out	CLKIN=75MHz	(11+2/7)t <sub>RCP</sub> +3	(11+2/7)t <sub>RCP</sub> +5	(11+2/7)t <sub>RCP</sub> +7	ns
		Dual-In/Single-Out	CLKIN=37.5MHz	(11+2/7)t <sub>RCP</sub> +3	(11+2/7)t <sub>RCP</sub> +5	(11+2/7)t <sub>RCP</sub> +7	
t <sub>DEH</sub>	DE Input High Time (Fig 9.)		-	2t <sub>RCP</sub>	-	-	
t <sub>DEL</sub>	DE Input Low Time (Fig 9.)	Single-In/Dual-Out	-	2t <sub>RCP</sub>	-	-	ns
t <sub>DEINT</sub>	DE Input Period (Fig 9.)		-	4t <sub>RCP</sub>	Must be 2n t <sub>RCP</sub> (n=integer)	-	

#### Table 10. AC Specifications

### AC Timing Diagrams

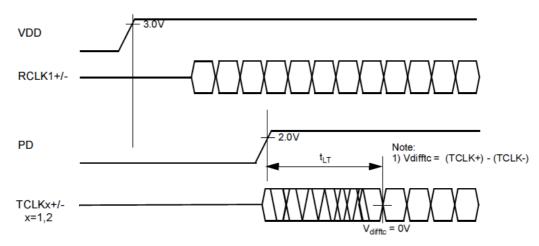


Figure 7	. Phase	Lock	Loop	Set	Time
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#### AC Timing Diagrams(Continued)

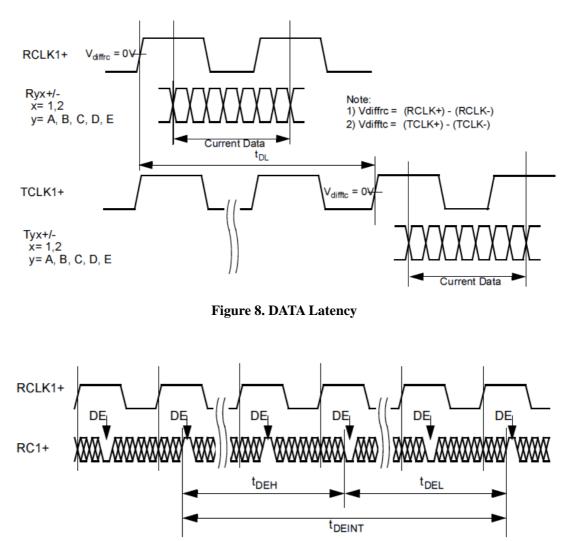


Figure 9. Single Link Input / Dual Link Output Mode RC1(DE) Input Timing



### LVDS Receiver AC Specifications

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>RCP</sub>	LVDS Clock Period	-	7.4	-	50	
t <sub>RCH</sub>	LVDS Clock High Duration	-	$2/7t_{RCP}$	$4/7t_{RCP}$	5/7t <sub>RCP</sub>	ns
t <sub>RCL</sub>	LVDS Clock Low Duration	-	$2/7t_{RCP}$	$3/7t_{RCP}$	5/7t <sub>RCP</sub>	
		CLKIN=75MHz <sup>(1)</sup>	480	-	-	
t <sub>RSUP</sub>	LVDS Data Input Setup Margin	CLKIN=112MHz <sup>(1)</sup>	250	-	-	ps
		CLKIN=135MHz <sup>(1)</sup>	220	-	-	
		CLKIN=75MHz <sup>(1)</sup>	480	-	-	
t <sub>RHLD</sub>	LVDS Data Input Hold Margin	CLKIN=112MHz <sup>(1)</sup>	250	-	-	ps
		CLKIN=135MHz <sup>(1)</sup>	220	-	-	
t <sub>RIP6</sub>	LVDS Data Input Position 6	-	2/7t <sub>RCP</sub> -t <sub>RHLD</sub>	$2/7t_{RCP}$	$2/7t_{RCP}+t_{RSUP}$	
t <sub>RIP5</sub>	LVDS Data Input Position 5	-	3/7t <sub>RCP</sub> -t <sub>RHLD</sub>	3/7t <sub>RCP</sub>	3/7t <sub>RCP</sub> +t <sub>RSUP</sub>	
t <sub>RIP4</sub>	LVDS Data Input Position 4	-	4/7t <sub>RCP</sub> -t <sub>RHLD</sub>	4/7t <sub>RCP</sub>	$4/7t_{RCP}+t_{RSUP}$	
t <sub>RIP3</sub>	LVDS Data Input Position 3	-	5/7t <sub>RCP</sub> -t <sub>RHLD</sub>	5/7t <sub>RCP</sub>	5/7t <sub>RCP</sub> +t <sub>RSUP</sub>	ps
t <sub>RIP2</sub>	LVDS Data Input Position 2	-	6/7t <sub>RCP</sub> -t <sub>RHLD</sub>	6/7t <sub>RCP</sub>	6/7t <sub>RCP</sub> +t <sub>RSUP</sub>	
t <sub>RIP1</sub>	LVDS Data Input Position 1	-	7/7t <sub>RCP</sub> -t <sub>RHLD</sub>	7/7t <sub>RCP</sub>	7/7t <sub>RCP</sub> +t <sub>RSUP</sub>	
t <sub>RIP0</sub>	LVDS Data Input Position 0	-	8/7t <sub>RCP</sub> -t <sub>RHLD</sub>	8/7t <sub>RCP</sub>	8/7t <sub>RCP</sub> +t <sub>RSUP</sub>	
t <sub>CK12</sub>	Skew Time Between RCLK1 and RCLK2	-	-0.3 t <sub>RCP</sub>	-	+0.3 t <sub>RCP</sub>	ps

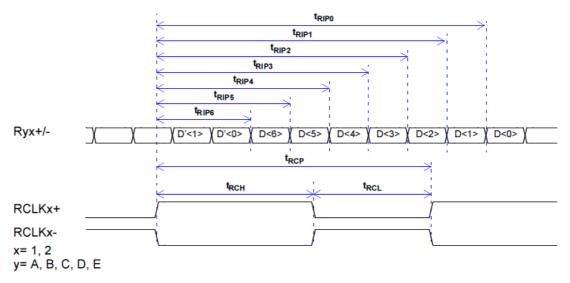
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#### Table 11. LVDS Receiver AC Specifications

(1)  $V_{IC_{RX}}=1.2V$ ,  $t_{RCH}=4/7 t_{RCP}$ 



### LVDS Receiver Input Timing



Ry1+/- skew margin is the one between RCLK1+/- and Ry1+/-. Ry2+/- skew margin is the one between RCLK2+/- and Ry2+/-.

Figure 10. LVDS Receiver Timing

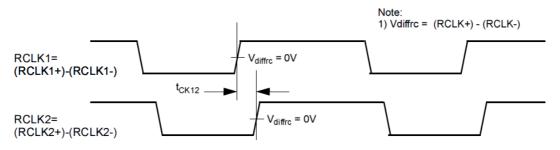


Figure 11. Skew time between RCLK1 and RCLK2



### LVDS Transmitter AC Specifications

			•			
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>TCP</sub>	LVDS Clock Period	-	11.76	-	50	
t <sub>TCH</sub>	LVDS Clock High Duration	-	-	$4/7t_{TCP}$	-	ns
t <sub>TCL</sub>	LVDS Clock Low Duration	-	-	3/7t <sub>TCP</sub>	-	
t <sub>TSUP</sub>	LVDS Data Output Setup	CLKOUT=75MHz	-	-	250	ps
t <sub>THLD</sub>	LVDS Data Output Hold	CLKOUT=75MHz	-	-	250	ps
t <sub>TOP6</sub>	LVDS Data Output Position 6	-	2/7t <sub>TCP</sub> -t <sub>THLD</sub>	2/7t <sub>TCP</sub>	$2/7t_{TCP}+t_{TSUP}$	
t <sub>TOP5</sub>	LVDS Data Output Position 5	-	3/7t <sub>TCP</sub> -t <sub>THLD</sub>	3/7t <sub>TCP</sub>	3/7t <sub>TCP</sub> +t <sub>TSUP</sub>	
t <sub>TOP4</sub>	LVDS Data Output Position 4	-	4/7t <sub>TCP</sub> -t <sub>THLD</sub>	$4/7t_{TCP}$	$4/7t_{TCP}+t_{TSUP}$	
t <sub>TOP3</sub>	LVDS Data Output Position 3	-	5/7t <sub>TCP</sub> -t <sub>THLD</sub>	5/7t <sub>TCP</sub>	5/7t <sub>TCP</sub> +t <sub>TSUP</sub>	ps
t <sub>TOP2</sub>	LVDS Data Output Position 2	-	6/7t <sub>TCP</sub> -t <sub>THLD</sub>	6/7t <sub>TCP</sub>	6/7t <sub>TCP</sub> +t <sub>TSUP</sub>	
t <sub>TOP1</sub>	LVDS Data Output Position 1	-	7/7t <sub>TCP</sub> -t <sub>THLD</sub>	7/7t <sub>TCP</sub>	7/7t <sub>TCP</sub> +t <sub>TSUP</sub>	
t <sub>TOP0</sub>	LVDS Data Output Position 0	-	8/7t <sub>TCP</sub> -t <sub>THLD</sub>	8/7t <sub>TCP</sub>	8/7t <sub>TCP</sub> +t <sub>TSUP</sub>	
t <sub>LVT</sub>	LVDS Transition Time (Fig 13.)	Fig.6	-	0.6	1.5	ns

#### Table 12. LVDS Transmitter AC Specifications



### LVDS Transmitter Output Diagram

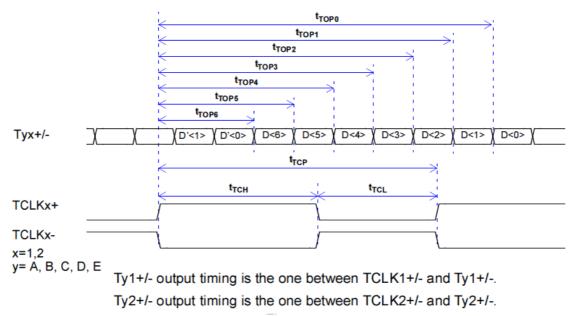
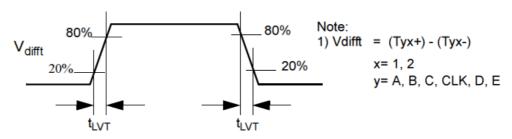


Figure 12. LVDS Transmitter Timing



**Figure 13. LVDS Transition Timing** 



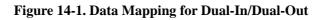
### LVDS Data Mapping

### Dual-In / Dual-Out

### LVDS-Rx Input Mapping

RCLK1+	
RA1+/-	) G1 [4] ) R1 [9] ) R1 [8] ) R1 [7] ) R1 [6] ) R1 [5] ) R1 [4] ) G3 [4] ) R3 [9] ) R3 [8] ) R3 [7] ) R3 [6] ) R3 [5] ) R3 [4] )
RB1+/-	X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B3 [5] X B3 [4] X G3 [9] X G3 [8] X G3 [7] X G3 [6] X G3 [5] X
RC1+/-	DE XVSYNCXHSYNCX B1 [9] X B1 [8] X B1 [7] X B1 [6] X DE XVSYNCXHSYNCX B3 [9] X B3 [8] X B3 [7] X B3 [6] X
RD1+/-	data11 B1 [3] B1 [2] G1 [3] G1 [2] G1 [2] R1 [3] R1 [2] data11 B3 [3] B3 [2] G3 [3] G3 [2] G3 [2] R3 [3] R3 [2] B3 [2] G3 [3] G3 [2] G3 [2] R3 [3] G3 [2] G3 [2] B3 [2] G3 [2]
RE1+/-	$\int data 12 \int B1 [1] \int B1 [0] \int G1 [1] \int G1 [0] \int R1 [1] \int R1 [0] \int data 12 \int B3 [1] \int B3 [0] \int G3 [1] \int G3 [0] \int R3 [1] \int R3 \int R3 [1]$
RCLK2+	
RA2+/	C32 [4] X R2 [9] X R2 [8] X R2 [7] X R2 [6] X R2 [5] X R2 [4] X G4 [4] X R4 [9] X R4 [8] X R4 [7] X R4 [6] X R4 [5] X R4 [4] X
RB2+/-	X B2 [5] X B2 [4] X G2 [9] X G2 [8] X G2 [7] X G2 [6] X R2 [5] X B4 [5] X B4 [4] X G4 [9] X G4 [8] X G4 [7] X G4 [6] X G4 [6] X G4 [5] X
RC2+/-	DE VSYNC HSYNC B2 [9] B2 [8] B2 [7] B2 [6] DE VSYNC HSYNC B4 [9] B4 [8] B4 [7] B4 [6]
RD2+/	data21 B2 [3] B2 [2] G2 [3] G2 [2] R2 [3] R2 [3] R2 [2] data21 B4 [3] B4 [2] G4 [3] G4 [2] G4 [2] R4 [2] R4 [3] B4 [2] G4 [3] G4 [2] B4 [2] B4 [2] C4 [3] C4 [2] C4 [3]
RE2+/-	$\int data22 \int B2 [1] \int B2 [0] \int G2 [1] \int G2 [0] \int R2 [1] \int R2 [0] \int data22 \int B4 [1] \int B4 [0] \int G4 [1] \int G4 [0] \int R4 [0] \int R4 [1] \int R4 [0] \int$
LVDS-Tx C	utput Mapping
TCLK1+	
	) G1 [4] ( R1 [9] ( R1 [8] ( R1 [7] ( R1 [6] ( R1 [5] ( R1 [4] ( G3 [4] ( R3 [9] ( R3 [8] ( R3 [7] ( R3 [6] ( R3 [4] ( R
TCLK1+	
TCLK1+ TA1+/	) G1 [4] ) R1 [9] ) R1 [8] ) R1 [7] ) R1 [6] ) R1 [5] ) R1 [4] ) G3 [4] ) R3 [9] ) R3 [8] ) R3 [7] ) R3 [6] ) R3 [6] ) R3 [4] )
TCLK1+ TA1+/- TB1+/-	X G1 [4] X R1 [9] X R1 [8] X R1 [7] X R1 [6] X R1 [5] X R1 [4] G3 [4] X R3 [9] X R3 [8] X R3 [7] X R3 [6] X R3 [5] X R3 [4] X X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B3 [5] X B3 [4] X G3 [9] X G3 [8] X G3 [7] X G3 [6] X G3 [5] X X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B3 [5] X B3 [4] X G3 [9] X G3 [9] X G3 [8] X G3 [7] X G3 [6] X G3 [5] X X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B3 [5] X B3 [4] X G3 [9] X G3 [9] X G3 [8] X G3 [7] X G3 [6] X G3 [5] X X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B3 [5] X B3 [4] X G3 [9] X G3 [9] X G3 [8] X G3 [7] X G3 [6] X G3 [5] X X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B3 [5] X B3 [5] X B3 [4] X G3 [9] X G3 [8] X G3 [7] X G3 [6] X G3 [5] X X B1 [5] X B1 [6] X B1
TCLK1+ TA1+/- TB1+/- TC1+/-	$ \begin{pmatrix} G1 \ [4] \\ R1 \ [9] \\ R1 \ [8] \\ R1 \ [7] \\ R1 \ [6] \\ R1 \ [5] \\ R1 \ [4] \\ G3 \ [4] \\ G3 \ [9] \\ R3 \ [8] \\ R3 \ [7] \\ R3 \ [6] \\ R3 \ [5] \\ R3 \ [6] $
TCLK1+ TA1+/- TB1+/- TC1+/- TD1+/-	$ \begin{pmatrix} G1 \ [4] \\ R1 \ [9] \\ R1 \ [8] \\ R1 \ [7] \\ R1 \ [6] \\ R1 \ [5] \\ R1 \ [6] \\ R1 \ [6] \\ R1 \ [6] \\ R1 \ [4] \\ G3 \ [6] \\ R3 \ [8] \\ R3 \ [7] \\ R3 \ [6] \ [6] \ R3 \ [6] \ [6] \ R3 \ [6] \ [6] \ [6] \ R3 \ [6] \ R3$
TCLK1+ TA1+/- TB1+/- TC1+/- TD1+/- TE1+/-	$ \begin{pmatrix} G1 \ [4] \\ R1 \ [9] \\ R1 \ [8] \\ R1 \ [7] \\ R1 \ [6] \\ R1 \ [5] \\ R1 \ [6] \\ R1 \ [6] \\ R1 \ [6] \\ R1 \ [4] \\ G3 \ [6] \\ R3 \ [8] \\ R3 \ [7] \\ R3 \ [6] \ [6] \ R3 \ [6] \ [6] \ R3 \ [6] \ [6] \ [6] \ R3 \ [6] \ R3$
TCLK1+ TA1+/- TB1+/- TC1+/- TD1+/- TE1+/- TCLK2+	(G1 [4])       (R1 [9])       (R1 [7])       (R1 [6])       (R1 [5])       (R1 [4])       (G3 [4])       (R3 [9])       (R3 [7])       (R3 [6])       (R3 [6]) <td< th=""></td<>
TCLK1+ TA1+/- TB1+/- TC1+/- TD1+/- TE1+/- TCLK2+ TA2+/-	G1 [4] R1 [9] R1 [8] R1 [7] R1 [6] R1 [5] R1 [4] G3 [4] R3 [9] R3 [8] R3 [7] R3 [6] R3 [5] R3 [4]         B1 [5] B1 [4] G1 [9] G1 [8] G1 [7] G1 [6] G1 [5] B3 [5] B3 [4] G3 [9] G3 [8] G3 [7] G3 [6] G3 [5]         DE VSYNC HSYNC B1 [9] B1 [8] B1 [7] B1 [6] DE VSYNC HSYNC B3 [9] B3 [8] B3 [7] B3 [6]         (data11) B1 [3] B1 [2] G1 [3] G1 [2] R1 [3] R1 [2] data11 B3 [3] B3 [2] G3 [3] G3 [2] R3 [3] R3 [2]         (data12) B1 [1] B1 [0] G1 [1] G1 [0] R1 [1] R1 [0] data12 B3 [1] B3 [0] G3 [1] G3 [0] R3 [1] R3 [0]         (G2 [4] R2 [9] R2 [8] R2 [7] R2 [6] R2 [5] R2 [4] G4 [4] R4 [9] R4 [8] R4 [7] R4 [6] R4 [5] R4 [4]
TCLK1+ TA1+/- TB1+/- TC1+/- TD1+/- TE1+/- TCLK2+ TA2+/- TB2+/-	(G1 [4] (R1 [9] (R1 [8] (R1 [7]) (R1 [6] (R1 [5] (R1 [4]) (G3 [4] (R3 [9] (R3 [8] (R3 [7]) (R3 [6] (R3 [5] (R3 [4] (P3 [9] (G1 [9] (G1 [9] (G1 [8] (G1 [7] (G1 [6] (G1 [5] (B3 [5] (B3 [4] (G3 [9] (G3 [8] (G3 [7] (G3 [6] (G3 [5] (P2 (NSYNC) (HSYNC)
TCLK1+ TA1+/- TB1+/- TC1+/- TD1+/- TE1+/- TCLK2+ TA2+/- TB2+/- TC2+/-	(G1 [4] (R1 [9] (R1 [8] (R1 [7]) (R1 [6] (R1 [5] (R1 [4] (G3 [4] (R3 [9] (R3 [8] (R3 [7] (R3 [6] (R3 [6] (R3 [4] (G3 [6] (G3 [5] (G3 [5] (G3 [5] (G3 [5] (G3 [6] (G3 [5] (G3 [6] (G3 [6] (G3 [5] (G3 [6] (G3 [6

Data bits "data11, data12, data21, data22" are available for additional data transmission.





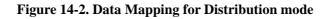
#### **Distribution Mode**

In Distribution mode, RCLK2+/- must be Hi-Z.

### LVDS-Rx Input Mapping

RCLK1+	
RA1+/-	(G1 [4] (R1 [9] (R1 [8] (R1 [7] (R1 [6] (R1 [5] (R1 [4] (G2 [4] (R2 [9] (R2 [8] (R2 [7] (R2 [6] (R2 [5] (R2 [4] (
RB1+/-	X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B2 [5] X B2 [4] X G2 [9] X G2 [8] X G2 [7] X G2 [6] X G2 [5] X
RC1+/-	DE VSYNC HSYNC B1 [9] X B1 [8] X B1 [7] X B1 [6] X DE VSYNC HSYNC B2 [9] B2 [8] X B2 [7] X B2 [6] X
RD1+/-	$\left( \frac{1}{2} \right) \left( \frac{1}{2} \right) $
RE1+/-	$\left( \frac{1}{2} \left( \frac{1}{2} \right)^{2} \left( \frac{1}{2} \right)^{2}$
RCLK2+	Hi-Z
RA2+/-	no care
RB2+/-	no care
RC2+/-	no care
RD2+/-	no care
RE2+/-	no care
	Dutput Mapping
TCLK1+	
TA1+/-	(G1 [4] (R1 [9] R1 [8] (R1 [7] (R1 [6] R1 [5] (R1 [5] (R1 [4] ) G2 [4] (R2 [9] (R2 [8] (R2 [7] (R2 [6] ) R2 [5] (R2 [4] )
TB1+/-	X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B2 [5] X B2 [4] X G2 [9] X G2 [8] X G2 [7] X G2 [6] X G2 [5] X
TC1+/-	DE XVSYNCXHSYNCX B1 [9] X B1 [8] X B1 [7] X B1 [6] X DE XVSYNCXHSYNCX B2 [9] X B2 [8] X B2 [7] X B2 [6] X
TD1+/-	$\left( data11 \right) \left( B1 \left[ 3 \right] \right) \left( B1 \left[ 2 \right] \right) \left( G1 \left[ 3 \right] \right) \left( G1 \left[ 2 \right] \right) \left( R1 \left[ 3 \right] \right) \left( R1 \left[ 2 \right] \right) \left( data11 \right) \left( B2 \left[ 3 \right] \right) \left( B2 \left[ 2 \right] \right) \left( G2 \left[ 3 \right] \right) \left( G2 \left[ 2 \right] \right) \left( R2 \left[ 3 \right] \right) \left( R2 \left[ 2 \right$
TE1+/-	$\int data 12 \int B1 [1] \int B1 [0] \int G1 [1] \int G1 [0] \int R1 [1] \int R1 [0] \int data 12 \int B2 [1] \int B2 [0] \int G2 [1] \int G2 [0] \int R2 [1] \int R2 [0] \int R2 [0]$
TCLK2+	
TA2+/-	(G1 [4] (R1 [9] (R1 [8] (R1 [7] (R1 [6] (R1 [5] (R1 [4] (G2 [4] (R2 [9] (R2 [8] (R2 [7] (R2 [6] (R2 [5] (R2 [4] (R2 [4) (R2 [4] (R2 [4) (R2 (1) (1) (R2 (1) (1) (R2 (1) (1) (R2 (1) (1) (1) (1) (1) (1) (1) (1) (1) (1)
TB2+/-	
TC2+/-	DE VSYNC HSYNC B1 [9] X B1 [8] X B1 [7] X B1 [6] X DE VSYNC HSYNC B2 [9] X B2 [8] X B2 [7] X B2 [6] X
TD2+/-	$\left( \frac{1}{2} \right) \left( \frac{1}{2} \right) $
TE2+/-	$\int data 12 \int B1 [1] \int B1 [0] \int G1 [1] \int G1 [0] \int R1 [1] \int R1 [0] \int data 12 \int B2 [1] \int B2 [0] \int G2 [1] \int G2 [0] \int R2 [1] \int R2 [0] \int R2 [0]$
	(Regardless of the Data Latency)







#### Single-In / Dual-Out

In Single-in / Dual-out mode, RCLK2+/- must be Hi-Z.

### LVDS-Rx Input Mapping

LVDS-KX	три таррі	ng					
RCLK1+		L					
RA1+/-	G1 [4] R1 [9]	R1 [8] R1 [7]	R1 [6] R1 [5]	R1 [4] G2 [4]	R2 [9] R2 [8]	R2 [7] R2 [6]	R2 [5] R2 [4]
RB1+/-	B1 [5] B1 [4]	G1 [9] X G1 [8]	G1 [7] G1 [6]	G1 [5] B2 [5]	B2 [4] G2 [9]	G2 [8] G2 [7]	G2 [6] G2 [5]
RC1+/-		HSYNC B1 [9]	B1 [8] B1 [7]	B1 [6] DE		B2 [9] B2 [8]	B2 [7] 82 [6]
RD1+/-	data11 B1 [3]	B1 [2] G1 [3]	G1 [2] R1 [3]	R1 [2] data11	B2 [3] 82 [2]	G2 [3] G2 [2]	R2 [3] R2 [2]
RE1+/-	data12 B1 [1]	B1 [0] X G1 [1]	G1 [0] R1 [1]	R1 [0] data12	B2 [1] 82 [0]	G2 [1] G2 [0]	R2 [1] R2 [0]
RCLK2+				Hi-Z			
 RA2+/				no care			
RB2+/-				no care			
RC2+/-				no care			
RD2+/-				no care			
RE2+/-				no care			
LVDS-Tx	Output Map	ping	l			[	
TA1+/	G1 [4]	R1 [9]	R1 [8]	R1 [7]		R1 [5]	(R1 [4] )
TB1+/-	B1 [5]	В1 [4]	G1 [9]	G1 [8]	G1 [7]	G1 [6]	G1 [5]
TC1+/-	DE		HSYNC	B1 [9]	(B1 [8]	B1 [7]	(B1 [6] )
TD1+/-	data11	B1 [3]	B1 [2]	G1 [3]	G1 [2]	R1 [3]	R1 [2]
TE1+/-	data12	B1 [1]	B1 [0]	G1 [1]	G1 [0]	R1 [1]	R1 [0]
TCLK2+							
TA2+/-	G2 [4]	R2 [9]	R2 [8]	R2 [7]	R2 [6]	R2 [5]	R2 [4]
TB2+/-	B2 [5]	B2 [4]	G2 [9]	G2 [8]	G2 [7]	G2 [6]	G2 [5]
TC2+/-	DE	VSYNC	HSYNC	B2 [9]	B2 [8]	B2 [7]	B2 [6]
TD2+/-	data11	B2 [3]	B2 [2]	G2 [3]	G2 [2]	R2 [3]	R2 [2]

(Regardless of the Data Latency)

R2 [1]

Data bits "data11, data12" are available for additional data transmission.

G2 [1]

G2 [0]

B2 [0]

Figure 14-3(a). Data Mapping for Single-In/Dual-Out

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data12

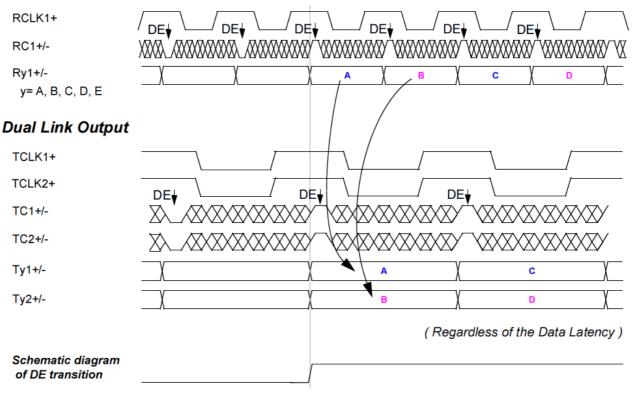
B2 [1]

TE2+/-

R2 [0]



### Single Link Input



Single-in / Dual-out mode uses DE signal L-to-H-edge to start distribution of input data.

Figure 14-3(b). Data Mapping for Single-In/Dual-Out



LVDS-Rx		ng					
RCLK1+			\				
RA1+/-	G1 [4]	R1 [9]	R1 [8]	R1 [7]	R1 [6]	R1 [5]	R1 [4]
RB1+/-	B1 [5]	B1 [4]	G1 [9]	G1 [8]	G1 [7]	G1 [6]	G1 [5]
RC1+/-	DE	VSYNC	HSYNC	B1 [9]	B1 [8]	B1 [7]	B1 [6]
RD1+/-	data11	B1 [3]	B1 [2]	G1 [3]	G1 [2]	R1 [3]	R1 [2]
RE1+/-	data12	B1 [1]	B1 [0]	G1 [1]	G1 [0]	R1 [1]	R1 [0]
RCLK2+							
RA2+/-	G2 [4]	R2 [9]	R2 [8]	R2 [7]	R2 [6]	R2 [5]	R2 [4]
RB2+/-	B2 [5]	B2 [4]	G2 [9]	G2 [8]	G2 [7]	G2 [6]	G2 [5]
RC2+/-	DE	VSYNC	HSYNC	B2 [9]	B2 [8]	B2 [7]	B2 [6]
RD2+/-	data21	B2 [3]	B2 [2]	G2 [3]	G2 [2]	R2 [3]	R2 [2]
RE2+/-	data22	B2 [1]	B2 [0]	G2 [1]	G2 [0]	R2 [1]	R2 [0]
LVDS-Tx	Output Map	oing		I			
TCLK1+							
TA1+/-							
-	G1 [4] R1 [9]	R1 [8] R1 [7]	R1 [6] R1 [5]	R1 [4] G2 [4]	R2 [9] R2 [8]	R2 [7] R2 [6]	R2 [5] X R2 [4] X
TB1+/	G1 [4] R1 [9]	R1 [8] R1 [7]	R1 [6] R1 [5]		R2 [9] R2 [8] B2 [4] G2 [9]	R2 [7] R2 [6]	R2 [5] R2 [4] G2 [6] G2 [5]
	B1 [5] B1 [4]						
TB1+/	B1 [5] B1 [4]	G1 [9] G1 [8]	G1 [7] G1 [6]	(G1 [5] (B2 [5]) (B1 [6] (DE)	B2 [4] G2 [9]	G2 [8] G2 [7]	G2 [6] \ G2 [5]
TB1+/	(B1 [5] B1 [4]	G1 [9] (G1 [8] (HSYNC( B1 [9] (B1 [2] (G1 [3]	(G1 [7] (G1 [6] (B1 [8] (B1 [7]	(G1 [5] (B2 [5]) (B1 [6] (DE) (R1 [2] (data21)		(G2 [8] (G2 [7]) (B2 [9] (B2 [8])	G2 [6] \ G2 [5] \ B2 [7] \ B2 [6] \
TB1+/- TC1+/- TD1+/-	B1 [5]         B1 [4]           DE         VSYNC           (data11)         B1 [3]	G1 [9] (G1 [8] (HSYNC( B1 [9] (B1 [2] (G1 [3]	(G1 [7] (G1 [6] (B1 [8] (B1 [7] (G1 [2] (R1 [3]	(G1 [5] (B2 [5]) (B1 [6] (DE) (R1 [2] (data21)	B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8]     G2 [7]       B2 [9]     B2 [8]       G2 [3]     G2 [2]	G2 [6] (G2 [5] ) B2 [7] (B2 [6] ) R2 [3] (R2 [2] )
TB1+/- TC1+/- TD1+/- TE1+/-	B1 [5]         B1 [4]           DE         VSYNC           (data11)         B1 [3]	G1 [9] (G1 [8] (HSYNC( B1 [9] (B1 [2] (G1 [3]	(G1 [7] (G1 [6] (B1 [8] (B1 [7] (G1 [2] (R1 [3]	(G1 [5] (B2 [5]) (B1 [6] (DE (R1 [2] (data21) (R1 [0] (data22)	B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8]         G2 [7]           B2 [9]         B2 [8]           G2 [3]         G2 [2]	G2 [6] (G2 [5] ) B2 [7] (B2 [6] ) R2 [3] (R2 [2] )
TB1+/- TC1+/- TD1+/- TE1+/- TCLK2+	B1 [5]         B1 [4]           DE         VSYNC           (data11)         B1 [3]	G1 [9] (G1 [8] (HSYNC( B1 [9] (B1 [2] (G1 [3]	(G1 [7] (G1 [6] (B1 [8] (B1 [7] (G1 [2] (R1 [3]	(G1 [5] (B2 [5]) (B1 [6] (DE) (R1 [2] (data21) (R1 [0] (data22) Hi-Z	B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8]         G2 [7]           B2 [9]         B2 [8]           G2 [3]         G2 [2]	G2 [6] (G2 [5] ) B2 [7] (B2 [6] ) R2 [3] (R2 [2] )
TB1+/- TC1+/- TD1+/- TE1+/- TCLK2+ TA2+/-	B1 [5]         B1 [4]           DE         VSYNC           (data11)         B1 [3]	G1 [9] (G1 [8] (HSYNC( B1 [9] (B1 [2] (G1 [3]	(G1 [7] (G1 [6] (B1 [8] (B1 [7] (G1 [2] (R1 [3]	(G1 [5]) (B2 [5]) (B1 [6]) (DE) (R1 [2]) (data21) (R1 [0]) (data22) Hi-Z Hi-Z	B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8]         G2 [7]           B2 [9]         B2 [8]           G2 [3]         G2 [2]	G2 [6] (G2 [5] ) B2 [7] (B2 [6] ) R2 [3] (R2 [2] )
TB1+/- TC1+/- TD1+/- TE1+/- TCLK2+ TA2+/- TB2+/-	B1 [5]         B1 [4]           DE         VSYNC           (data11)         B1 [3]	G1 [9] (G1 [8] (HSYNC( B1 [9] (B1 [2] (G1 [3]	(G1 [7] (G1 [6] (B1 [8] (B1 [7] (G1 [2] (R1 [3]	(G1 [5] (B2 [5]) (B1 [6] (DE) (R1 [2] (data21) (R1 [0] (data22) Hi-Z Hi-Z Hi-Z	B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8]         G2 [7]           B2 [9]         B2 [8]           G2 [3]         G2 [2]	G2 [6] (G2 [5] ) B2 [7] (B2 [6] ) R2 [3] (R2 [2] )
TB1+/- TC1+/- TD1+/- TE1+/- TCLK2+ TA2+/- TB2+/- TC2+/-	B1 [5]         B1 [4]           DE         VSYNC           (data11)         B1 [3]	G1 [9] (G1 [8] (HSYNC( B1 [9] (B1 [2] (G1 [3]	(G1 [7] (G1 [6] (B1 [8] (B1 [7] (G1 [2] (R1 [3]	(G1 [5] (B2 [5]) (B1 [6] (DE) (R1 [2] (data21) (R1 [0] (data22) Hi-Z Hi-Z Hi-Z Hi-Z	B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8]         G2 [7]           B2 [9]         B2 [8]           G2 [3]         G2 [2]	G2 [6] (G2 [5] ) B2 [7] (B2 [6] ) R2 [3] (R2 [2] )

### Dual-In / Single-Out LVDS-Rx Input Mapping

(Regardless of the Data Latency)

Data bits "data11, data12, data21, data22" are available for additional data transmission.

Figure 14-4. Data Mapping for Dual-In/Single-Out

Notes



#### 1) LVDS input pin connection

When LVDS line is not derived from the previous device, the line is pulled up to 3.3V internally in THC63LVD1027. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THC63LVD1027. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.

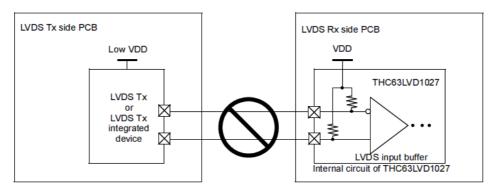


Figure 15. LVDS input pin connection

#### 2) Power On Sequence

Don't input RCLK1+/- and RCLK2+/- before THC63LVD1027 is on in order to keep absolute maximum ratings.



#### 3)Cable Connection and Disconnection

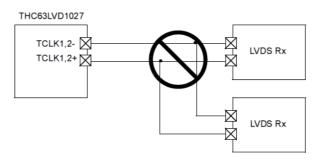
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

#### 4)GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THC63LVD1027 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

#### 5)Multi Drop Connection

Multi drop connection is not recommended.



#### Figure 16.Multi Drop Connection

#### 6)Asynchronous use

Asynchronous use such as following systems are not recommended. Page.11 tCK12 spec should be kept.

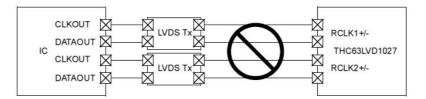


Figure 17-1. Asynchronous Use1

Asynchronous use such as following systems are not recommended.

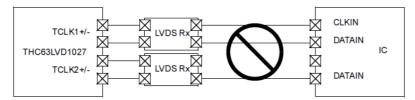
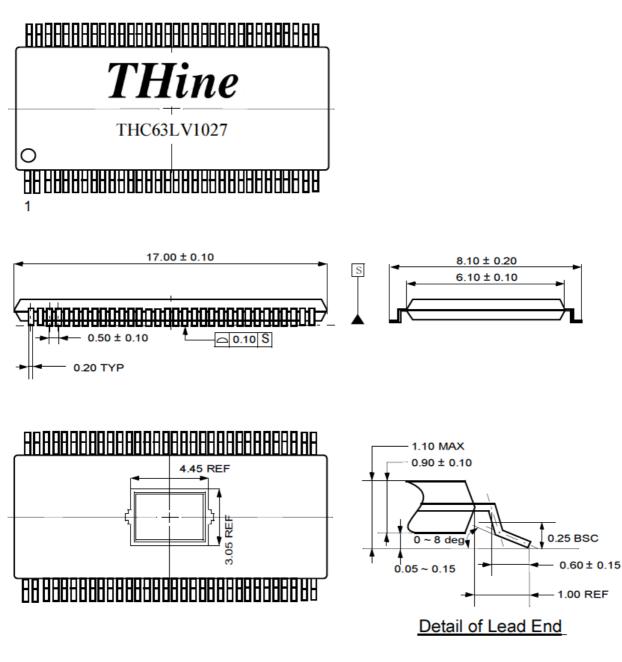


Figure 17-2. Asynchronous Use2



Package



Unit: mm

Exposed PAD is GND and must be soldered to PCB.

Figure 18. Package Diagram



#### **Notices and Requests**

- 1. The product specifications described in this material are subject to change without prior notice.
- 2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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- 5. This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
- 6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
- 7. Please note that this product is not designed to be radiation-proof.
- 8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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