

## Low Voltage H-Bridge Motor Drive

### FEATURES

- Support the input voltage range: motor power: 1.8 ~ 12 V, control power supply: 1.8 ~ 5.5 V
- LDMOSR<sub>dson</sub> (HS+LS) 280mΩ
- Ultra low power sleep mode
- Maximum 1.8 A current output capacity
- Built-in UVLO Protection
- Built-in Over Temperature Protection
- Built-in Short Circuit Protection
- Built-in Over Current Protection
- Built-in Charge Pump
- DFN8L 2\*2 package

### GENERAL DESCRIPTION

STI8837 is a low voltage DC motor driver IC , Internal integration 280m (HS+LS) H bridge NMOS switch, which can support the 1.8~12V input voltage range, The maximum current capacity of up to 1.8A, support for ultra low power sleep mode; built-in UVLO, Thermal Shutdown, OCP protection circuit can be used in camera, toys and consumer products

### APPLICATIONS

- Cameras
- Toys
- Consumer Products

### TYPICAL APPLICATION

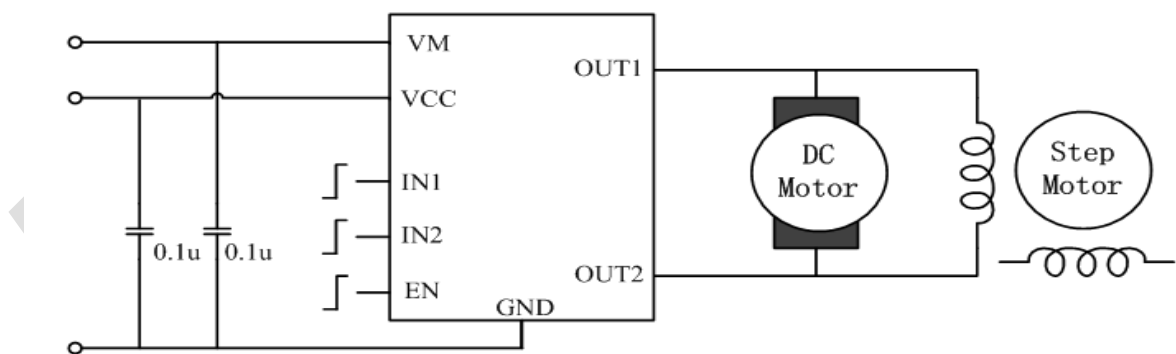
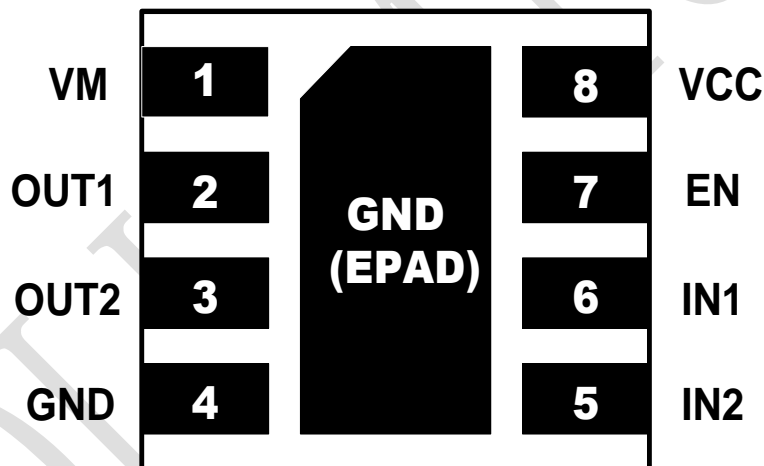


Figure 1. Basic Application Circuit

## ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
VM Voltage Range	-0.3~12	V
VCC,IN1,IN2,nSLEEP Voltages Range	-0.3~6	V
VSET/VOUT Voltage Range	-0.3~Vin+0.3	V
Storage Temperature Range	-50~150	°C
Junction Temperature	-40~150	°C
Package Thermal Resistance	10	°C/W

## PACKAGE/ORDER INFORMATION



DFN8L 2\*2

Top Mark: S8837YY XXX (S8837: Device Code,YY XXX: Inside Code)

Part Number	Package	Top mark	Quantity/ Reel
STI8837	DFN8L 2*2	S8837YY XXX	3000

**PIN FUNCTIONS**

Pin	Name	Function
1	VM	Power Supply for Driver Connect a 0.1u bypass ceramic capacitor to GND
2	OUT1	Motor Driver output 1
3	OUT2	Motor Driver output 2
4	GND	Ground pin
5	IN2	PWM input2
6	IN1	PWM input1
7	EN	Chip Enable Input 1:Enable, 2:Sleep Mode
8	VCC	Power Supply for Logic Input Connect a 0.1u bypass ceramic capacitor to GND

**ESD RATING**

Items	Description	Value	Unit
$V_{ESD}$	Human Body Model for all pins	±2000	V

**JEDEC specification JS-001**
**RECOMMENDED OPERATING CONDITIONS**

Items	Description	Min	Max	Unit
Voltage Range	VM	1.8	12	V
TA	Operating Temperature Range	-40	85	°C

## ELECTRICAL CHARACTERISTICS (Note 3)

( $V_{IN}=12V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VM Voltage Range	$V_{VM}$		1.8		12	V
VM Supply Current	$I_{VM}$	VM=5V VCC=3V No PWM		67		$\mu A$
		VM=5V VCC=3V 50kHz PWM		0.43		mA
VCC Voltage Surge	$V_{VCC}$		1.8		5.5	V
VCC Supply Current	$I_{VCC}$	VM=5V VCC=3V No PWM		105		$\mu A$
		VM=5V VCC=3V 50kHz PWM		0.28		mA
		VM=5V VCC=3V Sleep Mode		5		nA
Input Logic Low Voltage	$V_{IL}$		0.25x VCC	0.4x VCC		V
Input Logic High Voltage	$V_{IH}$			0.5x VCC	0.6x VCC	V
Input logic Hysteresis	$V_{HYS}$			0.1x VCC		V
Input Logic Low Current	$I_{IL}$		-5		5	$\mu A$
Input Logic High Current	$I_{IH}$				50	$\mu A$
Input Pull Down Resistor	$R_{IN}$			100		K $\Omega$
Output Switch On-Resistance	$R_{ON}$	VM=5V VCC=3V Iload=800mA		285		m $\Omega$
Output Switch Leakage Current	$I_{LEAK}$		-200		200	nA
VCC UVLO Voltage	$V_{UVLO}$			1.7		V
UVLO Hysteresis	$V_{UVLO\_HY}$			100		mV
Over Current Protection	$I_{OCP}$			2.2		A
Over Current Retry Time	$T_{OCP\_RT}$			1		mS
Thermal Shutdown Threshold	$T_{SDN}$			160		$^{\circ}C$

Thermal Shutdown Hysteresis	$T_{SDN\_HY}$			20		°C
Output Enable time	$T_1$			180		nS
Output Disable time	$T_2$			70		nS
Delay Time IN1 low to OUT2 high IN2 low to OUT1 high	$T_3$			140		nS
Delay Time IN2 high to OUT1 low IN1 high to OUT2 low	$T_4$			160		nS
Output rise time	$T_5$			60		nS
Output fall time	$T_6$			20		nS

**FUNCTIONAL BLOCK DIAGRAM**

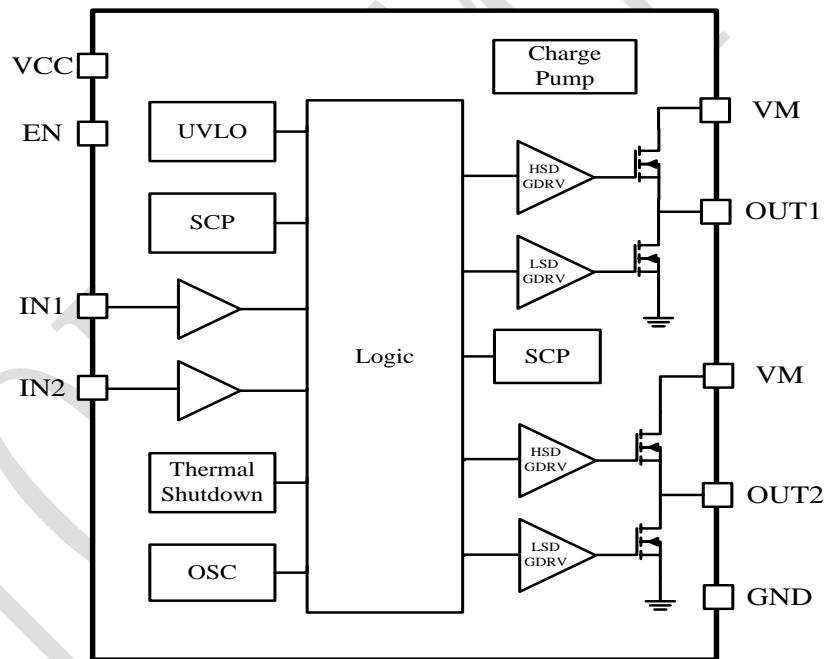
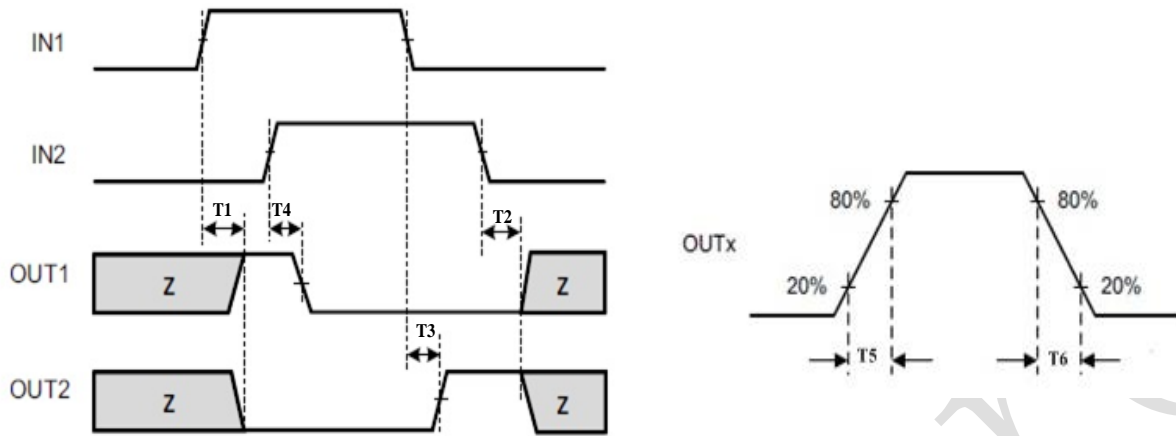


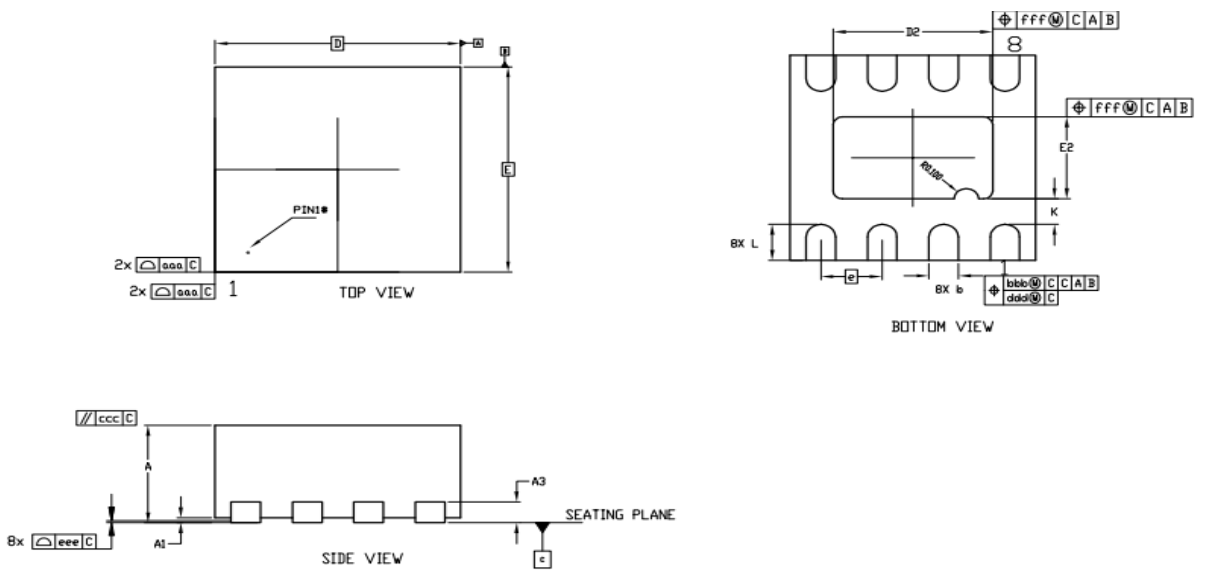
Figure 2. STI8837 Block Diagram

**INPUT OUTPUT LOGIC**



EN	IN1	IN2	OUT1	OUT2	Function
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	1	0	H	L	Forward
1	0	1	L	H	Reverse
1	1	1	L	L	Break

**PACKAGE INFORMATION**



DIM SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	-	0.20 REF	-
b	0.19	0.24	0.29
D	2.00BSC		
E	2.00BSC		
D2	1.25	1.30	1.35
E2	0.75	0.80	0.85
e	0.50BSC		
L	0.30	0.35	0.40
K	0.20		
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

DFN8L 2\*2

**Note:**

- 1) All dimensions are in millimeters.
- 2) Package length does not include mold flash, protrusion or gate burr.
- 3) Package width does not include inter lead flash or protrusion.
- 4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.
- 5) Pin 1 is lower left pin when reading top mark from left to right.

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