

## N-Channel Enhancement Mode MOSFET

### Feature

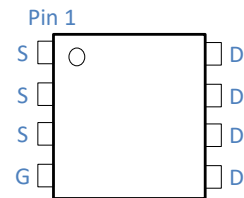
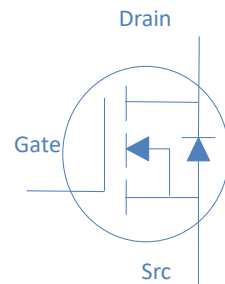
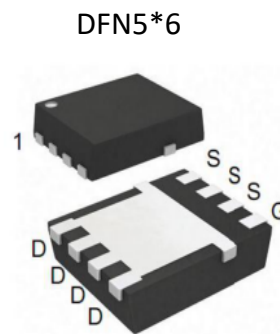
- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

$V_{DS}$		100	V
$R_{DS(on),typ}$	$V_{GS}=10V$	14	mΩ
$R_{DS(on),typ}$	$V_{GS}=4.5V$	22	mΩ
$I_D$ (Silicon Limited)		44	A
$I_D$ (Package Limited)		30	A

### Application

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Industrial

Part Number	Package	Marking
BSC160N10NS3G	DFN5*6	160N10



### Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^\circ\text{C}$	44	A
		$T_C=100^\circ\text{C}$	31	
		$T_C=25^\circ\text{C}$	30	
Continuous Drain Current (Package Limited)		$T_C=25^\circ\text{C}$	30	
Drain to Source Voltage	$V_{DS}$	-	100	V
Gate to Source Voltage	$V_{GS}$	-	$\pm 20$	V
Pulsed Drain Current	$I_{DM}$	-	180	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.4\text{mH}, T_C=25^\circ\text{C}$	45	mJ
Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	50	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 150	$^\circ\text{C}$

### Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	55	$^\circ\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$

**Electrical Characteristics at  $T_j=25^{\circ}\text{C}$  (unless otherwise specified)**

**Static Characteristics**

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.4	2.0	2.4	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS}=0V, V_{DS}=100V, T_j=25^{\circ}\text{C}$	-	-	1	$\mu A$
		$V_{GS}=0V, V_{DS}=100V, T_j=100^{\circ}\text{C}$	-	-	100	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$	-	14	17	$m\Omega$
		$V_{GS}=4.5V, I_D=10A$	-	22	26	
Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=15A$	-	42	-	S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}$ Open, $f=1\text{MHz}$	-	1.6	-	$\Omega$

**Dynamic Characteristics**

Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=50V, f=1\text{MHz}$	-	840	-	$pF$
Output Capacitance	$C_{oss}$		-	147	-	
Reverse Transfer Capacitance	$C_{rss}$		-	4.9	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=50V, I_D=15A, V_{GS}=10V$	-	16	-	$nC$
Total Gate Charge	$Q_g(4.5V)$		-	9	-	
Gate to Source Charge	$Q_{gs}$		-	3	-	
Gate to Drain (Miller) Charge	$Q_{gd}$		-	3	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=15A, V_{GS}=10V, R_G=10\Omega,$	-	6	-	$ns$
Rise time	$t_r$		-	3	-	
Turn off Delay Time	$t_{d(off)}$		-	13	-	
Fall Time	$t_f$		-	3	-	

**Reverse Diode Characteristics**

Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_F=20A$	-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_R=50V, I_F=15A, di_F/dt=500A/\mu s$	-	30	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	105	-	nC

Fig 1. Typical Output Characteristics

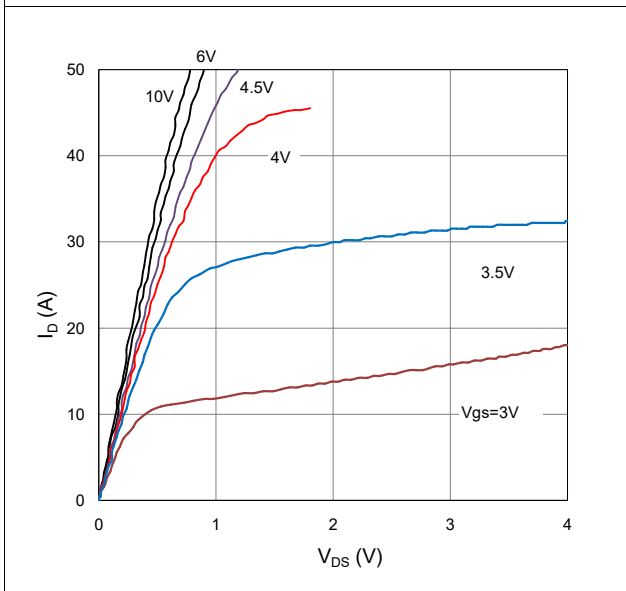


Figure 2. On-Resistance vs. Gate-Source Voltage

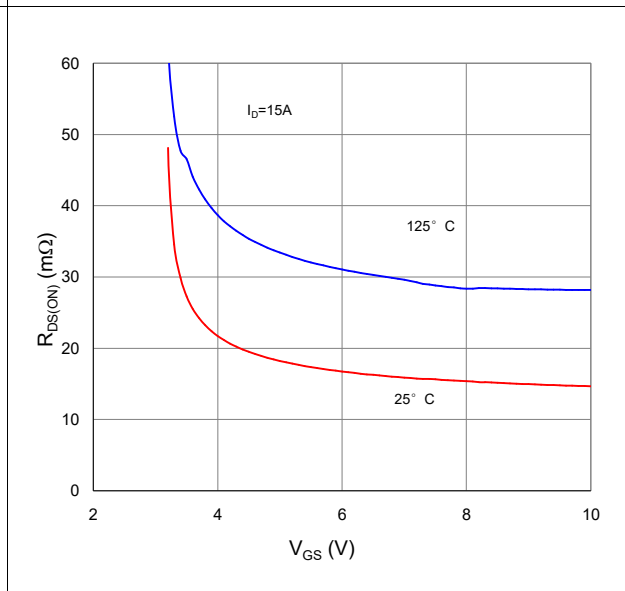


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

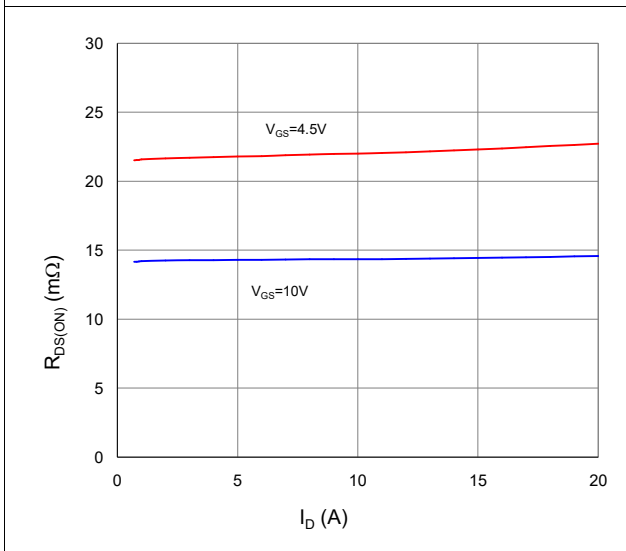


Figure 4. Normalized On-Resistance vs. Junction Temperature

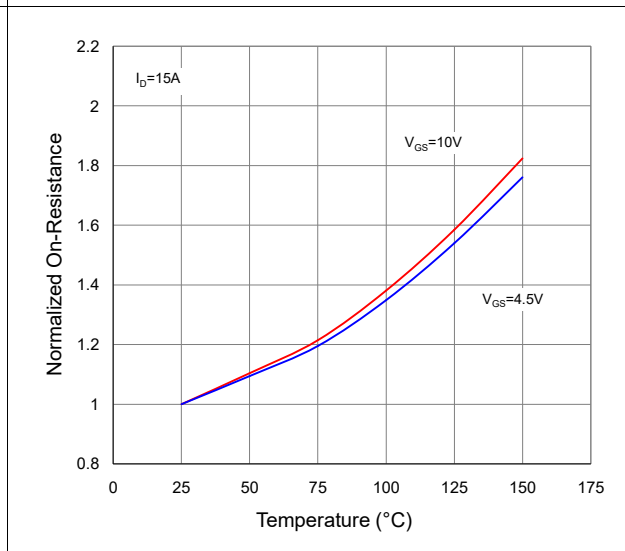


Figure 5. Typical Transfer Characteristics

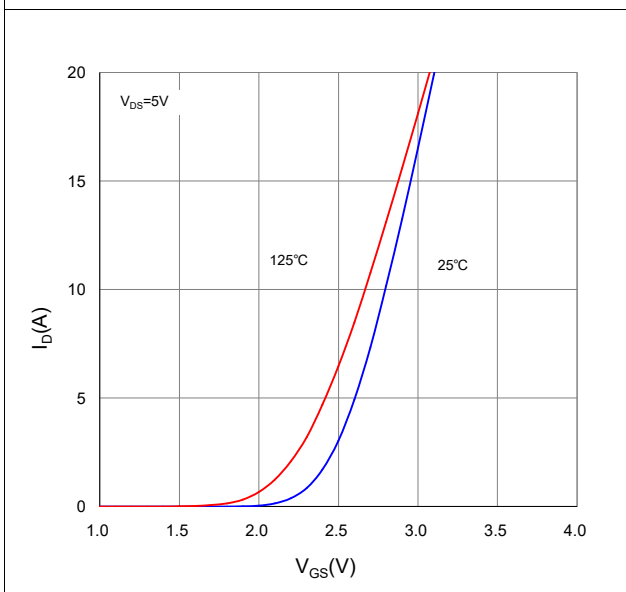


Figure 6. Typical Source-Drain Diode Forward Voltage

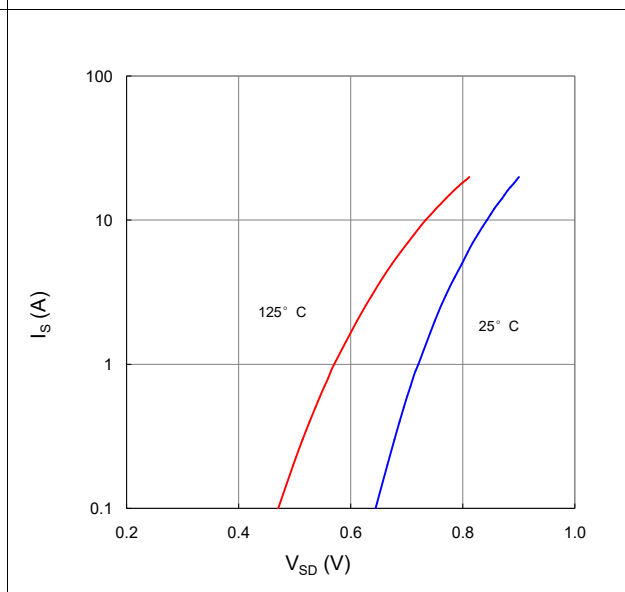


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

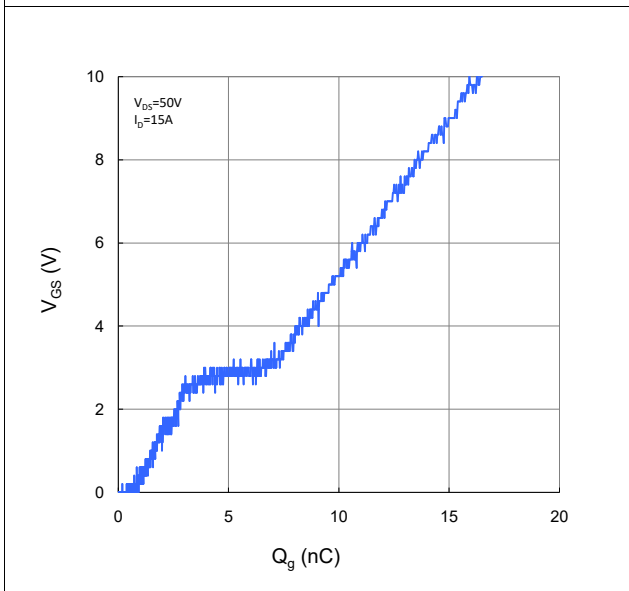


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

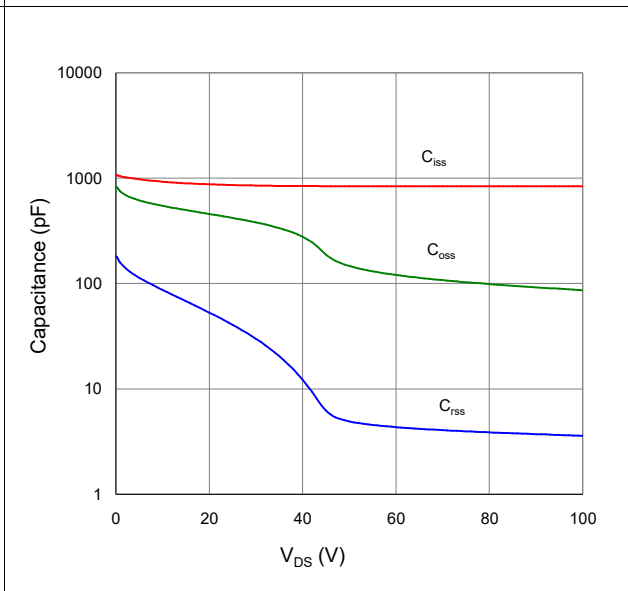


Figure 9. Maximum Safe Operating Area

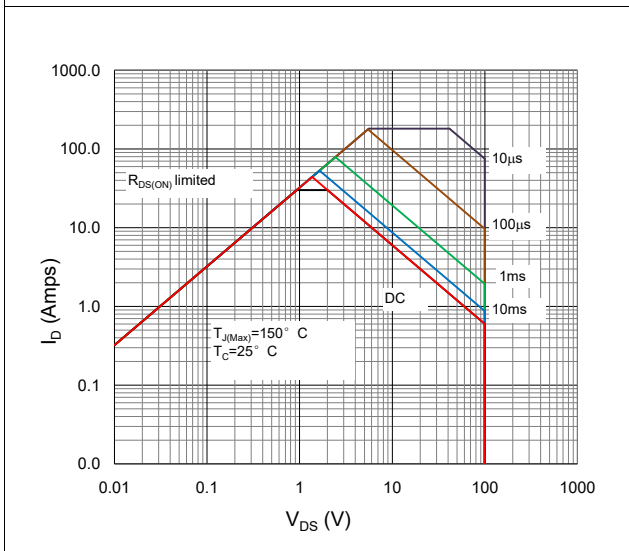


Figure 10. Maximum Drain Current vs. Case Temperature

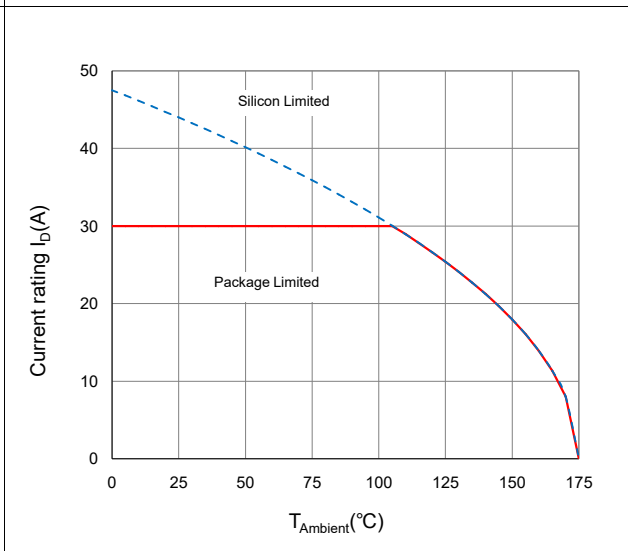
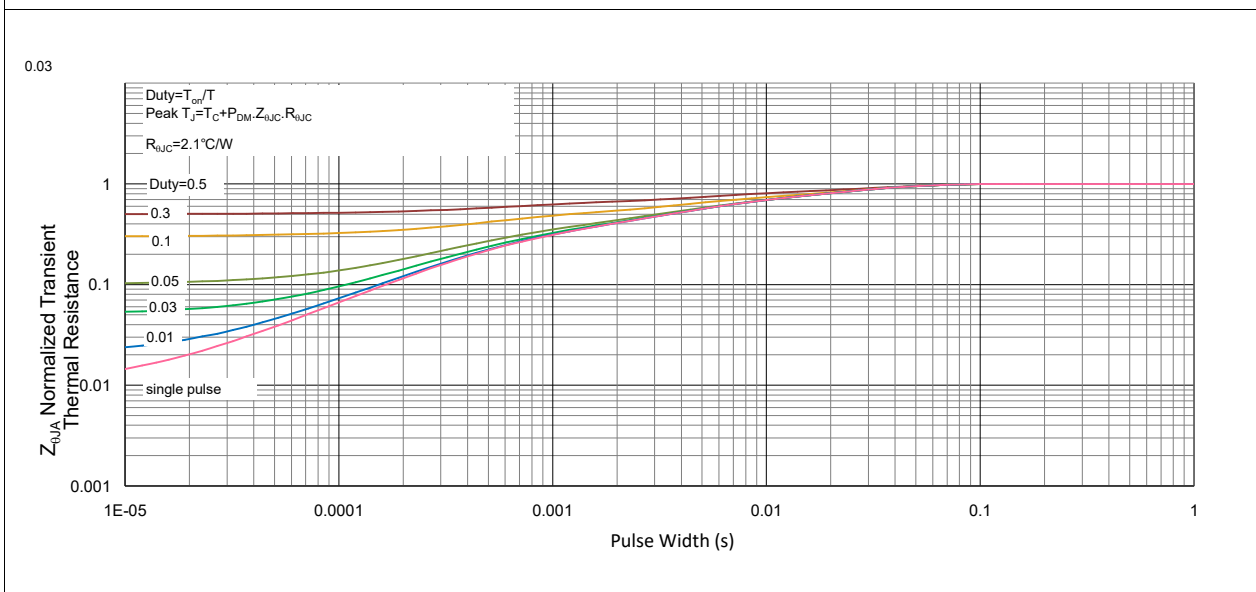
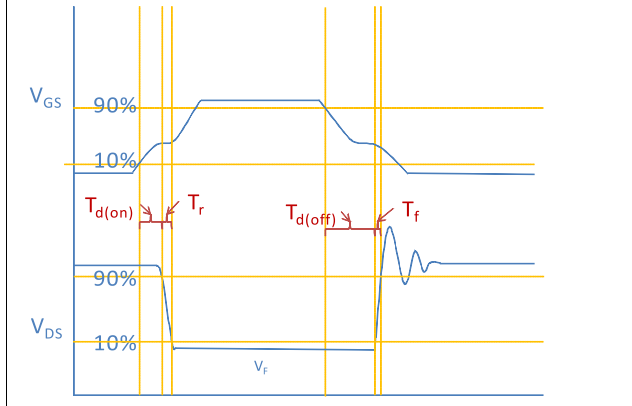
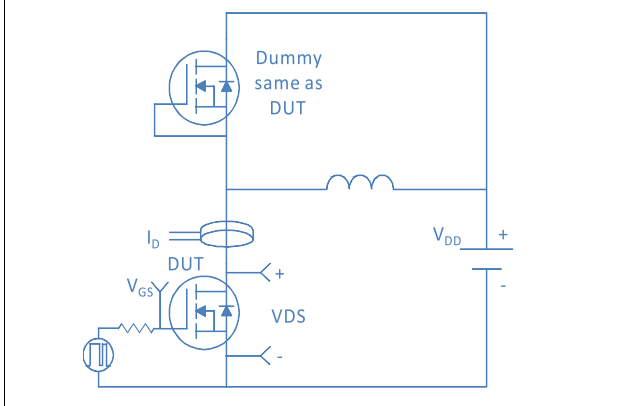


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

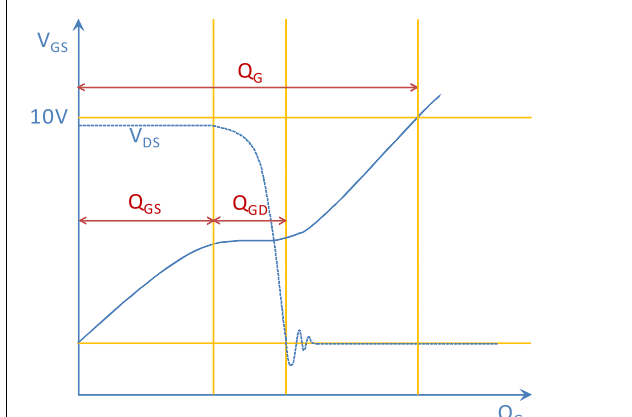
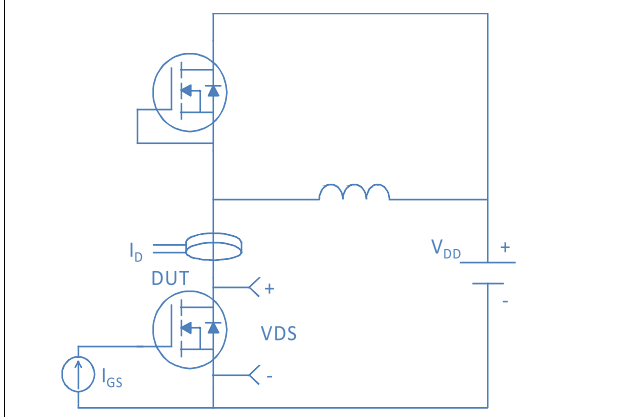




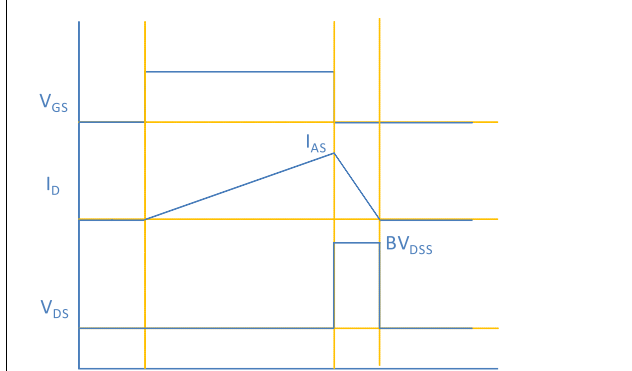
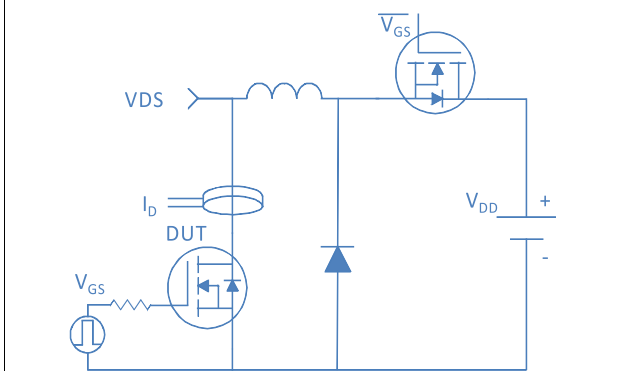
Inductive switching Test



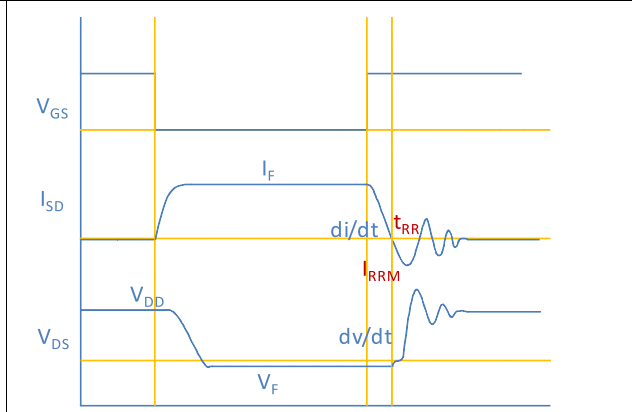
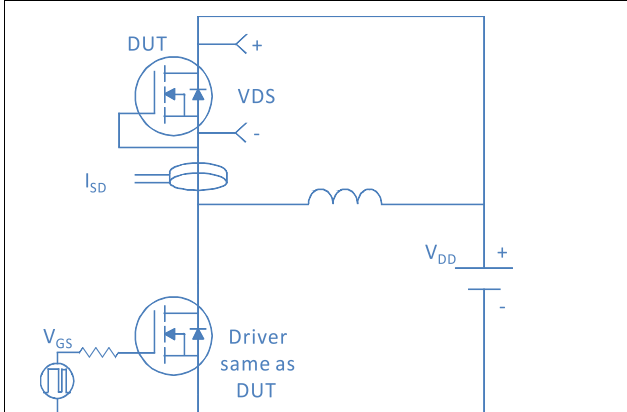
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

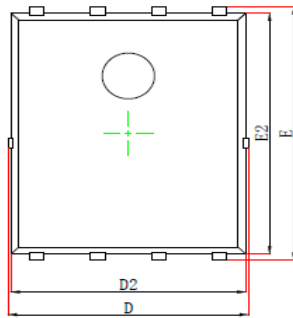


Diode Recovery Test

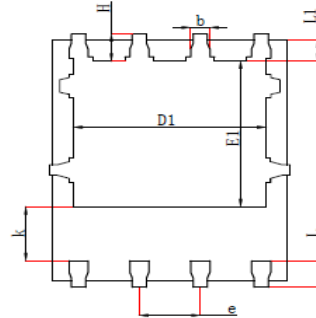


Package Outline

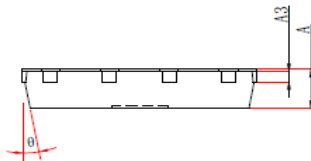
DFN5x6\_P, 8 Leads



Top View  
[顶视图]



Bottom View  
[背视图]



Side View  
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A3	0.254 REF		0.010REF	
D	4.680	5.120	0.184	0.202
E	5.900	6.126	0.232	0.241
D1	3.610	4.110	0.142	0.162
E1	3.380	3.780	0.133	0.149
D2	4.800	5.000	0.189	0.197
E2	5.674	5.826	0.223	0.229
k	1.100	1.390	0.043	0.055
b	0.330	0.510	0.013	0.020
e	1.270TYP		1.270TYP	
L	0.510	0.711	0.020	0.028
L1	0.424	0.576	0.017	0.023
H	0.410	0.726	0.016	0.029
θ	0°	12°	0°	12°

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